

U_TIDA-010949 Power Optimizer_Hardware
TIDA-010949 Power Optimizer_Hardware.SchDoc

U_TIDA-010949 Power Optimizer_PLC
TIDA-010949 Power Optimizer_PLC.SchDoc

U_TIDA-010949 Power Optimizer_Wireless
TIDA-010949 Power Optimizer_Wireless.SchDoc

Orderable:	Designed for: Public Release	Mod. Date: 9/26/2024
TID #:	TIDA-010949	Project Title: TIDA-010949
Number: TIDA-010949	Rev: E1	Sheet Title:
SVN Rev:	Assembly Variant: [No Variations]	Sheet: 1 of 8
Drawn By:	File: TIDA-010949 Power Optimizer_Top View.SchDoc	Size: A4
Engineer: Energy Infrastructure Team	Contact: http://www.ti.com/support	

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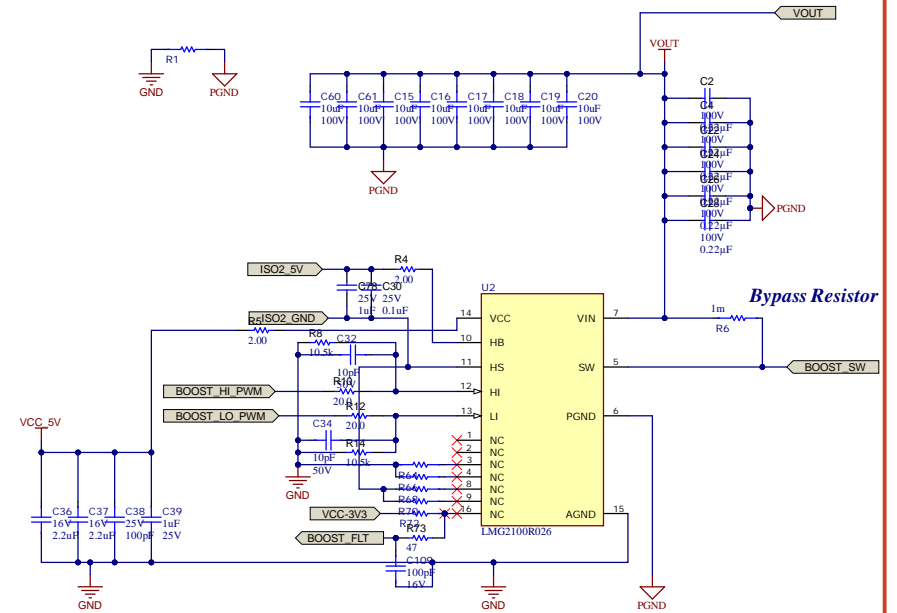
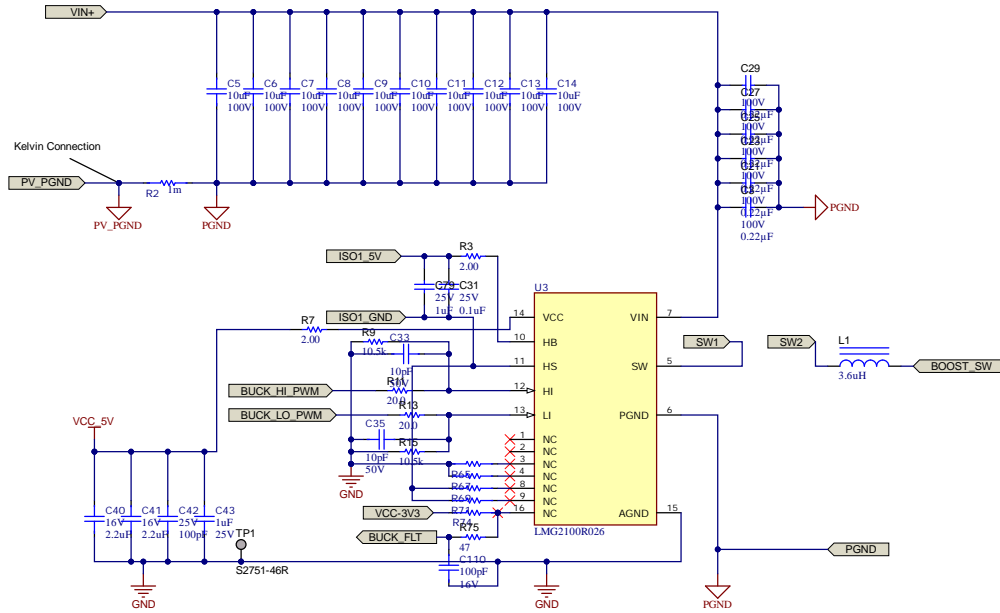
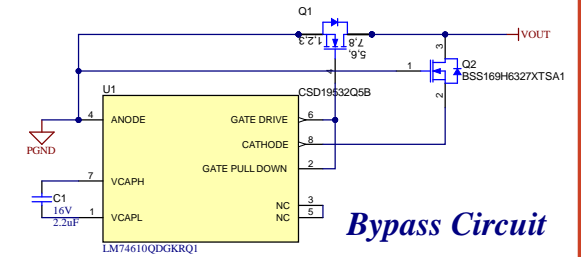
MCU C2000 TMS320F280013x

GND

Revision History

Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A

Power Stage

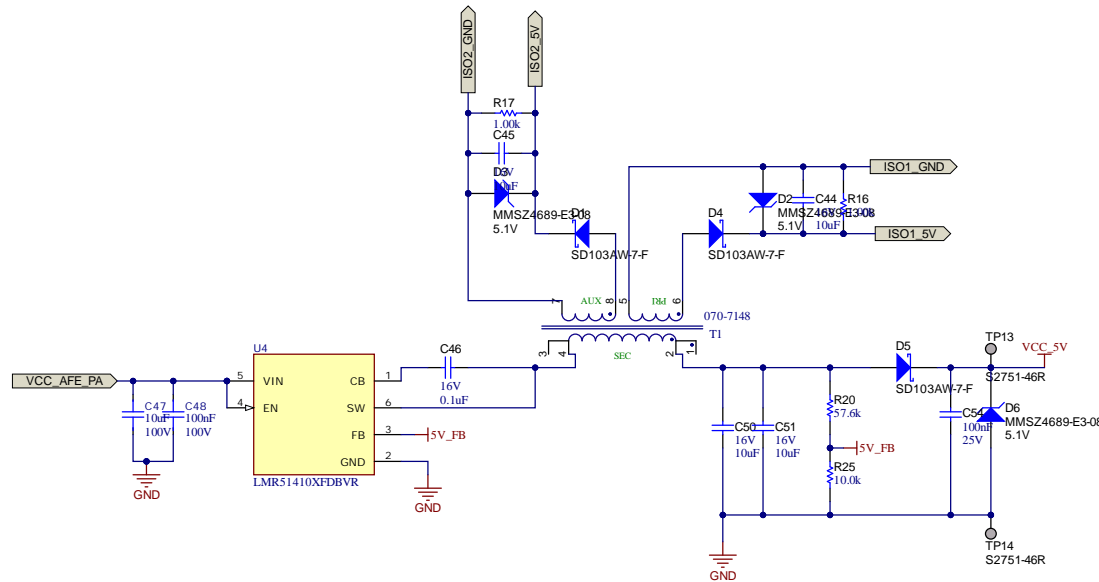


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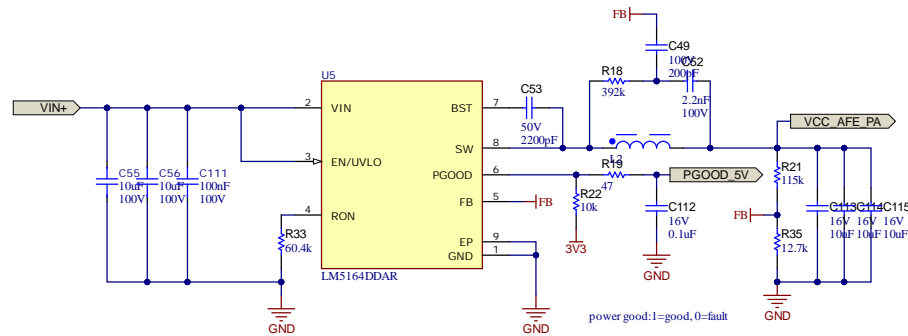
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Number: TIDA-010949	Rev: E1	Sheet Title:
SVN Rev:	Assembly Variant: [No Variations]	Sheet: 2 of 8
Drawn By:	File: TIDA-010949 Power Optimizer power stage.Sch	Size: B
Engineer: Energy Infrastructure Team	Contact: http://www.ti.com/support	



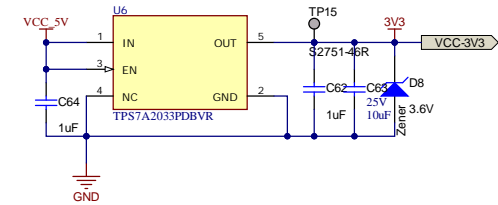
Aux Power



Fly-Buck for 2*LMG2100's ISO power and Non-ISO 5V



BUCK CONVERTER FOR AFE031's PA



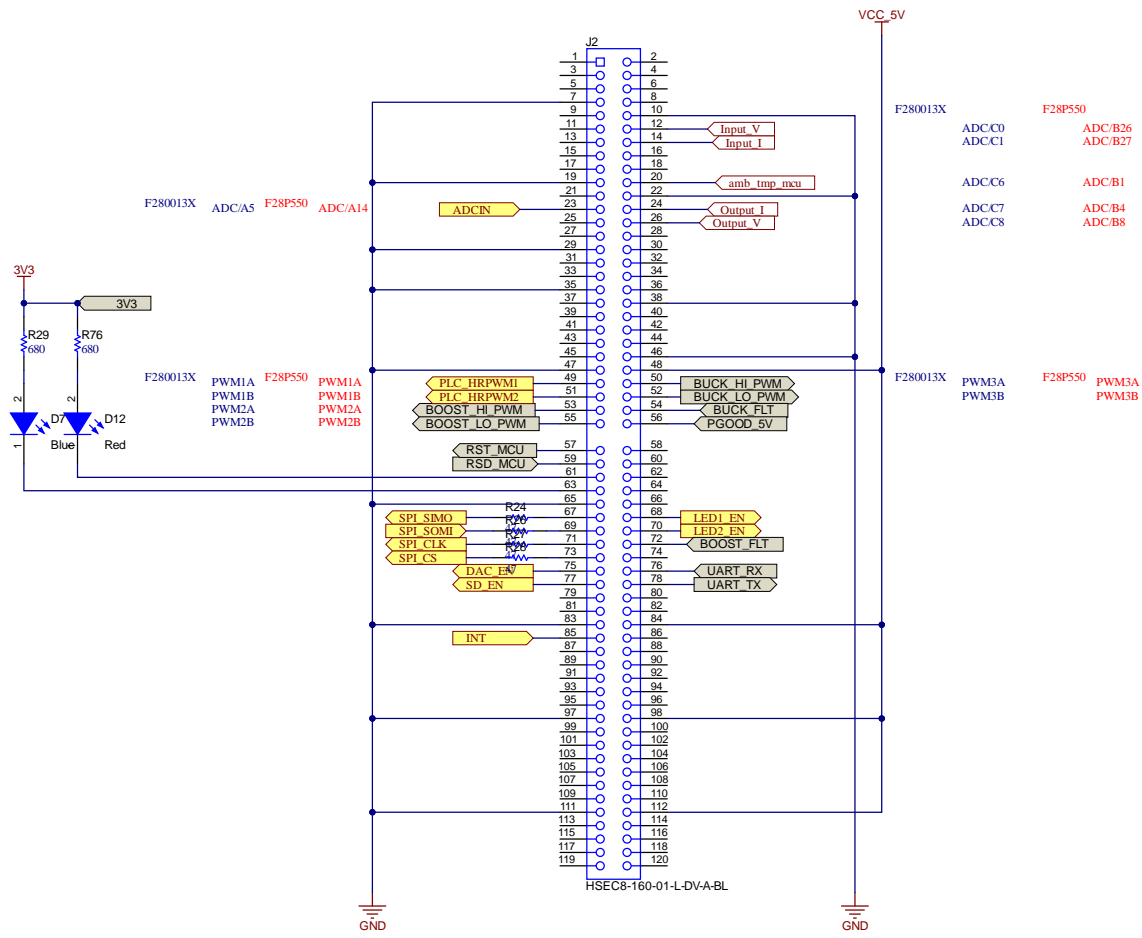
LDO for 3.3V

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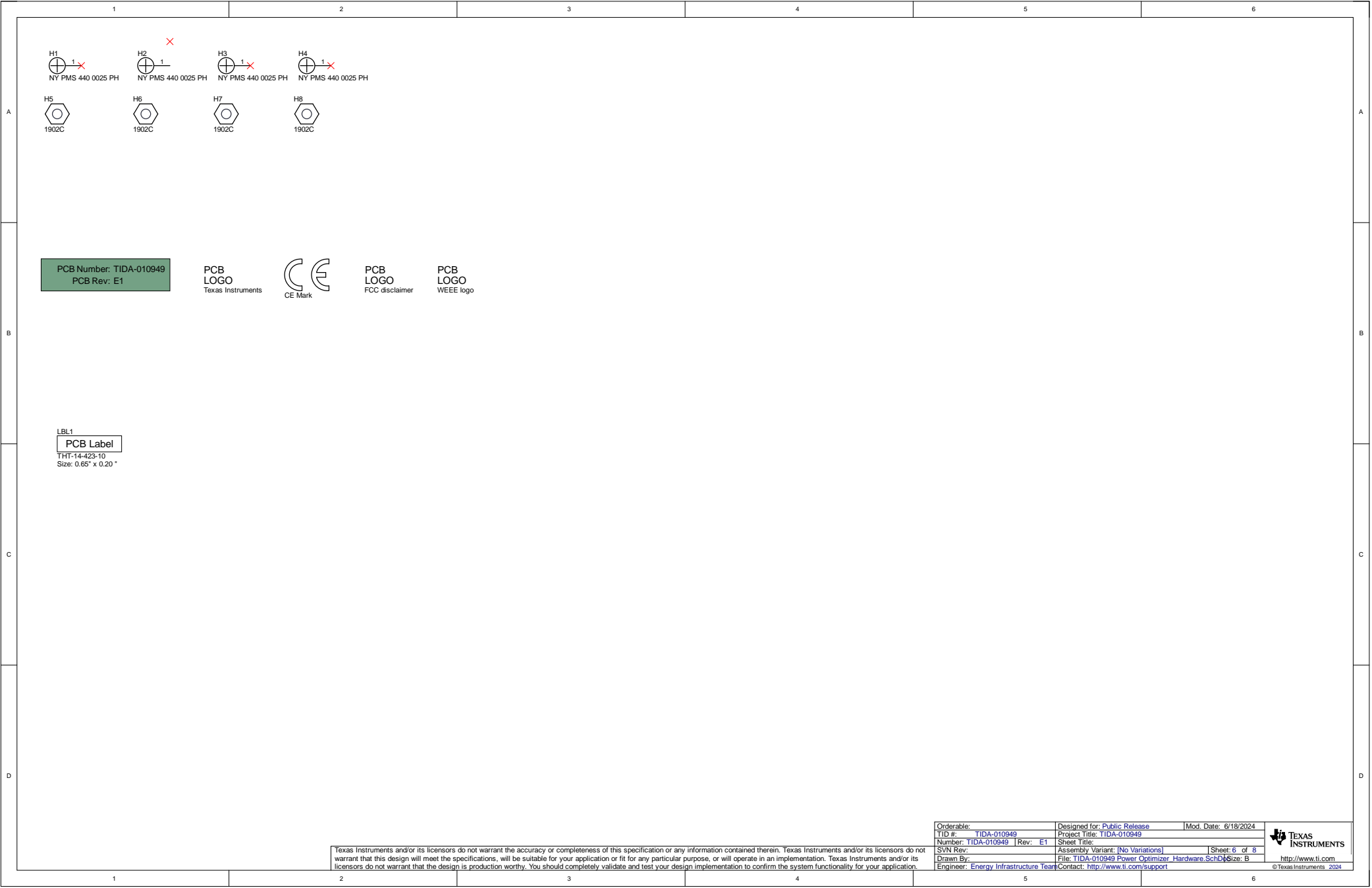
Orderable:	Designed for Public Release	Mod. Date: 9/30/2024
TID #: TIDA-010949	Project Title: TIDA-010949	
Number: TIDA-010949	Rev: E1	Sheet Title:
SVN Rev:	Assembly Variant: [No Variations]	Sheet 3 of 8
Drawn By:	File: TIDA-010949 Power Optimizer_Aux_SchDoc	Size: A3
Engineer: Energy Infrastructure Team	Contact: http://www.ti.com/support	

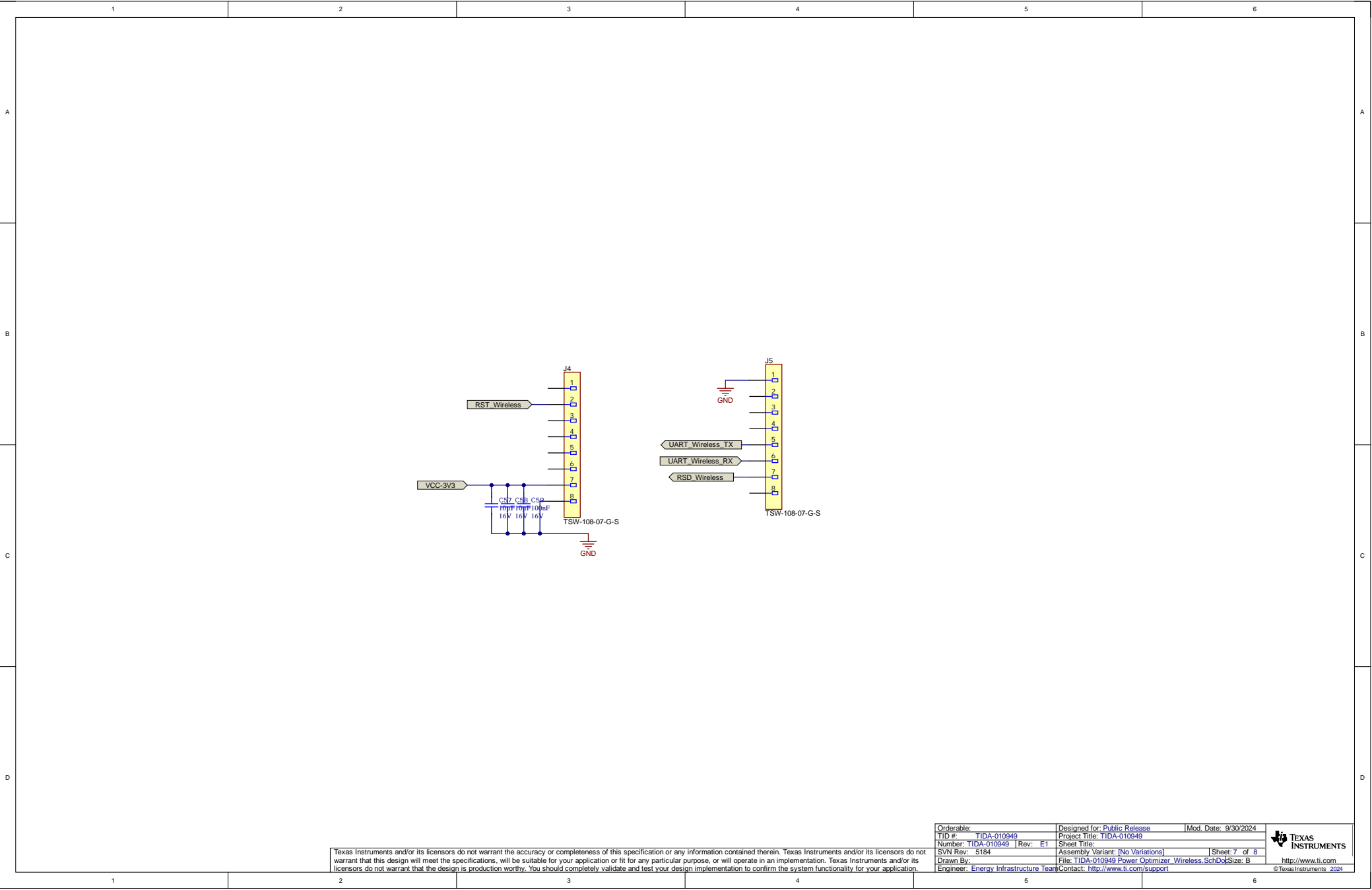


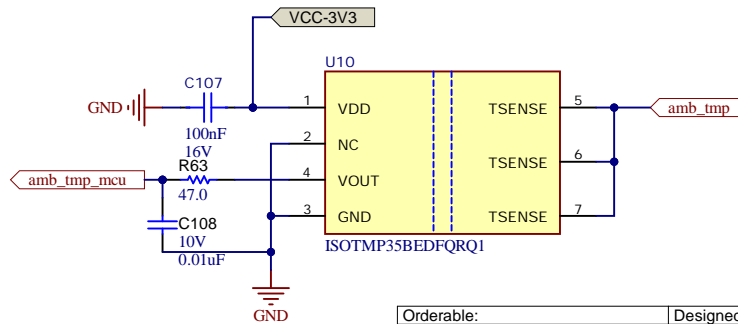
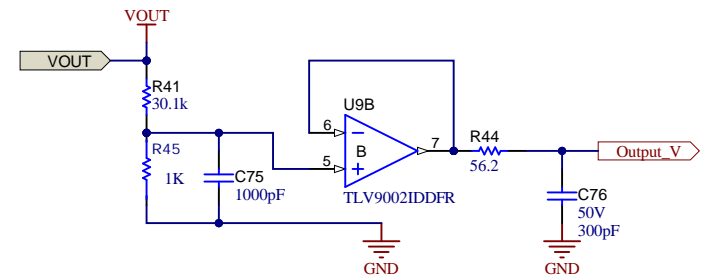
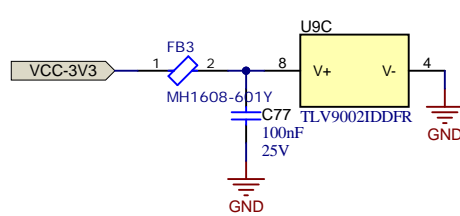
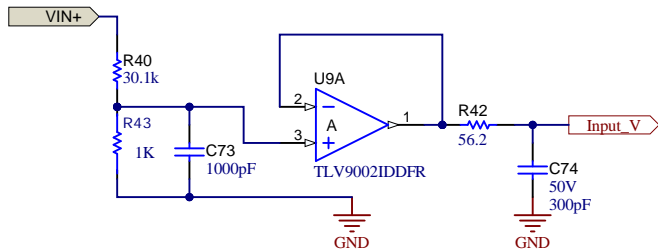
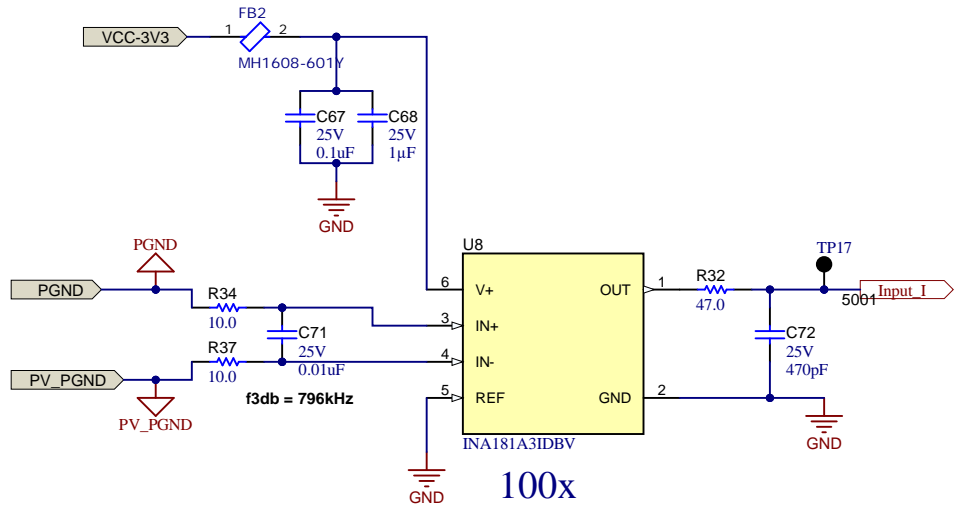
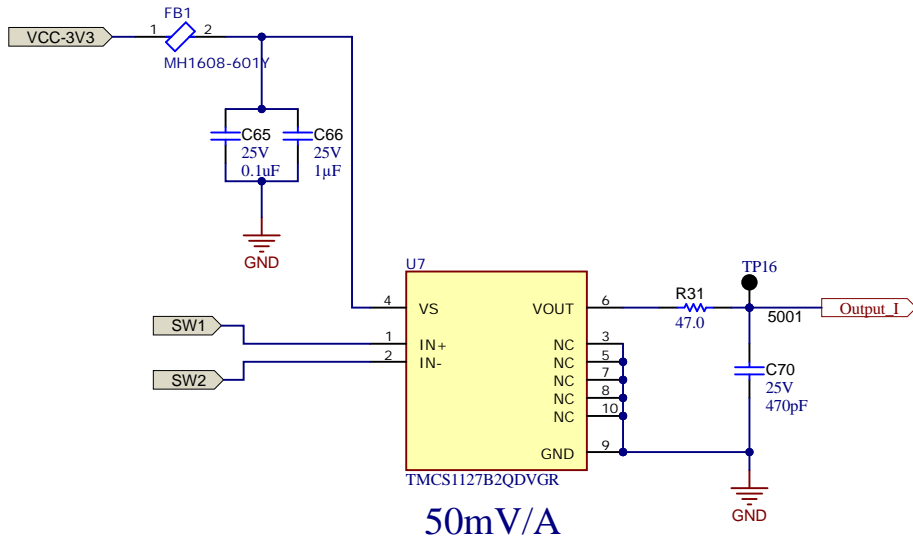
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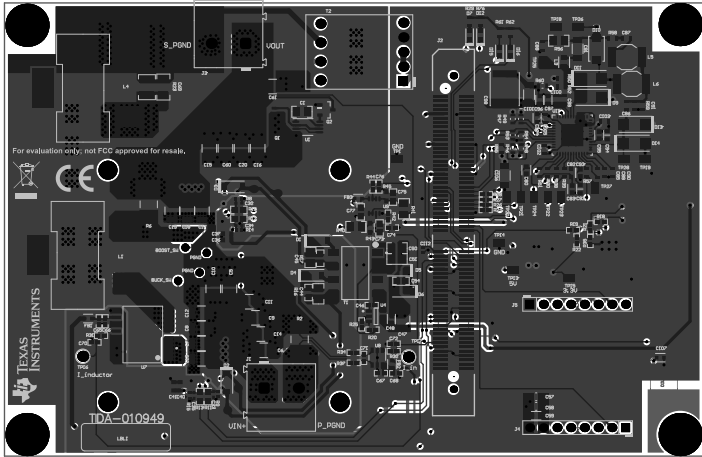






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TID #: TIDA-010949	Project Title: TIDA-010949	
Number: TIDA-010949	Rev: E1	Sheet Title:
SVN Rev:	Assembly Variant: [No Variations]	Sheet: 8 of 8
Drawn By:	File: TIDA-010949 Power Optimizer_Sampling_SchDoc	Size: A4
Engineer: Energy Infrastructure Team	Contact: http://www.ti.com/support	http://www.ti.com



COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED FOR PRODUCTION. 'DNP' COMPONENTS ARE NOT MANUFACTURED.
ASSEMBLY VARIANT: [No Variations]

REVISION: 1.0	DATE: 10/24/2019	BY: E1	DESCRIPTION: TIDA-010949 Power Optimizer
LAYER NAME = M18 Top Solder	TID #: TIDA-010949		
PLATTINUM TITANIUM Layer	Composited Version	GENERATED: 10/24/2019 10:56:57 AM	DESIGNED BY: TEXAS INSTRUMENTS

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Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Power1	CF-004	2.76mil		
	Dielectric 1	PP-006	2.80mil	4.1	
2	Ground1		2.76mil		
	Dielectric1	FR-4 High Tg	59.20mil	4.8	
3	Ground2		2.76mil		
	Dielectric 2	PP-006	2.80mil	4.1	
4	Power2	CF-004	2.76mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 7.874 MIL
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

☐ FR-4 ☒ FR-4 High Tg ☐ OTHER _____

THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER _____

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:

REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES

PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER _____

BOARD FINISH:

SILKSCREEN: ☒ TOP ☒ BOTTOM

SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____

SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER _____
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENERP
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER _____

ARRAY/PANEL: ☐ CUT AND TRM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: ☐ YES

BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

☒ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE: TIDA-010949	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010949 Power Optimizer.PcbDoc	
ENGINEER: Energy Infrastructure	LAYOUT BY: Energy Infrastructure
SCALE: 1.00	ALUM DESIGNER VERSION: 23.1.1.15