

A

B

C

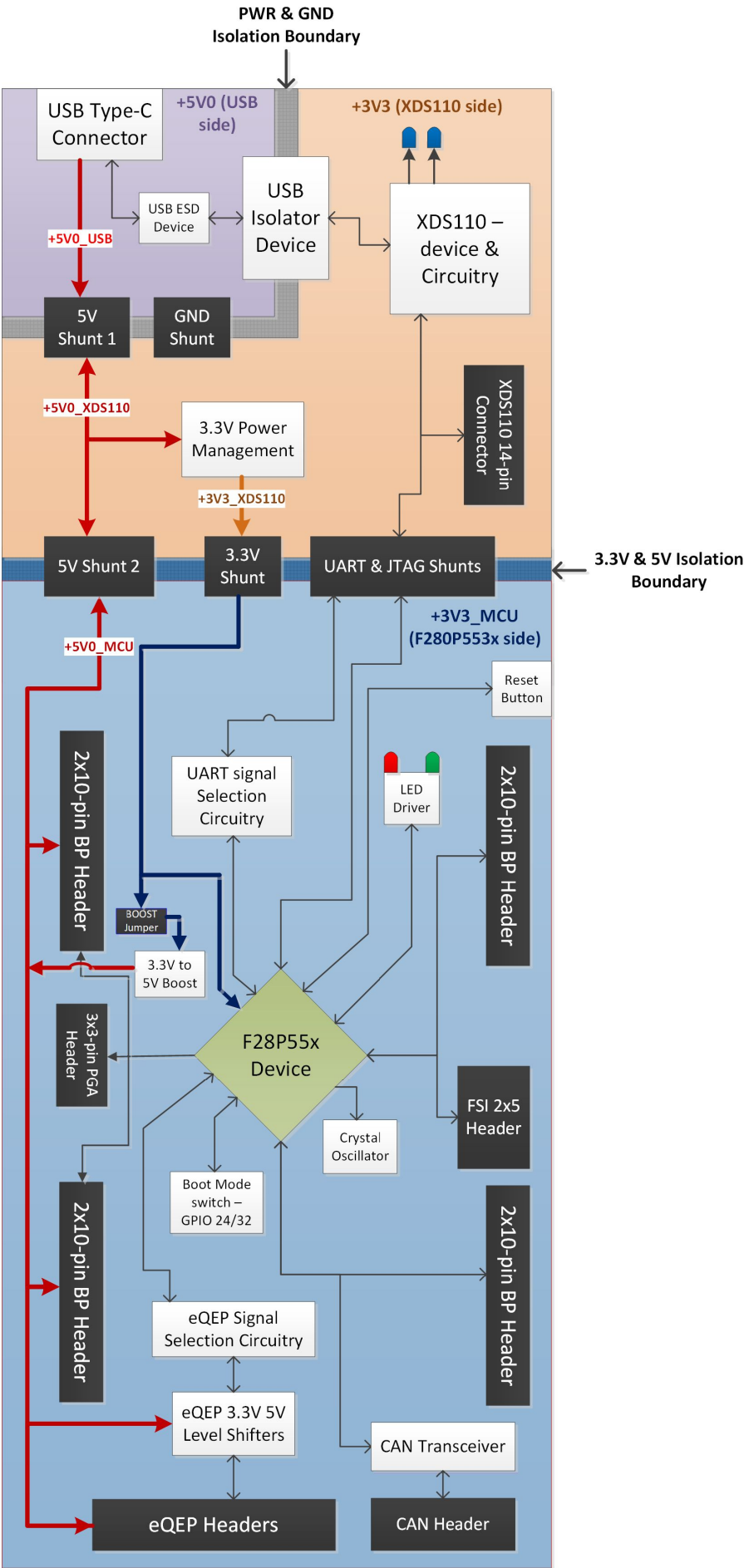
D

A


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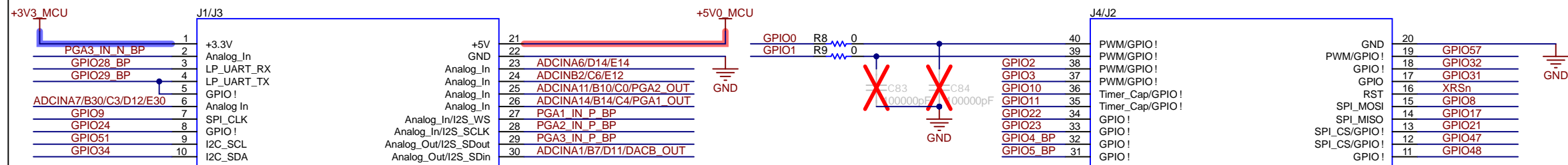
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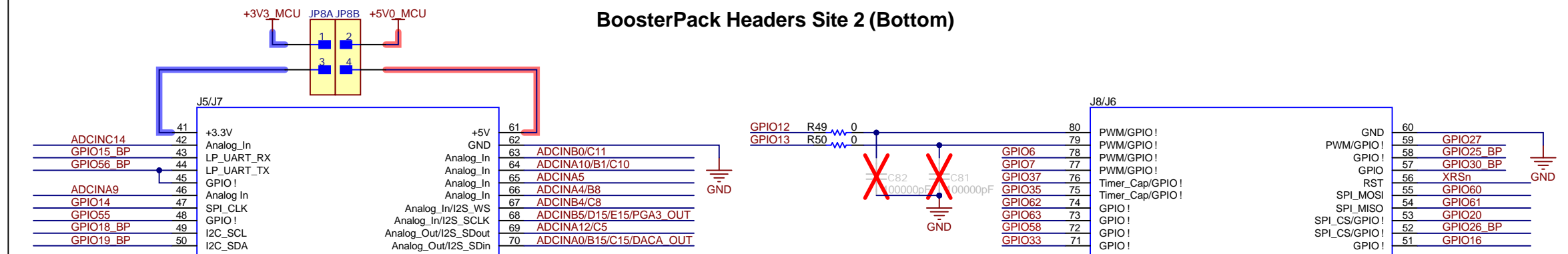
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Orderable: LAUNCHXL-F28P55X	Designed for: Public Release	Mod. Date: 2/20/2024	 http://www.ti.com © Texas Instruments 2024
TID #: N/A	Project Title: LAUNCHXL-F28P55X	Sheet: 1 of 8	
Number: MCU133	Rev: A	Size: B	
SVN Rev: Unknown revision	Assembly Variant: 001		
Drawn By: Stevan Duraskovic	File: MCU133A_Block_Diagram.SchDoc		
Engineer: Stevan Duraskovic	Contact: http://www.ti.com/support		

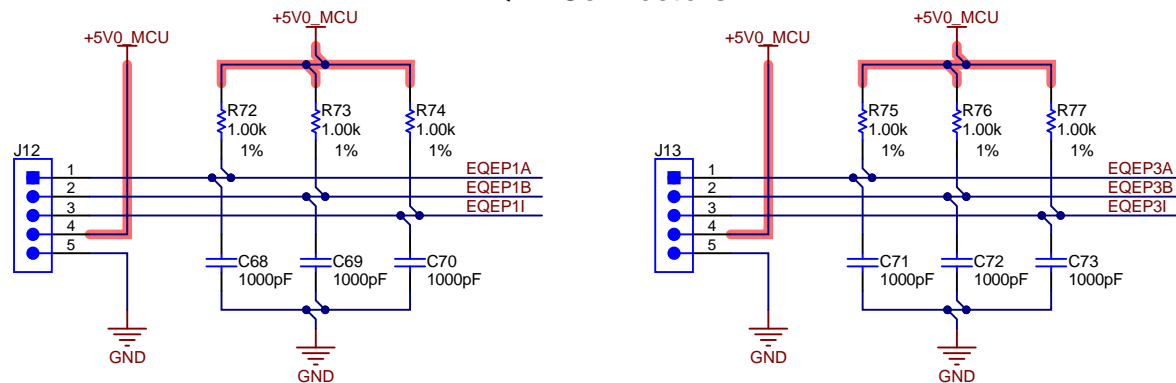
BoosterPack Headers Site 1 (Top)



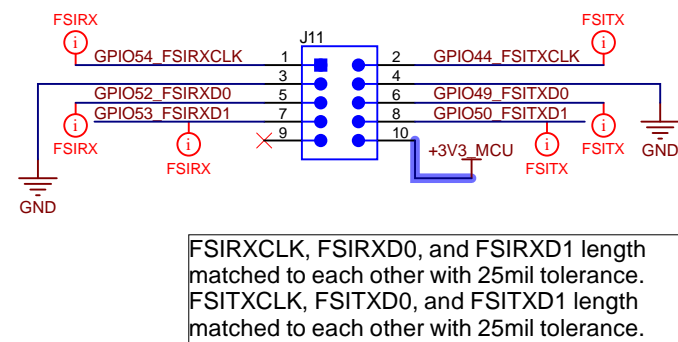
BoosterPack Headers Site 2 (Bottom)



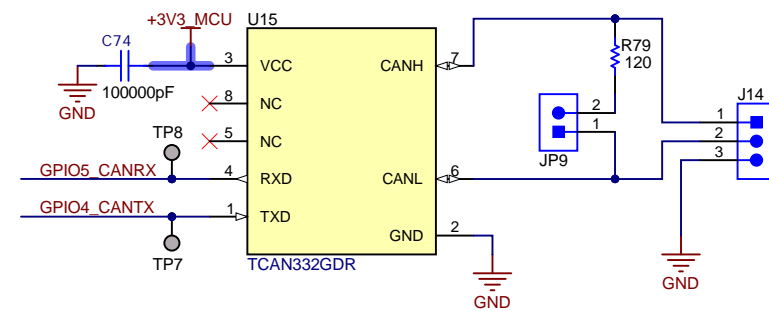
EQEP Connectors



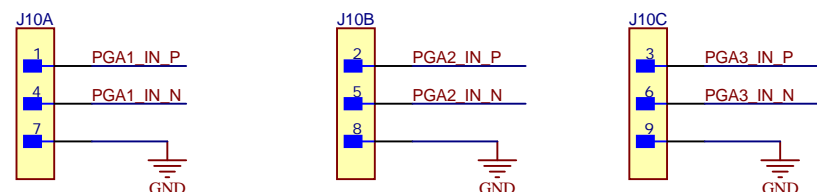
FSI Connector



CAN Transceiver & Connector



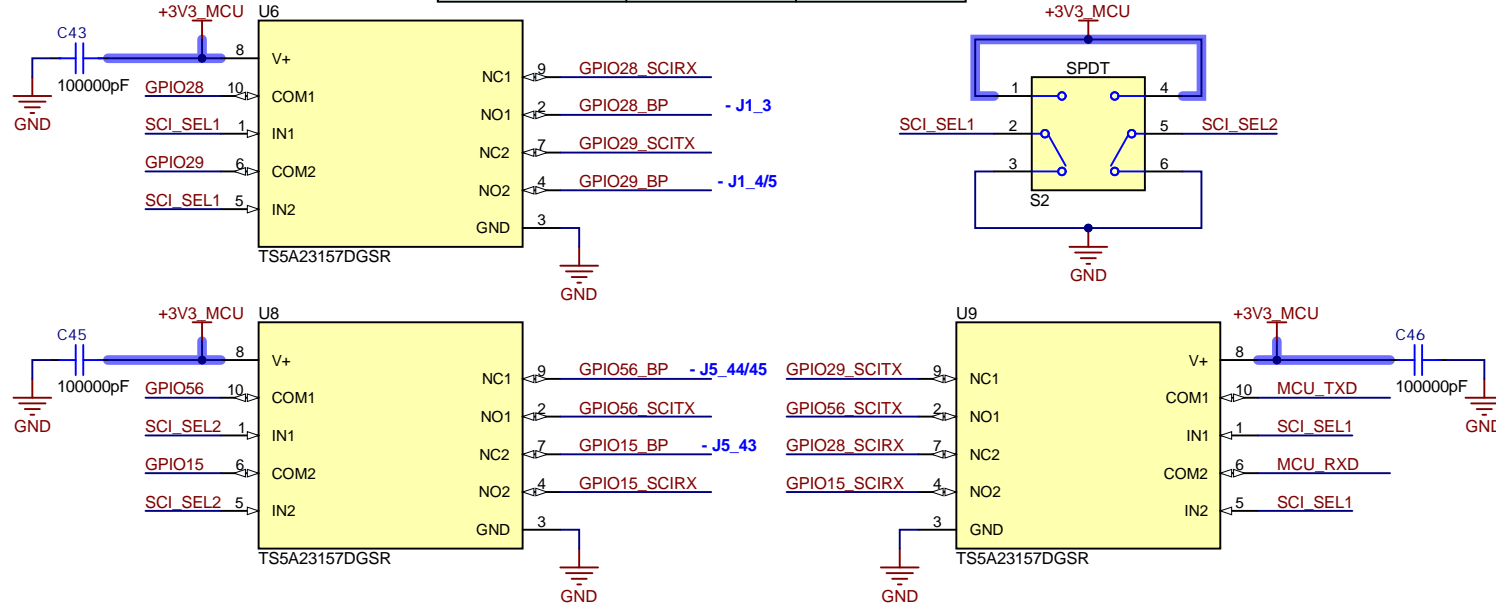
PGA Connector



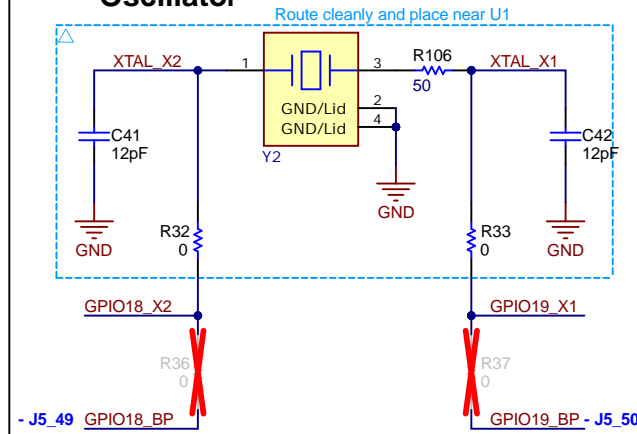
UART Routing

SCI_SEL1	SCI_SEL2	GPIO28/29 Route	GPIO15/56 Route
0	0	XDS110 COM Port	BP
0	1	XDS110 COM Port	NC
1	0	BP	BP
1	1	BP	XDS110 COM Port

- DEFAULT

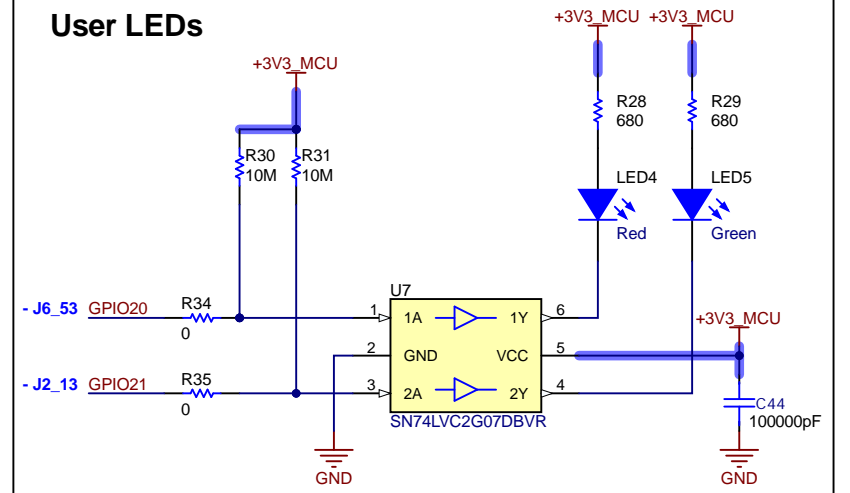


Oscillator

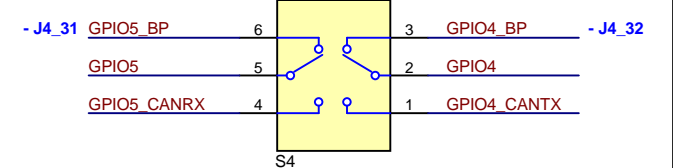


By default:
 - Crystal Y2 is connected between GPIO18_X2 and GPIO19_X1.
 - GPIO18_BP AND GPIO19_BP are connected to the BoosterPack headers.
 If GPIO18 and GPIO 19 are needed at the Boosterpac k Headers:
 - Remove R32 and R33, populate R36 and R37 with 0 ohm resistors
 - The F28P55x device's internal oscillator will need to be used

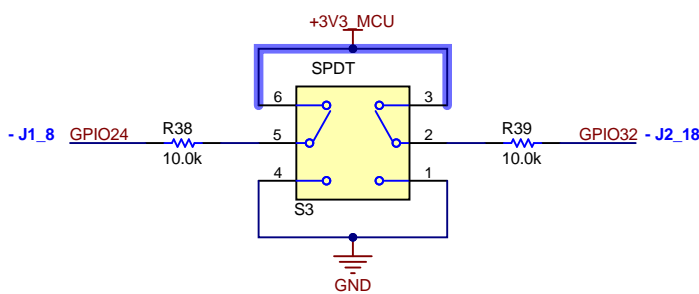
User LEDs



CAN Routing



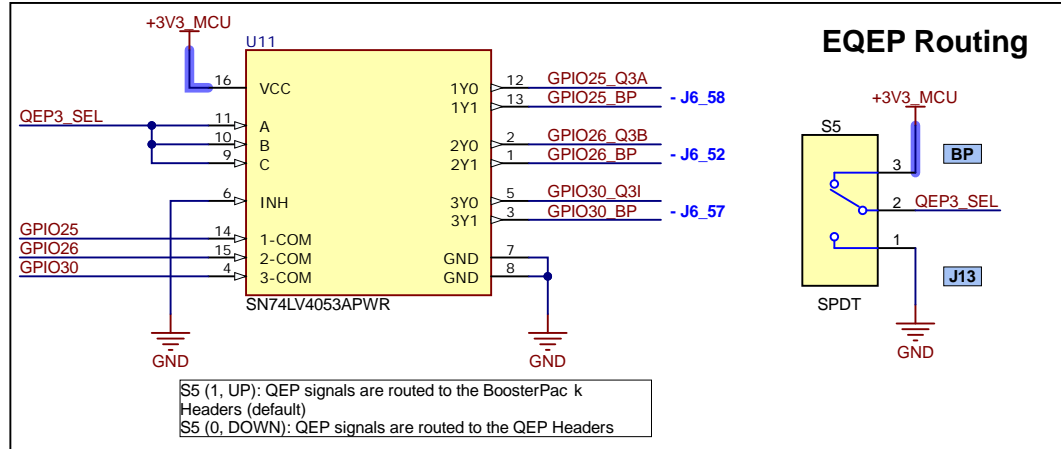
Boot Mode Select



Selected Boot Mode Chart

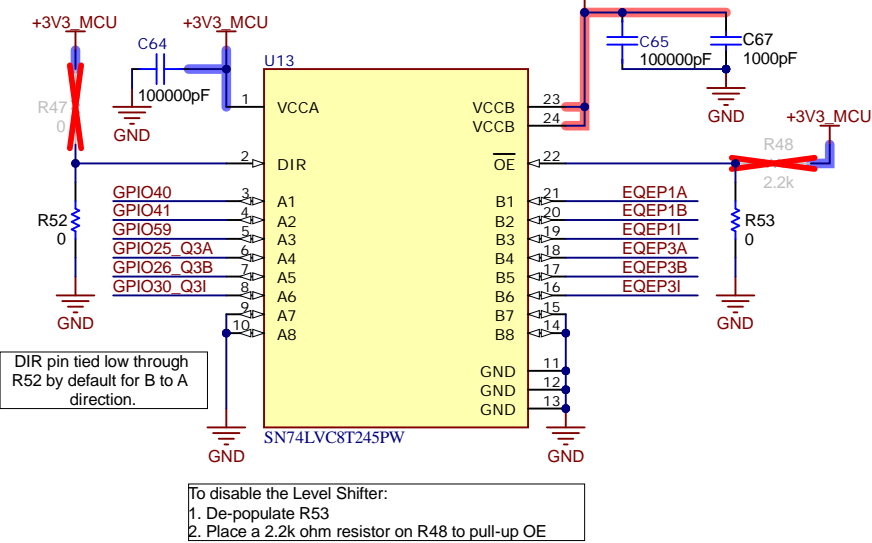
Mode #	GPIO24	GPIO32	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI / Wait Mode
02	1	0	Boot from CAN
03	1	1	Boot from Flash

EQEP Routing



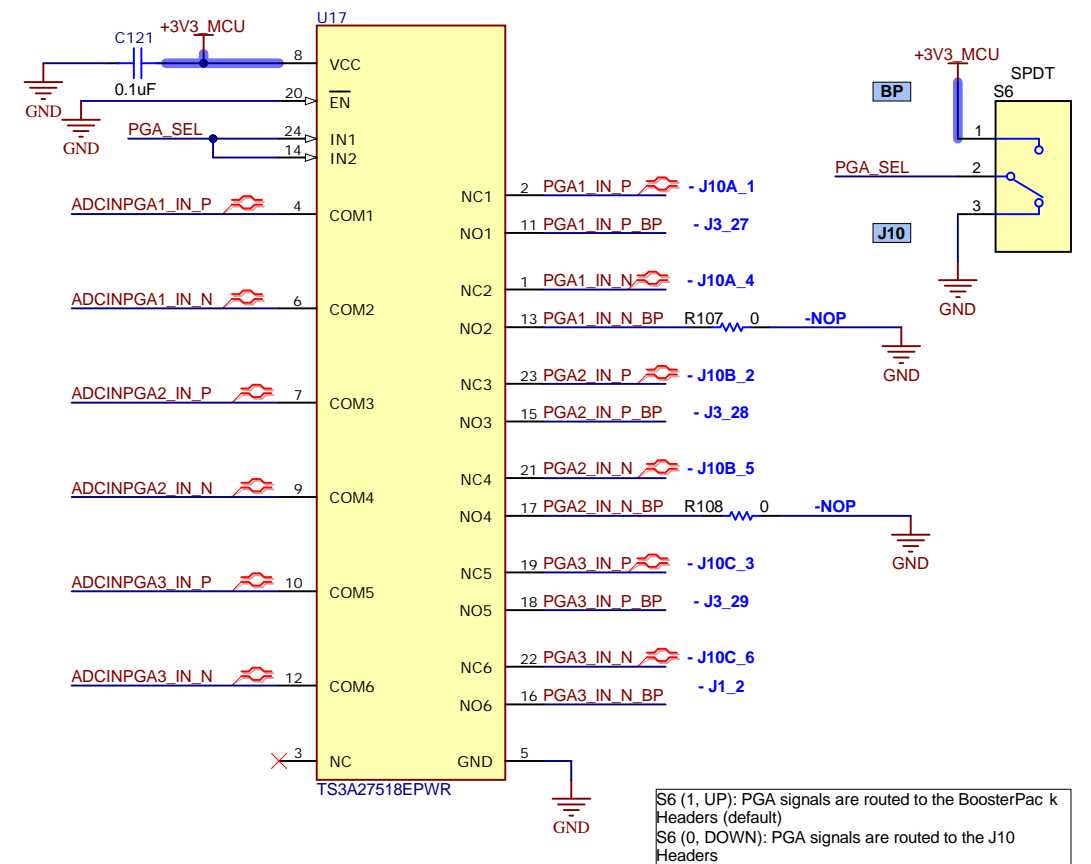
S5 (1, UP): QEP signals are routed to the BoosterPac k Headers (default)
 S5 (0, DOWN): QEP signals are routed to the QEP Headers

EQEP Level Shifter



To disable the Level Shifter:
 1. De-populate R53
 2. Place a 2.2k ohm resistor on R48 to pull-up OE

PGA Routing

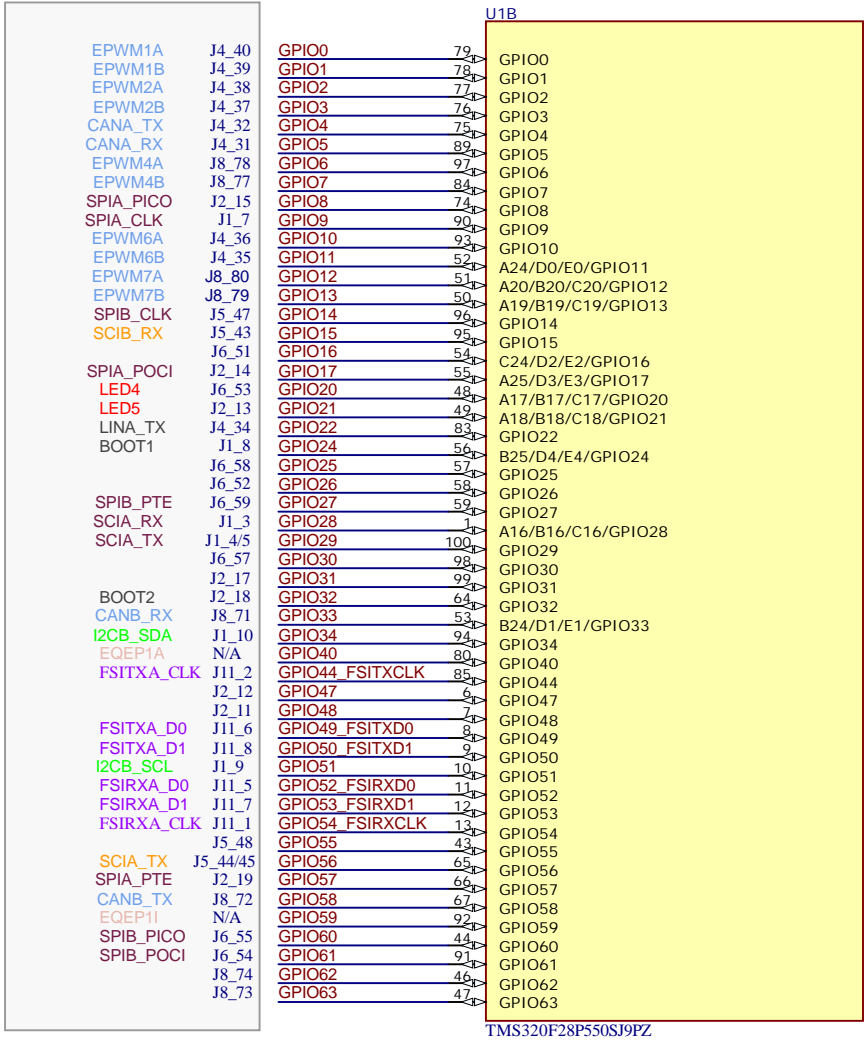
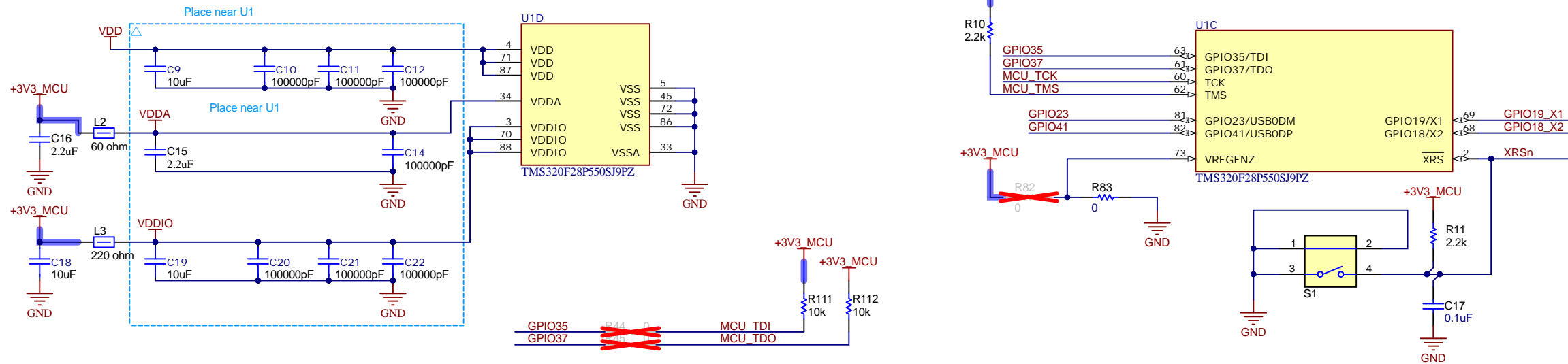


S6 (1, UP): PGA signals are routed to the BoosterPac k Headers (default)
 S6 (0, DOWN): PGA signals are routed to the J10 Headers

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Orderable: LAUNCHXL-F28P55X	Designed for: Public Release	Mod. Date: 3/1/2024
TID #: N/A	Project Title: LAUNCHXL-F28P55X	
Number: MCU133	Rev: A	Sheet Title:
SVN Rev: Unknown revision	Assembly Variant: 001	Sheet: 3 of 8
Drawn By: Stevan Duraskovic	File: MCU133A_AltRouting_Misc.SchDoc	Size: B
Engineer: Stevan Duraskovic	Contact: http://www.ti.com/support	

F28P55x Device



A

B

C

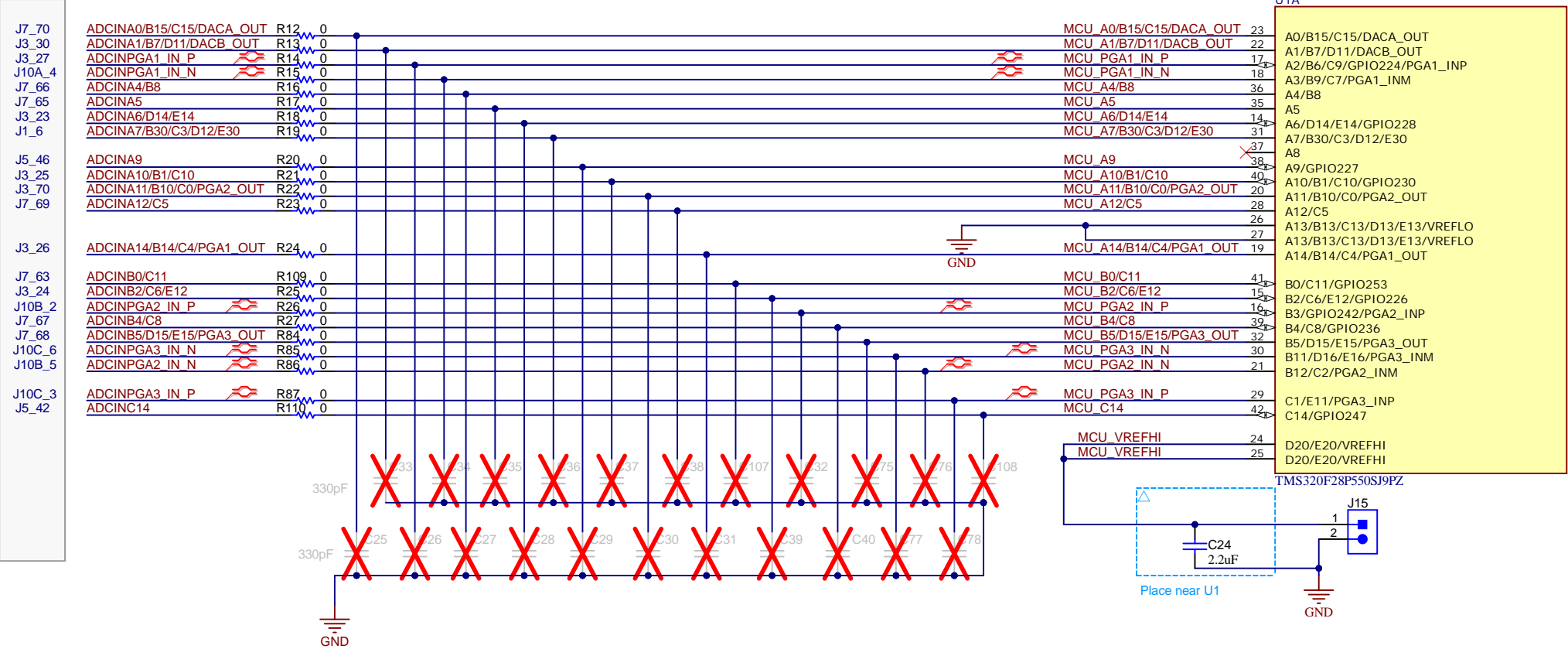
D

A

B

C

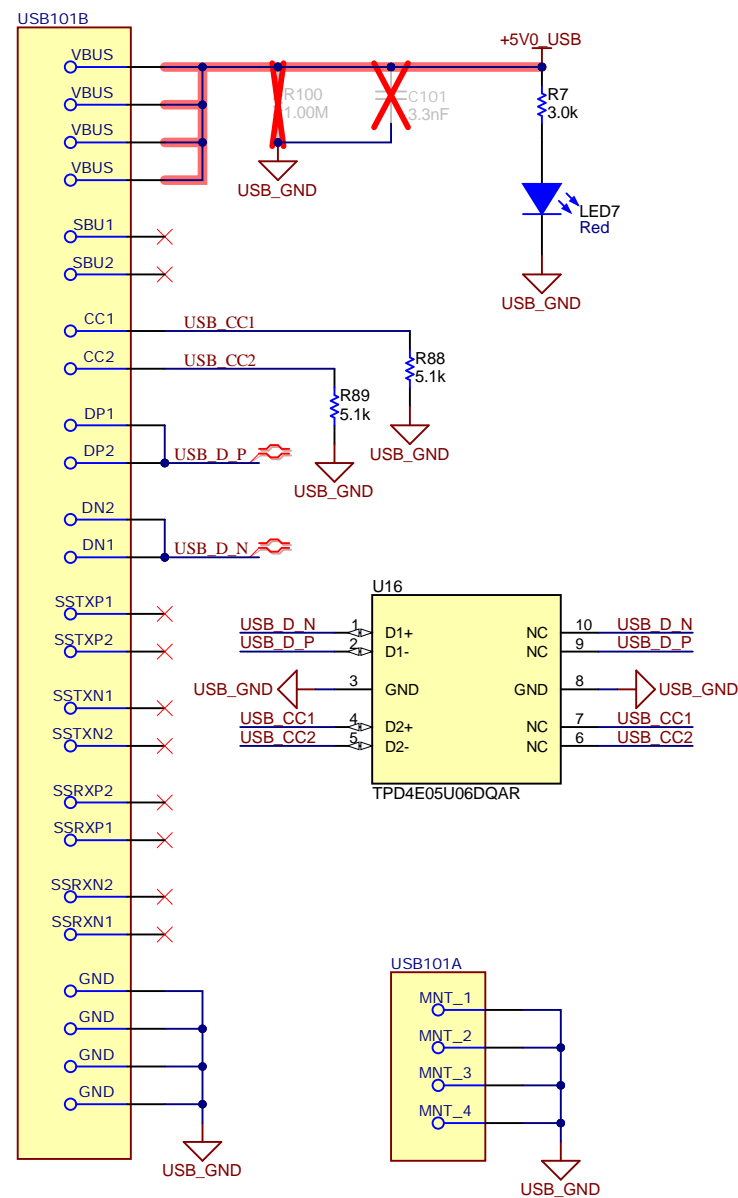
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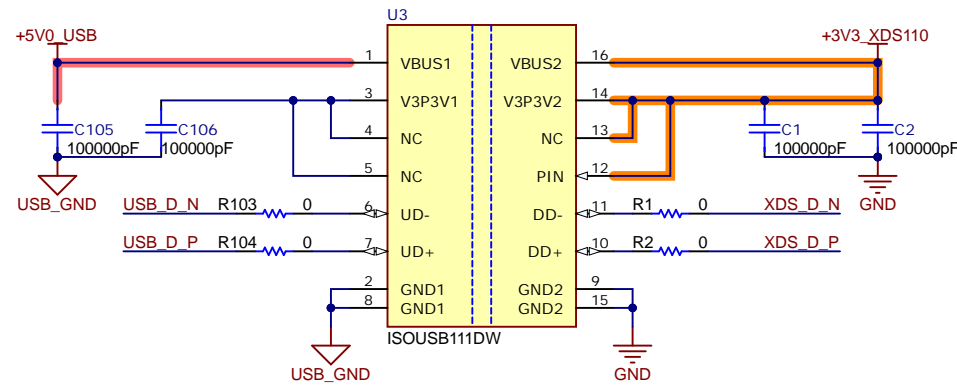
F28P55X ADC Pins

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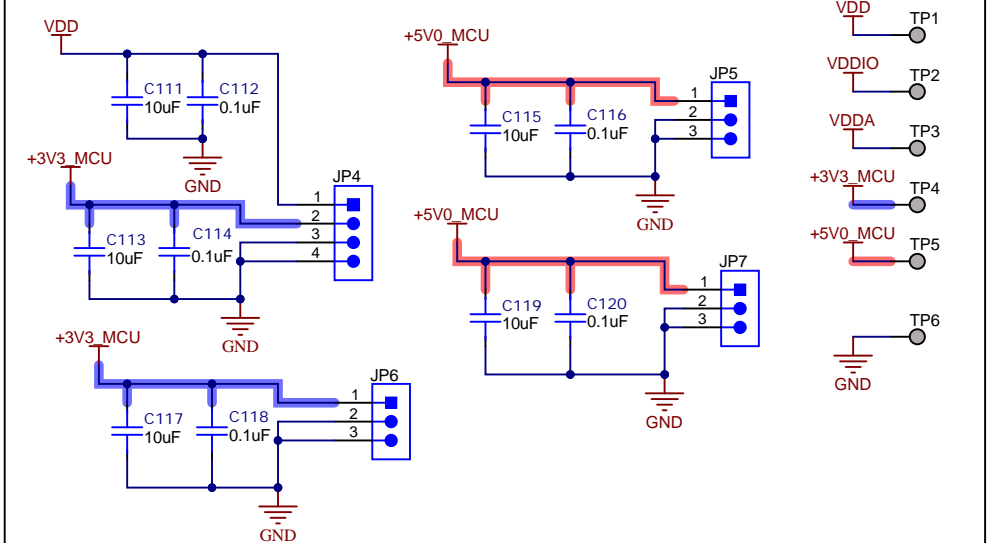
USB-C Connector



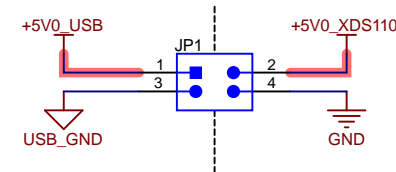
USB Isolation



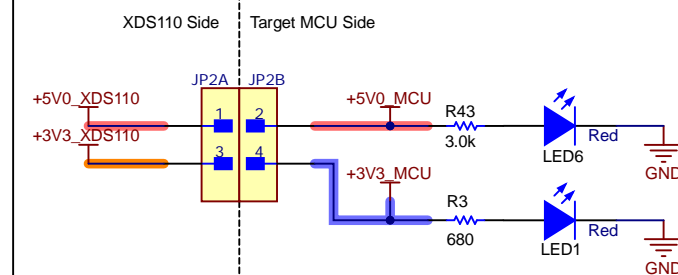
Power Headers and Test Points



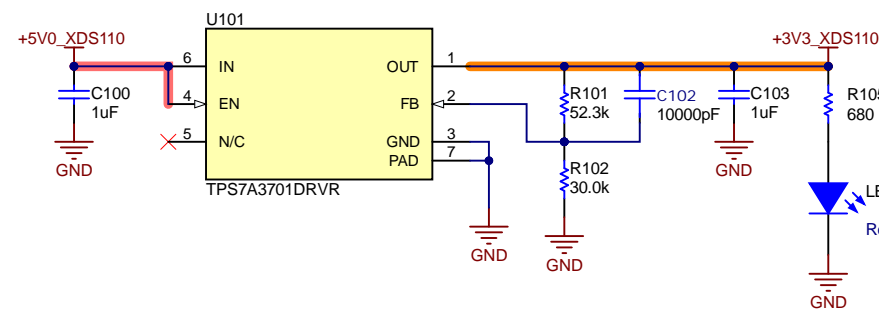
PWR & GND Isolation Boundary



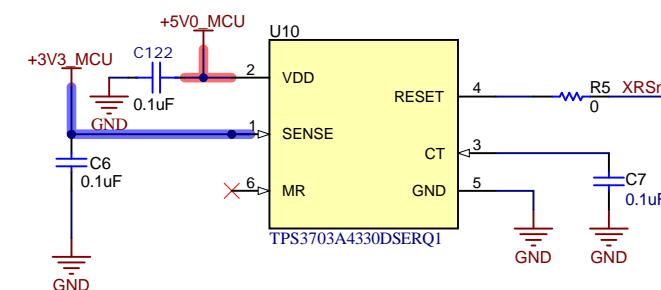
5V & 3.3V Isolation Boundary



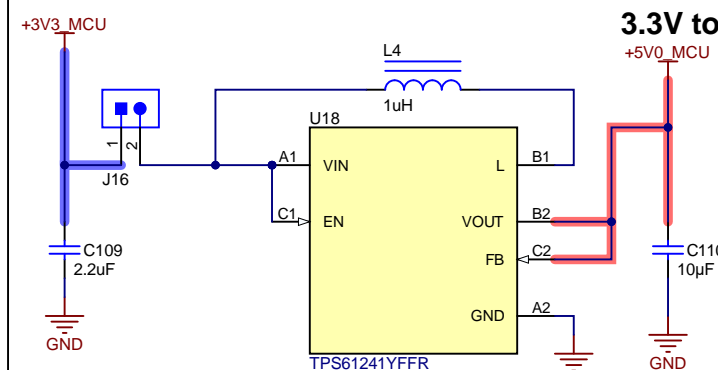
5V to 3.3V



System Supervisory Circuit



3.3V to 5V BOOST



A

B

C

D

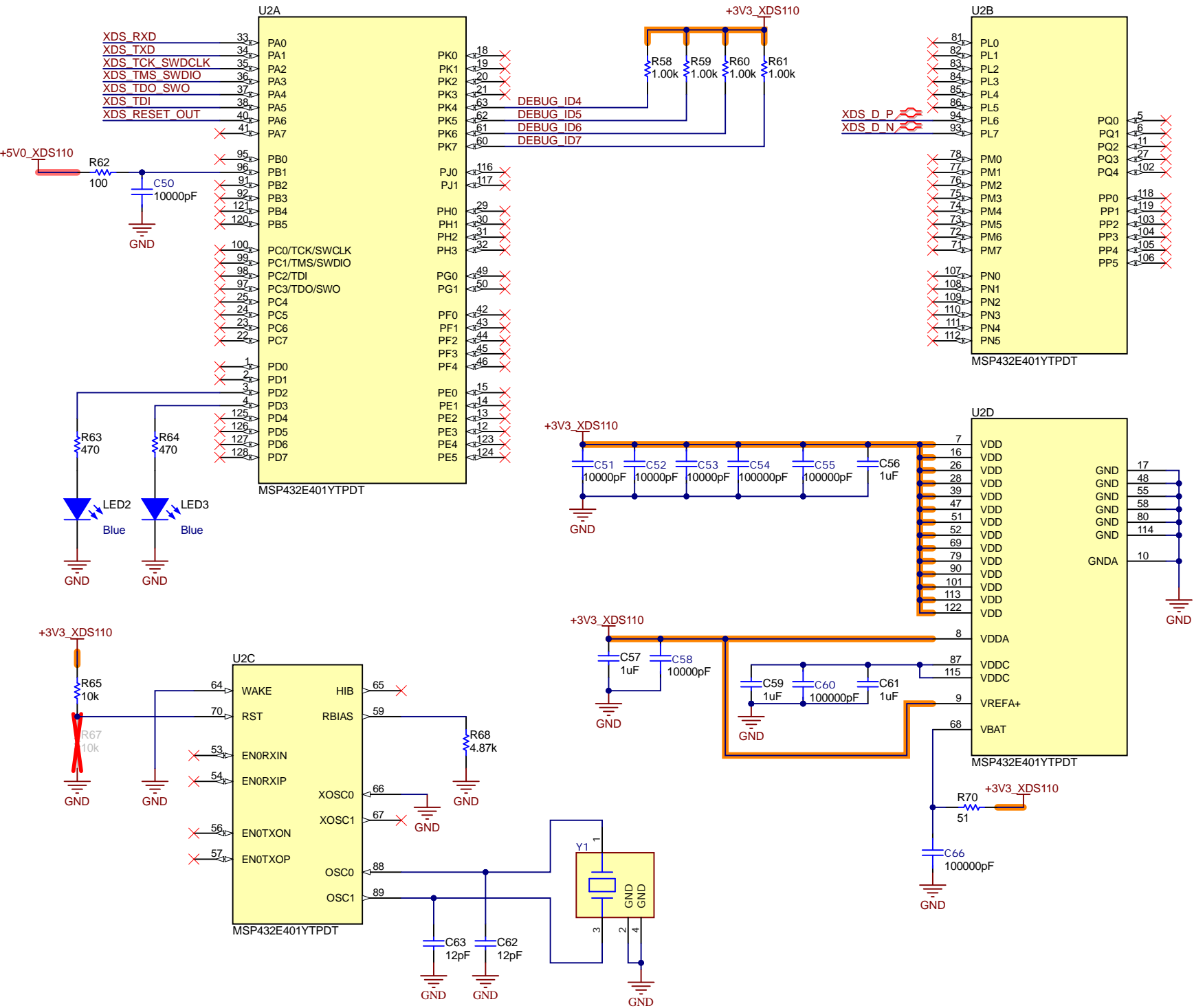
A

B

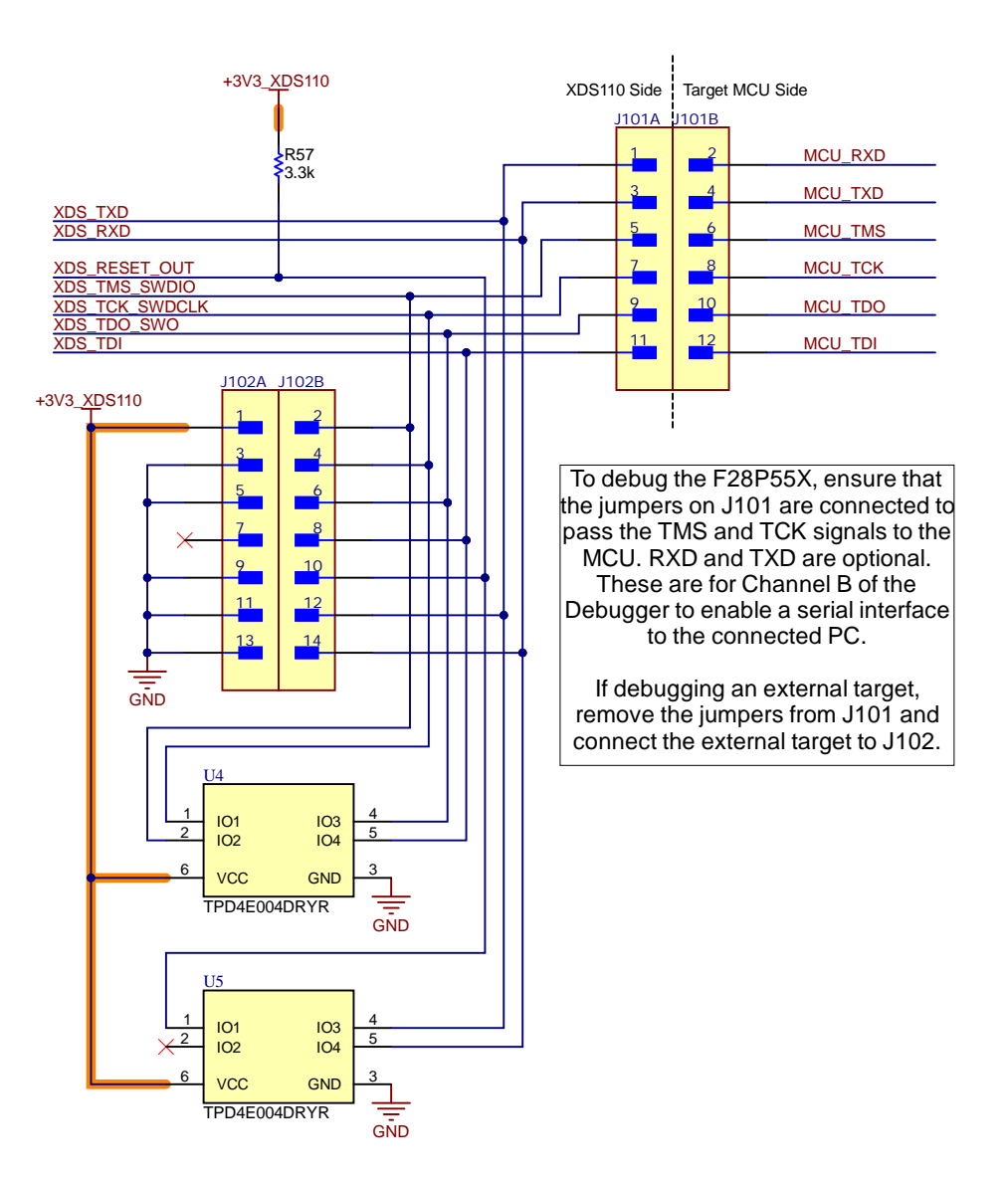
C

D

XDS110 Device




XDS110 Target Interface



To debug the F28P55X, ensure that the jumpers on J101 are connected to pass the TMS and TCK signals to the MCU. RXD and TXD are optional. These are for Channel B of the Debugger to enable a serial interface to the connected PC.

If debugging an external target, remove the jumpers from J101 and connect the external target to J102.

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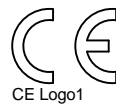


MH1 MH2

MH3 MH4

PCB Number: MCU133
PCB Rev: A

Logo1
PCB
LOGO
Texas Instruments



Logo3
PCB
LOGO
FCC disclaimer

Logo4
PCB
LOGO
WEEE logo

Logo5
PCB
LOGO
Texas Instruments



ZZ1

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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TID #: N/A	Project Title: LAUNCHXL-F28P55X			
Number: MCU133	Rev: A	Sheet Title:		
SVN Rev: Unknown revision		Assembly Variant: 001		Sheet: 8 of 8
Drawn By: Stevan Duraskovic		File: MCU133A_Hardware_SchDoc		Size: B
Engineer: Stevan Duraskovic		Contact: http://www.ti.com/support	http://www.ti.com © Texas Instruments 2024	