

# DISCLAIMER

\* TSU6111

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## File Description

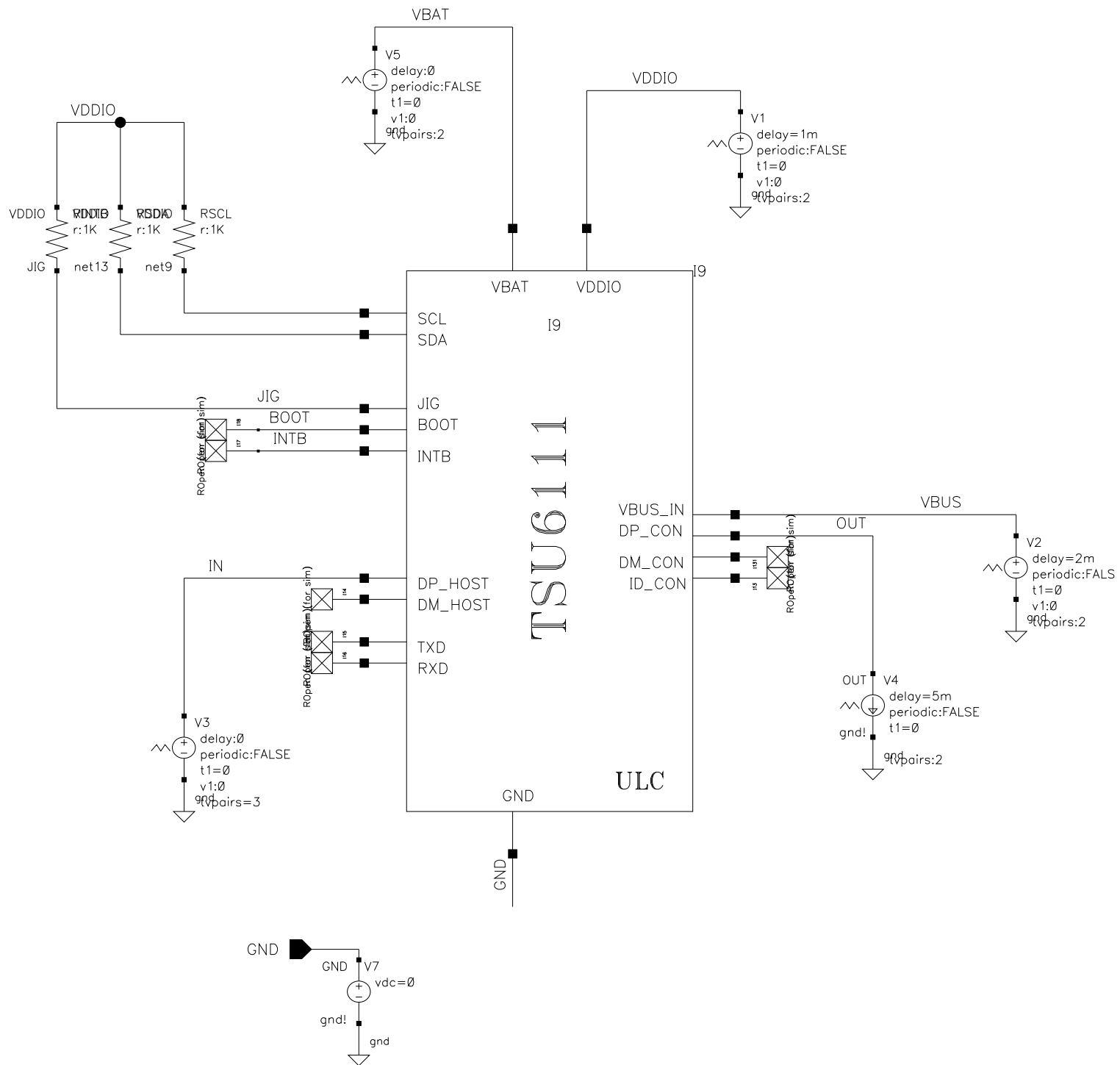
‘TSU6111\_ron\_usb\_tb.sp-which is the test bench- invokes other 2 files:

‘TSU6111\_subckts\_enc.sp’ –subcircuits’ definition, and ‘process\_models\_enc.lib’ –nominal  
process library; the latter one also invokes a veriloga script.

## **Instructions**

- 1) Open your simulator HSPICE -- E-2010.12 32-BIT on Linux
- 2) On the file menu, open and run file 'TSU6111\_ron\_usb\_tb.sp.

Plots of the test-setup schematic and simulation results are shown below:



# TSU6111: Hspice Simulation for Rds(on)

