

NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P12V" represents connection to the +12V power plane.
2. The netname "P3P3V" represents connection to the +3.3V power plane.
3. The netname "P1P8V" represents connection to the +1.8V digital power plane.
4. The netname "P1P15V" represents connection to the +1.15V power plane.
5. The netname "P1P8V_A" represents connection to the +1.8V controller analog supply power plane.
6. The netname "GND" represents connection to the ground plane.
7. A "Z" suffix on a signal name indicates an active low signal.
8. All components with designators "U", "Q", and "D" are electrostatic discharge sensitive.



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REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2139077: Initial Release	2/18/2014	
B	ECO 2141121: Updated to rev B	4/8/2014	
C	ECO 2142182: Updated to rev C	5/28/2014	
D	ECO 2143315: Updated to rev D	8/11/2014	

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		ENGR		12/13/2019			
		APVD		12/13/2019			
		MFG	XXXXXXXXXX		TITLE ESD, Single DLPC900 Hi-Res Main Board Reference Design		
	0314PO	QA	XXXXXXXXXX				
NEXT ASSY	USED ON				A3	DRAWING NO	2513756
APPLICATION		SW	Cadence 16.5		SCALE		SHEET 1 of 20
							REV H

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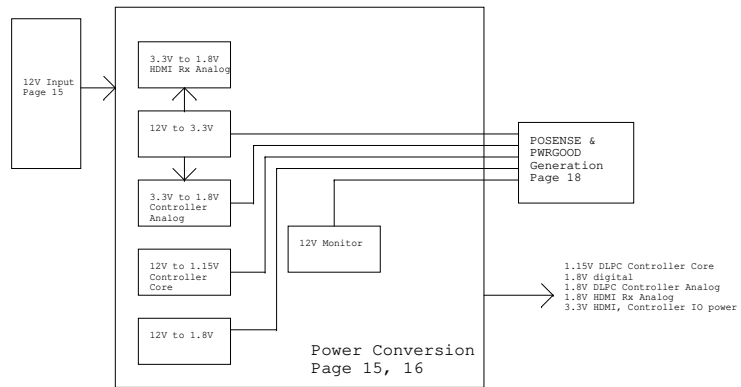
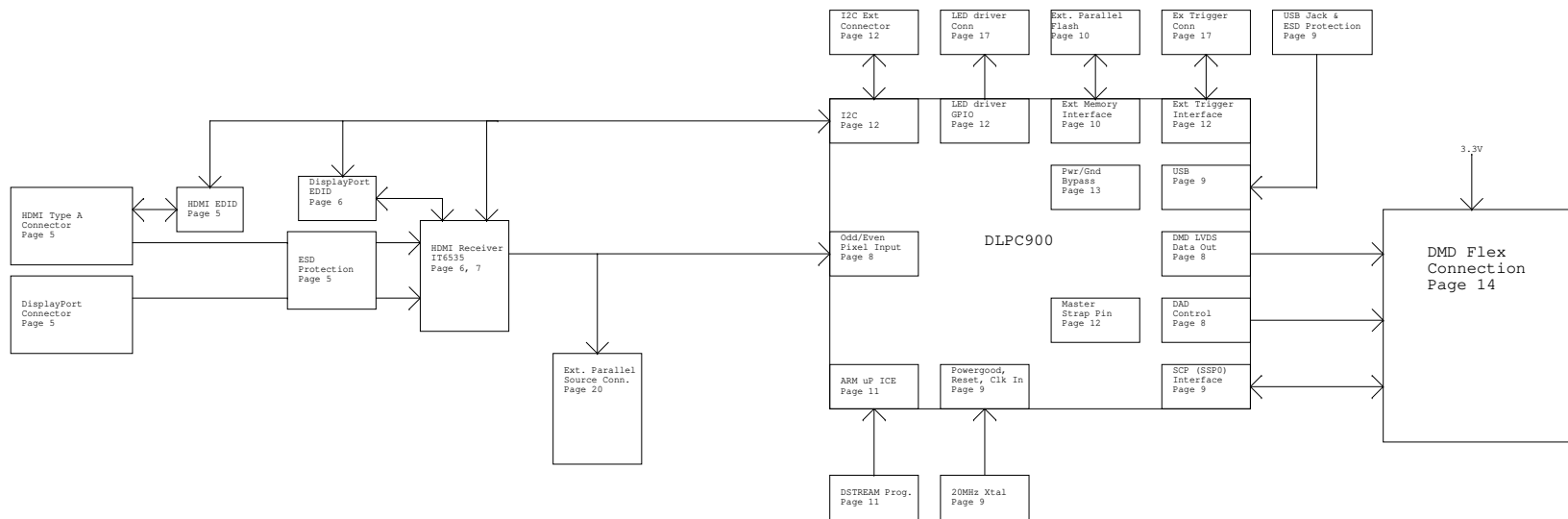
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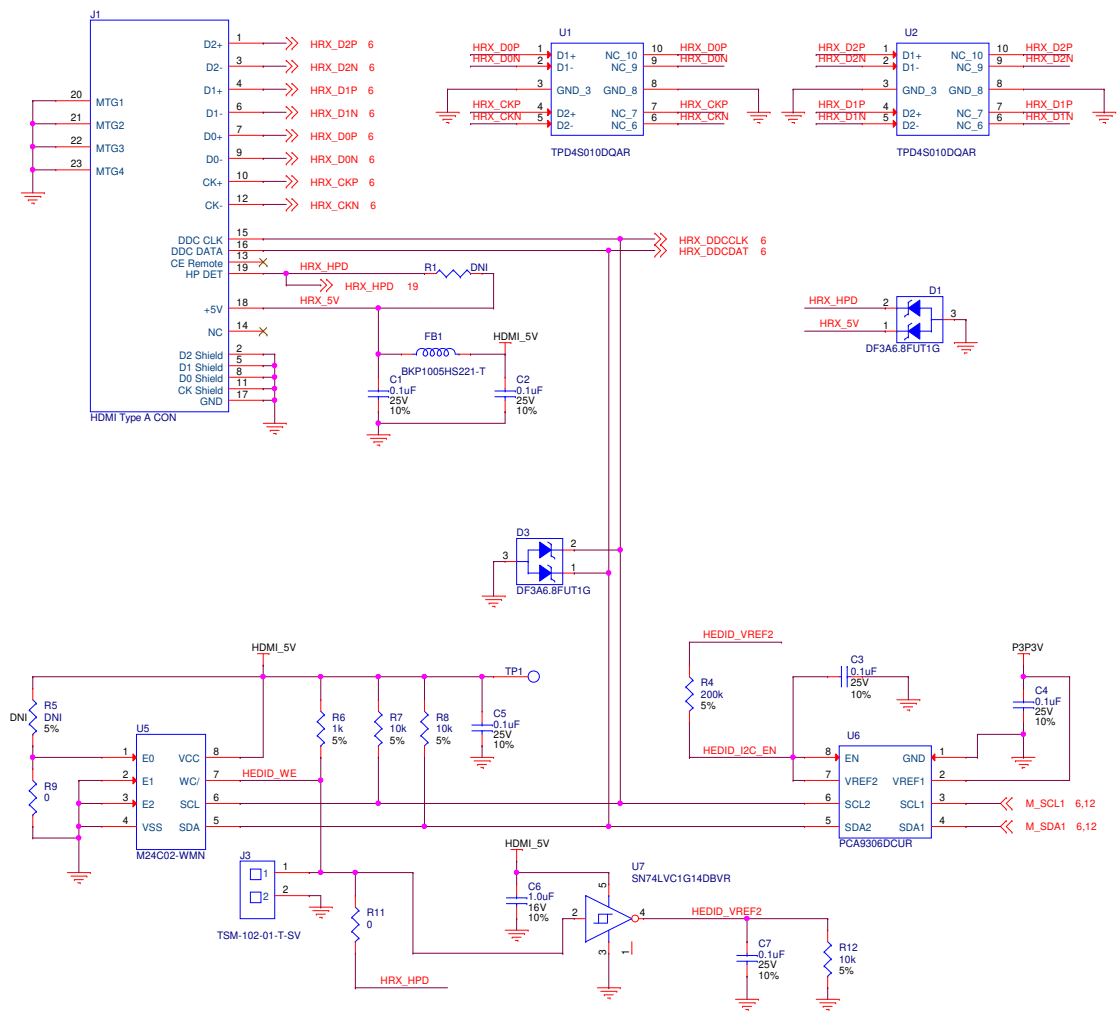
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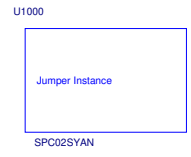
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9	DLPC Controller: USB, Reset/Clock, SSP0
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11	DLPC Controller: JTAG, ICE interface
12	DLPC Controller: I2C, Dual Controller ports, Trigger GPIOs
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16	Power Conv: LDOs
17	Input/output triggers, LED driver connector
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19	Notes & Revision History

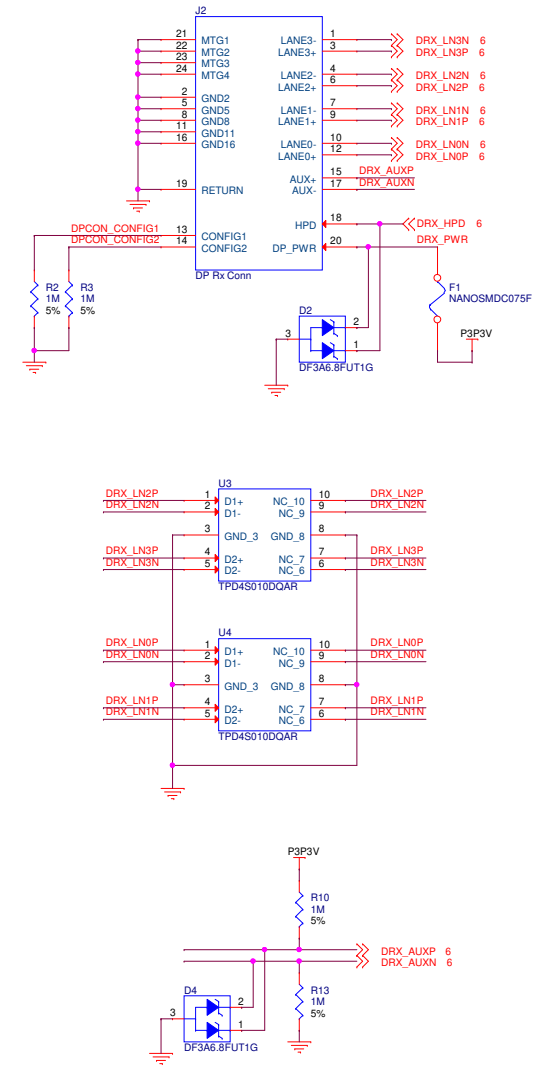




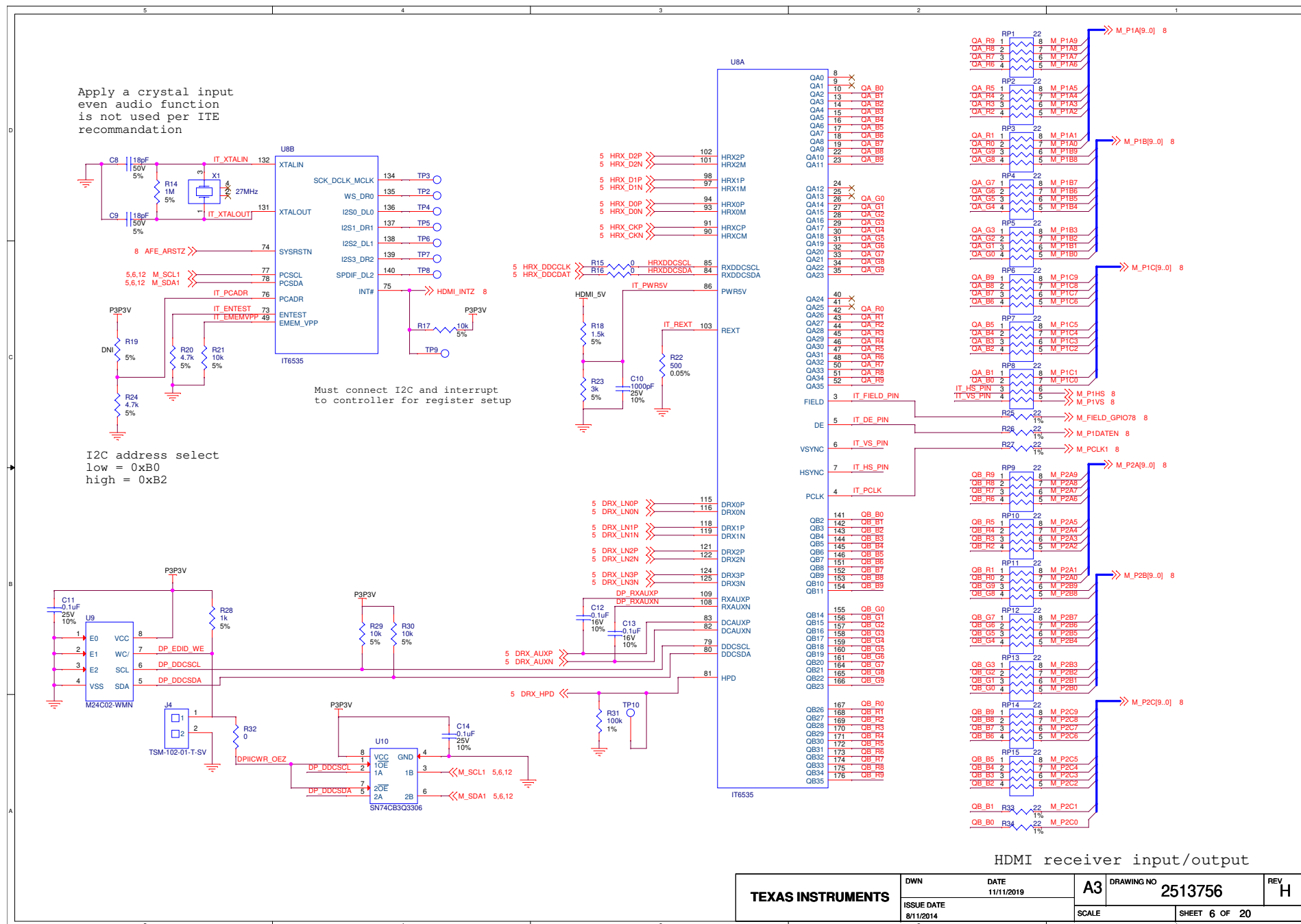
To program HDMI EDID
 - install jumper to enable PROM write and disable hot plug detect
 - connect HDMI cable to supply 5V
 - use TI control program to update EDID

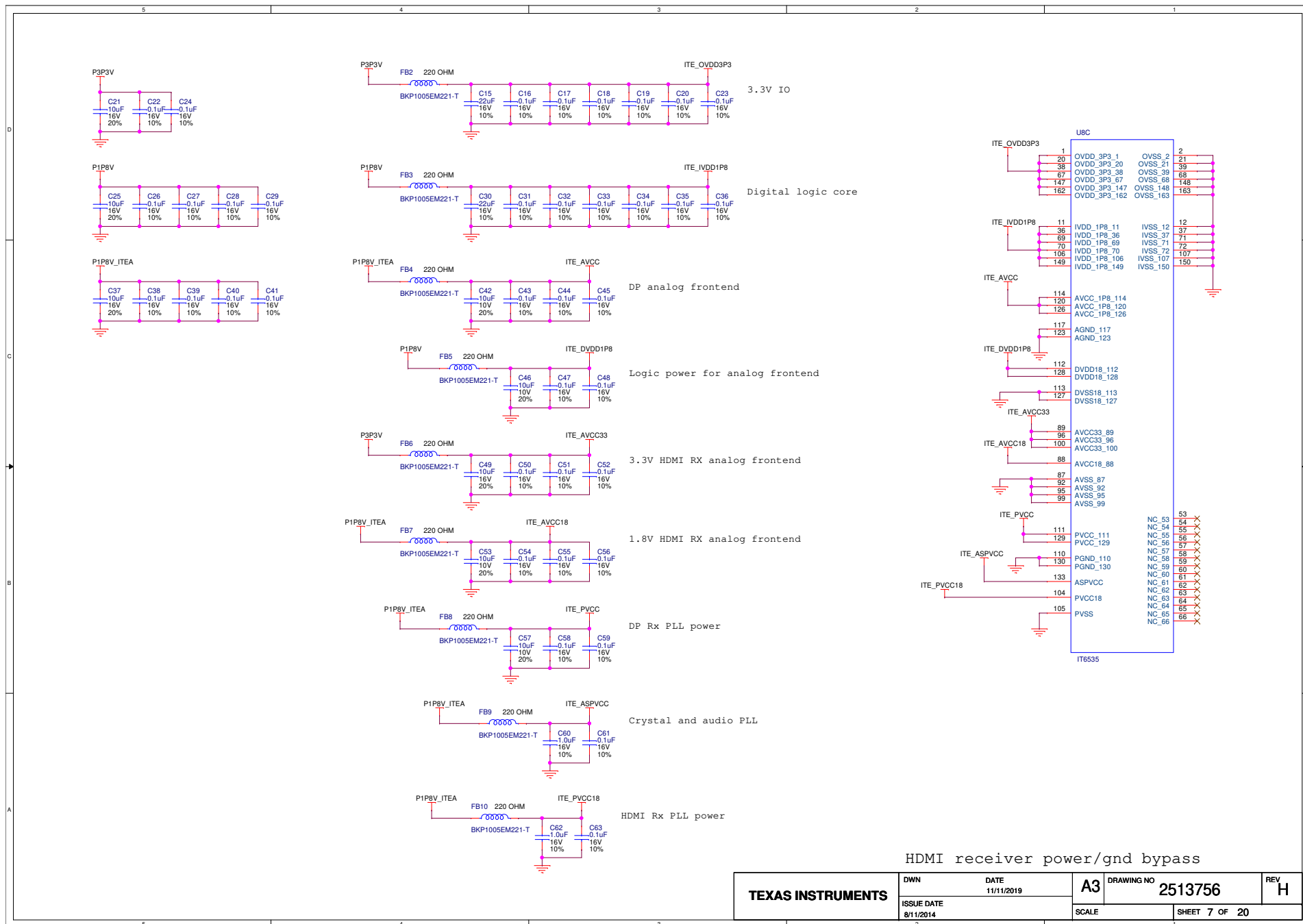


HDMI TypeA Rx Conn, ESD, and EDID



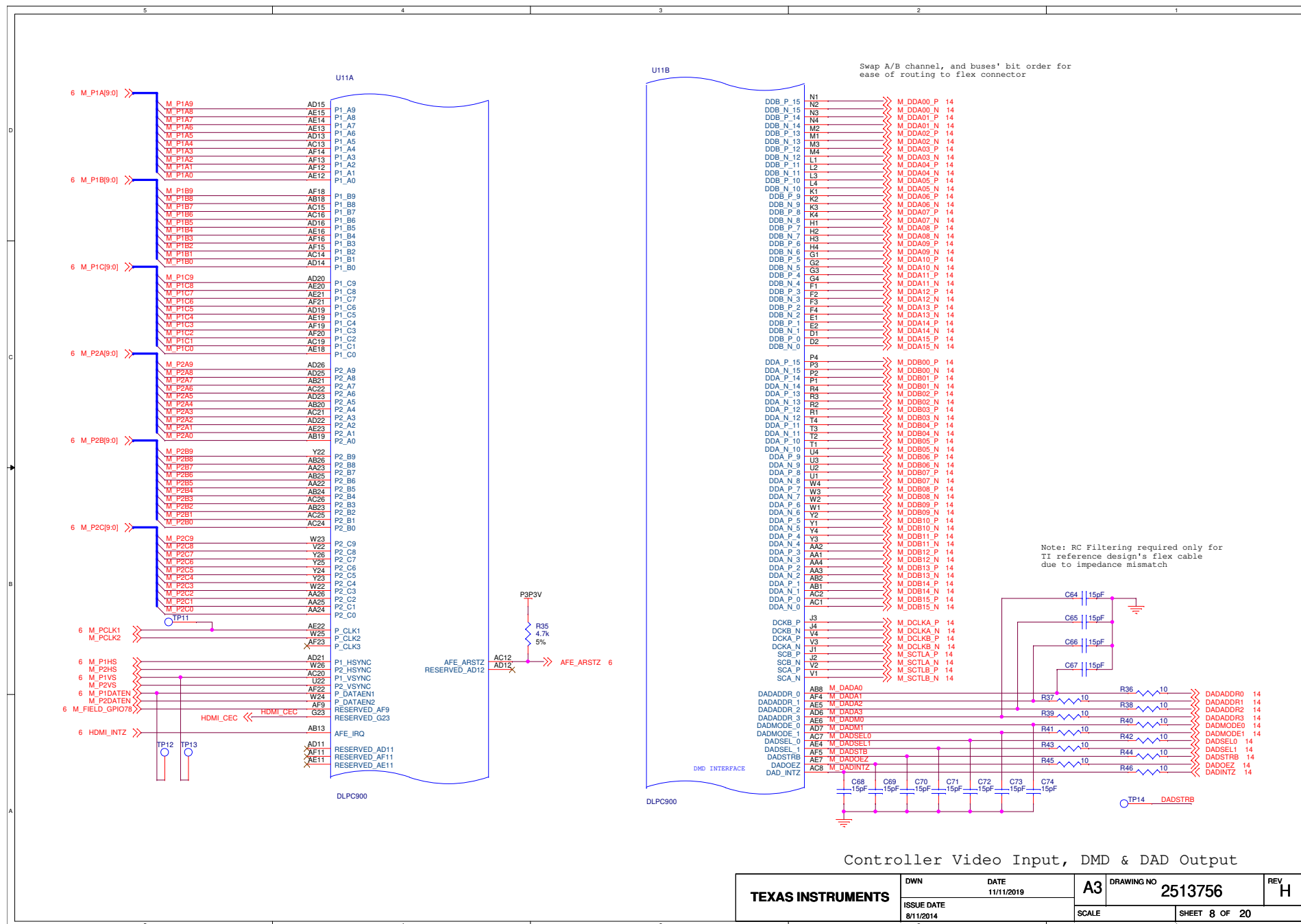
DisplayPort Rx Conn, ESD

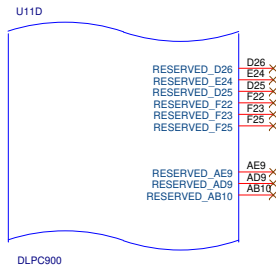




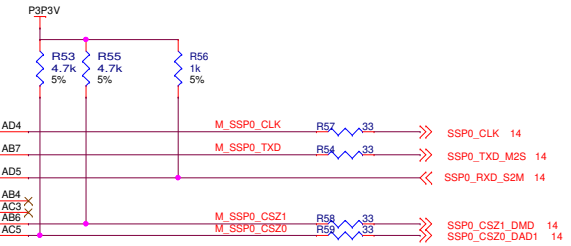
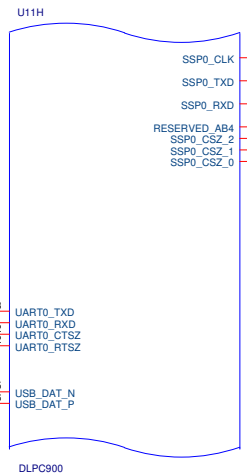
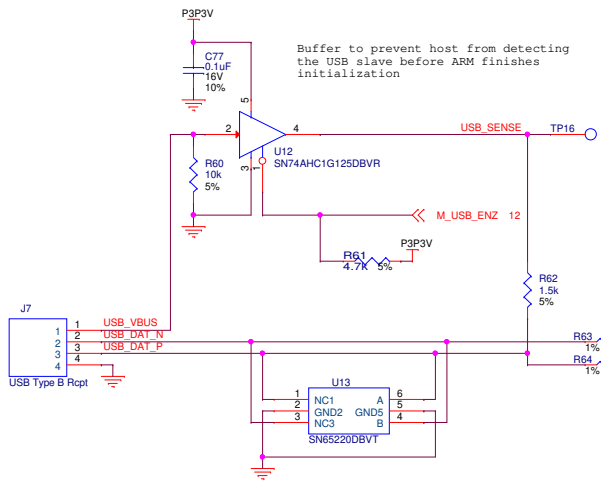
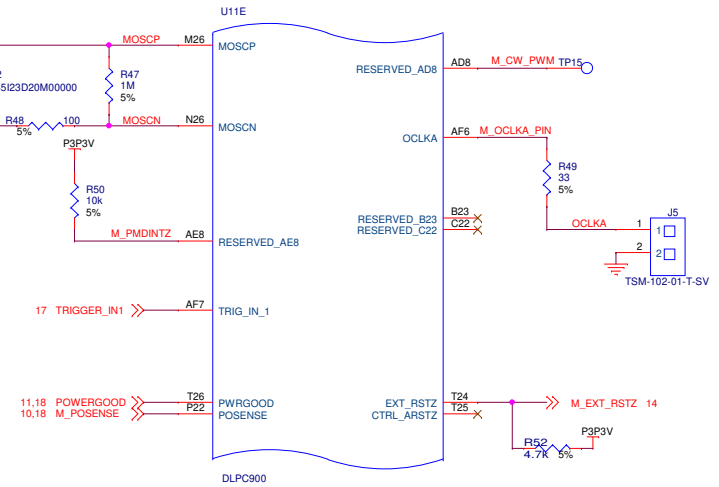
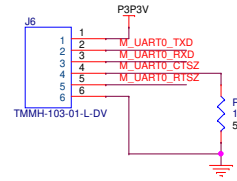
HDMI receiver power/gnd bypass

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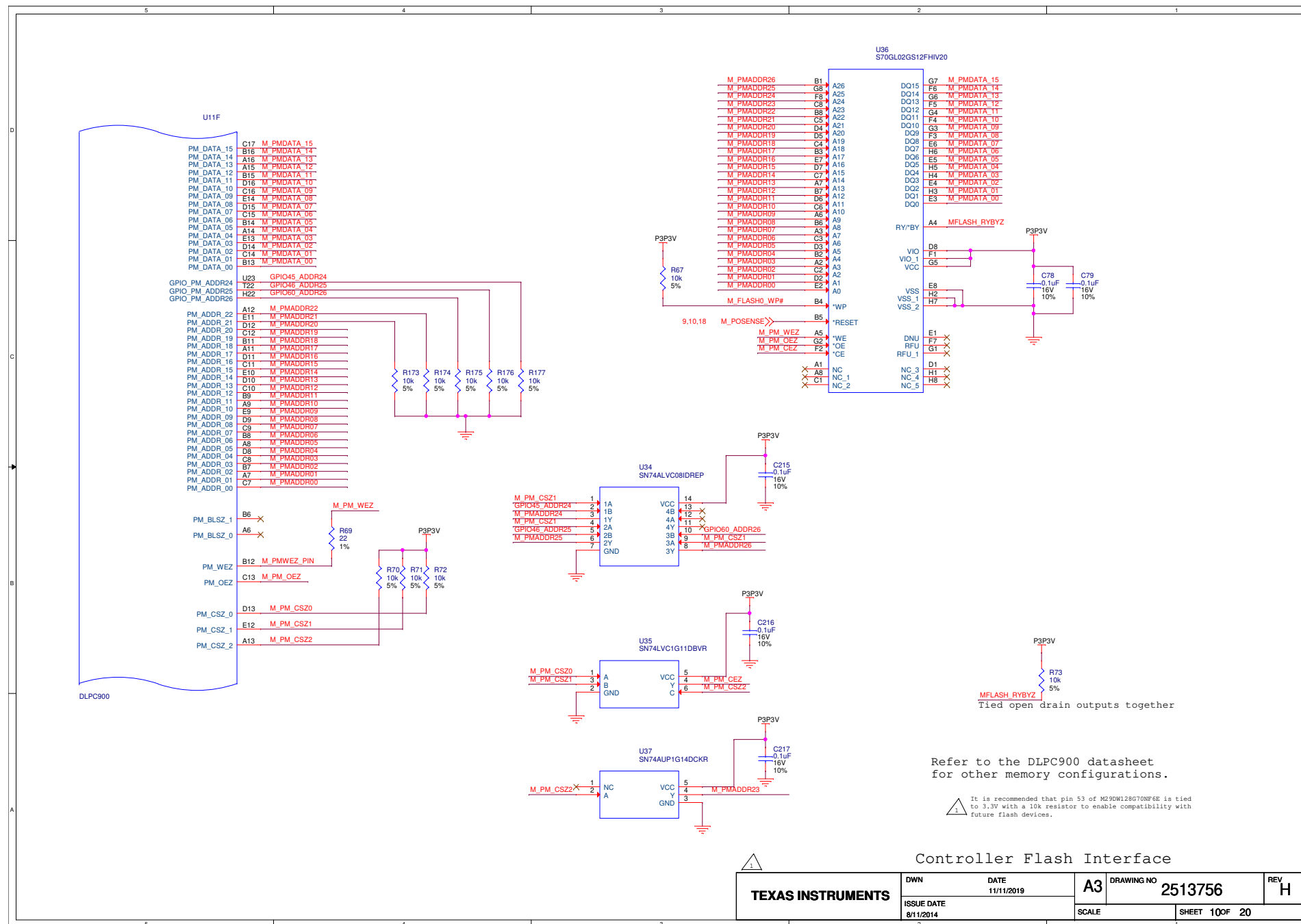


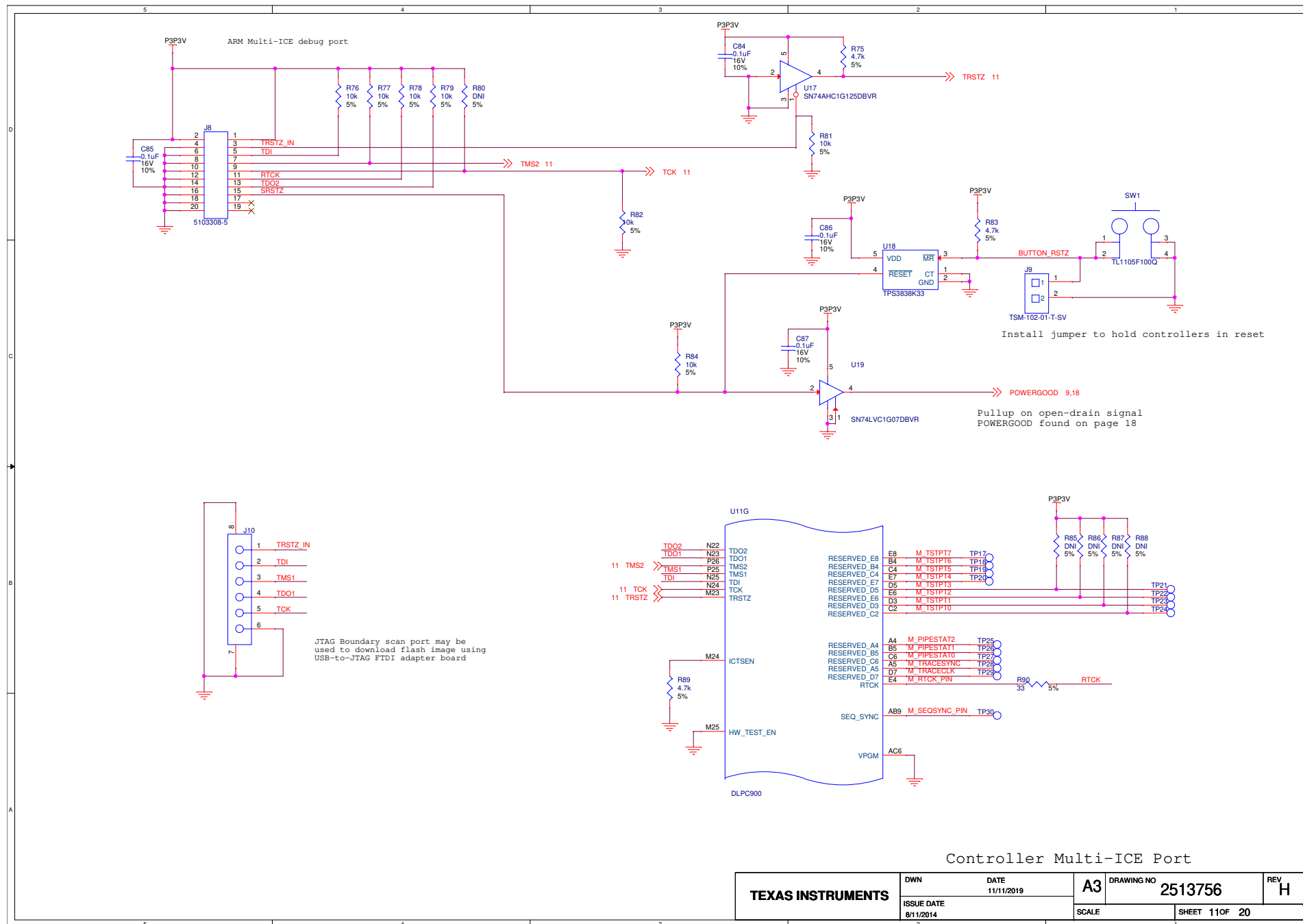
UART debug message port,
not needed for production

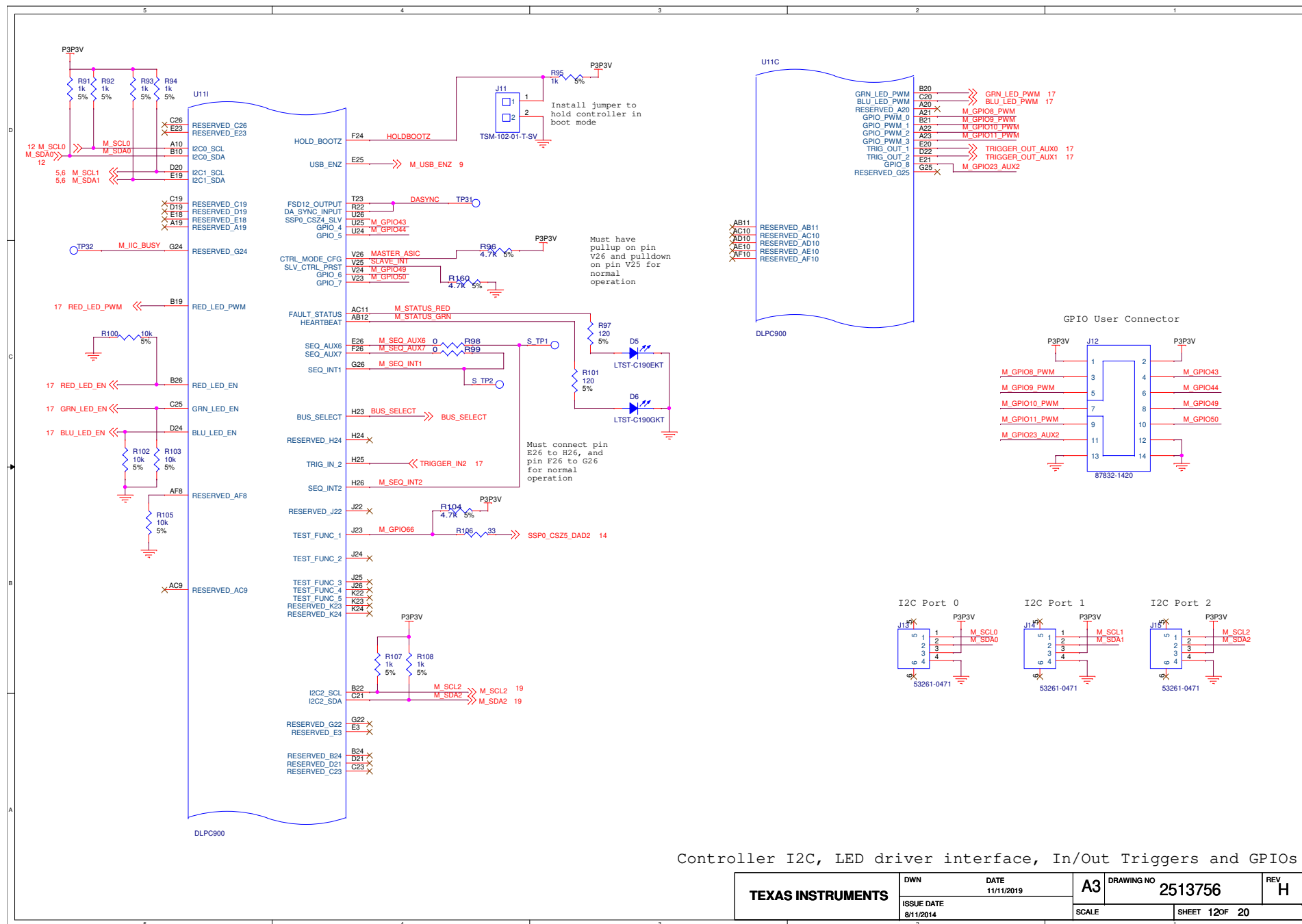


Controller SSP0, UART0, USB, Reset, OSC

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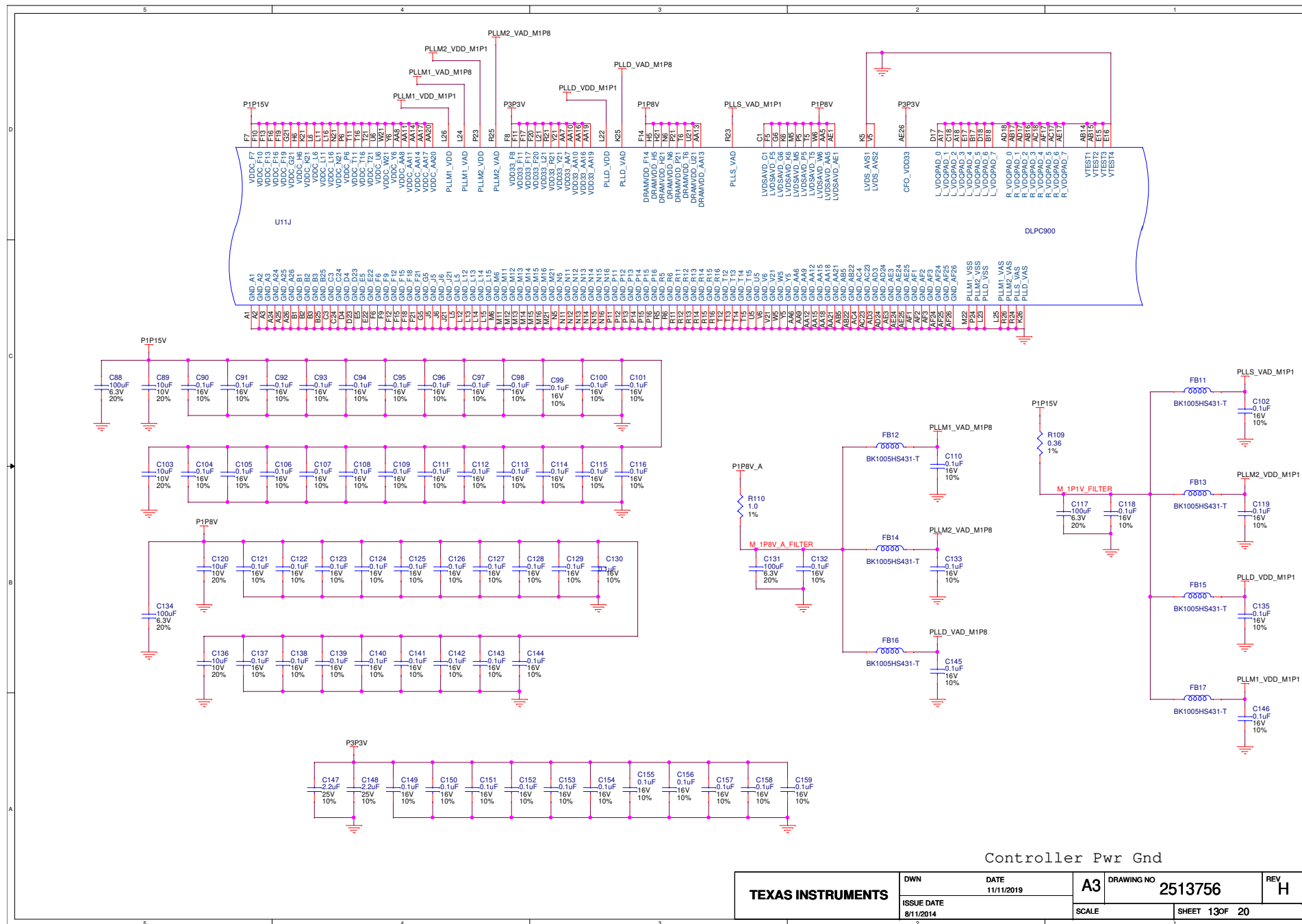






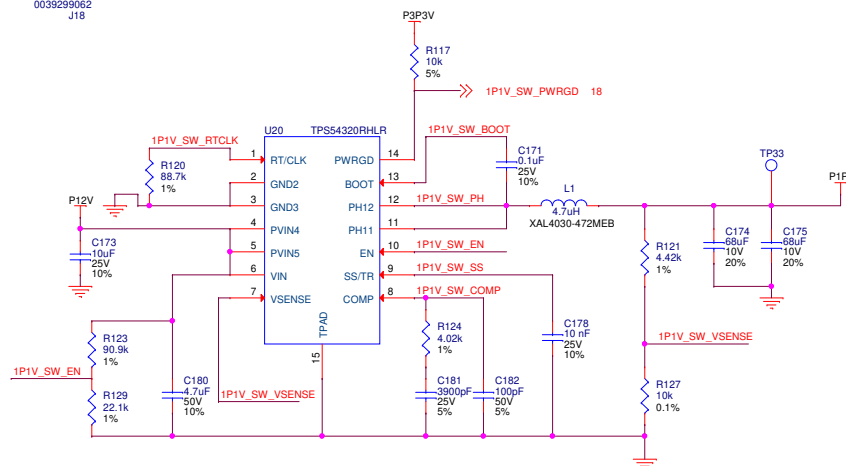
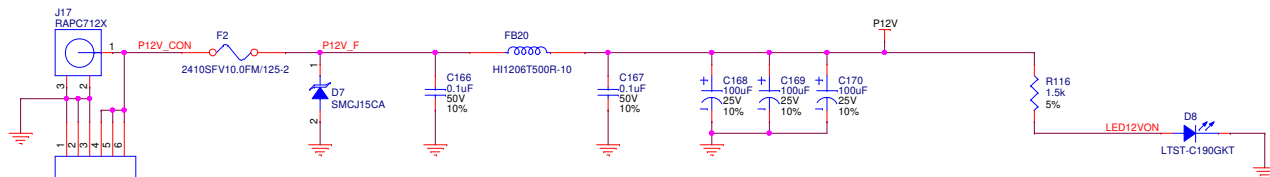
Controller I2C, LED driver interface, In/Out Triggers and GPIOs

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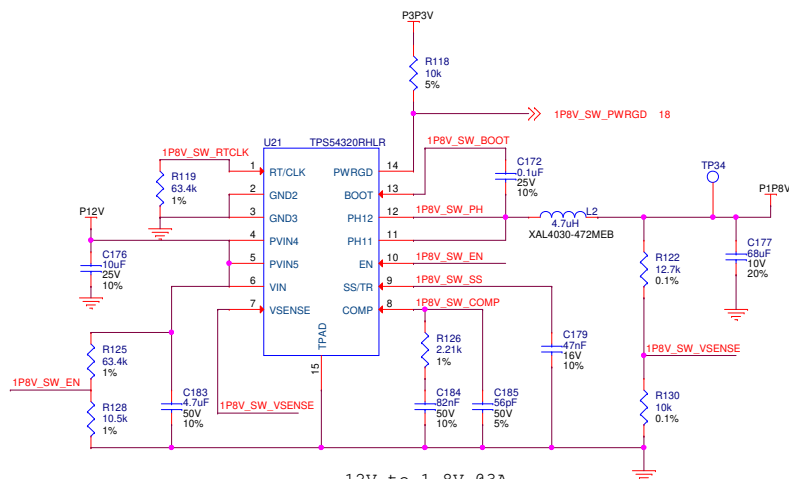


Controller Pwr Gnd

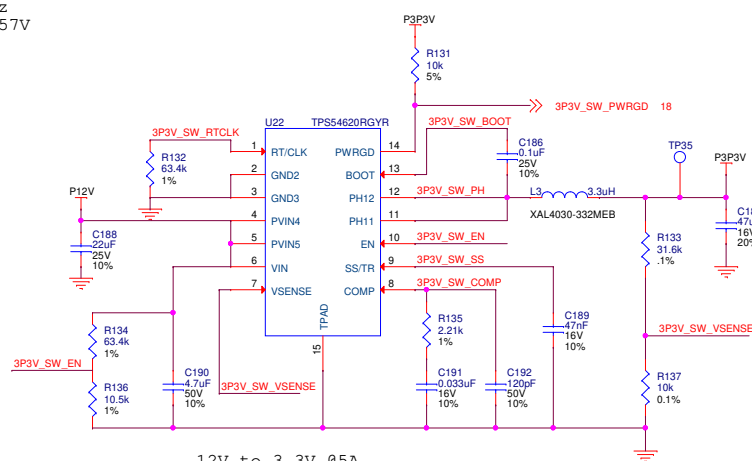
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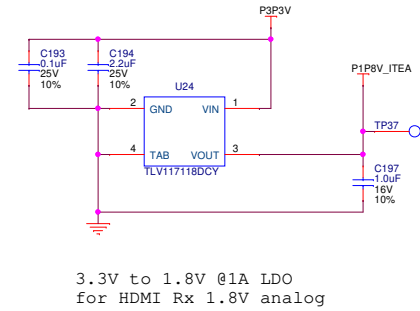
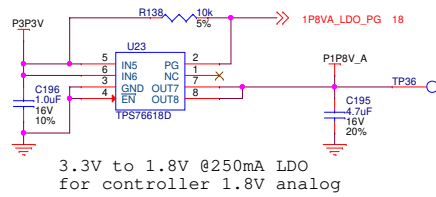


12V to 1.15V @2.5A
Switching Freq ~ 550KHz
Vstart/stop ~ 6.08V/5.57V
SS ~ 3.5ms



12V to 1.8V @3A
Switching Freq ~ 750KHz
Vstart/stop ~ 8.44V/7.95V
SS ~ 15ms

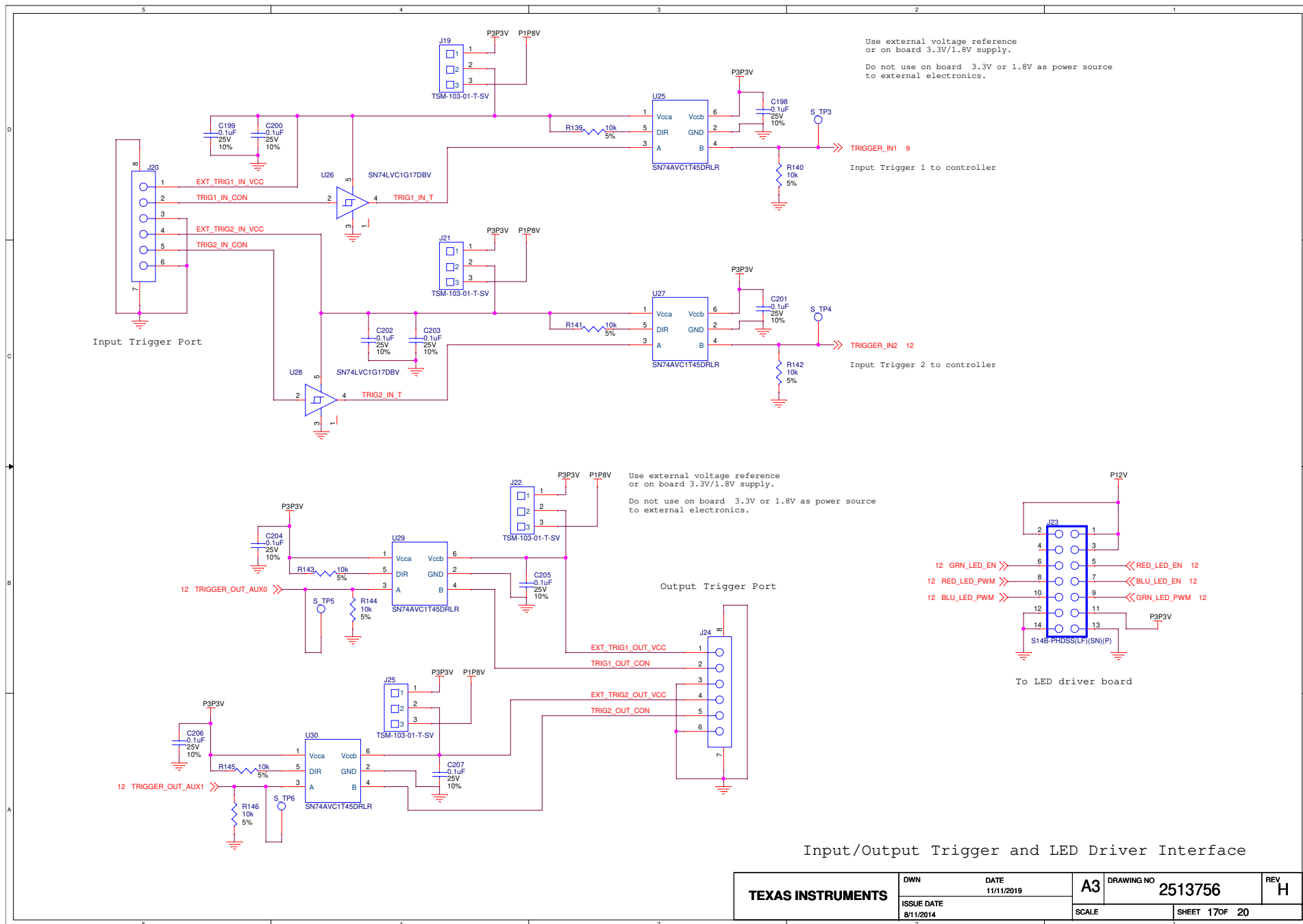




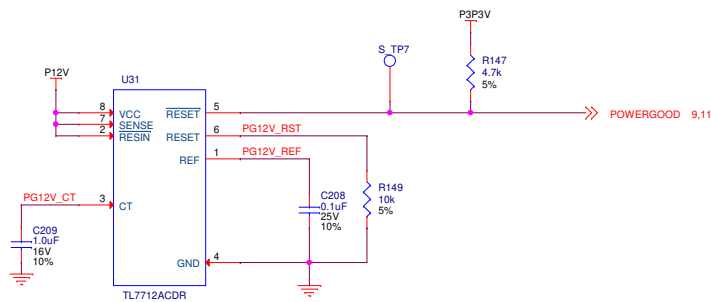
Distribute ground vias around PCB

Power Generation LDO 1.8V LDOs

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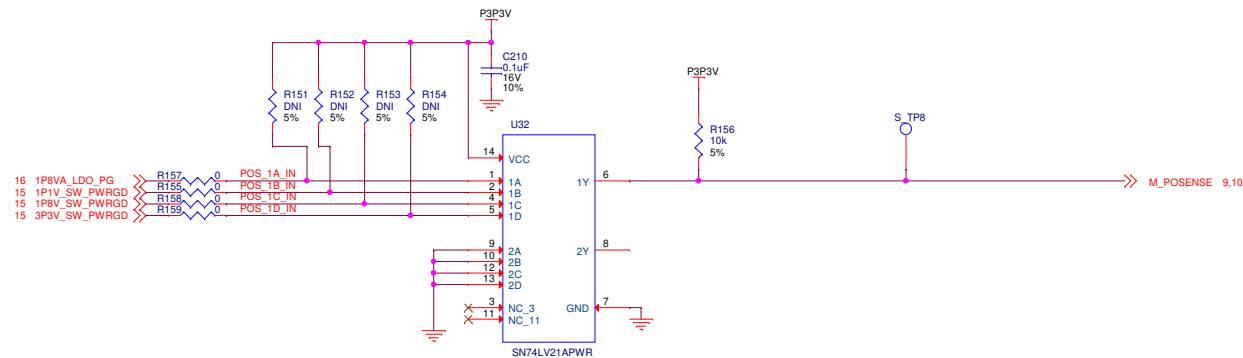
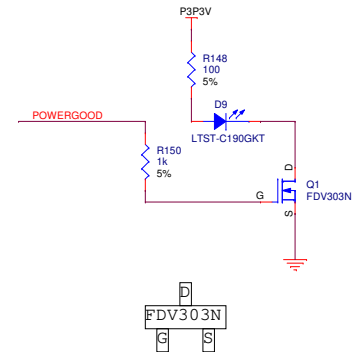


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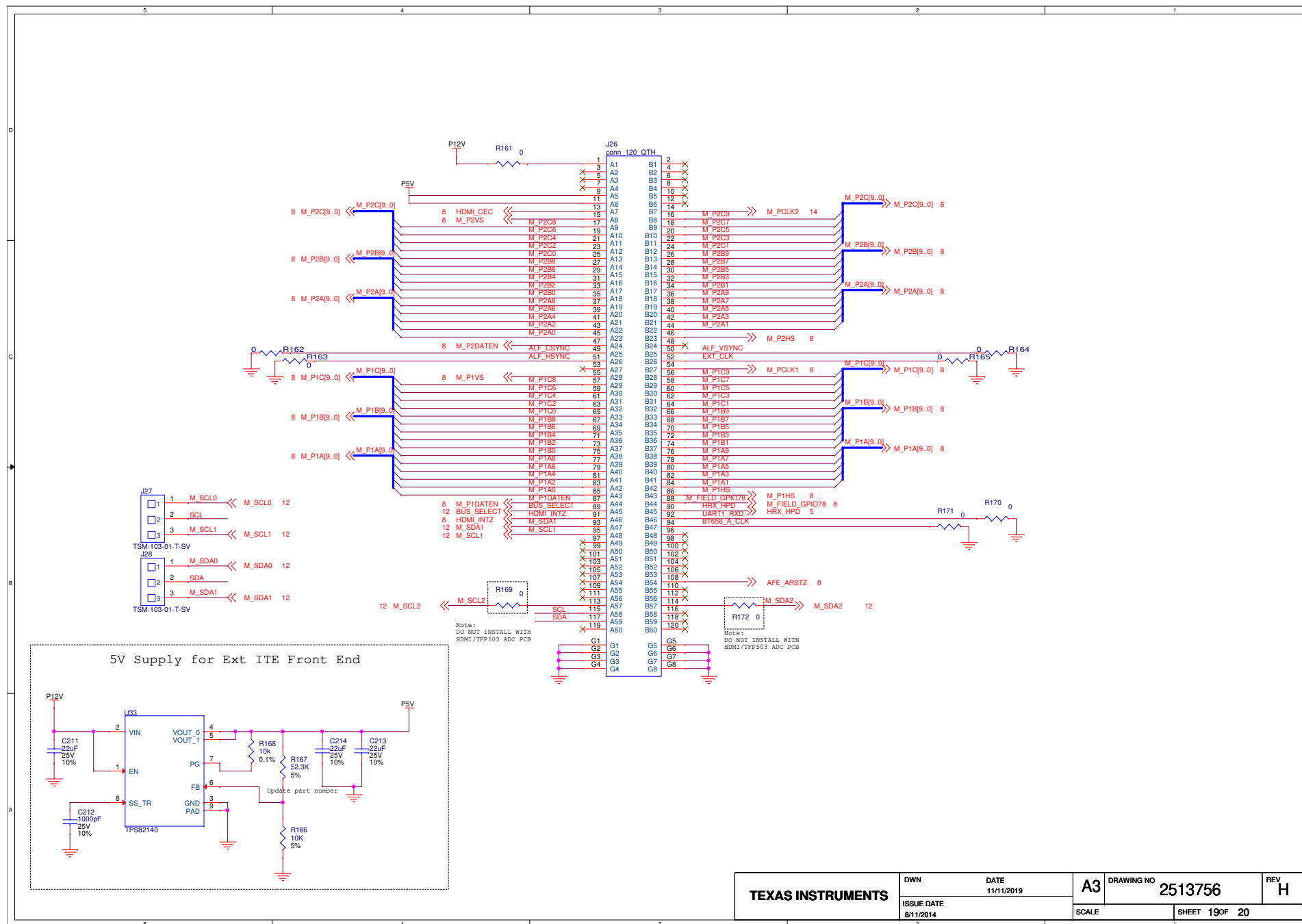
Per controller spec (Fig. 3), POWERGOOD has no impact on operation for 60ms after rising edge of POSENSE. In other words, during power up, controller will ignore the state of PG until the internal PLL is locked (require up to 60ms). Controller will then sample the PG input to begin normal operation.

During power down, POSENSE has to remain valid high for at least 500us after PG is deasserted to allow controller to complete the DMD parking procedure. The 300+ uF input caps on 12V would ensure the power monitor to trip at ~11V to deassert PG while keeping regulators operational to maintain POSENSE for > 500us.



Generate Powergood, POSENSE

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REVISION HISTORY

Rev A

PAGES - ALL

- initial rev

Rev B

PAGES for U11

- Updated pins' name to match datasheet

Rev C

Remove all references to DLPC910

Rev D

PAGE 17

- Removed reference to 5V

PAGE 5

- Updated U7

Rev F

Added External Parallel Video Connector and 5V rail

PAGE 20

- Added J26, J27, J28
- Added R162, R163, R164, R165, R166, R167, R168, R169, R170, R171, R172
- Added R162, R163, R164, R165, R166, R167, R168, R169, R170, R171, R172
- Added U33
- Added C211, C212, C213, C214

PAGE 8

- Added Net M_PCLK2 to U11A, W25
- Added Net M_P2HS to U11A, W26
- Added Net M_P2VS to U11A, U22
- Added Net M_P2DATEN to U11A, W24
- Added Net HDMI_CEC to U11A, G23

PAGE 12

- Added Net BUS_SELECT to U11I, W25

Replaced External Flash Memory to 256 MByte

PAGE 10

- Removed U14, U15, U16
- Removed R68, R74
- Removed C80, C81, C82, C83
- Added U34, U35, U36, U37
- Added C215, C216, C217
- Added Net GPIO45_ADDR24 to U11F, U23
- Added Net GPIO46_ADDR25 to U11F, T22
- Added Net GPIO60_ADDR26 to U11F, H22
- Added Net M_PMADDR24 to U34, 3
- Added Net M_PMADDR25 to U34, 6
- Added Net M_PMADDR26 to U34, 8
- Added Net M_PMADDR23 to U37, 4

Rev G

- Updated J10-1 pin net from TRSTZ to TRSTZ_IN
- Update HDMI_HPD to HRX_HPD

Rev H

- Pull-Down resistors added to address lines 21-26 (R173, R174, R175, R176, R177)
- Renamed Pin of U37 to "M_PM_CS22"
- U35 renamed Pin 4 to "M_PM_CEX2" and Pin 6 to "M_PM_CS22"

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