Design Guide: TIDA-010944

Single-Phase and Split-Phase Shunt Energy Metrology Reference Design

Description

This reference design implements a single-phase with neutral or split-phase energy measurement subsystem using one isolated and one non-isolated standalone multichannel analog-to-digital converters (ADC) with two shunts. The combination of shunt sensors and a low-power linear 3D Hall-effect sensor (TMAG5273) provides both protection and enables the detection of magnetic tampering attacks. The reference design achieves class 0.2 S accuracy across 4000:1 input range (25mA–100A) with 4kHz sampling rate and uses a TI Arm® Cortex®-M0+ host microcontroller for calculating the metrology parameters. The necessary software functionality is implemented in MSPM0-SDK Version: 2.01.00.03 and can be compiled with TI Code Composer Studio™.

Resources

TIDA-010944	Design Folder
MSPM0G1106	Product Folder
AMC131M03, ADS131M02	Product Folder
TMAG5273	Product Folder
ISO6731	Product Folder

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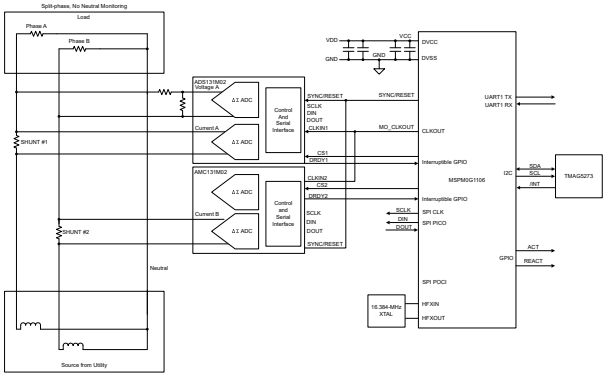
Features

- Single-phase two-wire (1P2W) class 0.2 S shunt metrology subsystem for electricity meters
- Split-phase two-wire (2P2W) class 0.2 S shunt metrology subsystem for electricity meters
- Energy metrology software with pulsed outputs to a reference test system including results displaying on a Microsoft® Windows® PC GUI
- Active and reactive energy and power, root mean square (RMS) current and voltage, power factor, and line-frequency calculations
- Capable of detecting magnetic tampering using a linear 3D Hall-effect sensor
- Tested across 25mA to 100A at 120V, includes an RS-232 5kV$_{RMS}$ isolation interface

Applications

- Electricity meter
- Power quality meter
- Power quality analyzer
- AC charging (pile) station



1 System Description

The TIDA-010944 reference design has the properties described in the following sections.

1.1 Key System Specifications

Table 1-1. Key System Specifications

FEATURES	DESCRIPTION
Number of phases	1 or 2 (each phase current is measured through a SHUNT), single voltage through a resistor divider
Accuracy class	Class 0.2 S
Dynamic range	1:10000 (accuracy tested for 1:1000 or 100mA - 100A)
Current sensor	SHUNT
Tested current range	0.1–100A
Tested voltage range	10V–270V
ADS131M02 and AMC131M03 CLKIN frequency	8,192,000Hz (Can be modified by changing the XTAL Y1)
ADS131M02 and AMC131M03 Delta-sigma modulation clock frequency	4,096,000Hz (= CLKIN / 2)
SPI Clock	19,968MHz (G1106)
Oversampling ratio (OSR)	1024
Digital filter output sample rate	4,000 samples per second (default) (adjustable per register setting)
Phase compensation implementation	Software
Phase compensation resolution	0.0176° at 50Hz or 0.0211° at 60Hz
Selected CPU clock frequency	79,87MHz
System nominal frequency	50 or 60Hz
Measured parameters	• Active, reactive, apparent power and energy • Root mean square (RMS) current and voltage • Power factor • Line frequency
Update rate for measured parameters	Approximately equal to 1 second
Communication options	PC GUI with UART (isolated RS-232 connector or non-isolated on J4 header)
Utilized LEDs	2 LEDs: ACTive energy and REACTive energy
Board power supply	3.3V and GND

1.2 End Equipment

Electricity meters and power quality meters are two popular system designs for accurate energy measurement in compliance with International Electrotechnical Commission (IEC), (EN), and American National Standards Institute (ANSI) standards with a common functionality for calculating the most relevant metrology parameters such as total and per-phase active (kWh), reactive (kvarh), and apparent energy (kVAh). Multiple power quality parameters in a polyphase energy measurement system can be also calculated, including:

- Per-phase voltage total harmonic distortion (THD)
- Per-phase current THD
- Voltage phase-to-phase angle
- Per-phase zero crossing

1.3 Electricity Meter

Utility providers and customers are driving the need for more features from electricity meters. As the accuracy requirements and amount of processing expected from electricity meters rapidly increase, it becomes more and more difficult to solve these issues with a single metrology system-on-chip (SoC). A dual-chip approach with a

standalone ADC and a host microcontroller (MCU) helps overcome the limitations of electricity meter SoCs and enables a mix-and-match solution, which can be optimized for cost or performance.

Using an accurate state-of-the-art standalone ADC with integrated power and data isolation, such as the AMC131M03, has the following advantages:

- Enables meeting the most stringent of accuracy requirements
- Enables meeting minimum sample rate requirements (without compromising on accuracy) that is sometimes not obtainable with application-specific products or metrology SoCs
- Enables flexibility in selecting the host MCU, based on the application requirements, such as processing capability in million instructions per second (MIPS), minimum random access memory (RAM) and flash area, the number of communications modules (for example, serial peripheral interface (SPI), universal asynchronous receiver - transmitter (UART), and inter-integrated circuit (I2C), real-time clock (RTC), and continuously transposed conductors (CRC) module.

To properly measure energy consumption, voltage, and current sensors, translate mains voltage and current to a voltage range that an ADC can detect. When a multiphase power distribution system is used, it is necessary for the current sensors to be isolated from phase-to-phase, so the sensors can properly detect the current drawn from one or two different lines (when neutral is measured or in split-phase configuration) without damaging the ADCs. This design uses two cost-effective shunt sensors, which are immune to magnetic tampering, and enables the implementation of electricity meters for single-phase with optional neutral line measurement or split-phase meters with two currents and a single voltage configuration.

TIDA-010944 is a class 0.2 S high-accuracy one-phase or split-phase SHUNT electricity meter reference design, using one three-channel standalone isolated AMC131M03 ADC, one non-isolated two-channel standalone ADS131M02 ADC, and a cost-effective MSPM0G1106 MCU. The reference design can also be used for energy metering in popular products such as electric vehicle (EV) chargers and AC wall boxes. The non-isolated ADCs senses the current and the voltage on Phase A, while the non-isolated ADC is used for current monitoring of the Neutral line or Phase B, depending on which configuration is used.

The TIDA-010944 firmware specifically supports calculation of various metrology parameters for single-phase with Neutral line or split-phase energy measurement. These parameters can be viewed from the calibration GUI or through the ACT and REACT pulsed outputs, connected to a reference metrology test system.

- Total and per-phase active (kWh), reactive (kvarh), and apparent energy (kVAh) with pulse-generation outputs
- Total and per-phase active (kW), reactive (kvar), and apparent power (kVA)
- Per-phase voltage and current root mean square (RMS)
- Power factor
- Line frequency

1.4 Power Quality Meter, Power Quality Analyzer

Except being used for electricity meters, this single- or split-phase ADC architecture applies also for power quality analyzers and power quality meters, and EV chargers or AC-chargers (also known as wallboxes). This end equipment is used to help utilities and industrial enterprises monitor and control power quality by measuring certain power quality parameters, such as voltage harmonics, current harmonics, supply voltage dips, supply voltage swells, and more. For all equipment, a lot of computation is required for calculating the power quality parameters. Also, it is important to be able to meet the accuracy requirements for the different power quality parameters, something well supported by having a standalone ADC and separate host MCU or MPU device, as is done in this design.

A couple of the parameters commonly measured by power quality meters and power quality analyzers are voltage and current harmonics. The system designer needs to implement coherent sampling for the most accurate harmonic calculations. One way of implementing coherent sampling is to vary the sampling clock based on the Mains frequency. The standalone ADCs in this design have the ability to take in a varying clock so the design can support coherent sampling. Although the clock to the standalone ADCs in this design can be varied, this design has no support for coherent sampling because the sampling clock from the host MCU to the standalone ADC cannot be varied with the proper fine resolution.

2 System Overview

2.1 Block Diagram

There are two configurations for the TIDA-010944 block diagram: either one- or single-phase (Phase A and Neutral, 1P2W, Wye) or split-phase (Phase A to Phase B, 2P2W, Delta) configuration.

In the split-phase configuration, the voltage is measured between Phase A and Phase B, which are 180 degrees apart.

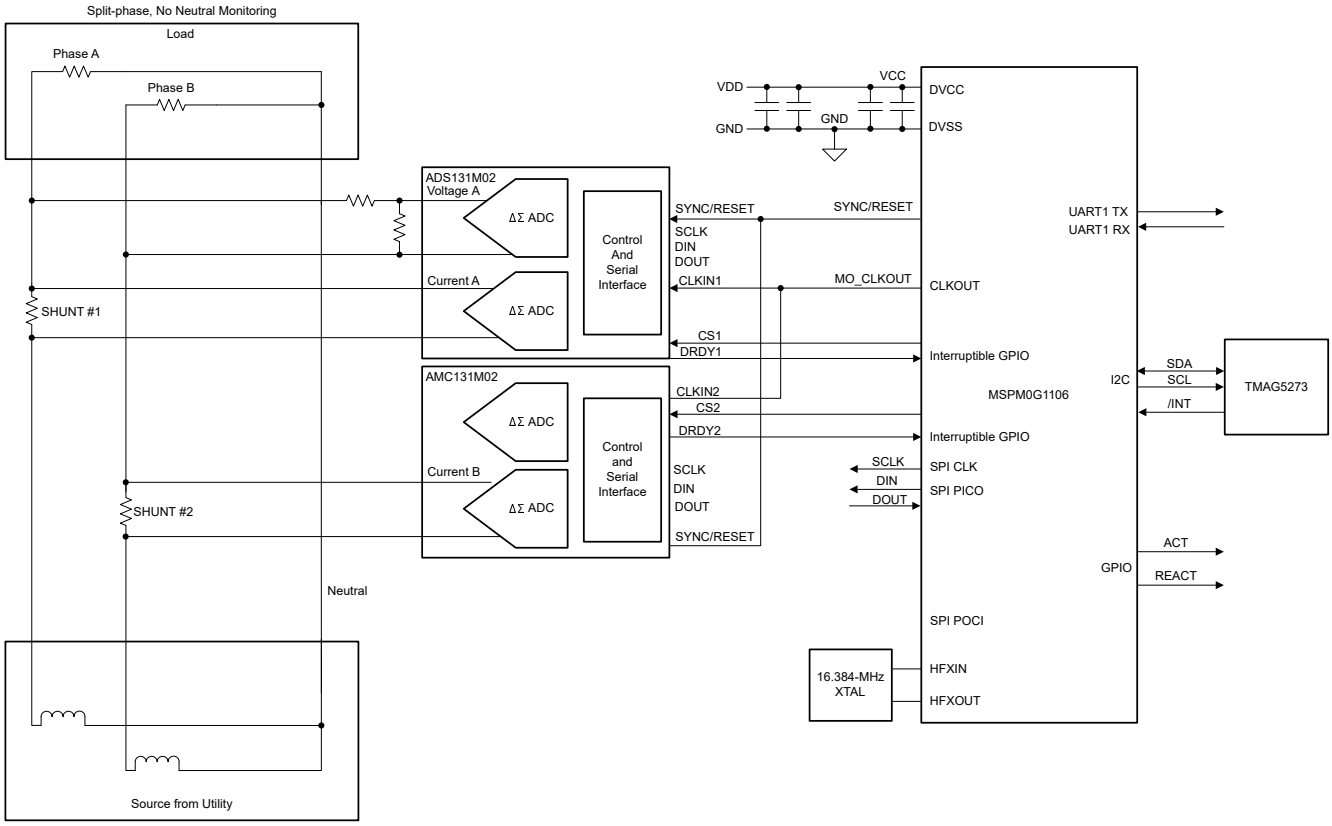


Figure 2-1. Split-Phase Energy Measurement Configuration

In the single-phase configuration the Phase (or line) A line-to-neutral voltage is directly measured, as well as the two currents on Phase A and Neutral. The non-isolated ADS131M02 standalone ADC is used to measure both current and voltage on Phase A, while the AMC131M03 only measures the current through Neutral.

A separate shunt sensor is used on each of the 2 phases for the current measurement while a simple voltage divider is used for dividing down the corresponding voltage between Phase A and Neutral or Phase A and Phase B. The selection of the shunt is made based on the current range required for the energy measurements, with common values being in the range of 150μΩ to 200μΩ, assuming that a maximum current per phase of 60A–120A has to be measured.

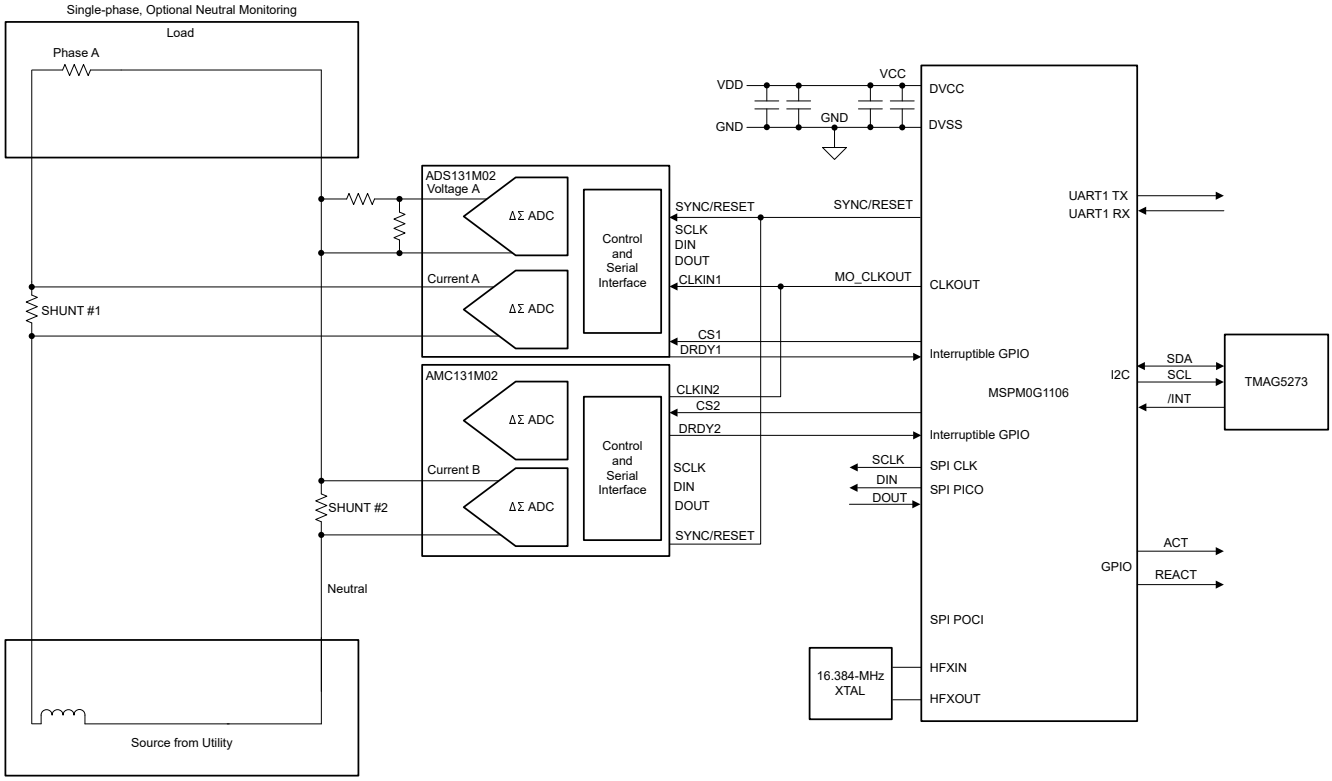


Figure 2-2. Single-Phase With Neutral Energy Measurement

In this design, the one AMC131M03 and one ADS131M02 devices interact with the MSPM0+ MCU in the following manner:

1. An external 16.384MHz XTAL supplies the MSPM0G1106 HFXIN and HFXOUT pins and runs through an internal divider by 2 to create the M0_CLKOUT signal, shared between both ADCs.
2. The AMC131M03 and the ADS131M02 devices divide the CLKIN input by 2 and use this divided clock as the delta-sigma modulation clock.
3. The SPI_SCLK (SPU Bus clock) signal (output from the MCU being the SPI controller) is fed into both ADCs to obtain synchronous SPI data transfer.
4. The SPI_SCLK, PICO, and POCI lines are shared between the two ADCs, making sure all ADCs run synchronously on the shared SPI bus.
5. Two separate $\overline{CS}$ lines are used, these are automatically controlled by the SPI peripheral of the MSPM0+ MCU.
6. When new ADC samples are ready, each AMC131M03 and the ADS131M02 device assert the $\overline{DRDY1}$ and $\overline{DRDY2}$ output pins, which alert the MCU that new data samples are available
7. In addition, the MCU also communicates to a PC GUI through either isolated RS232 port or non-isolated UART connection on J4.
8. ACT and REACT output signals from the MCU represent the active and reactive energy pulses used for accuracy measurement and calibration. Both are mandatory signals needed for calibrating the electricity meter against a reference meter.

2.2 Design Considerations

While the AMC131M03 is used on this two-layer PCB, the two-channel version AMC131M02 suffices, in case current and voltage only are to be measured. The third channel in AMC131M03 can support a temperature measurement at the SHUNT sensor, if required.

The choice of voltage divider resistors for the voltage channel makes sure that the mains voltage is divided down to adhere to the normal input range of the ADS131M02 device. Since this stand-alone ADC has a large dynamic range but only a small range is needed to measure voltage, the voltage front-end circuitry is purposely selected so that the maximum voltage observed at the inputs of the voltage channel ADCs are only a fraction of

the full-scale voltage. By reducing the voltage fed to the ADS131M02 voltage input channel, voltage to current crosstalk, which actually affects metrology accuracy more than voltage ADC accuracy, is reduced at the cost of voltage accuracy, thereby resulting in more accurate energy measurements at lower currents.

2.2.1 Magnetic Tamper Detection With TMAG5273 Linear 3D Hall-Effect Sensor

One common non-intrusive way to steal electricity is to apply a strong permanent magnet or an AC magnet near the electricity meter, thus tampering with the meter. A permanent magnet or an AC magnetic field can affect meter components like current transformer current sensors, shunt current sensors (shunts are only affected by AC magnets), or any power-supply transformer. As a result of the weaknesses of these components to magnetic tampering, utility customers can be undercharged for the energy consumption, thereby allowing consumers to essentially steal electricity.

Due to the susceptibility of meters to magnetic tampering, magnetic sensors are often used in electricity meters to detect external magnetic fields to take appropriate action, such as disconnecting services to the meter or applying a penalty fee for magnetic tampering. In this design, magnetic tamper detection is done with the TMAG5273 linear 3D Hall-effect sensor, which has the following advantages compared to other magnetic sensing devices and designs:

- **Ease of assembly:** Hall-effect sensors in general are not as fragile as reed switches, the latter of which can break during assembly.
- **Only one surface mount IC is needed:** Sensing in three directions with the TMAG5273 requires only one surface mount IC for 3D linear Hall-effect sensors instead of the three ICs in the case of 1D Hall-effect sensors. 3D linear Hall-effect sensors therefore enable a more compact printed circuit board (PCB) layout. In addition, having a surface mount-only implementation can reduce PCB manufacturing costs compared to a 1D Hall-effect sensor implementation that can require through-hole sensors for detecting some of the directions.
- **Flexibility for defining magnetic tampering threshold:** Since 3D linear Hall-effect sensors provide information about the actual sensed magnetic flux density value, it is possible to select the magnetic tampering threshold of each axis to anything within the magnetic sensing range of the 3D linear Hall-effect sensor. This enables configuring how to define what is tampering, which can vary between designs since the magnetic flux density sensed depends on the distance from the magnet to the sensor as well as the characteristics of the external magnets to be detected. This type of flexibility is not possible for Hall-effect switches with fixed magnetic operating point (B_{OP}) thresholds. Finding the appropriate tamper threshold definition can be done by using a magnetic calculation tool to determine what is the resulting magnetic flux density observed for the different magnet-to-sensor distances and magnet types that must be detected. The magnetic threshold can be then set to something lower than the magnetic flux density detected by the sensor when exposed to the desired tamper conditions. Typically, setting the threshold to be small enough to detect tamper magnets but also large enough so that the system does not see any false positives from any nearby equipment that causes a magnetic field that does not affect the functionality of the meter is desired. The magnet-to-sensor distance depends on where the sensor is placed on the PCB as well as the dimensions of the e-meter case. For small-sized systems, the magnetic sensor can be placed near the center of the board for symmetrical sensing coverage across the meter case, or the sensor can be placed near any components that are affected by magnetic tampering. For large-sized systems like certain polyphase meters, sometimes it is not possible for one magnetic sensor to sense tampering across the entire meter surface, so multiple 3D Hall-effect sensors can be used and placed spread out with respect to each other on the PCB to cover a large sensing area. The TMAG5273 has four sets of device orderables that are factory programmed with different I2C addresses, which enable multiple devices to share the same I2C bus.
- **Ability to change between multiple device power modes**: The TMAG5273 supports switching between multiple power modes, depending on if it is desired to reduce system current consumption. The TMAG5273 has an active mode for taking measurements, a sleep mode for minimizing current consumption, and a duty-cycle mode that automatically switches between active and sleep modes. The following list describes the typical use-cases of the different power modes for electricity meters:
  - Active mode is used for taking measurements and requires the most power out of the different power modes. An example scenario where active mode is typically used is when the Mains are available and the meter is running off the AC/DC power supply. When running off the AC/DC power supply, the relatively high active mode current consumption (2.3mA) of the TMAG5273 is negligible.

  - In duty cycle mode, the device takes measurements and then automatically goes to sleep for a user-specified amount of time. Duty-cycle mode is good for minimizing current consumption while still detecting magnetic tampering, such as when low-speed magnetic tamper detection is necessary when running off a backup battery. To reduce average current consumption in duty cycle mode, select a long sleep time. When selecting the sleep time, set the sleep time to be less than the desired response time for magnetic measurements. As an example, to sense magnetic tampering every 2ms using wakeup and sleep mode, set the sleep time to 1ms instead of 1 second.
  - In sleep mode, the device does not take any magnetic measurements. An alternative to wakeup and sleep mode is to have the MCU manually set the sensor to sleep mode and then manually set the sensor to wake up after the desired sleep time has passed. This requires more overhead from the MCU; however, this option can reduce the system current consumption if the MCU is going to have the wakeup and sleep mode that allows the MCU to reconfigure the TMAG5273 during each wakeup and sleep mode cycle. For systems that do not require detecting magnetic tampering when running off a backup battery, the TMA5273 can just be put in sleep mode to reduce system current consumption when running off a battery and then put back in active mode when the system is able to run off the AC/DC power supply again.
- **GPIO pin interrupts when magnetic tampering detected (depends on device)**: The TMAG5273 has the ability to set an interrupt pin when the sensed magnetic flux density of any axis goes beyond a user-defined magnetic switching threshold. To detect tampering, the user can set the magnetic switching point for interrupts to the desired magnetic tampering threshold. Since the interrupt pin of the Hall-effect sensor can wake up the microcontroller when the MCU is in low-power mode, and since the microcontroller does not have to read the Hall-effect sensor to determine magnetic tampering, the MCU can go to low-power mode when running off a backup power supply until woken up by the interrupt pin of the Hall-effect sensor. Used simultaneously, the general-purpose input/output (GPIO) pin interrupt feature and duty-cycle power mode can reduce system current consumption and extend the lifetime of the backup power supply. Once the GPIO pin of the Hall-effect sensor wakes up the microcontroller, the MCU can then retrieve the value of the sensed magnetic field reading that caused the interrupt and then enable wakeup and sleep mode with GPIO interrupts again.
- **Detection of AC magnets**: AC magnets do not only affect current transformers. AC magnets can also affect shunt and Rogowski coil current sensors. To detect AC magnets, a linear 3D Hall-effect sensor can also be used. Figure 2-3 shows that detecting AC magnets requires a fast-enough effective sampling period and a small enough sleep time to properly capture enough samples along a cycle of the AC magnet waveform. The effective sampling period corresponds to the time needed to get one set of samples, which is dependent on the internal sampling rate of the device. Since linear Hall-effect sensors provide information on the actual sensed magnetic flux densities, the sensors are better able to detect AC magnets than a low-sample rate Hall switch.

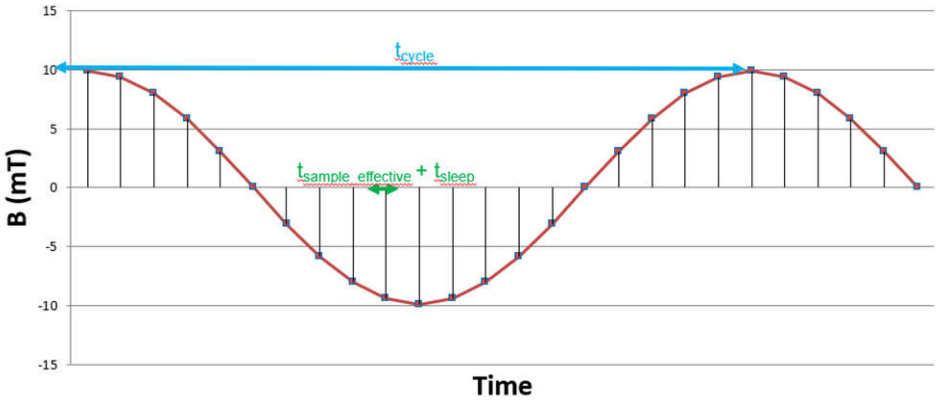


Figure 2-3. Detection AC Magnets

2.2.2 Analog Inputs of Standalone ADCs

The analog front end in this design consists of one AMC131M03 24-bit isolated delta-sigma standalone ADC with three integrated channel converters each and one ADS131M02 24-bit non-isolated ADC with two integrated channels. The analog inputs of each channel are differential and require that the input voltages at the pins do not exceed certain levels. To meet this input voltage specification, the current and voltage inputs must be divided down from Mains.

2.2.3 Voltage Measurement Analog Front End

The nominal voltage from the mains in many regions of the world varies from 100V–240V so the voltage needs to be scaled down to be sensed by an ADC. Figure 2-4 shows the analog front end used for this voltage scaling J2 is where the voltage is applied for Phase A to Neutral (one-phase, two-wire or 1P2W) or Phase A to Phase B (split-phase, two-wire or 2P2W).

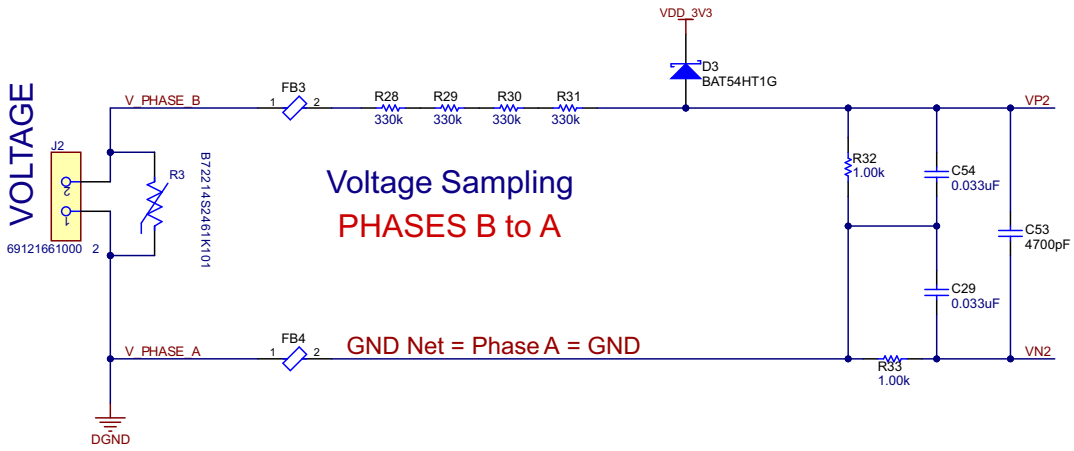


Figure 2-4. Analog Front End for Voltage Input

The analog front end for voltage inputs has a voltage divider network (R28, R29, R30, and R31), and an RC low-pass filter (R32, R33, C54, C29) and the C53.

At lower currents, voltage-to-current crosstalk affects active energy accuracy much more than voltage accuracy, if power offset calibration is not performed. To maximize the accuracy at these lower currents, in this design the entire ADC range is not used for the voltage channels. The reduced ADC range for the voltage channels in this design still provides more than enough accuracy for measuring voltage. Equation 1 shows how to calculate the range of differential voltages fed to the voltage ADC channel for a given Mains voltage and selected voltage divider resistor values.

$$V_{ADC\_Swing,\ Voltage} = \pm V_{RMS} \times \sqrt{2}\left(\frac{R_{32}}{R_{28} + R_{29} + R_{30} + R_{31}}\right) \quad (1)$$

Based on this formula and the selected resistor values in Equation 1, for a mains voltage of 120V (as measured between the line and neutral), the input signal to the voltage ADC has a voltage swing of ±128.56mV (90.90mV$_{RMS}$).

For a mains voltage of 230V (as measured between the line and neutral), the 230V input to the front-end circuit produces a voltage swing of ±246.42mV (174.24mV$_{RMS}$)). The ±128.56mV and the ±246.42mV voltage ranges are both well within the –1.3V to + 2.7V range, that can be sensed by the ADS131M02.

2.2.4 Analog Front End for Current Measurement

Figure 2-5 shows that the analog front end for current inputs is different from the analog front end for the voltage inputs.

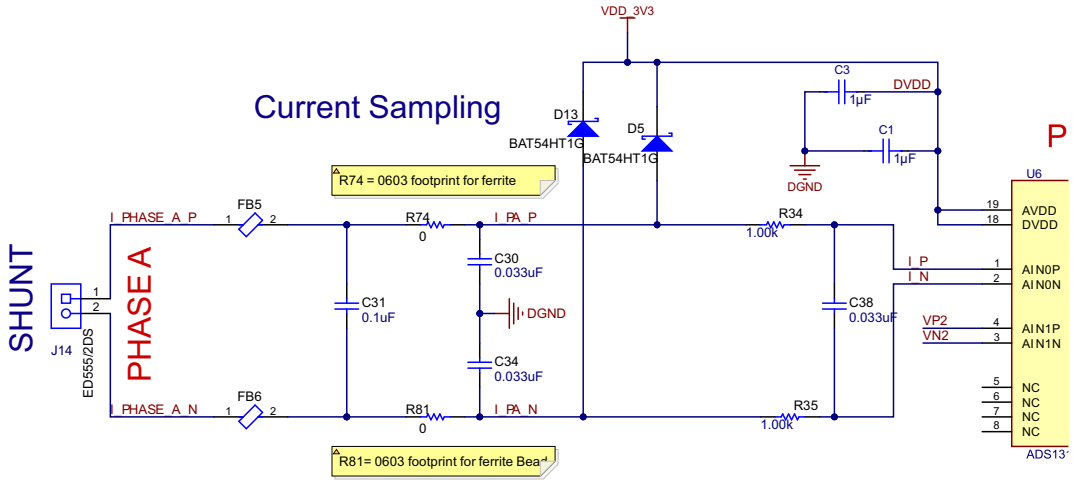


Figure 2-5. Analog Front End for Current Input

The positive and negative leads from the SHUNT sensor are connected to pins 1 and 2 of header J14 (for Phase A). The analog front end for current consists of footprints for electromagnetic interference filter beads (FB5 and FB6), and a two-stage RC low-pass filter (R74, R81, C30, C34) and R34, R35, and C38 that functions as an anti-aliasing filter.

Equation 2 shows how to calculate the range of differential voltages fed to the current ADC channel for a given maximum current, and shunt resistor value.

$$V_{ADC_{Swing},Current,Shunt} = \pm\sqrt{2}\left(R_{shunt}\right)I_{RMS,max} \quad (2)$$

Assuming a SHUNT value of 150µΩ, the input signal to the current ADC has a voltage swing of ±21,21mV when the maximum current rating of the meter (100A) is applied. This relatively low voltage, when using GAIN = 32 is well within the required Full-Scale Range of ±37.5mV. See also *full-scale range* table in the *AMC131M03 3-Channel, 64-kSPS, Simultaneous-Sampling, 24-Bit, Reinforced Isolated Delta-Sigma ADC With Integrated DC/DC Converter* data sheet.

2.3 Highlighted Products

2.3.1 AMC131M03

The AMC131M03 is a precision, three-channel, data- and power-isolated, simultaneous-sampling, 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC).

The AMC131M03 offers wide dynamic range, low power, and energy-measurement-specific features, making the device designed for energy metering and power metrology applications. The ADC inputs can be directly interfaced to a resistor-divider network or a shunt current sensor because of the device high-input impedance.

The AMC131M03 features a fully-integrated isolated DC/DC converter that allows single-supply operation from the low-side of the device. The reinforced capacitive isolation barrier is certified according to VDE V 0884-11 and UL1577. This isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage, making the AMC131M03 an excellent choice for polyphase energy metering applications using shunt current sensors.

The three isolated, simultaneous-sampling ΔΣ ADC channels feature differential inputs and a single-supply operation (3.3V or 5V) with an integrated DC/DC converter in the temperature range: –40°C to +125°C. The device has been optimized for low EMI and meets CISPR-11 and CISPR-25 standards and has the safety-

related certifications: – 7070V_{PEAK} reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 as well as 5000V_{RMS} isolation for 1 minute per UL1577.

The programmable data rate is a maximum 64ksps and the programmable gain up to 128, a low-drift internal voltage reference and an internal temperature sensor are included. Data and registers are being accessed through a 4-wire SPI with cyclic redundancy check (CRC).

If the 3rd input channel is not required (for example, for a temperature measurement with the 1%, 100kΩ linear thermistor TMP63), the very similar AMC131M02 2-channel device can be a used as a cost-effective alternative.

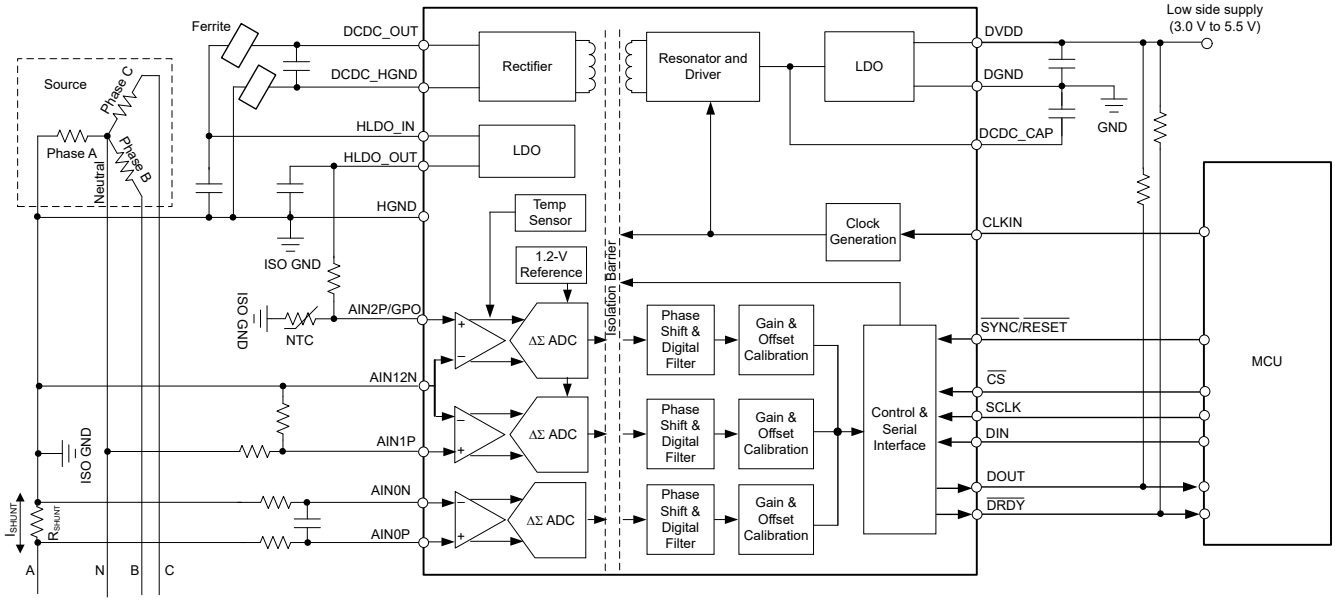


Figure 2-6. AMC131M03 Functional Block Diagram

2.3.2 ADS131M02

The ADS131M02 device is a two-channel, simultaneously-sampling, 24-bit, 2nd-order delta-sigma (ΔΣ), analog-to-digital converter (ADC) that offers wide dynamic range, and internal calibration features making the device well-designed for energy metering, power quality, and protection applications. The ADC inputs can be directly interfaced to a resistor-divider network, a transformer to measure voltage or current, or a Rogowski coil to measure current.

The individual ADC channels can be independently configured depending on the sensor input. A low-noise, programmable gain amplifier (PGA) provides gains ranging from 1 to 128 to amplify low-level signals. Additionally, these devices integrate channel-to-channel phase alignment and offset and gain calibration registers to help remove signal chain errors. A low-drift, 1.2V reference is integrated into the device reducing printed circuit board (PCB) area. cyclic redundancy check (CRC) options can be individually enabled on the data input, data output, and register map to provide communication integrity. Figure 2-7 shows a block diagram of this device.

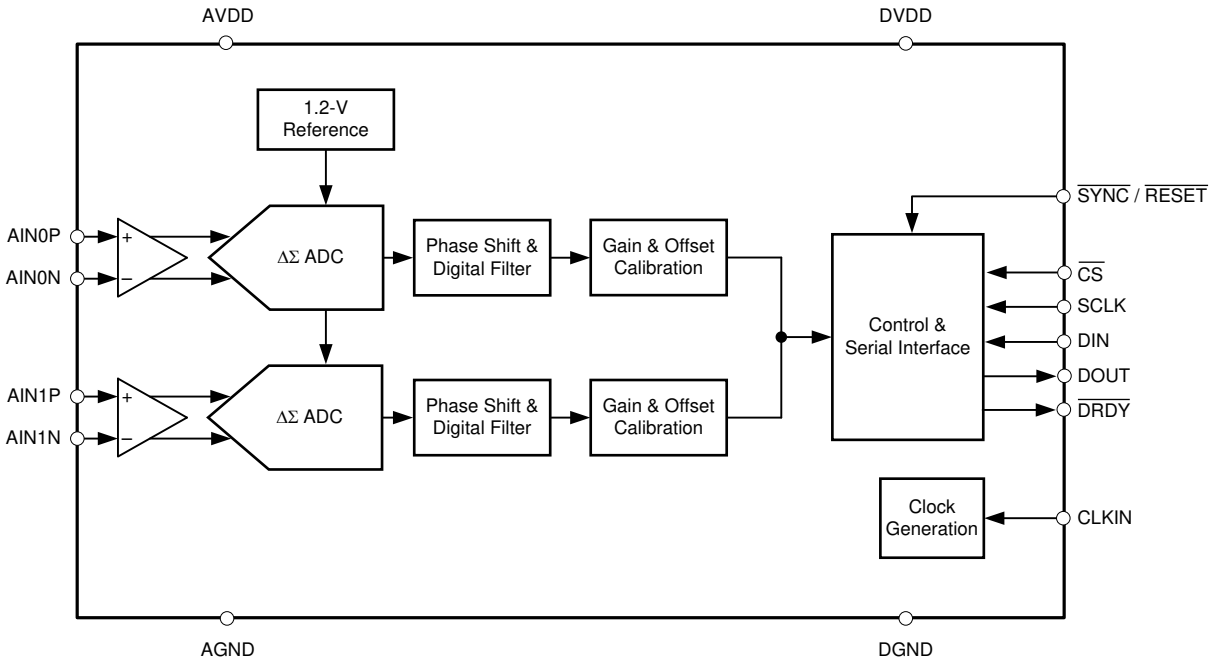


Figure 2-7. ADS131M02 Functional Block Diagram

2.3.3 MSPM0G1106

The MSPM0G device family integrates an Arm 32-bit Cortex-M0+ CPU with memory protection unit, clock frequency up to 80MHz and two SPIs, one of those supporting up to 32Mbits/s. Other relevant peripherals for running Energy Calculations are the Real Time Clock (RTC) with calendar function, CRC-16 or CRC-32 HW module, four UARTs, two I2Cs with 1Mbit/s and up to 60 GPIOs.

The MSPM0+ MCU in this design retrieves voltage and current samples from the four ADC devices and calculates the metrology parameters. In addition, the device also keeps track of time with the RTC module, and uses one of the UART interfaces to communicate to a PC GUI using either the isolated RS-232 or isolated RS-485 circuit of the board. The CRC16 hardware module of the MSPM0+ MCU is used to accelerate the CRC calculations needed to verify the integrity of the ADC sampling data packets sent by the ADCs.

Main features of MSPM0G1106 are the extended temperature range: –40°C up to 105°C; the wide supply voltage range: 1.62V to 3.6V; and the integrated 64KB of flash memory with built-in error correction code (ECC) and 32KB of ECC protected SRAM with hardware parity.

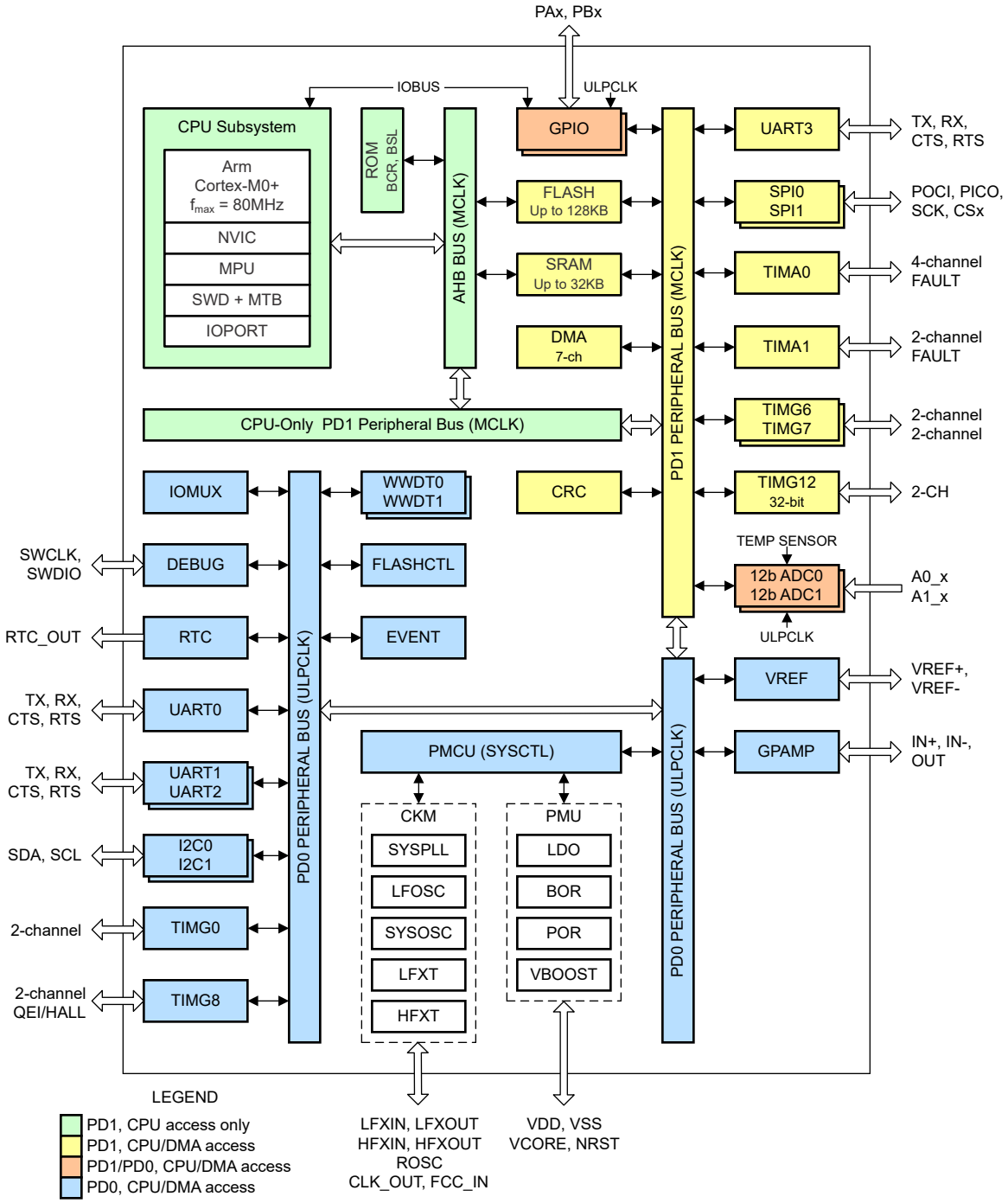


Figure 2-8. MSPM0G1106 Functional Block Diagram

2.3.4 TMAG5273

The TMAG5273 is a low-power linear 3D Hall-effect sensor designed for a wide range of industrial and personal electronics applications. This device integrates three independent Hall-effect sensors in the X, Y, and Z axes. A precision analog signal chain along with an integrated 12-bit ADC digitizes the measured analog magnetic field values. The I2C interface, while supporting multiple operating VCC ranges, provides seamless data communication with low-voltage microcontrollers. The device has an integrated temperature sensor available for multiple system functions, such as thermal budget check or temperature compensation calculation for a given magnetic field. The TMAG5273 can be configured through the I2C interface to enable any combination of magnetic axes and temperature measurements. Additionally, the device can be configured to various power options (including wake-up and sleep mode) allowing designers to optimize system power consumption based

on the system-level needs. Multiple sensor conversion schemes and I2C read frames help optimize throughput and accuracy. A dedicated INT pin can act as a system interrupt during low-power wake-up and sleep mode, and can also be used by a microcontroller to trigger a new sensor conversion. The ultra-low-power consumption is defined by 2.3mA active mode current, 1µA wake-up current, and just 5nA sleep mode current.

TMAG5273 operates from 1.7V to 3.6V supply voltage in the –40°C to +125°C temperature range at a maximum 1MHz I2C clock speed.

- The TMAG5273 is a linear 3D Hall-effect sensor that is designed for electricity meters.
- The TMAG5273 is offered in four different factory-programmed I2C addresses. The device also supports additional I2C addresses through the modification of a user-configurable I2C address register.
- Figure 2-9 shows how the TMAG5273 defines the X, Y, and Z directions.

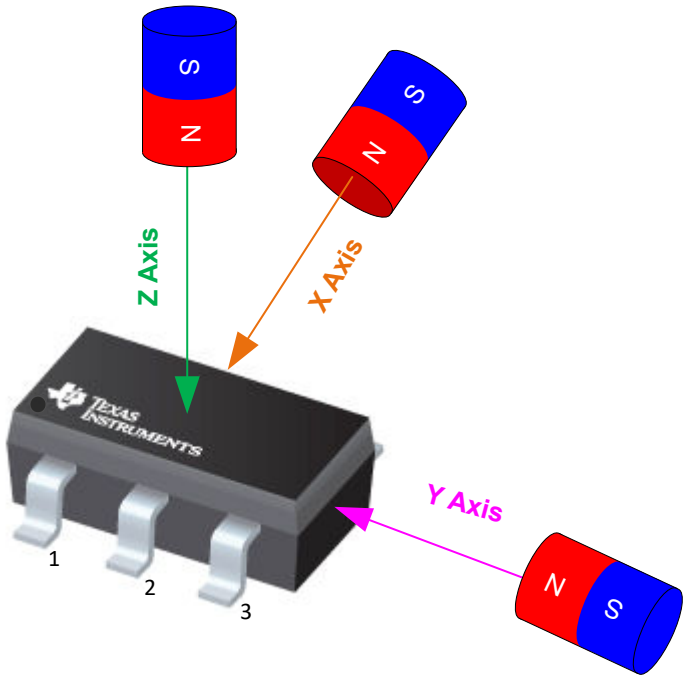


Figure 2-9. Field Direction Definition

2.3.5 ISO6731

To add isolation to the RS-232 connection to a PC, the isolated RS-232 portion of this reference design uses capacitive galvanic isolation, which has an inherent life span advantage over an opto-isolator. In particular, industrial devices are usually pressed into service for much longer periods of time than consumer electronics; therefore, maintenance of effective isolation over a period of 15 years or longer is important.

The ISO6731 device is a high-performance, triple-channel digital isolator designed for cost-sensitive applications requiring up to 5000V_{RMS} isolation ratings per UL 1577. This device is also certified by VDE, TUV, CSA, and CQC. The ISO6731 device provides high electromagnetic immunity and low emissions at low-power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by TI's double capacitive silicon dioxide (SiO2) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-host driving applications.

The ISO6731 device has two forward channels and one reverse-direction channel. In the event of input power or signal loss, the default output is high for the device without suffix F and low for the device with suffix F. In this design, two isolation channels are used for the TX and RX in RS-232 communication mode. This chip supports a signaling rate of 50Mbps and operates from a 1.71V to 1.89V and 2.25V to 5.5V supply in the temperature range: –40°C to +125°C.

2.3.6 TRS3232E

To properly interface with the RS-232 standard, a voltage translation system is required to convert between the 3.3V domain on the board and from the 12V on the port. To facilitate the translation, the design uses a TRS3232E device, which is capable of driving the higher voltage signals on the RS-232 port from only the 3.3V DVCC through a charge pump system.

The TRS3232E device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15kV electrostatic discharge (ESD) protection pin-to-pin (serial-port connection pins, including GND). The device meets the requirements of the Telecommunications Industry Association and Electronic Industries Alliance TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. The devices operate at data signaling rates up to 250kbps and a maximum of 30V/µs driver output slew rate.

2.3.7 TPS709

To power the data terminal equipment (DTE) side of the isolation boundary and the RS-232 charge pump, there are two choices: the interface can either implement an isolated power supply or harvest power from the RS-232 line. Integrating a power supply adds cost and complexity to the system, which is difficult to justify in low-cost sensing applications.

To implement the second option of harvesting power from the RS-232 port, this reference design uses the flow control lines that are ignored in most embedded applications. The RS-232 specification (when properly implemented on a host computer or adapter cable), keeps the request to send (RTS) and data terminal ready (DTR) lines high when the port is active. As long as the host has the COM port open, these two lines retain voltage. This voltage can vary from 5V to 12V, depending on the driver implementation. The 5V to 12V is sufficient for the use requirements in this design.

The voltage is put through a diode arrangement to block signals from entering back into the pins. The voltage charges a capacitor to store energy. The capacitor releases this energy when the barrier and charge pump pull more current than what is instantaneously allowed. The TPS70933 device is used to bring the line voltage down to a working voltage for the charge pump and isolation device.

The TPS70933 linear regulator is an ultra-low quiescent current device designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy overtemperature. A quiescent current of only 1µA makes these devices an excellent design for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse current protections for added safety. These regulators can be put into shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150nA (typical).

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

This reference design can be powered by connecting 3.3V and GND to the board connector J8.

The MSPM0G1106 device provides the minimum resources for running the metrology library and has the required peripherals to interface to the standalone ADCs and the PC GUI.

The required MCU peripheral modules are:

- HF Clocking subsystem using external XTAL
- SPI with DMA (data transfer between stand-alone ADCs and MSPM0 MCU)
- SPI for external SPI flash memory device
- UART with DMA (data transfer between external PC GUI and MSPM0 MCU for calibration and metrology values read out)
- GPIOs (inputs with interrupts or outputs for LEDs and ADCs control)
- I2C for TMAG5273 interface
- RTC (calendar mode based off 32.768kHz from internal LFOSC)

All the above peripherals or MCU modules are configured through the `TIDA-010944.syscfg` file in the MSPM0-SDK middleware, utilizing the graphical SysConfig tool, which enables intuitive MCU configuration changes over a GUI interface.

1. The M0+ clocking scheme is derived from the external 16.384MHz XTAL, which is feeding the PLL module and is being multiplied and divided with specific factors to generate the MCLK frequency (the CPU clock speed) of 79.87MHz. The same external 16.384MHz XTAL is divided by 2 and output to a GPIO pin with high-drive capability to create the 8.192MHz output frequency for M0_CLKOUT.
2. The SPI bus is shared between both ADCs and the MCU features an SPI controller with two separate $\overline{CS}$ (Chip Select) lines, one of each connecting to an ADC. The SPI bus runs at 19.968 or 13,312MHz data rate with DMA support using two channels, one for transmit and one for receive. The SPI PICO and POCI data lines are shared, as these are driven sequentially with only one $\overline{CS}$ line active at a time. The SPI clock from the M0+ MCU SPI peripheral is wired to both ADCs.
3. The MSPM0G1106 is configured to communicate to the PC GUI through a non-isolated UART connection at maximum 115,200 baud with 8N1. The UART driver supports a bidirectional transfer (two DMA channels are used, one for transmit and one for receive) with a minimum MCU interrupt load.
4. The two $\overline{DRDY}$ lines (one from each ADC) are wired to two GPIO inputs of MSPM0+ MCU with interrupt enabled on the falling edge. Three MCU GPIO outputs are needed: the SYNC_RESET line to trigger all ADCs simultaneously, which is shared by all ADCs, and ACT and REACT outputs. These pulsed outputs are for the Active and Reactive energy, being calculated by the metrology middleware and are used to measure the TIDA-01044 accuracy using an external test system, which reads the pulses.
5. An I2C interface is used to connect the TMAG5273 3D-Hall sensor device, with the MCU being the I2C transmitter.
6. The RTC module supports calendar mode, which is a common requirement for an electricity meter. The M0+ MCU internal 32.768kHz LFOSC is used as the clock source for the auxiliary clock (RTCCLK) of the device.
7. Due to the need to have a synchronous clock to both ADCs, the CLKIN signals are wired to the 8.192MHz M0_CLKOUT output pin.

3.1.1 Software Requirements

This section discusses the features of the test software and provides insight on how the calculation of many metrology parameters are implemented. The metrology software used for testing TIDA-010944 is delivered as a middleware example in the latest MSPM0 SDK, Version 2.01.00.03 or later.

The middleware contains hardware abstraction layers which enable communication between the standalone ADCs and an Arm Cortex-M0+ MCU and a library of metrology calculations for energy measurements. A Microsoft Windows PC GUI software is used to display metrology parameters from the TIDA-010944 reference design and can be found in MSPM0-SDK, see the `/tools` directory under `C:\ti\mspm0_sdk_2_01_00_03\tools\metrology_gui`.

The resource utilization of TIDA-010944 middleware code example, using optimization setting of 2 are:

- 34,668 Bytes FLASH for Application code
- 256 Bytes FLASH for calibration data
- 8,174 Bytes RAM memory

3.1.2 UART for PC GUI Communication

The MSPM0+ MCU is configured to communicate to the PC GUI through an UART interface on J4 in this reference design. The PC GUI polls data from the MSPM0G1106 using a UART module configured for 9600 baud with 8N1. The UART protocol for formatting the UART data is named DLT-645 and the UART module utilizes two DMA Channels: Channel 2 for data receive and Channel 3 for data transmit. See also the *MSP430AFE253 Test Report for China State Grid Specification* and *Single Phase and DC Embedded Metering (Power Monitor) Using MSP430I2040* application notes.

UART data is processed in the `HAL_startUARTDMAReceive()` function, by setting a trigger at 14 bytes, as this is the byte which codes the packet length (which can change dynamically from packet to packet). After decoding the byte 14, the UART DMA transfer length value gets updated to a new length, which equals the rest of the DLT-645 protocol packet, transmitted by the PC GUI.

3.1.3 Direct Memory Access (DMA)

The MCU DMA module transfers data packets between the MSPM0G1106 MCU and ADS131M02 and AMC131M03 devices with minimal hardware resources and timing overhead over the shared SPI bus. Two DMA channels are utilized for the SPI data transfer: DMA Channel 0 sends SPI data (0x00) to the ADCs and DMA Channel 1 simultaneously receives the measurements data from both ADCs over the shared SPI bus. Once a complete SPI data packet has been received from the first ADC, an DMA Ready interrupt is generated and the CRC16 verification of the data packet starts. After the CRC16 check was successful, the data packet is disassembled into voltage and current values for Phase A. Then the same occurs for the neutral line data from AMC131M03 where only the current value gets processed.

AMC131M03 transfers 15 bytes packets, while ADS131M02 uses 12 bytes packets, due to 3 and 2 analog input channels, respectively. If any of the analog channels are not enabled, the channels can still report data as 0x00 00 00 (in 24-bit format), so the data packet length does not change, regardless how many channels are enabled.

3.1.4 ADC Setup

The ADC131M03 and ADS131M02 device registers must be initialized to deliver proper measurement data on all relevant analog input channels. Figure 3-1 is followed at every start of the metrology application as well as each time the Calibrating and Viewing Results From PC metrology calibration procedure is performed.

The SPI module of the MSPM0+ MCU is configured as a controller device that uses 4-wire mode (the two chip-select signals are automatically asserted high and low by the SPI hardware module). After the SPI is set up, all interrupts are disabled and a reset pulse on the SYNC_RESET line is sent from the MSPM0+ MCU. Interrupts are then re-enabled and the MSPM0+ MCU sends SPI write commands sequential to ADS131M02 to configure the registers and then repeats the initialization step with AMC131M03:

- MODE register settings: 16-bit CCITT CRC used, 24-bit length for each word in the ADS131M02 and AMC131M03 data packet, the $\overline{\text{DRDY}}$ signal is asserted on the most lagging enabled channel, $\overline{\text{DRDY}}$ is asserted high when the conversion value is not available, $\overline{\text{DRDY}}$ is asserted low when the conversion values are ready.
- GAIN1 register settings for Voltage + Current: PGA gain = 1 used for the voltage channel, measuring the line-to-neutral or Phase A to Phase B voltage, PGA gain = 32 for the current channels on Phase A and Neutral or Phase B.
- CFG register settings: Current detection mode is unused on ADS31M02 and is not supported on AMC131M03
- CHx_CFG register settings (where x is the channel number: 0, 1 or 2)
  - one-phase mode: two ADC channel inputs connected to external ADC pins and the channel phase delay set to 0 for each channel (the software phase compensation in the SDK middleware is used instead of ADS131M02 or AMC131M03 hardware phase compensation)
- CLOCK register settings: 1024 OSR, all channels enabled, and high-resolution modulator power mode

The MSPM0+ MCU is configured at start-up to generate a port interrupt whenever a falling edge occurs on any of the two $\overline{\text{DRDY}}$ pins, which indicate that new measurement samples are available.

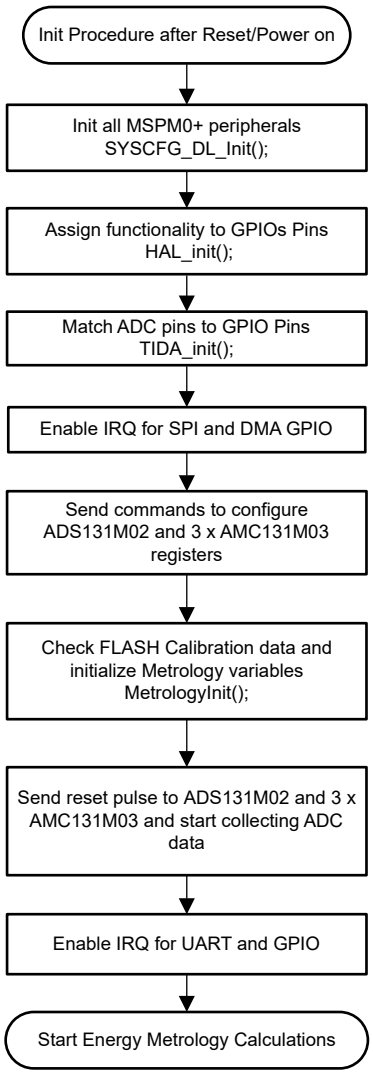


Figure 3-1. ADC Initialization Procedure

The ADC modulator clock is derived from the clock fed to the CLKIN pin which gets internally divided by two, to generate the ADC modulator clock. Equation 3 shows the definition of the sampling frequency of the ADC.

$$f_S = \frac{f_M}{OSR} = \frac{f_{CLKIN}}{2 \times OSR} \quad (3)$$

where

- f_S is the sampling rate
- f_M is the modulator clock frequency
- f_{CLKIN} is the clock fed to the ADS131M02 and AMC131M03 CLKIN pin
- OSR is the selected oversampling ratio

In this design, the M0_CLKOUT signal of the MSPM0+ MCU has a frequency of 8.192MHz. The oversampling ratio is selected to be 1024 with the appropriate register setting. As a result, the ADC modulator clock for both ADCs is set to 4.096MHz and the sample rate is set to 4000 samples per second.

For a single-phase system where each line-to-neutral voltage is measured, at least one ADS device is necessary to independently measure the phase voltage and current. In this design, the following ADC channel mappings are used in software for the single-phase and split-phase configuration:

- AIN0P and AIN0N of ADS131M02 (U6) → Current I1 (Phase A current)
- AIN1Pand AIN1N of ADS131M02 (U6) → Voltage V1 (Phase A line-to-neutral or Phase A line-to-phase B Voltage)
- AIN0P and AIN0N of AMC131M03 (U2) → Current I2 (Phase B current)

3.1.5 Foreground Process

The foreground process includes the initial setup of the MSPM0+ MCU hardware and software and the ADS131M02 and AMC131M03 registers immediately after a device RESET. Figure 3-2 shows the flowchart for this process.

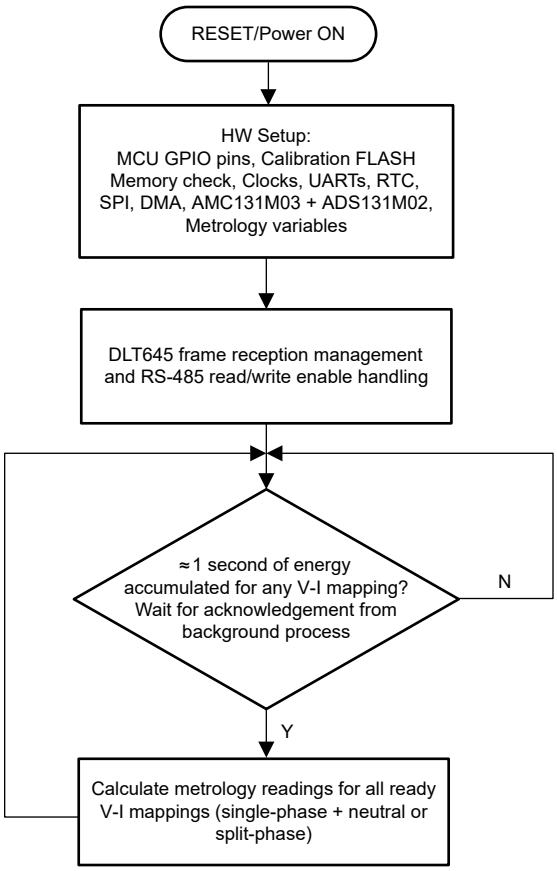


Figure 3-2. Foreground Process

The initialization routines involve the setup of the MSPM0G3507:

- General purpose input/output (GPIO) port pins
- Clock system (MCLK or CPU clock, RTC clock, SPI clock, I2C clock, CLK_OUT pin)
- 1 UART port
- 4 DMA channels, one each per SPI receive and transmit and one each per UART receive and transmit
- ADS131M02 and AMC131M03 registers
- Metrology variables

After the hardware is set up, any received frames from the GUI are processed. Next, the foreground process checks whether the background process has notified the foreground process to calculate new metrology parameters for any voltage-current mappings. This notification is accomplished through the assertion of the PHASE_STATUS_NEW_LOG status flag whenever a frame of data is available for processing. The data frame consists of the processed dot products that were accumulated for CYCLES_PER_COMPUTATION number of

cycles of data. The value for CYCLES_PER_COMPUTATION is 10 cycles when the nominal frequency setting in the software is 50Hz and 12 cycles when the nominal frequency setting in the software is set to 60Hz. When the measured line frequency is equal to the nominal frequency of the design, this is equivalent to 200 milliseconds of accumulated data.

The processed dot products include the V_{RMS}, I_{RMS}, active power, reactive power, fundamental voltage, fundamental active power, and fundamental reactive power. These dot products are used by the foreground process to calculate the corresponding metrology readings in real-world units. All the processed dot products are accumulated in separate 64-bit registers to further process and obtain the RMS and mean values. Using the calculated values of active and reactive power of the foreground process, the apparent power is calculated.

Similarly, using the calculated values of the foreground for the fundamental voltage, fundamental reactive power, and fundamental active power, the fundamental current, fundamental apparent power, voltage THD, and current THD are calculated. Additionally, voltage underdeviation and voltage overdeviation are calculated using the value of the calculated RMS voltage and the defined nominal voltage of the design. The frequency (in Hz) and power factor are also calculated using parameters calculated by the background process using the formulas in the Section 3.1.6.

The foreground process is also responsible for calculating the 1-cycle V_{RMS} readings that are used to update the sag, swell, and interruption state logging variables. The 1-cycle V_{RMS} readings are triggered by the background process after every negative-to-positive zero crossing. After the new V_{RMS} reading, the following state variables are updated accordingly:

- Swell variables
  - **Swell_events:** This variable logs the total number of swell events that have occurred since the design was first reset. The start of a swell event occurs whenever the 1-cycle RMS is above a user-defined sag. The end of a swell threshold event occurs when the 1-cycle RMS is below the user-defined swell threshold minus a user-defined hysteresis value.
  - **Max_swell_value:** This variable is the maximum 1-cycle RMS reading that was observed during the current ongoing swell event. If a swell event is not currently occurring, this variable represents the maximum 1-cycle RMS reading during the previously completed swell event.
  - **Swell_duration:** This variable logs the number of cycles during the current ongoing swell event. If a swell event is not currently occurring, this variable represents the duration of the previously completed swell event.
- Sag Variables
  - **Sag_events:** This variable logs the total number of sag events that have occurred since the design was first reset. The start of a sag event occurs whenever the 1-cycle RMS is below a user-defined sag threshold but is still greater than the user-defined interruption threshold. The end of a sag event occurs when the 1-cycle RMS is above the user-defined sag threshold plus a user-defined hysteresis value.
  - **Min_sag_value:** This variable is the minimum 1-cycle RMS reading that was observed during the current ongoing sag event. If a sag event is not currently occurring, this variable represents the minimum 1-cycle RMS reading during the previously completed sag event.
  - **Sag_duration:** This variable logs the number of cycles during the current ongoing sag event. If a sag event is not currently occurring, this variable represents the duration of the previously completed sag event.
- Interruption Variables
  - **Interruption_events:** This variable logs the total number of interruption events that have occurred since the design was first reset. The start of an interruption event occurs whenever the 1-cycle RMS is below a user-defined interruption threshold, which is lower than the sag voltage threshold.
  - **Interruption_duration:** This variable logs the number of cycles during the current ongoing sag event. If a sag event is not currently occurring, this variable represents the duration of the previously completed interruption event. This variable does not increment when there is no voltage applied to the design since there are no cycles to count; however, the absence of voltage is still able to be counted as an interruption event.

For the one-phase configuration, there are two voltage-current mappings, where each voltage-to-current mapping has a different voltage and current channel. Specifically, the line-to-neutral voltage measurement for

line A and the line A current measurement are associated with each other for one mapping and the line B current measurement is used for neutral current monitoring (no voltage associated).

For the two-phase configuration, there are two voltage-current mappings, where Phase A and Phase B both share the voltage measured with ADS131M02. Specifically, the same line-to-line voltage measurement (180 degrees shift between the voltages on Phase A and Phase B) is associated with the line A and line B current measurements, on ADS131M02 and AMC131M03, respectively.

For simplicity, each voltage-to-current mapping is referred to as a phase in this document as well as in the PC GUI.

3.1.6 Formulas

3.1.6.1 Standard Metrology Parameters

This section briefly describes the formulas used for the voltage, current, power, and energy calculations. As previously described, voltage and current samples are obtained at a sampling rate of 7812.5Hz. All of the samples that are taken in approximately 10 or 12 cycle frames are kept and used to obtain the RMS values for voltage and current for each phase.

The RMS, voltage overdeviation, and voltage underdeviation values are obtained with the following formulas:

$$V_{RMS,ph} = K_{v,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample Count}} V_{ph}(n) \times V_{ph}(n)}{\text{Sample Count}}} - V_{offset,ph} \tag{4}$$

$$V_{underdeviation,ph} = \begin{cases} 0, & \text{if } V_{RMS,ph} > V_{Nom} \\ \left(\frac{V_{Nom} - V_{RMS,ph}}{V_{Nom}} \right) \times 100, & \text{if } V_{RMS,ph} \leq V_{Nom} \end{cases} \tag{5}$$

$$V_{overdeviation,ph} = \begin{cases} 0, & \text{if } V_{RMS,ph} < V_{Nom} \\ \left(\frac{V_{RMS,ph} - V_{Nom}}{V_{Nom}} \right) \times 100, & \text{if } V_{RMS,ph} \geq V_{Nom} \end{cases} \tag{6}$$

$$I_{RMS,ph} = K_{i,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample Count}} I_{ph}(n) \times I_{ph}(n)}{\text{Sample Count}}} - I_{offset,ph} \tag{7}$$

where

- ph = V-I mapping being calculated [that is, V-I_A (= 1) V-I_B (= 2) and V-I_C (= 3)]
- $V_{ph}(n)$ = Voltage sample at a sample instant n
- $V_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the voltage converter. This is in units of mV.
- V_{Nom} = Defined nominal voltage of design
- $I_{ph}(n)$ = Each current sample at a sample instant n
- $I_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the current converter. This is in units of µA.
- Sample count = Number of samples within the present frame
- $K_{v,ph}$ = Scaling factor for voltage
- $K_{i,ph}$ = Scaling factor for current

Power and energy are calculated for active and reactive energy samples of one frame. These samples are phase-corrected and passed on to the foreground process, which uses the number of samples (sample count) to calculate phase active and reactive powers through the following formulas:

$$P_{ACT,ph} = \left(K_{ACT,ph} \times \frac{\sum_{n=1}^{\text{Sample Count}} V_{ph}(n) \times i_{ph}(n)}{\text{Sample Count}} \right) - P_{ACT\_offset,ph} \quad (8)$$

$$P_{REACT,ph} = \left(K_{REACT,ph} \times \frac{\sum_{n=1}^{\text{Sample Count}} V_{90,ph}(n) \times I_{ph}(n)}{\text{Sample Count}} \right) - P_{REACT\_offset,ph} \quad (9)$$

$$P_{APP,ph} = \sqrt{P_{ACT,ph}^{\ 2} + P_{REACT,ph}^{\ 2}} \quad (10)$$

where

- $V_{90,ph}(n)$ = Voltage sample at a sample instant ‘n’ shifted by 90°
- $K_{ACT,ph}$ = Scaling factor for active power
- $K_{REACT,ph}$ = Scaling factor for reactive power
- $P_{ACT\_offset,ph}$ = Offset used to subtract effects of crosstalk on the active power measurements from other currents
- $P_{REACT\_offset,ph}$ = Offset used to subtract effects of crosstalk on the reactive power measurements from other currents

For reactive energy, the 90° phase shift approach is used for two reasons:

1. This approach allows accurate measurement of the reactive power for very small currents.
2. This approach conforms to the measurement method specified by IEC and ANSI standards.

The calculated mains frequency is used to calculate the 90 degrees-shifted voltage sample. Because the frequency of the mains varies, the mains frequency is first measured accurately to phase shift the voltage samples accordingly.

To get an exact 90° phase shift, interpolation is used between two samples. For these two samples, a voltage sample slightly more than 90 degrees before the most recent voltage sample and a voltage sample slightly less than 90 degrees before the most recent voltage sample are used. The phase shift implementation of the application consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap FIR filter. In the test software, a lookup table provides the filter coefficients that are used to create the fractional delays.

Using the calculated powers, energies are calculated with the following formulas :

$$E_{ACT,ph} = P_{ACT,ph} \times \text{Sample Count} \quad (11)$$

$$E_{REACT,ph} = P_{REACT,ph} \times \text{Sample Count} \quad (12)$$

$$E_{APP,ph} = P_{APP,ph} \times \text{Sample Count} \quad (13)$$

The calculated energies are then accumulated into buffers that store the total amount of energy consumed since system reset. These energies are different from the working variables used to accumulate energy for outputting energy pulses. There are three sets of buffers that are available: one for each V-I mapping. Within each set of buffers, the following energies are accumulated:

1. Active import energy (active energy when active power ≥ 0)
2. Active export energy (active energy when active power < 0)
3. Fundamental active import energy (fundamental active energy when fundamental active power ≥ 0)

4. Fundamental active export energy (fundamental active energy when fundamental active power < 0)
5. React. Quad I energy (reactive energy when reactive power ≥ 0 and active power ≥ 0; inductive load)
6. React. Quad II energy (reactive energy when reactive power ≥ 0 and active power < 0; capacitive generator)
7. React. Quad III energy (reactive energy when reactive power < 0 and active power < 0; inductive generator)
8. React. Quad IV energy (reactive energy when reactive power < 0 and active power ≥ 0; capacitive load)
9. Apparent import energy (apparent energy when active power ≥ 0)
10. Apparent export energy (apparent energy when active power < 0)

The background process also calculates the frequency in terms of samples-per-mains cycle. The foreground process then converts this samples-per-mains cycle to Hertz with Equation 14:

$$\text{Frequency}\left(\text{Hz}\right) = \frac{\text{SampleRate}\left(\text{inunitsofsamplesper second}\right)}{\text{Frequency}\left(\text{inunitsofsamplespercycle}\right)} \tag{14}$$

After the active power and apparent power have been calculated, the absolute value of the power factor is calculated. In the internal representation of power factor of the system, a positive power factor corresponds to a capacitive load; a negative power factor corresponds to an inductive load. The sign of the internal representation of power factor is determined by whether the current leads or lags voltage, which is determined in the background process. Therefore, the internal representation of power factor is calculated with Equation 15:

$$\text{Internal Representation of Power Factor} = \begin{cases} \dfrac{P_{ACT}}{P_{App}}, & \text{if capacitive load} \\ -\dfrac{P_{ACT}}{P_{App}} & \text{if inductive load} \end{cases} \tag{15}$$

3.1.6.2 Power Quality Formulas

For calculating the fundamental RMS voltage, a pure sine wave is generated and tightly locked to the fundamental of the incoming voltage waveform. Using the generated waveform, the fundamental voltage, fundamental active power, and fundamental reactive power are calculated by the following equations:

$$V_{fund,ph} = K_{v\_fund,ph} \times \frac{\sum_{n=1}^{\text{Sample Count}} V_{pure,ph}(n) \times V_{ph}(n)}{\text{SampleCount}} - V_{fund\_offset,ph} \tag{16}$$

$$P_{ACT\_fund,ph} = \left(K_{ACT\_fund,ph} \times \frac{\sum_{n=1}^{\text{Sample Count}} V_{pure,ph}(n) \times i_{ph}(n)}{\text{SampleCount}} \right) - P_{ACT\_fund\_offset,ph} \tag{17}$$

$$P_{REACT\_fund,ph} = \left(K_{REACT\_fund,ph} \times \frac{\sum_{n=1}^{\text{Sample Count}} V_{90\_pure,ph}(n) \times I_{ph}(n)}{\text{SampleCount}} \right) - P_{REACT\_fund\_offset,ph} \tag{18}$$

where

- $V_{pure,ph}(n)$ = Voltage sample of the pure sine wave generated, taken at a sample instant *n*
- $V_{90\_pure,ph}(n)$ = Voltage sample of the waveform that results from shifting $V_{pure,ph}(n)$ by 90° , taken at a sample instant n
- $K_{v\_fund,ph}$ = Scaling factor for fundamental voltage
- $K_{ACT\_fund,ph}$ = Scaling factor for fundamental active power
- $K_{REACT\_fund,ph}$ = Scaling factor for fundamental active power
- $V_{fund\_offset\_,ph}$= Offset to subtract from fundamental voltage calculation. This is in units of mV.
- $P_{ACT\_fund\_offset,ph}$= Offset to subtract from fundamental active power calculation. This is in units of mW.

- $P_{REACT\_fund\_offset,ph}$ = Offset to subtract from fundamental reactive power calculation. This is in units of mvar.

After calculating the fundamental voltage, fundamental active power, and fundamental reactive power, the fundamental current and fundamental apparent power are calculated with the following formulas:

$$I_{fund,ph} = \left(K_{i_{fund},ph} \times \frac{\sqrt{P^2_{ACT_{fund},ph} + P^2_{REACT_{fund},ph}}}{V_{fund,ph}} \right) - I_{fund\_offset,ph} \quad (19)$$

$$P_{APP\_fund,ph} = \sqrt{P^2_{ACT_{fund},ph} + P^2_{REACT_{fund},ph}} \quad (20)$$

where

- $K_{i\_fund,ph}$ = Scaling factor for fundamental current
- $I_{fund\_offset\_,ph}$ = Offset to subtract from fundamental current calculation. This is in units of µA.

Once the fundamental current and fundamental voltage are calculated, the voltage THD and current THD can also be calculated. This software supports three different methods of calculating THD that are referred to as THD_{IEC_F}, THD_{IEC_R}, and THD_{IEEE}. The formulas used to calculate voltage THD (V_THD) and current THD (I_THD) with the different methods as follows:

$$V\_THD_{IEC\_F,ph} = \frac{\sqrt{V^2_{RMS,ph} - V^2_{fund,ph}}}{V_{fund,ph}} \quad I\_THD_{IEC\_F,ph} = \frac{\sqrt{I^2_{RMS,ph} - I^2_{fund,ph}}}{I_{fund,ph}} \quad (21)$$

$$V\_THD_{IEC\_R,ph} = \frac{\sqrt{V^2_{RMS,ph} - V^2_{fund,ph}}}{V_{RMS,ph}} \quad I\_THD_{IEC\_R,ph} = \frac{\sqrt{I^2_{RMS,ph} - I^2_{fund,ph}}}{I_{RMs,ph}} \quad (22)$$

$$V\_THD_{IEEE,ph} = \frac{V^2_{RMS,ph} - V^2_{fund,ph}}{V^2_{fund,ph}} \quad I\_THD_{IEEE\_F,ph} = \frac{I^2_{RMS,ph} - I^2_{fund,ph}}{I^2_{fund,ph}} \quad (23)$$

To calculate THD correctly, it is necessary to select the proper method of THD calculation and to make sure that any reference meter used for measuring THD uses the same THD method as the method selected in software.

3.1.7 Background Process

Figure 3-3 shows the different events that occur when sampling voltage and current, where the items in green are done by the MSPM0G1106 hardware modules.

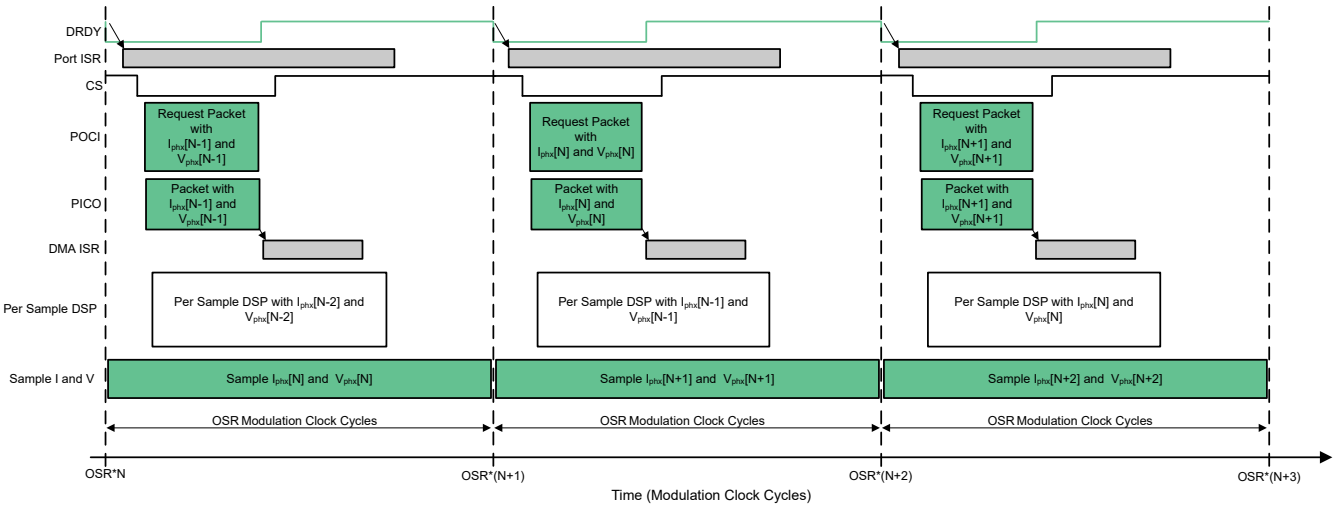


Figure 3-3. Voltage and Current Sampling Events

New current samples for each phase are ready every OSR, or 1024 modulation clock cycles for this design, thus resulting in 4000 samples per second over the SPI bus to MSPM0+ MCU. The data transfer consists of two transactions: sample contains 12 Bytes, with three Bytes data on each of the two ADS131M02 channels and then another 15 Bytes, with data for one channel for the shunt and twice 0x00 00 00 data for the unused and disabled per software other two analog input channels for AMC131M03.

Suppose the most recently ready phase current and voltage samples from the ADS131M02 and AMC131M03 devices corresponds to the $N^{th} - 1$ current and voltage sample, or $I_{phx}[N - 1]$ and $V_{phx}[N - 1]$. Once new samples are ready, the $\overline{DRDY}$ pin is asserted low by the ADS131M02. The falling edge on the $\overline{DRDY}$ pin on the ADS131M02 causes a GPIO port interrupt on the MSPM0+ MCU, which triggers the Port ISR, and the background process is run within the Port ISR. The AMC131M03 also raises the $\overline{DRDY}$ pin interrupt and that is served immediately after the ADS131M02 read out over SPI is finished.

Figure 3-4 shows the background process, which mainly deals with timing-critical events in the test software.

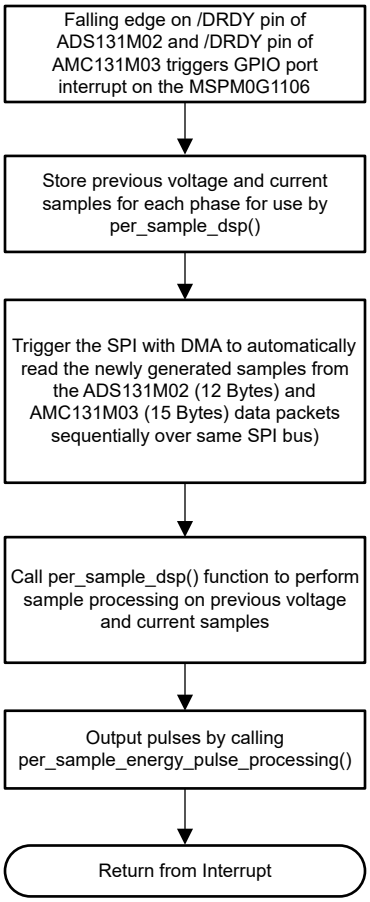


Figure 3-4. Background Process

In the background process, the previously-obtained voltage samples ($V_{phx}[N – 2]$) and previously obtained current samples ($I_{phx}[N – 2]$) are stored so that these samples can be used later by the `per_sample_dsp ()` function, which is responsible for updating the intermediate dot product quantities used to calculate metrology parameters.

After the previously-obtained voltage and current samples from ADS131M02 and AMC131M03 are stored, communication to the ADS131M02 is enabled by asserting the respective chip select signal low. The DMA is then configured to both send a request for the newest current and voltage samples ($I_{phx}[N – 1]$ and $V_{phx}[N – 1]$) of the ADS131M02 device and also to receive the data packet response from the ADS131M02. The request (transmitting dummy data of 0x00) and reception of the latest ADC data samples is done automatically by the DMA module.

Figure 3-5 shows the packet that is transmitted by the DMA of the MSPM0+ MCU and the response packet from the ADS131M02 or AMC131M03 that is received by the DMA as well. The transmission and reception packets contain four or five words, where each word is three bytes long, resulting in 12 or 15 Bytes DMA transaction over the SPI bus. Note that the ADS131M02 packet is 12 Bytes long, as only two channels with three bytes each are read out through the DMA transaction, while AMC131M03 needs 15 Bytes. The firmware handles the ADC device selection automatically and reads data out in a round-robin manner, as the firmware updates the DMA parameters for each ADC, including the packet data length and activates the correct $\overline{CS}$ line to each ADC.

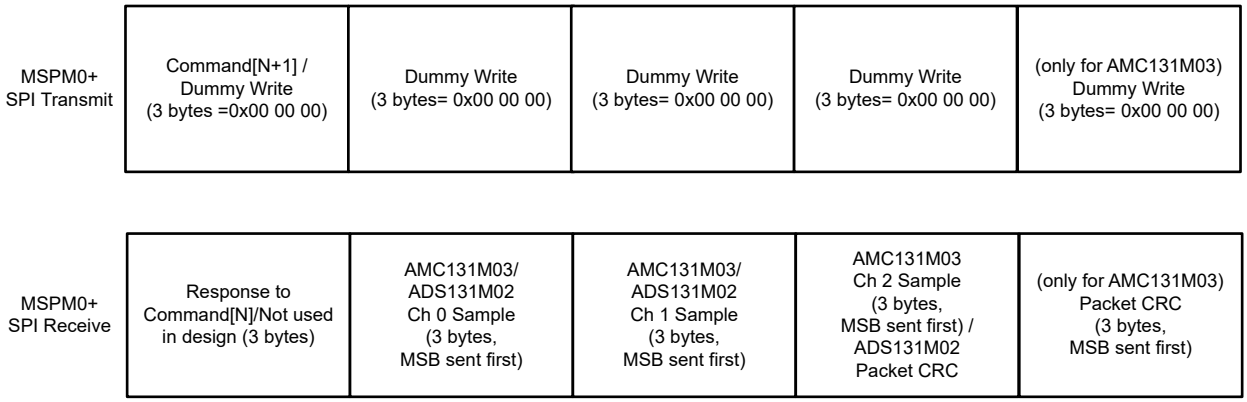


Figure 3-5. ADS131M02 and AMC131M03 ADC Sample Request Packet

When requesting the ADC data from the ADS131M02 device, the first word that has to be sent to by MSPM0+ MCU is the command word. Since the test software does not need to change the settings of the ADS131M02 or read any registers during typical ADC sample readouts, a NULL command is sent to the ADS131M02, which allows the designer to get the ADC samples from the ADS131M02 without changing the state of the device.

The actual size of the null command is 16 bits; however, since 24-bit words are used, the 16-bit command must be padded with an extra value of 0x00 at the end of the command. The NULL command word sent; therefore, has a value of 0x00 00 00. While the MSPM0+ MCU is shifting out the command word, the MCU is simultaneously shifting in the response word to the command word of the previous packet. The response word to a NULL command is the contents of the STATUS register. The contents of the STATUS register is not used in this design so the first word received from the ADS131M02 is ignored (not processed in the software code).

After writing the command word, a dummy write must be performed for each byte that is to be read. The dummy byte write is necessary to enable the SPI clock, which is necessary to read a byte from the ADS131M02 device. For each dummy byte write, a value of 0x00 is written to the SPI transmit register. Immediately after writing the command byte, writing three dummy bytes allows the MSPM0+ MCU to receive the 3-byte ADC value from channel 0 of the ADS131M02. Writing the next 3 dummy bytes gets the ADC data for channel 1 and writing the next three dummy bytes gets the CRC word. The CRC word is 24-bits; however, note that the actual CRC is only 16 bits, which are placed in the most significant bits of the 24-bit word. As a result, when parsing the CRC word, the last byte is not needed (note though that the dummy write for this zero-padded byte must still be sent though for proper ADS131M02 operation).

Whenever the DMA has received the entire $I_{phx}[N - 1]$ packet, the DMA ISR is automatically called. Within the ISR, the CRC is calculated over the three command and the ADC channel data words (3 × 3 = 9 Bytes in total). This CRC calculation can be done in two modes: either using the CRC module of the MSPM0G110 MCU or using the `memcpy()` function to move the 9 Bytes ADC data to a special memory area where CRC16 is auto-calculated.

Immediately after the SPI data from AMC131M03 is read out, but using the NULL command and three channels of 24-bit data and CRC16 with a padded 0x00 Byte. This completes the read in of the current samples $I_{phx}[N - 1]$ of the AMC131M03 device, then the CRC16 checksum is also checked.

See the `ADS_verifyADSCRC()` and `AMC_verifyAMCCRC()` routines for details of the CRC16 check implementation. The `memcpy()` implementation achieves almost 5 × faster calculation than using the CRC16 registers with bytewise feed and is hence used by default. The CRC module can be fed with 8- or 16-bit data, and since there are nine bytes total, the CRC module is being updated byte for byte. Once the CRC has been calculated over the packet, the check is compared to the CRC obtained in the packet sent from the ADS131M02. The sent CRC is parsed from Bytes 10 and 11 (the last Byte 12 is the zero-padding for CRC16, so this value gets ignored).

If the calculated CRC and the parsed CRC are equal, then the CRC check is correct and the ADC data is parsed to get the values of the voltage and current samples at time N – 1. Two variables are used to count the good and bad CRC16 packets for each ADC, called `crcPassCount` and `crcFailCount`. The parsed voltage and current samples are put in temporary buffers so that this information is used when the `per_sample_dsp()` function is called at the next interrupt. When the SPI transfer over DMA ends, the $\overline{CS}$ (chip select) line is automatically pulled back high again from the MSPM0+ MCU to properly reset the AMC131M03 communication before the next time current samples are ready for readout.

In parallel to transferring the latest current and voltage samples $I_{phx}[N – 1]$ and $V_{phx}[N – 1]$ to the MSPM0+ MCU using the DMA channels, the ADS131M02 is already sampling the next voltage ($V_{phx}[N]$) and current samples ($I_{phx}[N]$) while the test software performs per-sample processing on the earlier voltage ($V_{phx}[N – 2]$) and current samples ($I_{phx}[N – 2]$) obtained from the ADS131M02 and AMC131M03. This per-sample processing is used to update the intermediate dot product quantities that are used to calculate the metrology parameters. After sample processing, the background process uses the `per_sample_energy_pulse_processing` for the calculation and output of energy-proportional pulses. The test software exits from the port ISR once the `per_sample_energy_pulse_processing` is completed.

In summary there are two SPI read data cycles during a single $\overline{DRDY}$ cycle, the ADS131M02 device is read out first and then the AMC131M03. The only difference between these two SPI transactions is that ADS131M02 has two channels while AMC131M03 has three, so the SPI data packet length is either 12 Bytes or 15 Bytes total.

3.1.8 Software Function per_sample_dsp()

Figure 3-6 shows the flowchart for the per_sample_dsp() function. The per_sample_dsp() function is used to calculate intermediate dot product results that are fed into the foreground process for the calculation of metrology readings. Both voltage and current samples are processed and accumulated in dedicated 64-bit registers. Per-phase active power and reactive power are also accumulated in 64-bit registers.

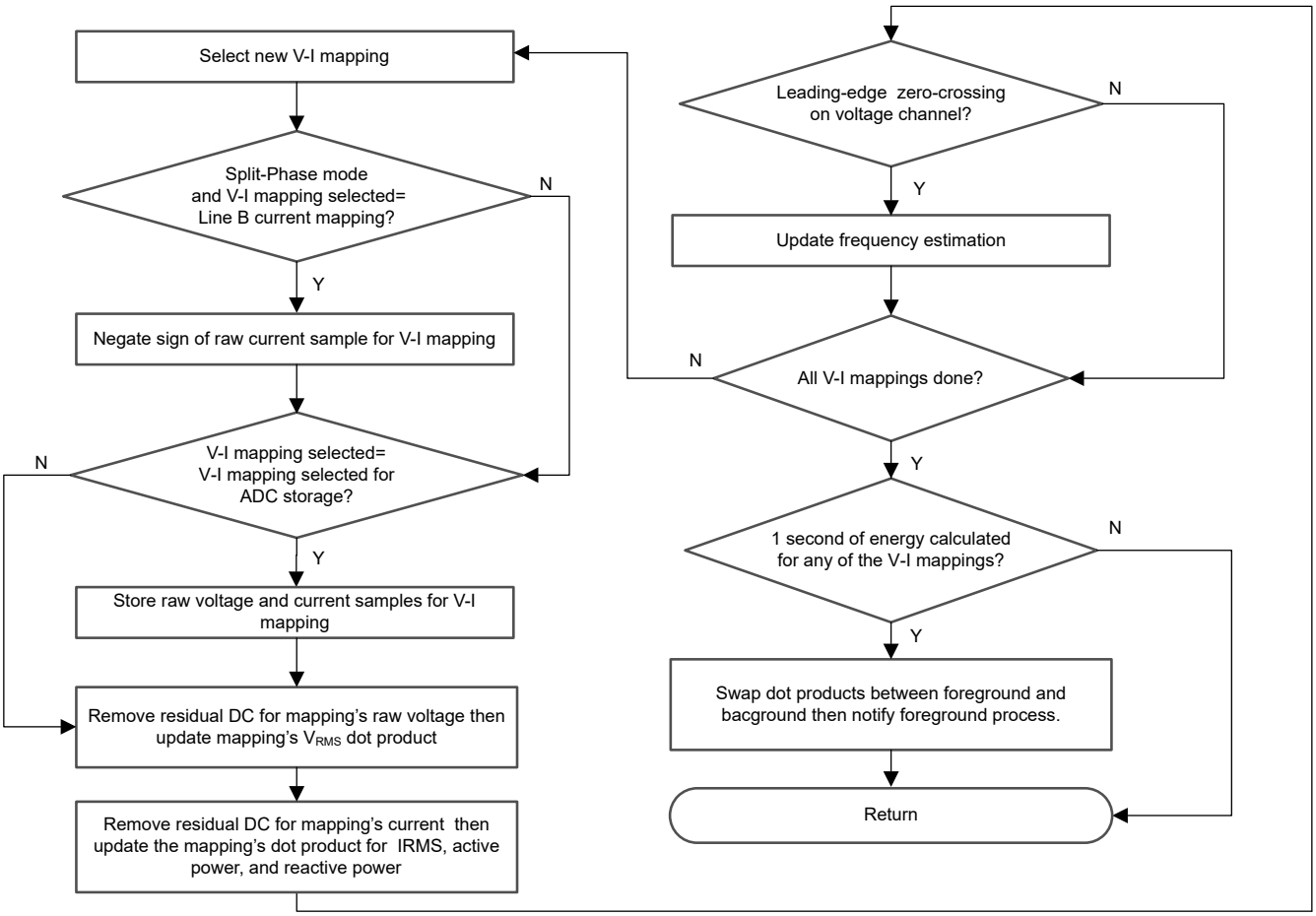


Figure 3-6. per_sample_dsp () Function

After *CYCLES_PER_COMPUTATION* number of cycles (10 cycles if F_{NOM} = 50Hz and 12 cycles if F_{NOM} = 60Hz) have been accumulated, the background process triggers the foreground function to calculate the final values of RMS voltage and current; active, reactive, and apparent powers; active, reactive, and apparent energy; frequency; power factor; fundamental voltage, fundamental current, fundamental active power, fundamental reactive power, and fundamental apparent power; voltage underdeviation and voltage overdeviation; and voltage THD and current THD. In the software, there are two sets of dot products: at any given time, one is used by the foreground for calculation and the other used as the working set by the background. After the background process has sufficient samples, the process swaps the two dot products so that the foreground uses the newly acquired dot products that the background process just calculated and the background process uses a new empty set to calculate the next set of dot products.

Whenever there is a leading-edge zero-crossing (− to + voltage transition) on a voltage channel, the per_sample_dsp() function is also responsible for updating the frequency (in samples per cycle) of the corresponding phase and triggering the calculation of the foreground of the 1-cycle V_{RMS} reading. This 1-cycle V_{RMS} reading is a different calculation than the V_{RMS} reading that is updated every *CYCLES_PER_COMPUTATION* number of cycles. The 1-cycle V_{RMS} reading is specifically used for updating the sag, swell, and interruption state variables. The 1-cycle V_{RMS} calculation uses the same dot-product swapping scheme as the scheme used for the *CYCLES_PER_COMPUTATION* dot products.

The `per_sample_dsp()` function is also responsible for outputting a voltage zero crossing pin (optional). Whenever there is a negative to positive zero crossing on a voltage channel and the corresponding 1-cycle V_{RMS} reading of the voltage channel is greater than the interruption threshold, a falling edge is asserted on this pin. If there is a positive to negative zero crossing on a voltage channel and the 1-cycle V_{RMS} reading of the voltage channel is greater than the interruption threshold, a rising edge is asserted on this pin. To reduce the impact of outputting the zero crossing pin on the accuracy of the design, the zero crossing output needs to not be selected to be on a GPIO pin connected to a LED.

The following sections describe the various elements of electricity measurement in the `per_sample_dsp()` function.

3.1.9 Voltage and Current Signals

The test software of the design has support for storing the raw voltage and current ADC values for phases A and B, or A and Neutral. These raw ADS131M02 and AMC131M03 samples are signed integers and any stray DC or offset value on these converters are removed using a DC tracking filter. A separate DC estimate for all voltages and currents is obtained using the filter, voltage, and current samples, respectively. This estimate is then subtracted from each voltage and current raw ADC sample.

The resulting instantaneous voltage and current samples are used to generate the following intermediate results:

- Accumulated squared values of voltages and currents, which is used for V_{RMS} and I_{RMS} calculations, respectively
- Accumulated energy samples to calculate active energy
- Accumulated energy samples using current and 90° phase-shifted voltage to calculate reactive energy

The foreground process processes these accumulated values.

3.1.10 Pure Waveform Samples

To calculate the fundamental and THD readings, the software generates a pure sinusoid waveform and locks the sinusoid waveform to the fundamental of the incoming voltage waveform. Since the generated waveform is locked to the fundamental of the incoming voltage, the correlation of this pure waveform with the waveform from the voltage ADC can be used to find the amplitude of the fundamental component of the waveform sensed by the voltage ADC. Similarly, the correlation of the current and the pure voltage waveform can be used to calculate the fundamental active power. For fundamental reactive power, the correlation of the 90° shifted pure waveform and the current can be used for calculating this parameter.

To generate a sine wave, information on the amplitude, phase, and frequency of the desired waveform is necessary. For the generated pure waveform, the amplitude is set to full scale to maximize the value of the fundamental dot products, the frequency is set to the measured frequency (in units of cycles per sample) that is used to calculate the mains frequency in final real-world units of Hertz, and the phase of the generated waveform is iteratively adjusted so that the generated waveform is locked to the phase of the fundamental voltage. After the frequency is correctly calculated and the generated phase of the waveform is locked to the fundamental voltage, the fundamental readings can then be correctly calculated.

3.1.11 Frequency Measurement and Cycle Tracking

The instantaneous voltage, currents, active powers, and reactive powers are accumulated in 64-bit registers. A cycle tracking counter keeps track of the number of cycles accumulated. When `CYCLES_PER_COMPUTATION` number of cycles have been accumulated, the background process stores these accumulation registers and notifies the foreground process to produce the average results, such as RMS and power values. Cycle boundaries are used to trigger the foreground averaging process because this process produces very stable results.

For frequency measurements, a straight line interpolation is used between the zero crossing voltage samples. Figure 3-7 shows the samples near a zero cross and the process of linear interpolation.

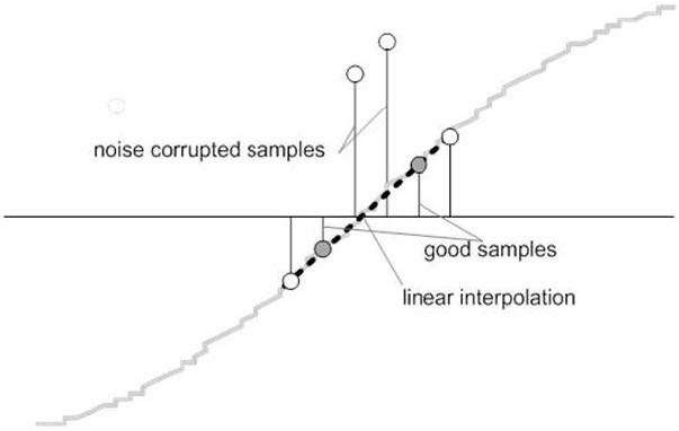


Figure 3-7. Frequency Measurement

Because noise spikes can also cause errors, the application uses a rate-of-change check to filter out the possible erroneous signals and make sure that the two points are interpolated from genuine zero crossing points. For example, with two negative samples, a noise spike can make one of the samples positive, thereby making the negative and positive pair appear as if there is a zero crossing.

The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out any cycle-to-cycle variations. This filtering results in a stable and accurate frequency measurement that is tolerant of noise.

3.1.12 LED Pulse Generation

In electricity meters, the energy consumption of the load is normally measured in a fraction of kilowatt-hour (kWh) pulses. This information can be used to accurately calibrate any meter for accuracy measurement. Typically, the measuring element (the MSPM0+ microcontroller) is responsible for generating pulses proportional to the energy consumed. To serve both these tasks efficiently, the pulse generation must be accurate with relatively little jitter. Although time jitters are not an indication of bad accuracy, time jitters give a negative indication of the overall accuracy of the meter. The jitter must be averaged out due to this negative indication of accuracy.

This application uses average power to generate these energy pulses. The average power accumulates at every $\overline{\text{DRDY}}$ port ISR interrupt, thereby spreading the accumulated energy from the previous one-second time frame evenly for each interrupt in the current one-second time frame. This accumulation process is equivalent to converting power to energy. When the accumulated energy crosses a threshold, a pulse is generated. The amount of energy above this threshold is kept and a new energy value is added on top of the threshold in the next interrupt cycle. Because the average power tends to be a stable value, this way of generating energy pulses is very steady and free of jitter.

The threshold determines the energy *tick* specified by meter manufacturers and is a constant. The tick is usually defined in pulses-per-kWh or just in kWh. One pulse must be generated for every energy tick. For example, in this application, the number of pulses generated per kWh is set to 6400 for active and reactive energies. The energy tick in this case is 1kWh / 6400. Energy pulses are generated and available on the ACT and REACT pins headers and also through light-emitting diodes (LEDs) on the board. GPIO pins are used to produce the ACT and REACT energy pulses.

In the reference design, the LED that is labeled *Active* corresponds to the active energy consumption for the single-phase or split-phase sum. *Reactive* corresponds to the cumulative split-phase reactive energy sum.

Figure 3-8 shows the flow diagram for pulse generation with a pulse constant of 6400, though TI recommends reducing this value to 3600 or even lower if the energy meter supports currents beyond 80A.

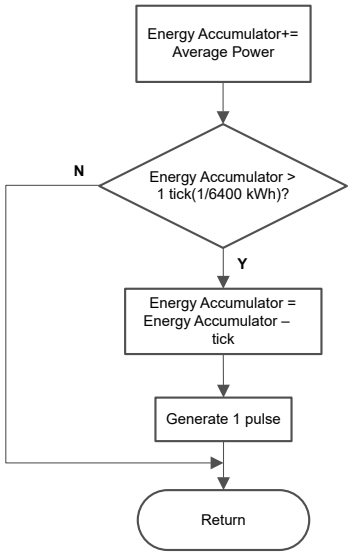


Figure 3-8. Pulse Generation for Energy Indication

The average power is in units of 0.001W and a 1kWh threshold is defined in Equation 24.

$$\text{1kWh threshold} = \frac{1}{0.001} \times 1\ \text{kW} \times \left(\text{Number of interrupts per second}\right) \times \left(\text{Number of seconds in one hour}\right) = 1000000 \times 8000 \times 3600 = 0\text{x1A3185C50000} \quad (24)$$

3.1.13 Phase Compensation

When a current transformer (CT) is used as a sensor, the CT introduces additional phase shift on the current signals. Also, the passive components of the voltage and current input circuit can introduce another phase shift. The designer must compensate the relative phase shift between voltage and current samples to provide accurate measurements.

The implementation of the phase shift compensation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap finite impulse response (FIR) filter that interpolates between two samples, similar to the FIR filter used for providing 90°-shifted voltage samples for reactive energy measurements. In the test software, a lookup table provides the filter coefficients that are used to create the fractional delays. The lookup table provides fractional phase shifts as small as 1/256th of a sample. The 4000Hz sample rate used in this application corresponds to a 0.0176° degree resolution at 50Hz. In addition to the filter coefficients, the lookup table also has an associated gain variable for each set of filter coefficients. This gain variable is used to cancel out the resulting gain from using a certain set of filter coefficients.

An alternative option to the software phase compensation used in this design is to use the phase compensation feature on the ADS131M02 and AMC131M03 devices. If this hardware phase compensation scheme is used, filter coefficients are not necessary so it is not necessary to divide by the gain of the filter coefficients.

3.2 Test Setup

Top View of TIDA-010944 Design With Components Highlighted shows the TIDA-010944 photo with all functions on the top layer of the PCB; the bottom layer of the PCB has no components.

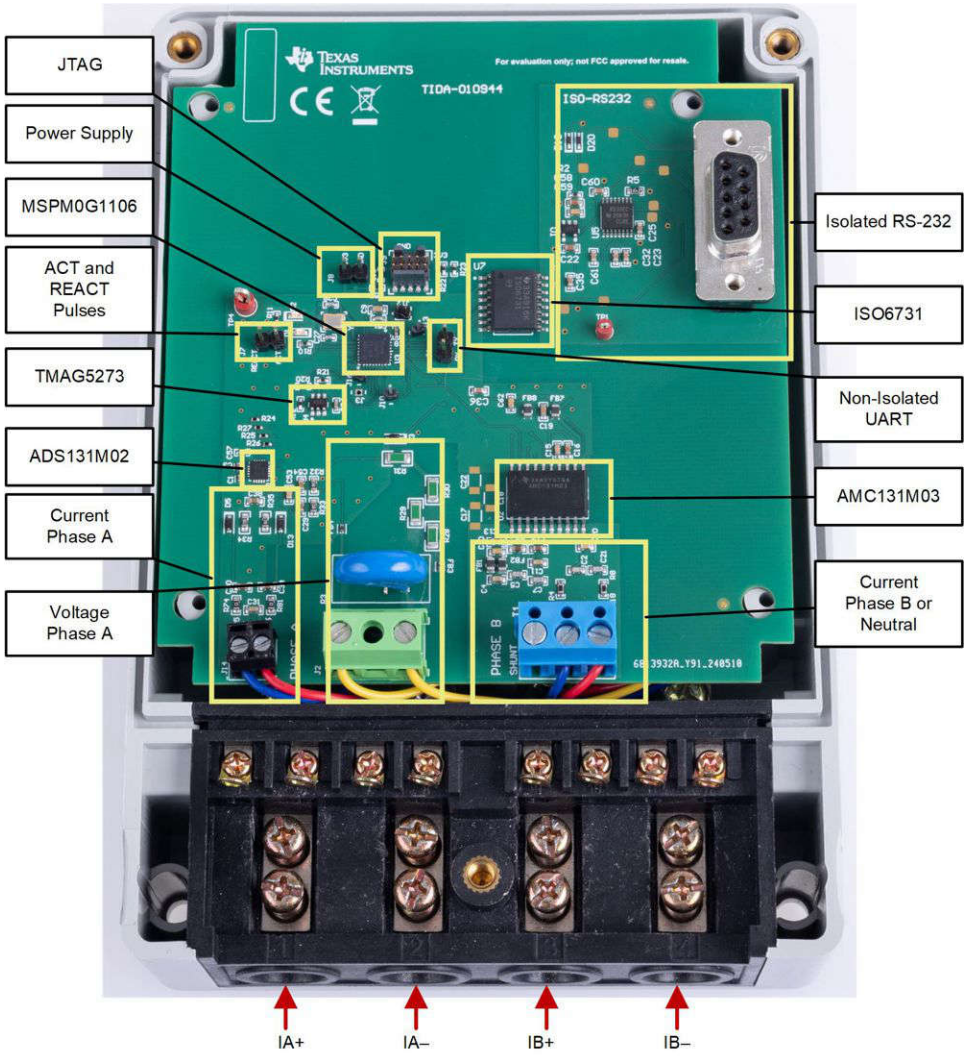


Figure 3-9. Top View of TIDA-010944 Design With Components Highlighted

The Phase A voltage is applied to J2, whereas terminal blocks J1 and J14 are used to connect the shunts for Phase B and A respectively.

Terminal blocks J2 has two positions: position 1 connects to Phase A voltage, whereas position 2 connects either to Neutral (single-phase *star* with 1P2W) or Phase B voltage (split-phase *delta* with 2 line voltages of 180° apart or 2P2W).

3.2.1 Power Supply Options and Jumper Setting

The M0+ MCU and the two stand-alone ADCs are powered from an external power supply by connecting a 3.3V external power supply to J8, which provides access to GND and VDD_3V3 pins. The UART port for communication to the PC GUI is accessible at the isolated 9-pin RS232 connector RS1 or non-isolated on J4. The J7 header provides access to ACT and REACT pulse outputs, needed for calibration.

Note that J4 is not isolated, so do not use measuring equipment there (especially if the system is referenced with respect to the line) when running off the Mains. This applies, unless either isolators external to the board of the design are used to connect at the headers, if the equipment is battery powered and does not connect to Mains, or if AC mains is isolated.

At high currents, the terminal block can get warm. In addition, note that the phase voltages are fed to the board so take the proper precautions.

WARNING

Hot Surface! Contact can cause burns. Do not touch. Take the proper precautions when operating.

CAUTION

High Voltage! Electric shocks are possible when connecting the board to live wires. The board must be handled with care by a professional. For safety, use of isolated test equipment with overvoltage or overcurrent protection is highly recommended.

3.2.2 Electricity Meter Metrology Accuracy Testing

To test for metrology accuracy in the electricity meter configuration, a source generator is used to provide the voltages and currents to the system at the proper locations mentioned in Figure 3-9. In this design, a nominal voltage of 120V between the line and neutral, calibration current of 10A, and nominal frequency of 50Hz are used for each of the two phases.

When the voltages and currents are applied to the system, the system outputs the cumulative active energy pulses and cumulative reactive energy pulses at a rate of 6400 pulses per kWh. This pulse output is fed into a reference meter (in the test equipment for this reference design, this pulse output is integrated in the same equipment used for the source generator) that determines the energy % error based on the actual energy provided to the system and the measured energy as determined by the active and reactive energy output pulse of the system. For the split-phase configuration, cumulative active energy error testing, cumulative reactive energy error testing, individual phase active energy testing, and frequency variation testing are performed after performing the energy gain calibration and phase compensation as described in Section 3.2.4. In addition to the energy error tests, the RMS voltage % error and RMS current % error are measured as well.

3.2.3 Viewing Metrology Readings and Calibration

This section describes the methods used to verify the results of this design with the test software.

3.2.3.1 Calibrating and Viewing Results From PC

To view the metrology parameter values from the GUI, perform the following steps:

1. Connect the reference design to a PC using an RS-232 cable. If the PC does not have an RS-232 adapter, use a serial RS-232 adapter to create a COM port on the PC when the adapter is plugged in, the default UART setting is 9600,8,n,1.
2. Open the GUI folder and open *calibration-config.xml* in a text editor.
3. Change the *port name* field within the *meter* tag to the COM port connected to the system. As Figure 3-10 shows, this field is changed to *COM7*.

```
260       </correction>
261     </phase>
262     <temperature/>
263     <rtc/>
264   </cal-defaults>
265   <meter position="1">
266     <port name="com7" speed="9600"/>
267   </meter>
268   <reference-meter>
269     <port name="USB0::0x0A69::0x0835::A66200101281::INSTR"/>
270     <type id="chroma-66202"/>
271     <log requests="on" responses="on"/>
272     <scaling voltage="1.0" current="1.0"/>
273   </reference-meter>
```

Figure 3-10. GUI Configuration File Changed to Communicate With Energy Measurement System

4. Run the *calibrator.exe* file, which is located in the GUI folder. If the COM port in the *calibration-config.xml* was changed in the previous step to the COM port connected to the reference design, the GUI opens (see Figure 3-11). If the GUI connects to the design properly, the top-left button is green. If there are problems with connections or if the code is not configured correctly, the button is red. Click the green button to view the results.

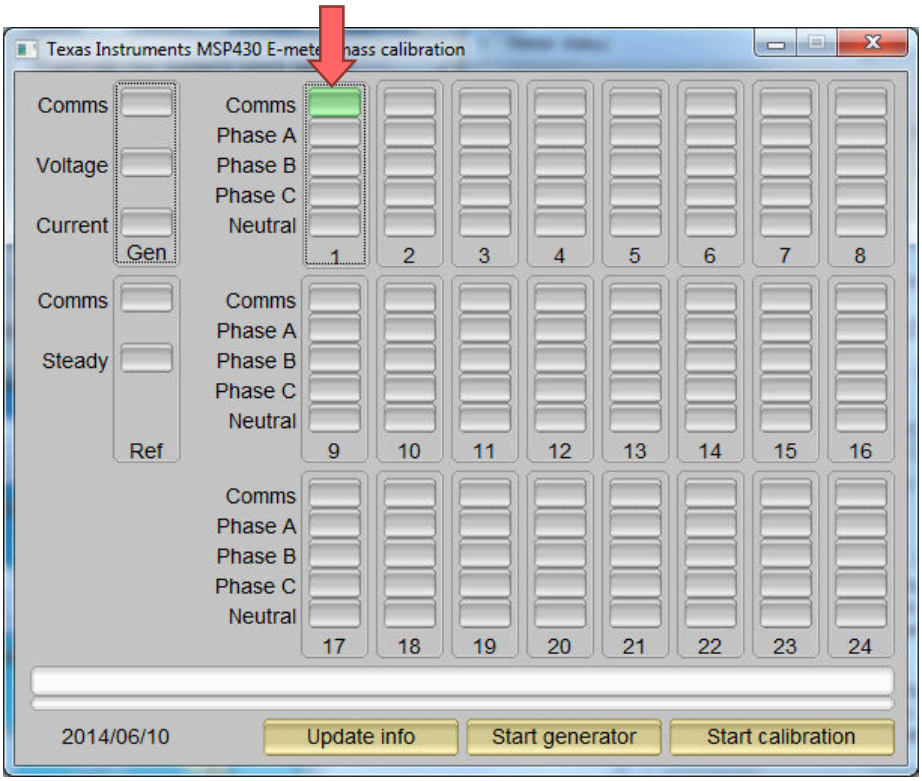


Figure 3-11. GUI Start-Up Window

Upon clicking on the green button, the results window opens (see Figure 3-12). In the figure, there is a trailing "L" or "C" on the *Power factor* values to indicate an inductive or capacitive load, respectively.

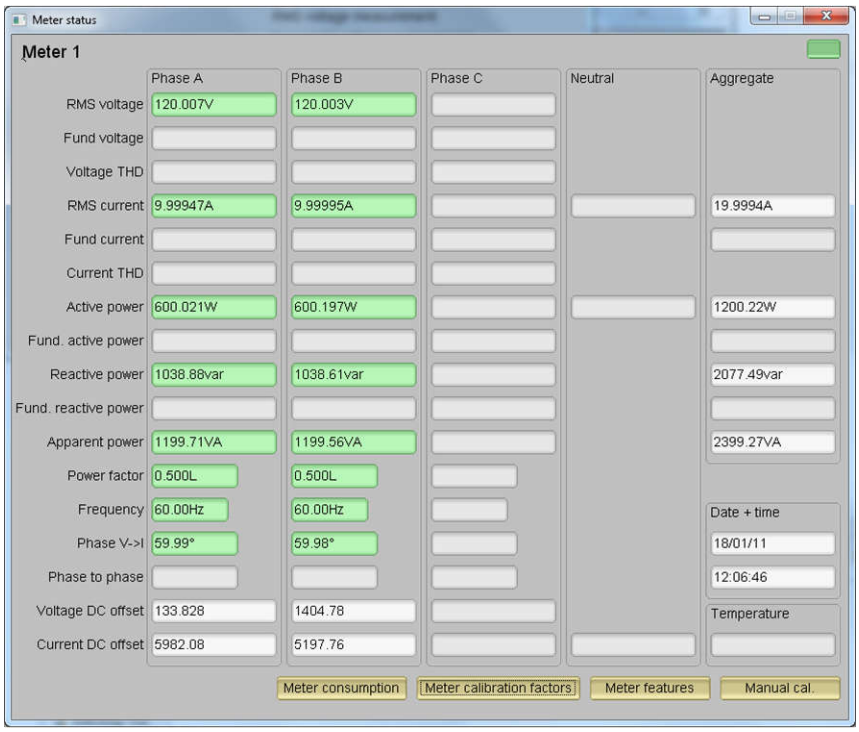


Figure 3-12. GUI Results Window

From the results window, view the total-energy consumption readings by clicking the *Meter Consumption* button. After the user clicks this button, the *Meter events and consumption* window pops up, as Figure 3-13 shows.

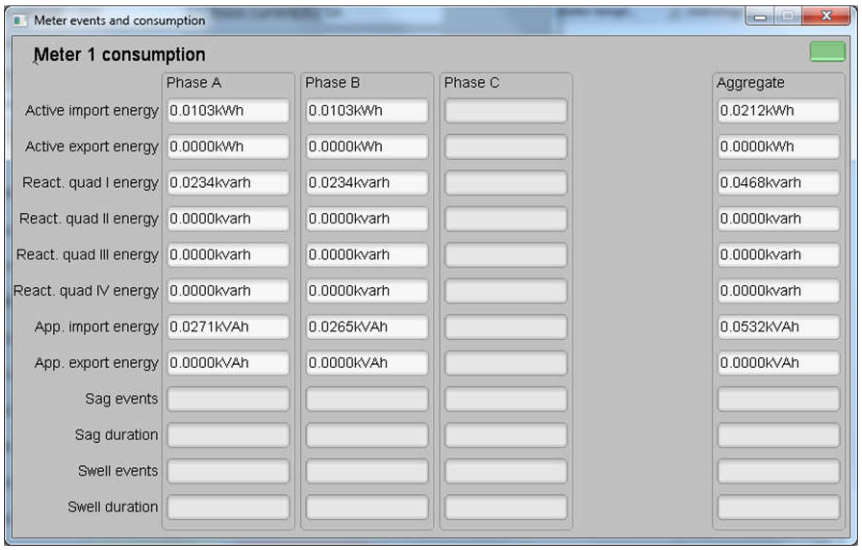


Figure 3-13. Meter Events and Consumption Window

From the results window, the user can also view the meter settings by clicking the *Meter features* button, view the system calibration factors by clicking the *Meter calibration factors* button, or open the window used for calibrating the system by clicking the *Manual cal.* button.

3.2.4 Calibration and FLASH Settings for MSPM0+ MCU

Calibration is key to any meter performance, and calibration is absolutely necessary for every meter to go through this process. Initially, every meter exhibits different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify the effects, every meter must be calibrated. To perform calibration accurately, there must be an accurate AC test source and a reference meter available. The source must be able to generate any desired voltage, current, and phase shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section discusses a simple and effective method of calibration of this split-phase electricity meter design.

The GUI used for viewing measurement results can also easily be used to calibrate the design. During calibration, parameters called calibration factors are modified in the test software to give the least error in measurement. For this meter, there are six main calibration factors for each phase: voltage scaling factor, active power offset (erroneously called voltage AC offset in the GUI), current scaling factor, reactive power offset (erroneously called current AC offset in the GUI), power scaling factor, and the phase compensation factor. The voltage, current, and power scaling factors translate measured quantities in metrology software to real-world values represented in volts, amps, and Watts, respectively. The power offset is used to subtract voltage to current crosstalk, which appears as a constant power offset and causes greater inaccuracies at lower currents. Offset calibration was not used for testing this specific design. The last calibration factor is the phase compensation factor, which is used to compensate any phase shifts introduced by the current sensors and other passives. The voltage, current, and power calibration factors are independent of each other. Therefore, calibrating voltage does not affect the readings for RMS current or power.

When the meter software is flashed on the MSPM0G1106 device for the first time, default calibration factors are loaded into these calibration factors. Calibration factors or values are modified through the GUI during calibration. The calibration factors are also stored in the last MSPM0+ MCU FLASH sector and therefore, remain the same if the meter is restarted.

Calibrating any of the scaling factors is referred to as gain correction. Calibrating the phase compensation factors is referred to as phase correction. For the entire calibration process, the AC test source must be ON, meter connections consistent with Figure 3-9, and the energy pulses connected to the reference meter.

3.2.5 Gain Calibration

Usually, gain correction for voltage and current can be done simultaneously for all phases. However, energy accuracy (%) from the reference meter for each individual phase is required for gain correction for active power. Also, when performing active power calibration for any given phase, the other phases must be turned OFF by turning off the current but leaving the other voltages still enabled.

3.2.6 Voltage and Current Gain Calibration

To calibrate the voltage and current readings, perform the following steps:

1. Connect the GUI to view results for voltage, current, active power, and the other metering parameters.
2. Configure the test source to supply the desired voltage and current for all phases. Make sure that these are the voltage and current calibration points with a zero-degree phase shift between each phase voltage and current. For example, for 120V, 10A, 0° (PF = 1). Typically, these values are the same for every phase.
3. Click on the *Manual cal.* button in Figure 3-12. The screen in Figure 3-14 pops up:

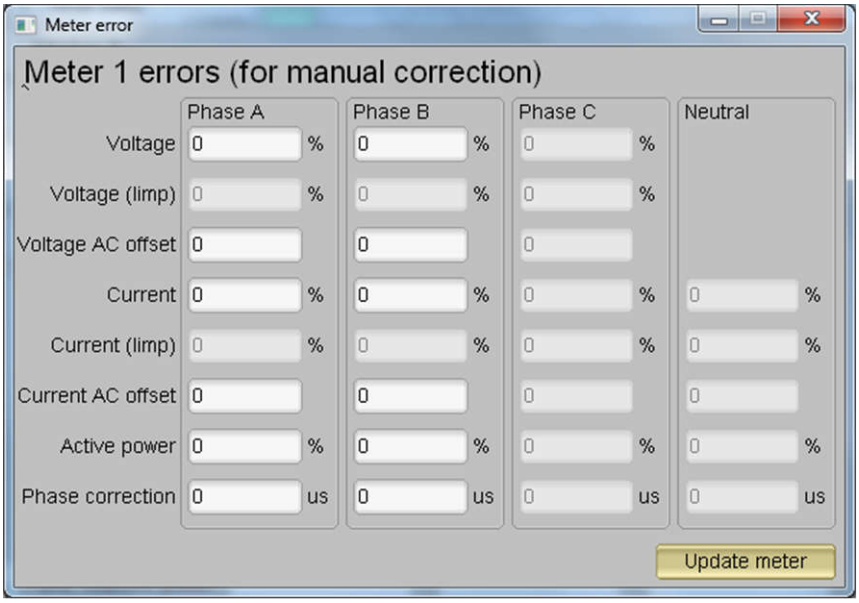


Figure 3-14. Manual Calibration Window

4. Calculate the correction values for each voltage and current. The correction values that must be entered for the voltage and current fields are calculated using Equation 25:

$$\text{Correction (\%)} = \left(\frac{\text{value}_{\text{observed}}}{\text{value}_{\text{desired}}} - 1 \right) \times 100 \tag{25}$$

where

- $\text{value}_{\text{observed}}$ is the value measured by the TI meter
- $\text{value}_{\text{desired}}$ is the calibration point configured in the AC test source

5. After calculating for all voltages and currents, input these values as is (±) for the fields *Voltage and Current* for the corresponding phases.
6. Click on the *Update meter* button and the observed values for the voltages and currents on the GUI settle immediately to the desired voltages and currents.

3.2.7 Active Power Gain Calibration

Note

This section is an example for one phase. Repeat these steps for the other two phases.

After performing gain correction for voltage and current, complete *gain correction* for active power. Gain correction for active power is done differently in comparison to voltage and current. Although, conceptually, calculating the active energy % error as is done with voltage and power can be done, avoid using this method because the method is not the most accurate.

The best option to get the *Correction (%)* is directly from the reference meters measurement error of the active power. This error is obtained by feeding energy pulses to the reference meter. To perform active power calibration, complete the following steps:

1. Turn off the system and connect the energy pulse output of the system to the reference meter. Configure the reference meter to measure the active power error based on these pulse inputs.
2. Turn on the AC test source.
3. Repeat step 1 to step 3 from Voltage and Current Gain Calibration with the identical voltages, currents, and 0° phase shift that were used in the same section.
4. Obtain the % error in measurement from the reference meter. A negative value is possible here.
5. Enter the error obtained in step 4 into the *Active Power* field under the corresponding phase in the GUI window. This error is already the value and does not require calculation.

6. Click the *Update meter* button and the error values on the reference meter immediately settle to a value close to zero.

3.2.8 Offset Calibration

After performing gain calibration, if the accuracy at low currents is not acceptable, perform offset calibration. Offset calibration removes any crosstalk, such as the crosstalk to the current channels of a phase from the line voltages.

To perform active power offset calibration for a phase, simply add the offset to be subtracted from the active power reading (in units of mW) to the current value of the active power offset (labeled "Voltage AC off" in Figure 3-15) and then enter this new value in the *Voltage AC offset* field in the Manual Calibration window. As an example, if the *Voltage AC off* has a value of 200 (0.2W) in Figure 3-15, and it is desired to subtract an additional 0.300mW, then enter a value of 500 in the *Voltage AC offset* field in the Manual Calibration window. After entering the value in the *Voltage AC offset* field in the Manual Calibration window, press the *Update meter* button.

To perform reactive power offset calibration for a phase, a similar process is followed as the process used to perform active power offset calibration. Add the offset to be subtracted from the reactive power reading (in units of mvar) to the current value of the reactive power offset (labeled "Current AC offset" in Figure 3-15) and then enter the value in the *Current AC offset* field in the Manual Calibration window. After entering the value in the *Current AC offset* field in the Manual Calibration window, press the *Update meter* button.

3.2.9 Phase Calibration

After performing power gain correction, perform the phase calibration. Similar to active power gain calibration, to perform phase correction on one phase, the other two phases must be disabled. To perform phase correction calibration, complete the following steps:

1. If the AC test source has been turned OFF or reconfigured, perform step 1 to step 3 from Voltage and Current Gain Calibration using the identical voltages and currents used in that section.
2. Disable all other phases that are not currently being calibrated by setting the current of these phases to 0A.
3. Modify only the phase-shift to a non-zero value; typically, +60° is chosen. The reference meter now displays a different % error for active power measurement. This value can be negative.
4. If the error from step 3 is not close to zero, or is unacceptable, perform phase correction by following these steps:
    a. Enter a value as an update for the *Phase Correction* field for the phase that is being calibrated. Usually, a small ± integer must be entered to bring the error closer to zero. Additionally, for a phase shift greater than 0 (for example: +60°), a positive (negative) error requires a positive (negative) number as correction.
    b. Click on the *Update meter* button and monitor the error values on the reference meter.
    c. If this measurement error (%) is not accurate enough, fine-tune by incrementing or decrementing by a value of 1 based on Step 4a and Step 4b. Note that after a certain point, the fine-tuning only results in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.
    d. Change the phase to −60° now, and check if this error is still acceptable. Ideally, errors must be symmetric for same phase shift on lag and lead conditions.

After performing phase calibration, calibration is complete for one phase. Gain calibration, offset calibration, and phase calibration must be performed for the other phases.

This completes calibration of voltage, current, and power for both phases. View the new calibration factors (see Figure 3-15) by clicking the *Meter calibration factors* button of the GUI metering results window in Figure 3-12. For these displayed calibration factors, note that the *Voltage AC off* parameter actually represents the active power offset (in units of mW) subtracted from each measurement and the *Current AC offset* parameter actually represents the reactive power offset subtracted (in units of mvar) from reactive power readings. Also, this shows example calibration factors for a meter that uses the two-voltage configuration. If the same meter is set for one-voltage configuration, the voltage and active power scaling factors are approximately half of what it is in Figure 3-12, since the line-to-line voltage measurement is used for the voltage readings of both phases instead of measuring the two line-to-neutral voltages. Under the best conditions for a split-phase system, the line-to-line

voltage measurement has an RMS value that is twice each of the two line-to-neutral RMS measurements, which means that the voltage fed to the ADC is also twice as much when measuring line-to-line voltage compared to when measuring line-to-neutral voltage. As a result, for one-voltage configurations, the voltage and power readings have to be divided by an additional factor of two, which is automatically done by following the active power and voltage gain calibration steps.

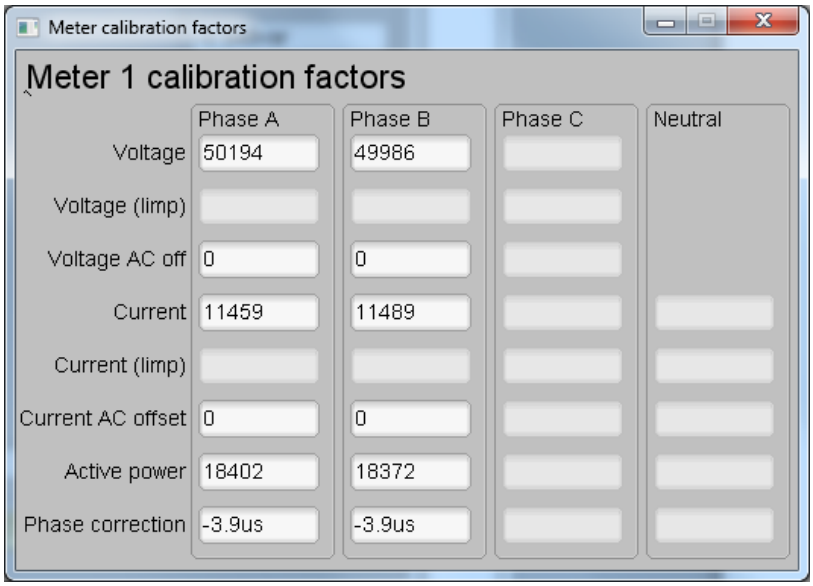


Figure 3-15. Calibration Factors Window

View the configuration of the system by clicking on the *Meter features* button (illustrated in Figure 3-12) to get to the window that Figure 3-16 shows.

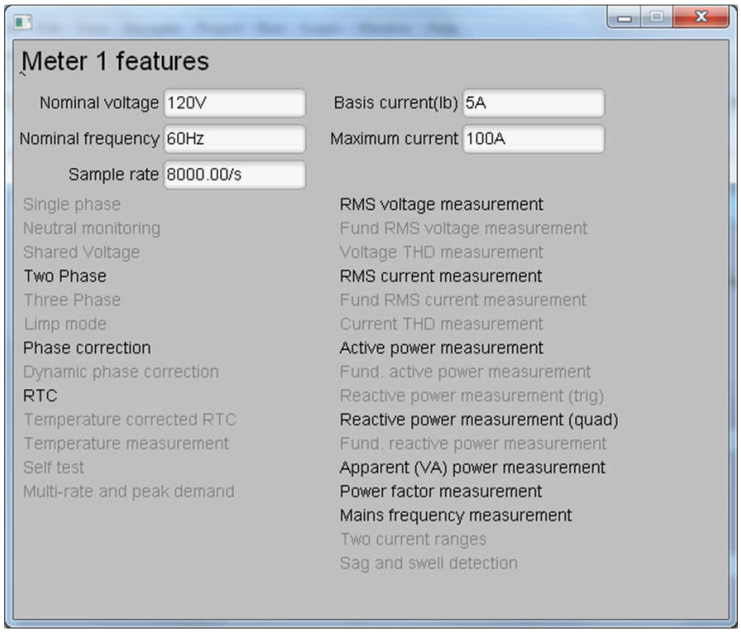


Figure 3-16. Meter Features Window

3.3 Test Results

To test for metrology accuracy, a source generator is used to provide the voltage (J2) and current (J14 and J1) to the system. Additionally, a nominal voltage of 120V, calibration current of 10A with phase calibration at 60° and nominal frequency of 60Hz are used. During all of the tests, the board is powered directly using the 3V3 power supply from bench.

When the voltage and current are applied to the system, the system outputs the active energy pulses and reactive energy pulses at a rate of 6400 pulses/kWh. The pulse output is fed into a reference meter (in the test equipment for this reference design, this pulse output is integrated in the same equipment used for the source generator) that determines the energy % error based on the actual energy provided to the system and the measured energy as determined by the active and reactive energy output pulse of the system. In this reference design, active energy error testing and reactive energy error testing are performed after running energy gain calibration, phase calibration, and energy offset calibration.

All active and reactive energy testing is performed using two 200µΩ shunts and the current is varied from 100mA to 100A while voltage is held at 120V.

3.3.1 Energy Metrology Accuracy Results

For the following test results, gain, phase, and offset calibration are applied to the meter. At higher currents, the % error shown is dominated by shunt resistance drift caused by the increased heat generated at high currents.

For cumulative active energy error, cumulative reactive energy error testing, and individual phase active energy testing, current is varied from 100mA to 100A. For cumulative active energy and individual phase error testing, a phase shift of 0° (PF = 1), PF = 0.5i (inductive) and PF = 0.8c (capacitive) is applied between the voltage and current waveforms fed to the reference design. Based on the error from the active energy output pulse, a plot of active energy % error versus current is created for the three PF values.

For cumulative reactive energy error testing, a similar process is followed except that a phase shift of 90° (sin ϕ = 1i), sin ϕ = 0.5i (inductive) and sin ϕ = 0.8c (capacitive) are used, and cumulative reactive energy error is plotted instead of cumulative active energy error.

In both cumulative active and reactive energy testing, the sum of the energy reading of each phase is tested for accuracy. In contrast, the individual phase energy readings (Phase A and Phase B, if split-phase mode is used) are tested for the individual phase active energy testing. When testing the individual energy accuracy of a phase, the other phase is disabled by providing 0A input for the current of this other phase so that the cumulative active energy reading is ideally equal to the individual phase voltage, which allows the cumulative energy pulse output to be used for testing individual phase accuracy. All these tests were run using the 4kSPS sample rate setting of the ADS131M02 and AMC131M03 devices.

For the V_{RMS} accuracy test on both Phase A and B, the voltage was varied from 10V to 270V while current was held steady at 10A. Testing beyond 270V can also be done; however, this requires the 275V varistors to be removed from the design and replaced with varistors that are rated for a higher voltage.

For the I_{RMS} accuracy test on both Phase A and B, the voltage was kept steady at 120V, while current was varied from 0.1A to 100A.

The following 4 plots for Active and Reactive Power for Star and Delta Configurations are per IEC 62053-22 limits for class 0.2 S accuracy, assuming $I_{nominal}$ = 15A, hence the 5% point of $I_{nominal}$ is at 750mA.

The average error for each measurement is calculated from five test series, taken sequentially for each current value, and the maximum deviation from these five measurements is calculated (not shown in the plots below) to confirm the stability of this metrology subsystem being below 10% of the maximum error allowed.

Table 3-1. ACTive Energy % Error Versus Current, 200µΩ Shunts, Star (Wye) Configuration

CURRENT (A)	AVG ERROR % PF = 1, cos ϕ = 0°	LIMIT (%) [CLASS 0.2] IEC 62053-22 (PF 0.5i/0.8c)	LIMIT (%) [CLASS 0.5] IEC 62053-22 (PF 0.5i/0.8c)	AVG ERROR % PF = 0.5i, cos ϕ = 60°	LIMIT (%) [CLASS 0.2] IEC 62053-22 (PF 0.5i/0.8c)	LIMIT (%) [CLASS 0.5] IEC 62053-22 (PF 0.5i/0.8c)	AVG ERROR % PF = 0.8c, cos ϕ = –36.87°
0.1	0.198	0.4	1.0	0.143	0.5	1.0	0.125
0.5	0.0574	0.4	1.0	–0.014	0.5	1.0	–0.0356
0.75	0.0416	0.4	1.0	–0.053	0.5	1.0	0.0344
1.5	0.038	0.2	0.5	–0.085	0.3	0.6	0.0678
3	0.0042	0.2	0.5	–0.081	0.3	0.6	0.085
7.5	0.0098	0.2	0.5	–0.105	0.3	0.6	0.1116
15	0.0174	0.2	0.5	–0.061	0.3	0.6	0.1406
30	0.017	0.2	0.5	–0.078	0.3	0.6	0.0476
60	–0.016	0.2	0.5	–0.076	0.3	0.6	0.1118
75	–0.0778	0.2	0.5	–0.151	0.3	0.6	0.0774
100	–0.0144	0.2	0.5	–0.2	0.3	0.6	–0.0968

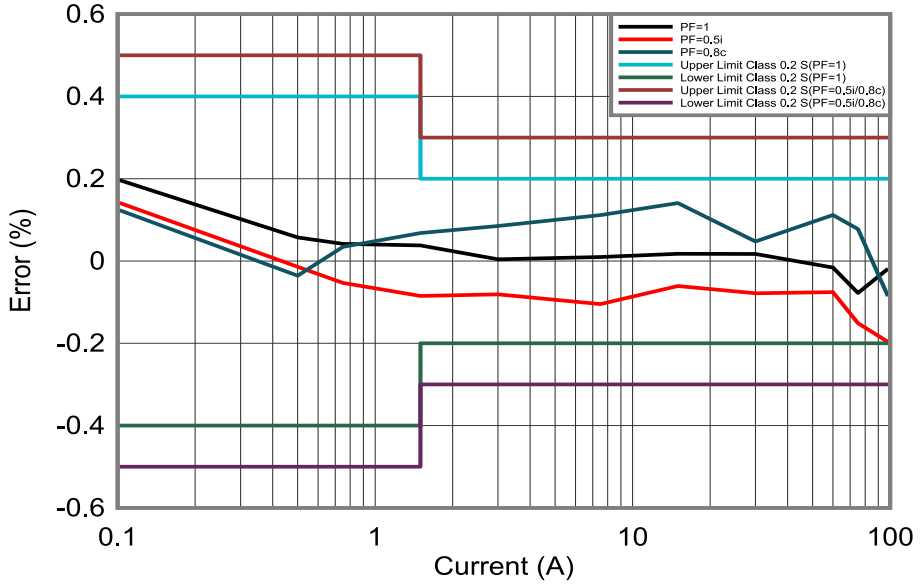


Figure 3-17. ACTive Energy % Error Versus Current, 200µΩ Shunts, Star (Wye) Configuration

Table 3-2. REACTive Energy % Error Versus Current, 200µΩ Shunts, Star (Wye) Configuration

CURRENT (A)	AVG ERROR % sin ϕ = 1i (90°)	AVG ERROR % sin ϕ = 0.5i (30°)	AVG ERROR % sin ϕ = 0.8c (–53.13°)
0.1	0.1	0.25	0.07
0.5	0.05	0.26	0.08
0.75	–0.09	0.32	0.09
1.5	0.06	0.28	0.08
3	0.04	0.28	0.11
7.5	0.04	0.29	0.09
15	0.07	0.28	0.1
30	0.07	0.27	0.09
60	0.02	0.27	0.08
75	–0.06	0.21	0.02
100	–0.38	–0.15	–0.12

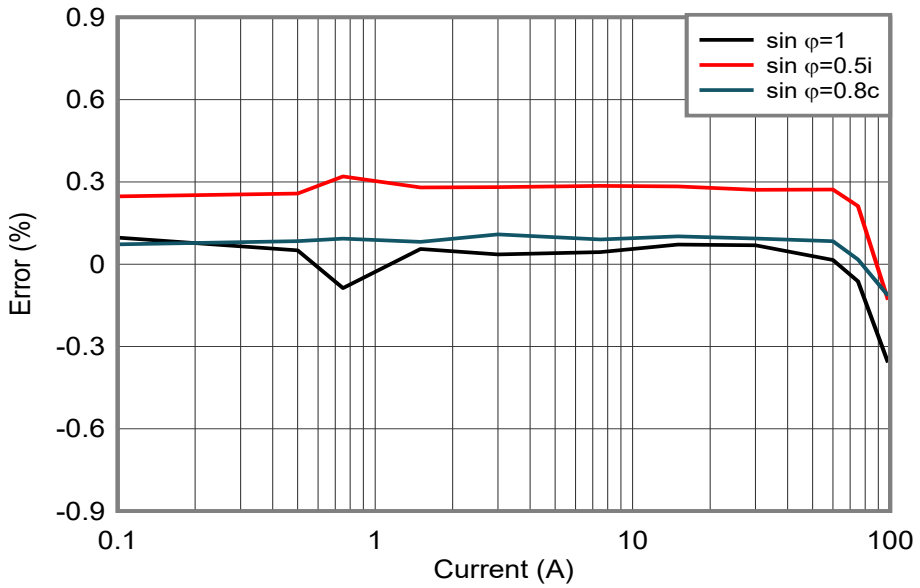


Figure 3-18. REACTive Energy % Error Versus Current, 200µΩ Shunts, Star (Wye) Configuration

Table 3-3. ACTive Energy % Error Versus Current, 200µΩ Shunts, Delta Configuration

CURRENT (A)	AVG ERROR % PF = 1, cos ϕ = 0°	LIMIT (%) [CLASS 0.2] IEC 62053-22 (PF 0.5i/0.8c)	LIMIT (%) [CLASS 0.5] IEC 62053-22 (PF 0.5i/0.8c)	AVG ERROR % PF = 0.5i, cos ϕ = 60°	LIMIT (%) [CLASS 0.2] IEC 62053-22 (PF 0.5i/0.8c)	LIMIT (%) [CLASS 0.5] IEC 62053-22 (PF 0.5i/0.8c)	AVG ERROR % PF = 0.8c, cos ϕ = –36.87°
0.1	0.240	0.4	1.0	0.381	0.5	1.0	0.307
0.5	0.073	0.4	1.0	0.059	0.5	1.0	0.1
0.75	0.091	0.4	1.0	0.042	0.5	1.0	0.122
1.5	0.09	0.2	0.5	0.016	0.3	0.6	0.064
3	0.082	0.2	0.5	0.025	0.3	0.6	0.098
7.5	0.074	0.2	0.5	0.001	0.3	0.6	0.055
15	0.049	0.2	0.5	0.017	0.3	0.6	0.086
30	0.106	0.2	0.5	0.032	0.3	0.6	0.127
60	0.083	0.2	0.5	0.031	0.3	0.6	0.145
75	0.089	0.2	0.5	–0	0.3	0.6	0.081
100	0.037	0.2	0.5	–0.04	0.3	0.6	0.011

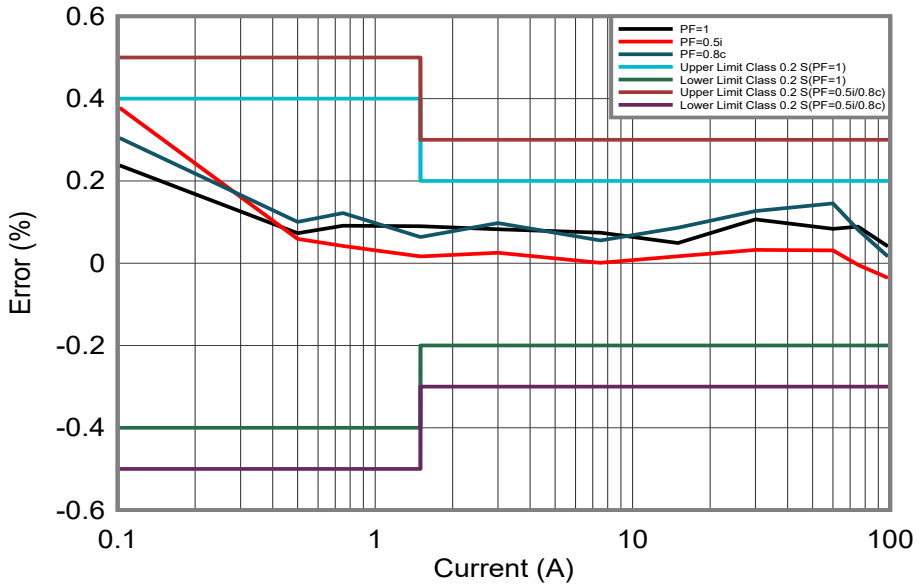


Figure 3-19. ACTive Energy % Error Versus Current, 200µΩ Shunts, Delta Configuration

Table 3-4. REACTive Energy % Error Versus Current, 200µΩ Shunts, Delta Configuration

CURRENT (A)	AVG ERROR % sin ϕ = 1i (90°)	AVG ERROR % sin ϕ = 0.5i (30°)	AVG ERROR % sin ϕ = 0.8c (–53.13°)
0.1	–1.93	–3.3	5.14
0.5	0.54	–1.34	1.11
0.75	–0.19	–0.8	0.75
1.5	–0.06	–0.35	0.39
3	0.02	–0.1	0.22
7.5	0.06	0.08	0.1
15	0.08	0.13	0.07
30	0.08	0.11	0.06
60	0.07	–0.01	0.01
75	0.01	–0.17	–0.02
100	–0.15	–0	–0.12

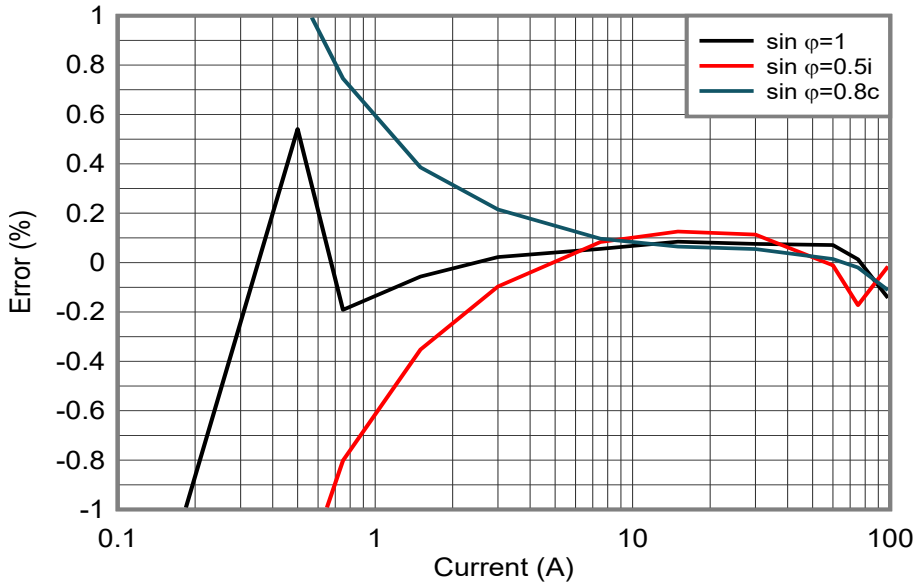


Figure 3-20. REACTive Energy % Error Versus Current, 200µΩ Shunts, Delta Configuration

Figure 3-21 through Figure 3-24 show the I_{RMS} and V_{RMS} per each phase, where the % error column is generated by comparing the respective MTE Reading and the GUI reading. For these plots single measurements were recorded.

Table 3-5. V_{RMS} % Error at 10A, 200µΩ Shunts, Phase A

VOLTAGE (V)	% ERROR
10	–0.013
30	–0.01
50	0.003
70	–0.017
90	–0.025
100	–0.005
120	–0.013
140	–0.040
160	–0.015
180	–0.028
200	–0.022
220	–0.022
230	–0.027
240	–0.029
260	–0.019
270	–0.022

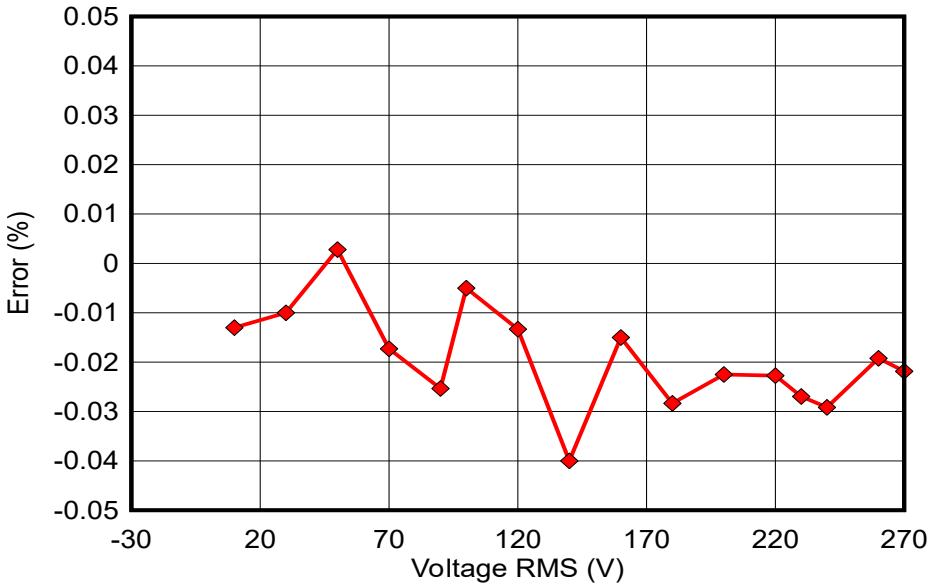


Figure 3-21. V_{RMS} % Error at 10A, 200µΩ Shunts, Phase A

Table 3-6. I_{RMS} % Error at 120V, 200µΩ Shunts, Phase A

CURRENT (A)	% ERROR
0.01	–36.318
0.025	–14.410
0.05	–3.246
0.1	–0.751
0.25	–0.107
0.5	–0.030
1	–0.053
2	–0.049
5	–0.038
10	–0.039
20	–0.056
30	–0.041
40	–0.028
50	–0.003
60	–0.011
70	–0.015
80	0.020
90	0.029
100	0.071

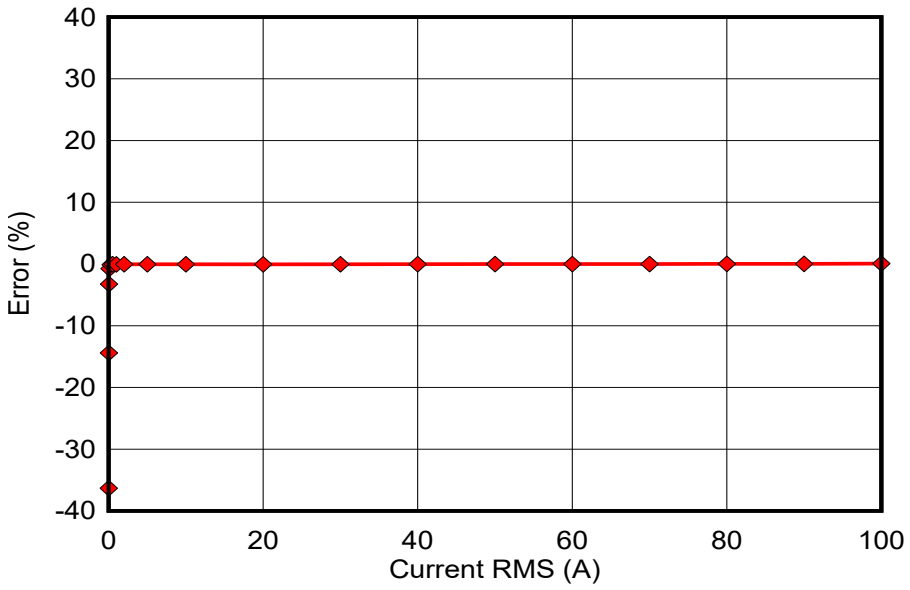


Figure 3-22. I_{RMS} % Error at 120V, 200µΩ Shunts, Phase A

Table 3-7. V_{RMS} % Error at 10A, 200µΩ Shunts, Phase B

VOLTAGE (V)	% ERROR
9	0.253
10	0.070
30	–0.034
50	–0.012
70	–0.026
90	–0.016
100	0.009
120	–0.013
140	–0.036
160	–0.024
180	–0.036
200	–0.033
220	–0.035
230	–0.036
240	–0.045
260	–0.049
270	–0.025

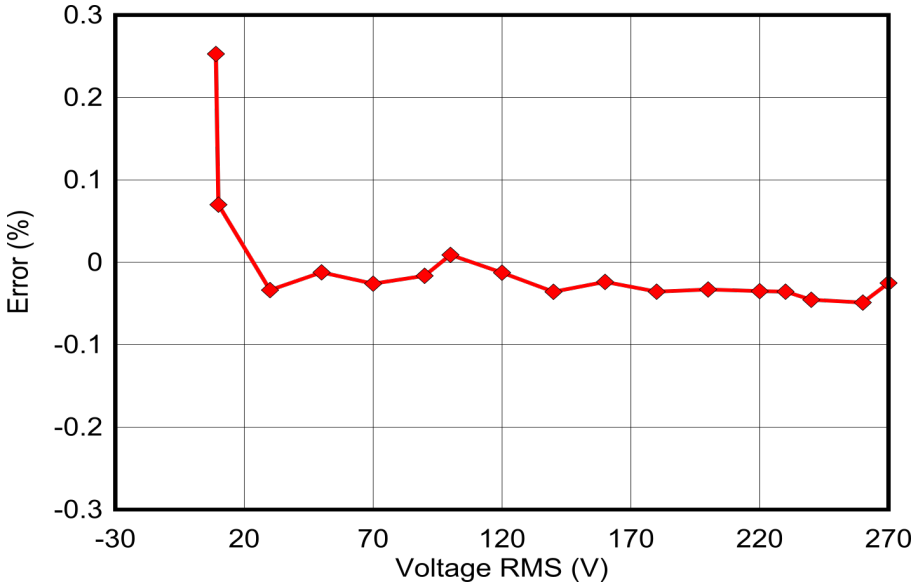


Figure 3-23. V_{RMS} % Error at 10A, 200µΩ Shunts, Phase B

Table 3-8. I_{RMS} % Error at 120V, 200µΩ Shunts, Phase B

CURRENT (A)	% ERROR
0.01	–32.557
0.025	–13.645
0.05	–5.802
0.1	–0.323
0.25	–0.199
0.5	–0.117
1	–0.057
2	–0.051
5	–0.028
10	–0.046
20	–0.034
30	–0.037
40	–0.035
50	–0.034
60	–0.013
70	0.018
80	0.035
90	0.106
100	0.189

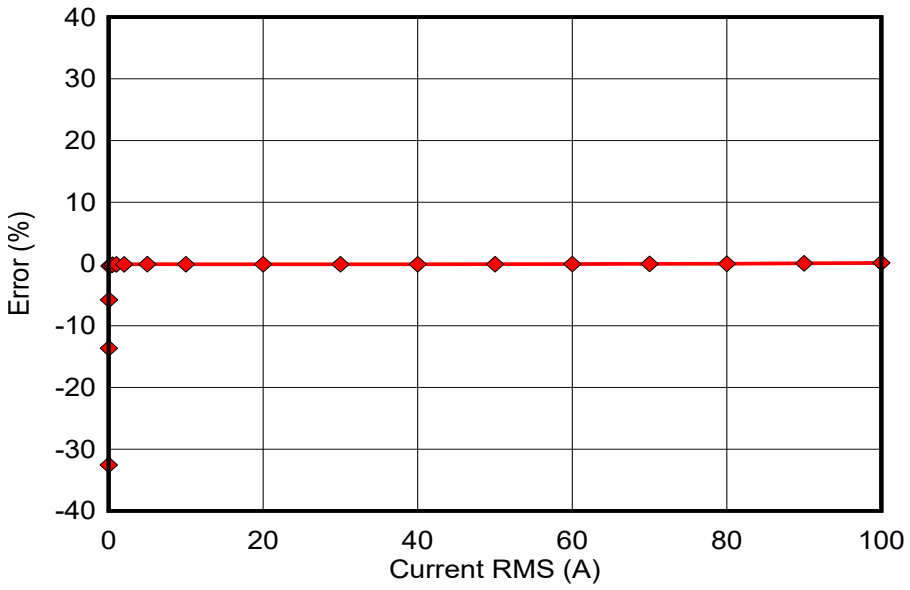


Figure 3-24. I_{RMS} % Error at 120V, 200µΩ Shunts, Phase B

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010944.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010944.

4.1.3 PCB Layout Recommendations

For this design, follow these general guidelines:

- Place decoupling capacitors close to the associated pins.
- Use ground planes instead of ground traces and minimize the cuts in the ground plane, especially near the ADS131M02 and AMC131M03. In this design, there is a ground plane on both the top and bottom layer for the HGND (high voltage side) for both Phase A and Phase B. Make sure that there is good stitching between the planes through the liberal use of vias.
- Keep the two traces to the inputs of each ADC channel symmetrical and as close as possible to each other.
- Crosstalk from the voltage to current channels can reduce accuracy at lower currents if power offset is not performed.
- For the ADS131M02 and AMC131M03 devices, place the 0.1µF capacitor closer to the AVDD pin than the 1µF capacitor. Do the same thing for the 0.1µF and 1µF capacitors connected to DVDD.
- Minimize the length of the traces used to connect the crystal to the microcontroller. Place guard rings around the leads of the crystal and ground the crystal housing. In addition, there must be clean ground underneath the crystal and avoid placing any traces underneath the crystal. Also, keep high-frequency signals away from the crystal.
- Use wide traces for power-supply connections.
- Use a different ground plane for the isolated RS-232. This other ground plane is at the potential of the RS-232 ground and not the GND used elsewhere in the board.
- Make sure that the recommended clearance and creepage spacing are met for the ISO6731 isolation device.

4.1.4 Layout Prints

To download the layer plots, see the design files at TIDA-010944.

4.1.5 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010944.

4.1.6 Gerber Files

To download the Gerber files, see the design files at TIDA-010944.

4.1.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010944.

4.2 Tools and Software

Tools

CCSTUDIO	Code Composer Studio™ integrated development environment (IDE)
SYSCONFIG	System configuration tool with an intuitive graphical user interface for configuring pins, peripherals, radios, software stacks, RTOS, clock tree, and other components.

Software

TIDA-010944 Firmware	Source code of Energy Library for TIDA-010944 in latest MSPM0 SDK with default install path: `C:\ti\mspm0_sdk_2_01_00_03\examples\nortos\LP_MSPM0G3507\energy_metrology\split-phase\TIDA_010944_SW`

4.3 Documentation Support

1. Texas Instruments, *AMC131M03 3-Channel, 64-kSPS Simultaneous-Sampling 24-Bit Isolated Delta-Sigma ADC With Integrated DC/DC Converter Data Sheet*
2. Texas Instruments, *ADS131M02 2-Channel, Simultaneously-Sampling, 24-Bit, Delta-Sigma ADC Data Sheet*
3. Texas Instruments, *MSPM0G110x Mixed-Signal Microcontrollers Data Sheet*
4. Texas Instruments, *ISO6731 General-Purpose Triple-Channel Digital Isolator with Robust EMC Data Sheet*
5. Smart Energy International, *Implementing magnetic tamper detection in electricity meters* .

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.5 Trademarks

5 About the Authors

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