Design Guide: TIDA-010260

4T5R Space-Grade Integrated Transceiver Reference Design

Description

This reference design is a 4T5R transceiver designed for space applications and the board is compliant to the VITA-57 form factor. The design is centered around the AFE7950-SP RF sampling transceiver. The design Optimized for X-band and S-band applications. A JESD204B compliant clocking design and a power supply design are also included.

Resources

TIDA-010260	Design Folder
AFE7950-SP	Product Folder
LMK04832-SEP	Product Folder
LMX2694-SEP	Product Folder
TRF0208-SEP	Product Folder
TRF0208-SP	Product Folder
TPS7H4010-SEP	Product Folder
TPS7H4003-SEP	Product Folder
TPS73801-SEP	Product Folder

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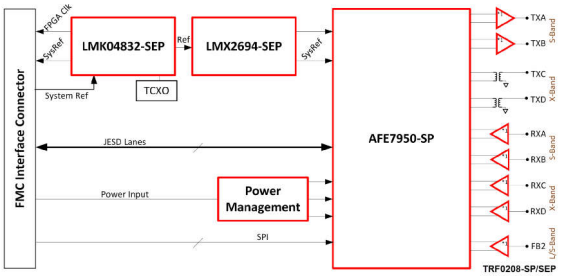
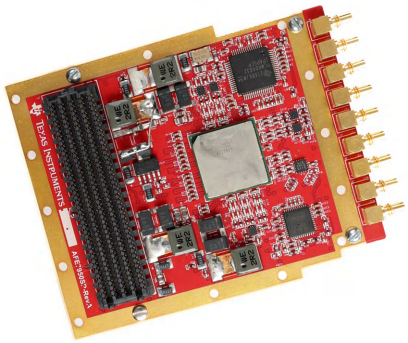
Features

- Independent NCO for each band
- Option for internal or external clocking
- Efficient on-board power supply design
- Space-grade passive component compatible
- External or localized low frequency reference
- VITA-57 compliant form factor

Applications

- Communications payload
- Radar imaging payload
- Command and data handling (C&DH)





1 System Description

Satellite payload applications related to communications and radar need multi-channel, high frequency transceivers. In these systems, there is a need to address different functions related to the communication channel across different bands, telemetry, and GPS. Although these functions can be independently created, integrating all functions into one design saves physical space and reduces complexity. The design requires radiation hardened active devices and space-grade passives to support operation in Low Earth Orbit (LEO) satellite applications.

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the block diagram of the reference design.

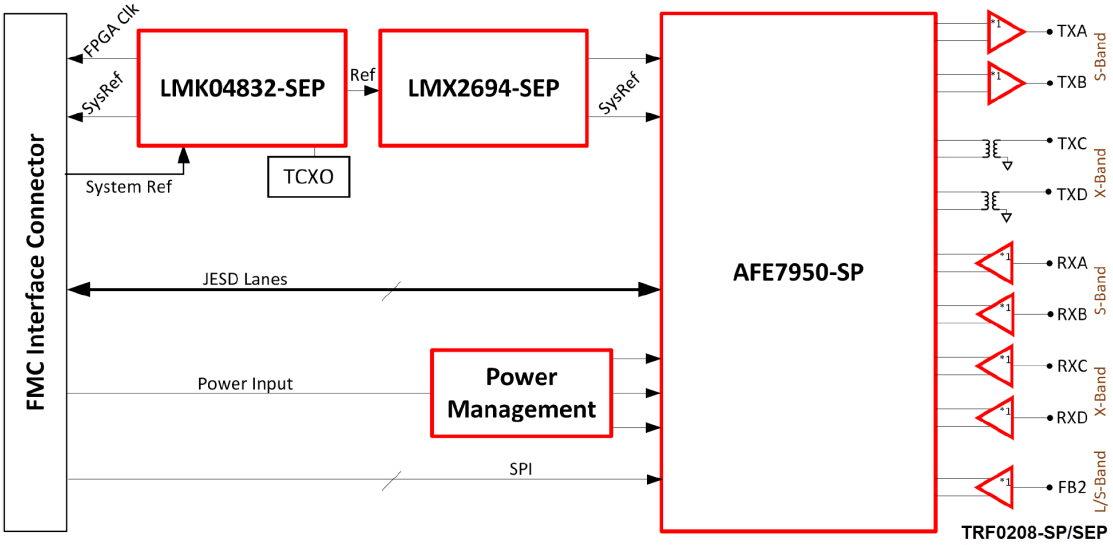


Figure 2-1. TIDA-010260 Block Diagram

Figure 2-2 shows the block diagram of the power supply design.

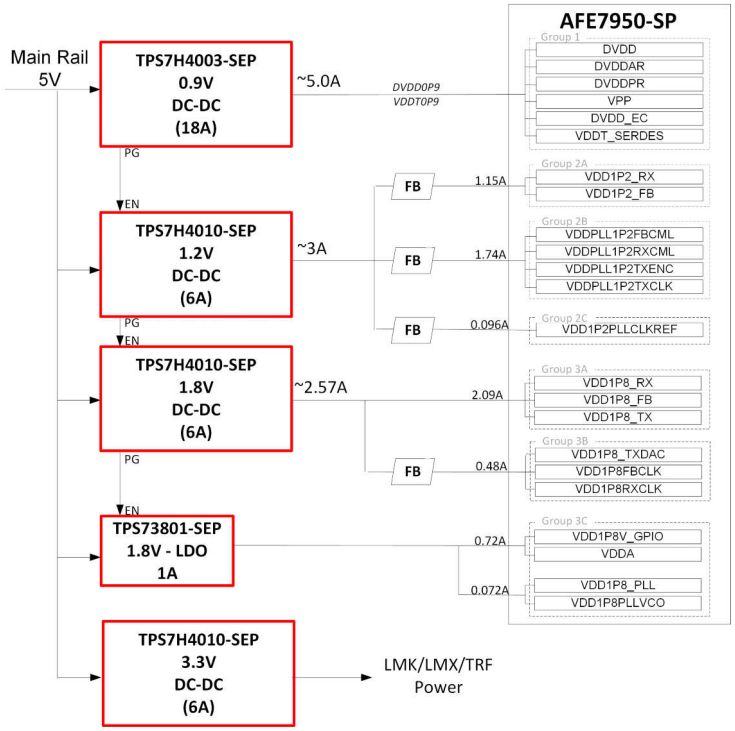


Figure 2-2. Reference Design Power Supply Design

2.2 Design Considerations

The design is centered on the AFE7950-SP integrated RF sampling transceiver. The LMK04832-SEP provides a low frequency reference to the LMX2694-SEP. The LMK04832-SEP also provides the low frequency clock signals for the FPGA and the SysRef signals to the AFE and FPGA to support the JESD204B digital interface protocol. The LMX2694-SEP provides the low phase noise, high frequency sampling clock to the AFE. All of the receive channels utilize active baluns to convert single-ended inputs to differential outputs to interface with the ADC input. The lower frequency transmit channels also use active baluns to convert differential DAC output to single-ended. The high frequency transmit channels use a passive balun to convert differential to single-ended. Due to the small physical space allocation, the power supply is streamlined using DC-DC converters for most of the rails to minimize part count and maintain best efficiency.

2.3 Highlighted Products

2.3.1 AFE7950-SP

The AFE7950-SP is a radiation tolerant integrated RF sampling transceiver supporting up to 4 transmit and 6 receive channels. The AFE7950-SP incorporates an internal PLL/VCO to generate a local high frequency sampling clock. Alternatively, the device accepts an external sampling clock if an improved phase noise source is needed. Each channel incorporates Numerically Controlled Oscillators (NCOs) to independently program the signal to any arbitrary RF frequency band. Each channel also includes a Digital Step Attenuator (DSA). The device supports instantaneous signal bandwidth up to 1200MHz. There are many configuration options to adjust data rates, serdes speeds, and frequency bands to optimize for any given application.

2.3.2 LMK04832-SEP

The LMK04832-SEP is a radiation tolerant, high performance clock conditioner with JESD204B/C support. The LNK04832-SEP has 14 clock outputs configurable as clock or SysRef outputs and has two PLLs (Phased Locked Loops). The first PLL operates as a jitter cleaner to lock a localized low jitter reference source, like a VCXO, to a low frequency system reference. The second PLL locks the internal VCO (Voltage Controlled Oscillator) to the low jitter reference. The device supports dual PLL, single PLL, or clock distribution modes.

2.3.3 LMX2694-SEP

The LMX2694-SEP device is a radiation tolerant, low phase noise, wideband phase-locked loop (PLL) with an integrated voltage-controlled oscillator (VCO) supporting a frequency between 39.3MHz and 15.1GHz. The device has two outputs with independent output divider control.

2.3.4 TRF0208-SEP

The TRF0208-SEP is a radiation-tolerant, fully differential RF amplifier (FDA) that operates from near-DC to 11GHz. This RF FDA amplifier can function as a single-ended to differential RF amplifier (S2D) or a differential to single-ended RF amplifier (D2S). The TRF0208-SEP requires a single 3.3V supply, drawing 138mA (455mW).

2.3.5 TPS7H4010-SEP

The TPS7H4010-SEP is a radiation tolerant synchronous step-down DC/DC converter capable of driving up to 6A of load current from a supply voltage ranging from 3.5V to 32V. The device provides exceptional efficiency and output accuracy in a very small design size.

2.3.6 TPS73801-SEP

The TPS73801-SEP is a radiation tolerant low-dropout (LDO) regulator optimized for fast transient response. The device can output up to 1A of current with a dropout voltage of 300mV. The device output supply noise is very low which makes the device an excellent choice for sensitive RF supply applications.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

Evaluation of the reference design with TI tools requires the following hardware.

- TIDA-010260 Reference Design Board
- FMC interface board
- TSW14J56EVM
- External fans for cooling
- USB2ANY programming pod
- High quality 491.52MHz Wenzel Oscillator or equivalent
- Bandpass filter for desired receiver frequencies of interest
- SSMC to SMA Adapters: Radial 5945-9503-000 (or equivalent)

Testing the reference design requires the following test equipment.

- Agilent PSA E4445A Spectrum Analyzer or equivalent
- Rohde and Schwarz SMA100B Signal Generator or equivalent
- TSW14J56 Power Supply (5V, 3.5A)
- TIDA-010260 Reference Design Power Supply (5V, 5.0A)
- High Speed Oscilloscope (optional)

3.2 Software Requirements

Evaluation of the reference design requires released versions of the software available through ti.com.

- HSDC Pro GUI
- TICS Pro GUI
- AFE7950 Latte:
  - Access latest EVM GUI software from MySecure Folder per requested link
  - Reference AFE7950EVM User's Guide for additional information

3.3 Test Setup

Figure 3-1 shows a block diagram of the test setup. Figure 3-2 shows a picture of the setup.

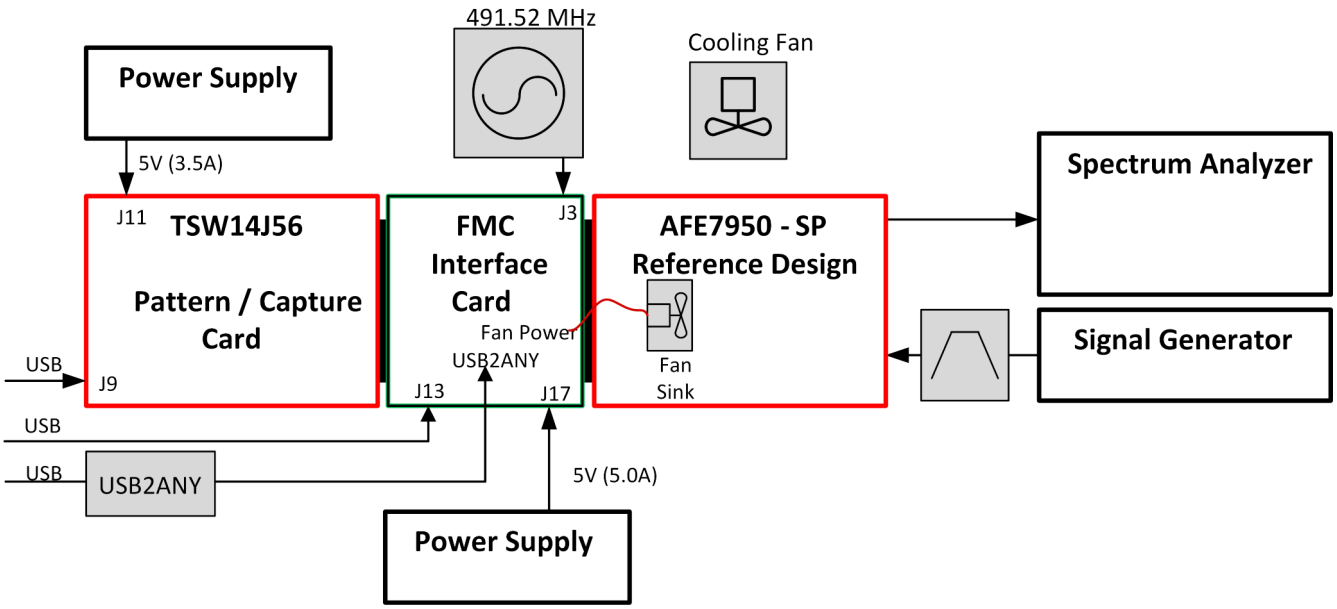


Figure 3-1. Test Setup Block Diagram

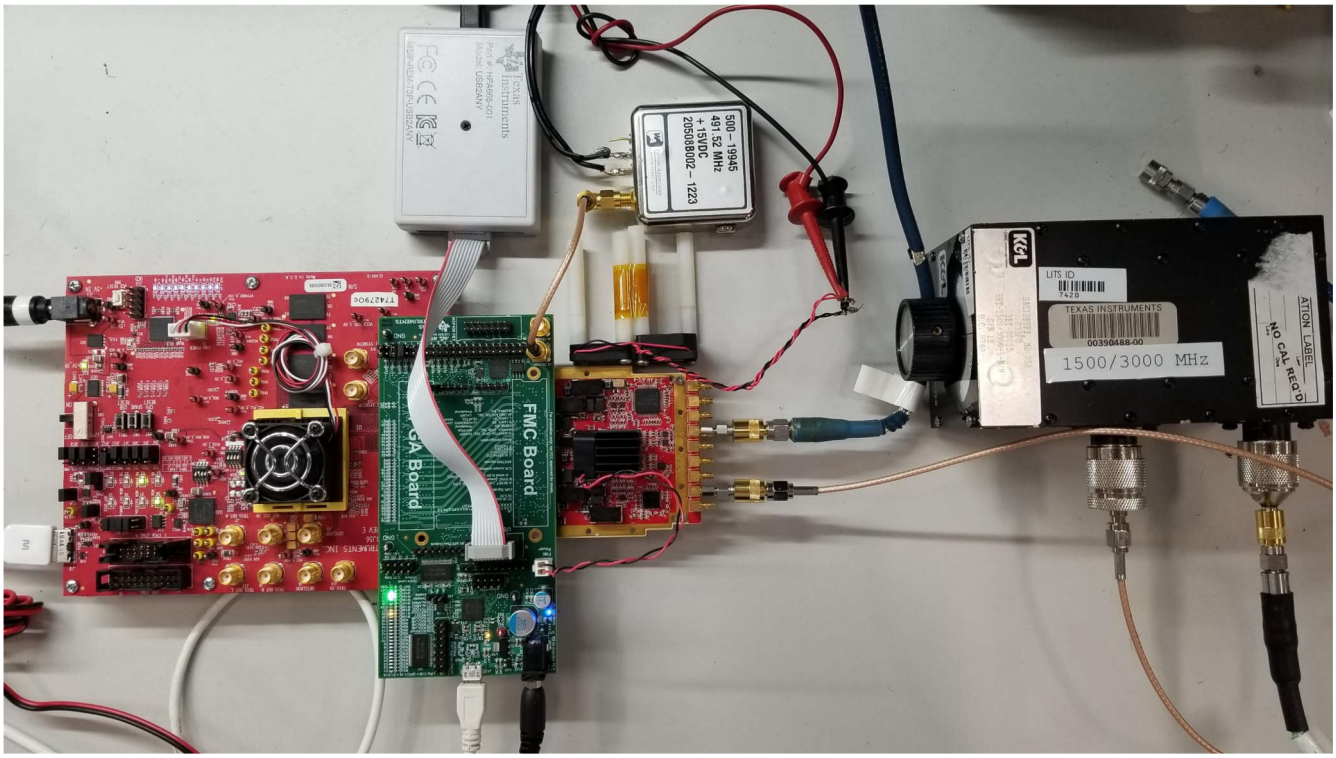


Figure 3-2. Test Setup

3.4 Hardware Configuration

Follow this procedure to setup the boards and equipment.

- Connect TSW14J56
  - Plug in 5V power cable to TSW14J56
  - Set voltage to 5.0V (or up to 5.5V)
  - Make sure current limit is set for 3.5A or higher
  - Connect PC to EVM through USB connection
  - Make sure power switch on the board is on
- Plug in FMC Interface Board to TSW14J56
  - Plug in external 491.52MHz Wenzel Oscillator (or equivalent) to J3 CLKINP SMA connector
  - Plug in cable from USB2ANY to connector labelled “USB2ANY”
  - Plug in 5V power cable; set voltage to 5.2V (make sure current limit is 5A or greater)
  - Plug PC to FMC Interface Board through USB connector
  - Verify jumpers placed at J6 location K, L, N
  - Jumper J6 location M selects programming to LMK or LMX device. Initially, verify that jumper is not placed.
- Plug in TIDA-010260 Reference Design to the FMC Interface Board.
  - Connect fan power to *Fan Power* connector on the interface board
  - Make sure additional cooling fans are on and blowing over the AFE7950-SP board
  - Connect TXA output to Spectrum Analyzer
  - Connect Signal Generator through BPF to RXA input
- Spectrum Analyzer Setup
  - Set center frequency to: 2210MHz
  - Set frequency span to: 5MHz
  - Ref Level: 8.8dBm
  - RBW: 3kHz
  - VBW: 3kHz
  - Attn: 28dB

3.5 Test Procedure

3.5.1 Initial TSW14J56 Setup

Initial setup for the TSW14J56. Once completed, no further setup on the ‘J56 Is needed as long as there is no power or data glitch.

- Launch HSDC Pro
- Select available board; click OK
- Stay on ADC tab
  - Load *AFE79xx_2x2RX_24410* ini file
  - Select Data Capture Options > Capture Options; change # of samples to 16384
  - Select Test Options > Notch Frequency Bins: change notch for the fundamental to 100
  - Change Analysis Window (samples) to 16384
  - Change ADC Output Data Rate to 245.75M
  - Press OK on the pop-up window for lane rate
- Switch to the DAC Tab
  - Load *AFE79xx_2x2TX_44210* ini file
  - Change Scaling Factor to 0.9
  - Change Data Rate to 491.52M
  - Change Tone BW to 1; change # to 1; change Tone Center to 10M
  - Change Tone Selection from Real to Complex
  - Press Create Tone
  - Press Send

3.5.2 Reference Design Test Procedure

This is the basic test procedure for evaluating the reference design.

- Engage power supply for the AFE7950-SP Reference Design
  - Set power supply voltage to **5.2V** (headroom for voltage loss over cable)
  - Set current limit to **5.0 Amps** (*** Critical: device draw over 4 Amps ***)
  - Turn on 5V power supply
  - Verify initial current is 1.25A +/-0.2 Amps
- Setup LMK04832-SEP Low Frequency Clocks
  - Launch TICS Pro GUI
  - Verify jumper J6 location M on the interface board is *not* placed so the LMK device is programmed.
  - Select: Select Device > Clock Generator/Jitter Cleaner (Dual Loop) > LMK04832-SP
  - Select File > Load > LMK04832-SEP_TICsPro_122p88M_CLKINBypass_LMXRef.tcs
  - Supply Current increases to: 1.47A +/-0.2A
  - Debug/Verification tricks
    - LED D2 on the TSW14J56 starts flashing indicating that TSW14J56 is getting the proper clock
    - Scope Probe on C95 cap on LMK output to confirm 122.88MHz signal
- Set-up LMX2694-SEP High Frequency Clock
  - Place jumper at J6 location M on the interface board to engage LMX programming
  - In TICS Pro, select: Select Device > PLL + VCO > LMX2694
  - Select File > Load > LMX2694-SEP_122p88Ref_122p88PFD_11796p48M.tcs
  - Supply Current increases to: 1.55A +/-0.2A
- Set-up AFE7950-SP through Latte
  - Launch AFE79xx Latte
  - Select Setup.py; Press F5 to launch
    - Executes in about 8 seconds
    - Expect no errors
  - Select devInit.py; Press F5 to launch
    - Executes in about 30 seconds
    - Expect 1 error which can be ignored
    - Only needs to be launched once per new session

  - Select AFE7950-SP_12GClk_ExtClk.py; Press F5 to execute
    - Executes in 30 to 90 seconds
    - Expect no errors
    - Current fluctuates up and down during the bring-up programming
    - Supply current is: 3.95A +/- 0.3A
    - Debug trick:
      - If link is not established well, re-initiate a sync pulse with this Latte command: AFE.adcDacSync()
      - Verify LED D2 on TSW14J56 is still flashing
      - Verify supply current is at the expected level
- Verify TX and RX Operation
  - After bring-up and no Latte errors, verify TX output tone at 2110MHz at around 4dBm.
    - Verify that cable loss at frequency of interest is accounted for
  - Switch HSDC Pro tab to ADC; Press Capture
    - Verify Channel selection is Channel 1 corresponding to RXA
    - Verify a successful FFT capture; verify LED D4 on TSW14J56 is flashing

3.6 Test Results

3.6.1 TXA/B DAC Output Test Results

The config file is setup on channels TXA and TXB with the NCO set to 2.1GHz. The TSW14J56 is setup with a tone at 10MHz offset. Expect the output tone at about 2110MHz. Note, the offset is not exactly 10MHz due to the multi-tone set-up. Figure 3-3 shows the output tone performance.

The spur at 1MHz offset is from the 1.2V, 1.8V, and 3.3V DC-DC switchers. The 1.2V supply couples most prominently to the external clock due to the proximity.

The output power is approximately 4dBm. Note, the config file engages a 10dB attenuator on the AFE7950-SP to maintain that the TRF0208-SEP device is not over-driven.

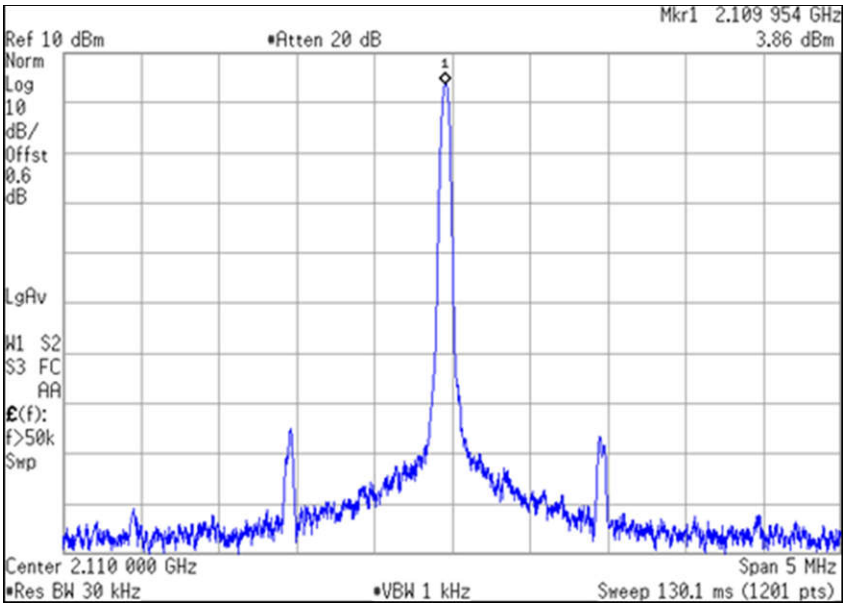


Figure 3-3. TXA/B DAC Output Performance

3.6.2 TXC/D DAC Output Test Results

The config file is setup on channels TXC and TXD with the NCO set to 8.2GHz. The expected output tone is about 8210MHz. These channels do not use the TRF0208-SEP; instead there is a passive balun. Hence, there is no need to engage the digital attenuators. Figure 3-4 shows the output performance.

As before, the 1.0MHz offset spurs are from the DC-DC converters. TXD is well matched for 8.2GHz; however, TXC has the balun on the opposite side of the board and the additional via inductance skewed the match from optimum. As such, this channel has low gain which can be recovered with a layout or match tweak.

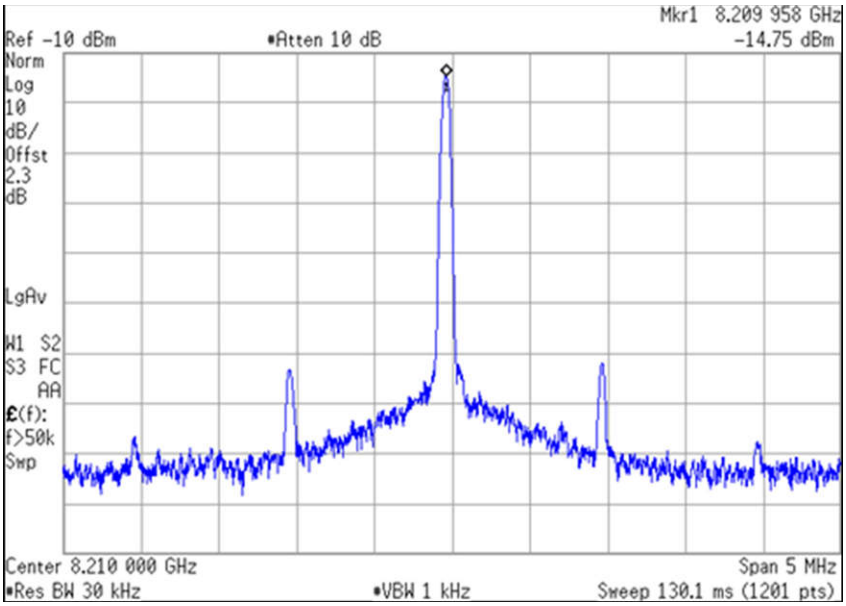


Figure 3-4. TXD DAC Output Performance

3.6.3 RXA/B ADC Test Results

The config file also has RXA and RXB channels configured with the NCO set to 2.1GHz. Inject a tone at 2140MHz. For proper SNR performance, the signal must be filtered. Adjust the amplitude of the fundamental signal to read approximately -3dBFS. This is likely a signal generator power around -10 to -12dBm.

Figure 3-5 shows the FFT spectrum from the single tone capture. SNR performance is around 51dBFS. SFDR performance is around 66dBFS. HD2,HD3 performance is very good at less than 85dBFS. Note, TXA and TXB are disengaged to eliminate any bleed-through component impacting the FFT capture.

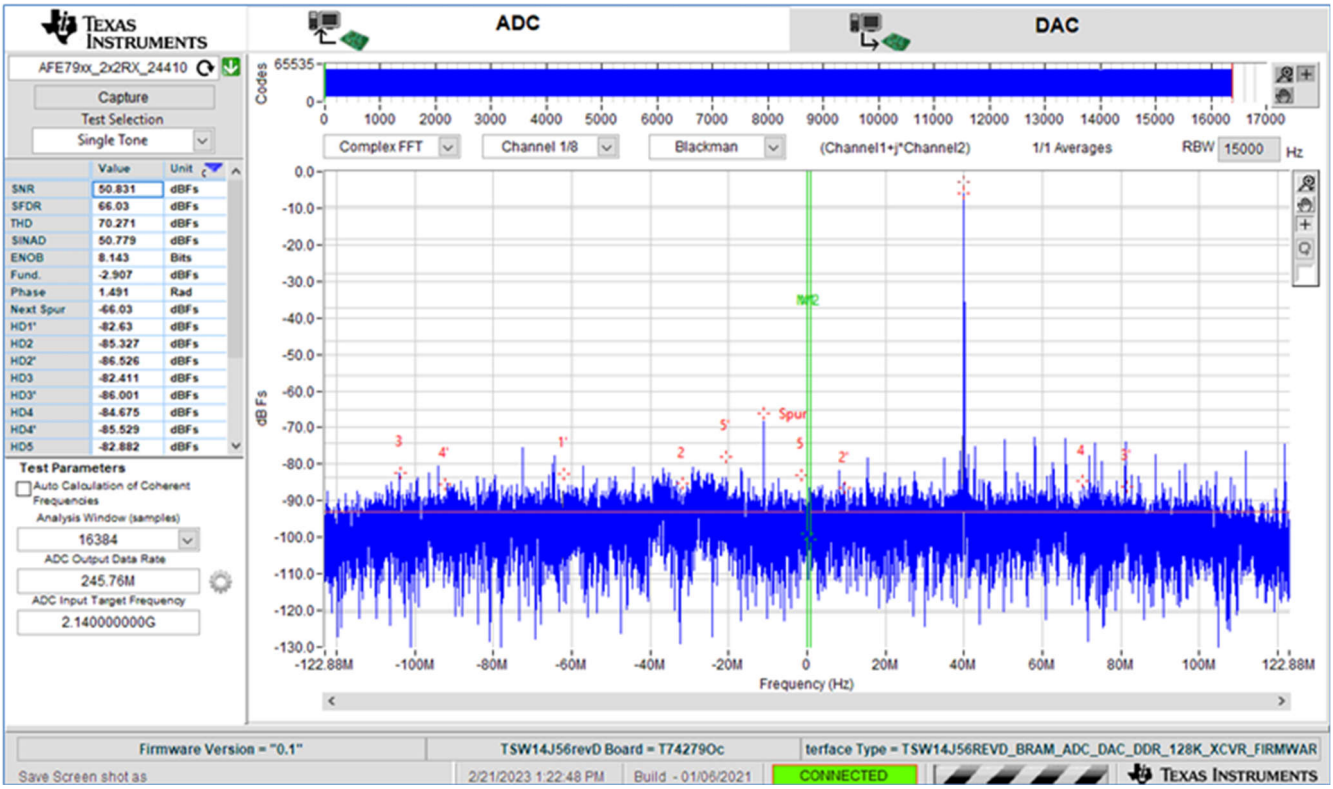


Figure 3-5. RXA/B ADC FFT Spectrum

3.6.4 RXC/D ADC Test Results

The config file is setup on channels RXC and RXD with the NCO set to 7.9GHz. The signal generator is set to 7.94GHz and feeds through an appropriate filter. Set the signal generator to achieve a -12dBFS fundamental signal. The signal generator power is around -2 to 0dBm, depending on cable and filter losses.

Figure 3-6 shows the FFT spectrum from the single tone capture. SNR performance is around -54dBFS. SFDR performance is around -70dBFS. HD2, HD3 performance is very good at less than -86dBFS.

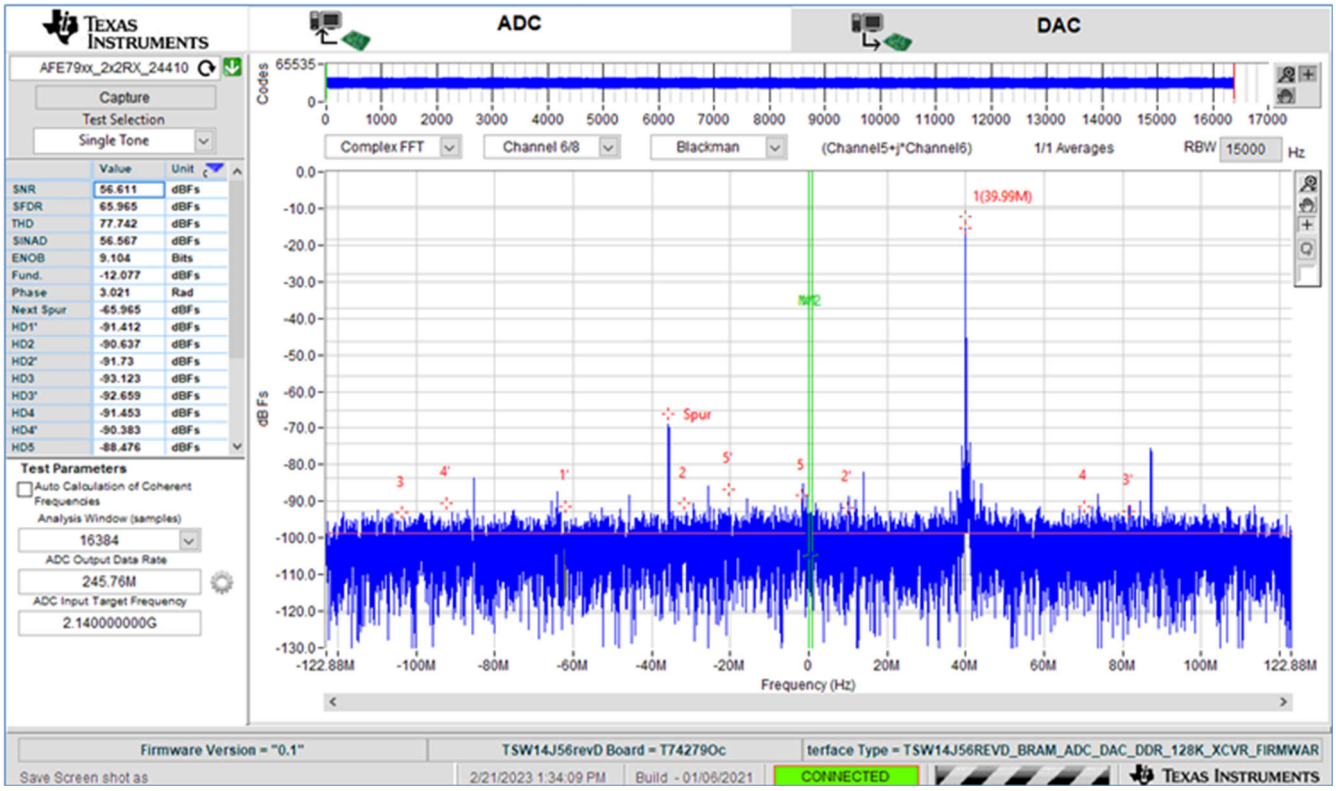


Figure 3-6. RXC ADC FFT Spectrum

3.6.5 FB2 ADC Test Results

The config file sets FB2 channel NCO to 1.7GHz. Inject a tone at 1740MHz through an appropriate band pass filter. For capturing the feedback channel, change the HSDC pro ini file to: AFE79xx_1x2FB_44210. Change the ADC data rate to 491.52M.

Adjust the amplitude of the fundamental signal to read approximately -3dBFS. This is likely a signal generator power around -10 to -14dBm depending on cable and filter loss.

Figure 3-7 shows the FFT spectrum from the single tone capture. SNR performance is around 43dBFS. All TX outputs are disengaged to maintain that FB spectrum is not contaminated.

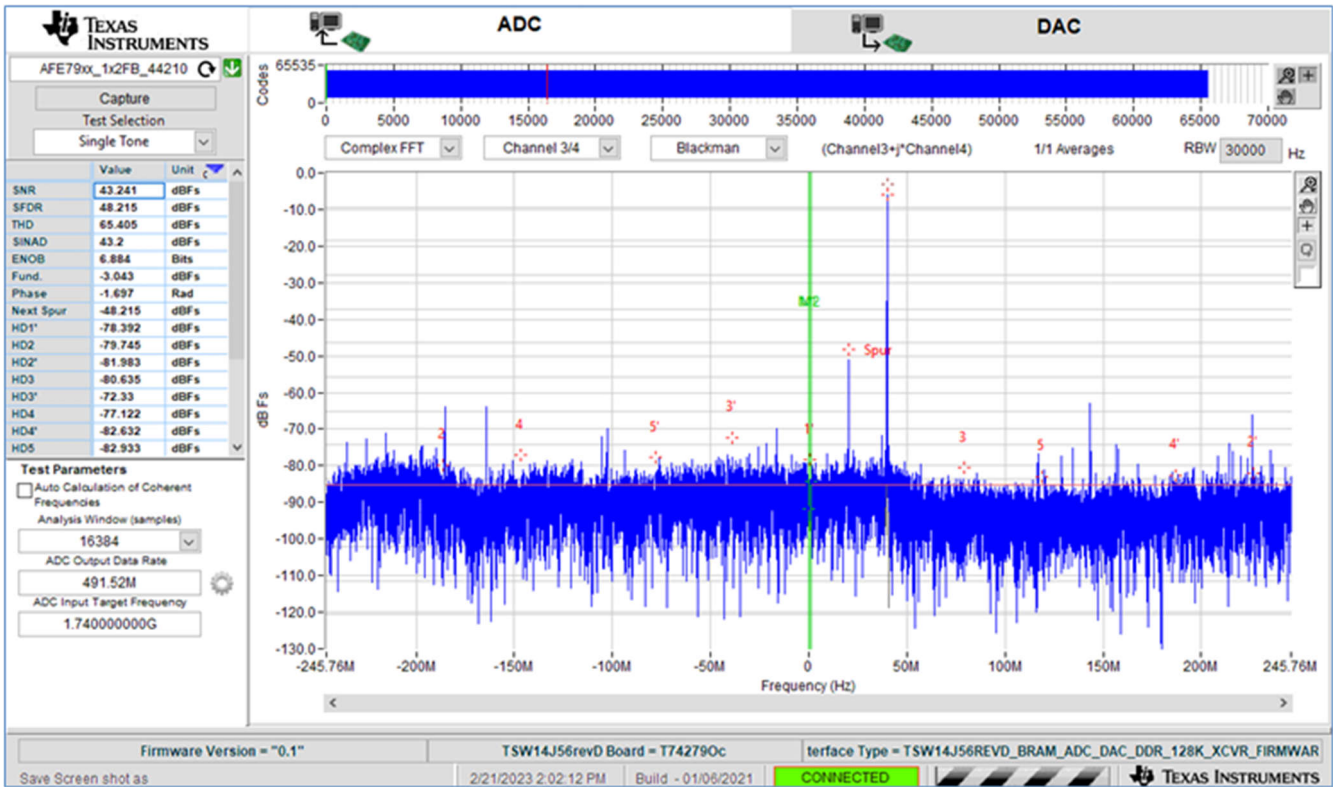


Figure 3-7. FB2 ADC Output FFT Spectrum

3.7 Alternative Configurations

3.7.1 Internal AFE7950-SP PLL/VCO

3.7.1.1 The Easy Way - Internal PLL/VCO

There is an option to use the internal PLL/VCO of the AFE7950-SP device. The *easy way* uses the existing connections and only modifies the software programming. The technique is to program the LMX2694 to supply a 491.52MHz reference signal instead of the high frequency clock. Though this is the easy modification on the reference board, in practice, the appropriate approach as outlined in the next section is to use only the LMK04832-SEP to generate the clock reference to the AFE7950-SP.

This approach follows the primary bring up procedure, but substitutes a different LMX2694 file and a different Latte file.

- LMX2694-SEP: LMX2694-SEP_122p88Ref_122p88PFD_491p52M.tcs
- Latte: AFE7950-SP_EVM_Mode2H.py

This LMX file outputs a 491.52MHz signal that the AFE7950-SP uses as the reference for the internal PLL/VCO. The Latte file engages the internal PLL/VCO. As an example, Figure 3-8 shows the TXA output spectrum when using the internal PLL/VCO.

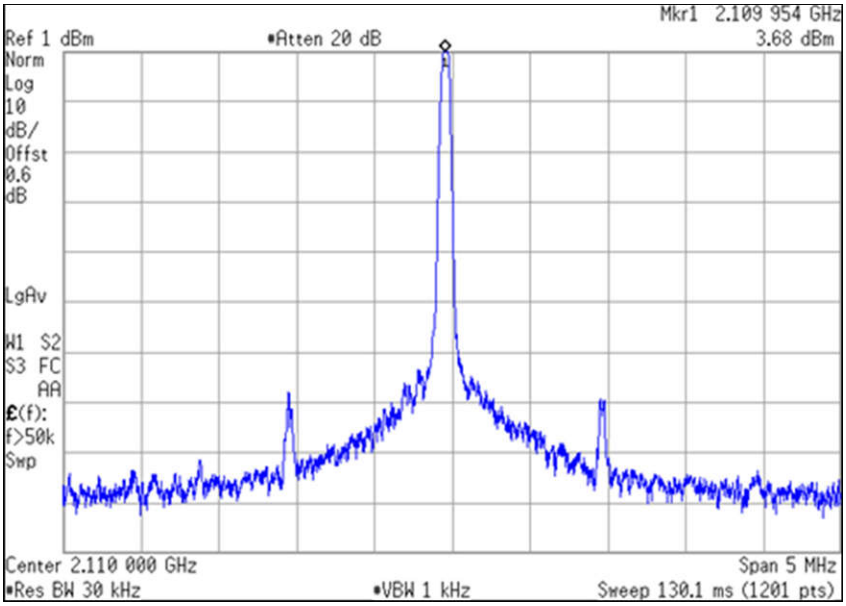


Figure 3-8. TXA Output Spectrum with AFE7950-SP Internal PLL/VCO

3.7.1.2 The Proper Way - Internal PLL/VCO

The *proper way* for using the internal PLL/VCO is to bypass the LMX2694 completely and drive the reference directly from the LMK04832. This approach requires solder modifications on the board (this is not the *easy way*).

The following hardware changes are needed to implement this configuration:

- C181, C194: Do Not Install
- C28, C45: Place 0.1uF coupling caps
- R48: Do Not Install (disengages power to the LMX2694)

The bring-up sequence modifies programming files per the following:

- LMK04832-SEP: LMK04832-SEP_TICsPro_491p52_CLKINBypass_LMXBypass.tcs
- Latte: AFE7950-SP_EVM_Mode2H.py

The LMK file outputs a 491.52MHz reference that feeds directly to the AFE7950-SP clock input. No programming is done on the LMX part.

3.7.2 Internal TCXO Operation

The default test procedure outlines uses an external high-quality reference oscillator at 491.52MHz which is buffered or divided by the LMK04832-SEP in bypass mode. Alternatively, the reference design has an on-board 30.72MHz TCXO. This TCXO can serve as the reference for the LMK internal PLL/VCO. With this approach, the internal PLL/VCO is locked to 2949.12MHz. That output signal is divided down to supply the necessary clocks to the AFE, LMX, and FPGA.

Implement this approach by executing the following config file during the bring-up of the LMK04832:

- LMK04832-SEP: LMK04832-SEP_TICsPro_2949p12M_VCO_30p72_TCXO.tcs

The disadvantage of this approach is the degraded phase noise performance of the AFE reference signal that is derived from the LMK VCO compared to a high quality TCXO like a Wenzel Oscillator. Figure 3-9 shows performance of the AFE7950-SP with internal PLL/VCO clock where the reference is derived from the LMK VCO.

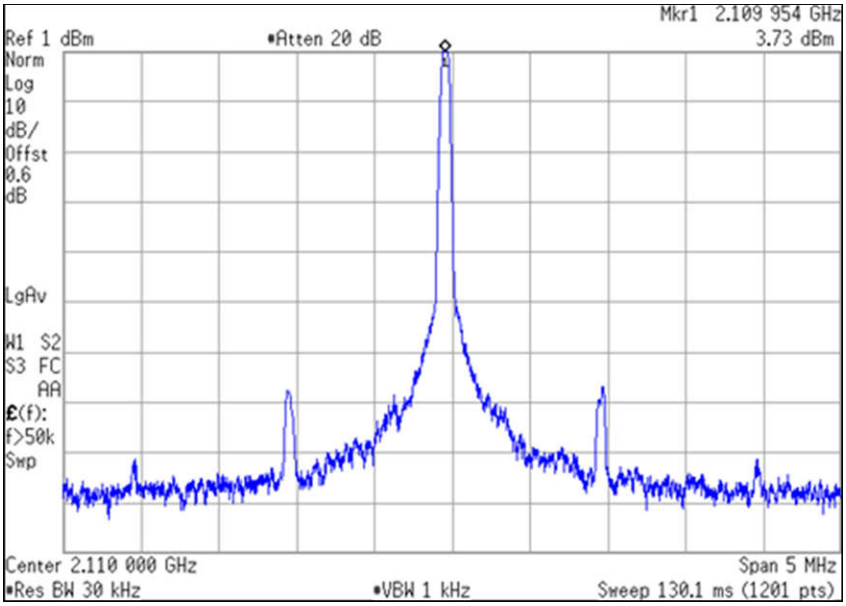


Figure 3-9. TXA Output With LMX Reference Derived From TCXO

3.7.3 400MHz Bandwidth RX Configuration

The default configuration uses an ini file with a JESD LMFS setting and configuration that supports a 245.76MSPS data rate corresponding to a 200MHz receiver bandwidth. The configuration can be modified to support a 491.52MSPS data rate corresponding to a 400MHz bandwidth. Substitute the following Latte file.

- Latte: AFE7950-SP_EVM_Mode3H_Clk12G.py

In HSDC Pro, complete the following modifications:

- Load new ini file: AFE79xx_2x2RX_44210.ini
- Sample Rate: 491.52M

Note, in this configuration, all RX channels are configured for 491.52MSPS and all lanes are consumed, so the feedback path is disabled.

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010260

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010260.

4.2 Tools

TSW14J56 JESD204B FPGA Pattern/Capture Card

4.2.1 Latte Commands

The following table lists useful Latte commands for modifying or evaluation the board condition.

Parameter	Latte Command	Notes
Adjust Channel Outputs	AFE.TOP.overrideTdd(15,2,15)	Rx, Fb, Tx 15(d) = 1111(b)= All On
Adjust DSA Setting	AFE.DSA.set<Path>Dsa(<Ch>,<Attn>)	<Path> = Tx, Rx, Fb <Ch> = 0, 1, 2, 3 for example, AFE.DSA.SetTxDsa(0,10)
Adjust NCO Settings	AFE.update(<Path>Nco(<Ch>,Freq)	<Path> = Tx, Rx, Fb <Ch> = 0, 1, 2, 3 for example, AFE.updateTxNco(0,2100)
Re-sync DAC	AFE.adcDacSync()	
Measure Temperature	AFE.getDeviceTemp()	

4.2.2 Config Files

4.2.2.1 Latte Config Files

The following Latte config files are referenced in this document.

AFE7950-SP_12GClk_ExtClk.py	11,796.48MHz External Clock
AFE7950-SP_EVM_Mode2H.py	11,796.48MHz Internal Clock
AFE7950-SP_EVM_Mode3H_Clk12G.py	11,796.48MHz Int Clk; RX Fd = 491.52M

4.2.2.2 LMK / LMX Config Files

The following config files are used to program the LMK04832-SEP.

- LMK04832-SEP_TICsPro_122p88_CLKINBypass_LMXRef.tcs
  - 491.52MHz in; 122.88MHz out
- LMK04832-SEP_TICsPro_491p52_CLKINBypass_LMXBypass.tcs
  - 491.52MHz in; 491.52MHz out
- LMK04832-SEP_TICsPro_2949p12M_VCO_30p72_TCXO.tcs
  - 30.72MHz in; 122.88MHz out

The following config files are used to program the LMX2694-SEP.

- LMX2694-SEP_122p88Ref_122p88PFD_11796p48M.tcs
  - 11,796.48MHz clock output
- LMX2694-SEP_122p88Ref_122p88PFD_491p52M.tcs

  - 491.52MHz clock output

4.2.3 Troubleshooting

This section gives some guidance for resolving common issues.

- No flashy light on ‘J56
  - Check that 491.52MHz reference is working
  - Verify LMK jumper on interface board is properly placed/not placed for programming
- TX output noise is very high
  - Issue a Re-Sync DAC command
  - Power cycle and re-initiate from scratch
- One or more RX channels has no data
  - Verify override does not have channel disabled
  - Verify FMC connector is seated properly
- One or more RX channels has very high noise
  - Verify proper ini file
  - Power cycle and re-initiate from scratch
  - Power cycle ‘J56 and re-initiate HSDC Pro
- Latte reports errors during bring-up
  - Verify voltage and current limit are appropriately set
  - Power cycle and re-initiate from scratch

4.3 Hardware Identification Information

4.3.1 Rework Modifications

Hardware modifications on the board for optimum performance are listed in the following table.

Area	Rework	Notes
Ref Clock	DNI C78, C85	Disables DCLK2 path to OscOut contingency

4.3.2 Reference Design Board Location Identification

Figure 4-1 identifies key components and ports on the board.

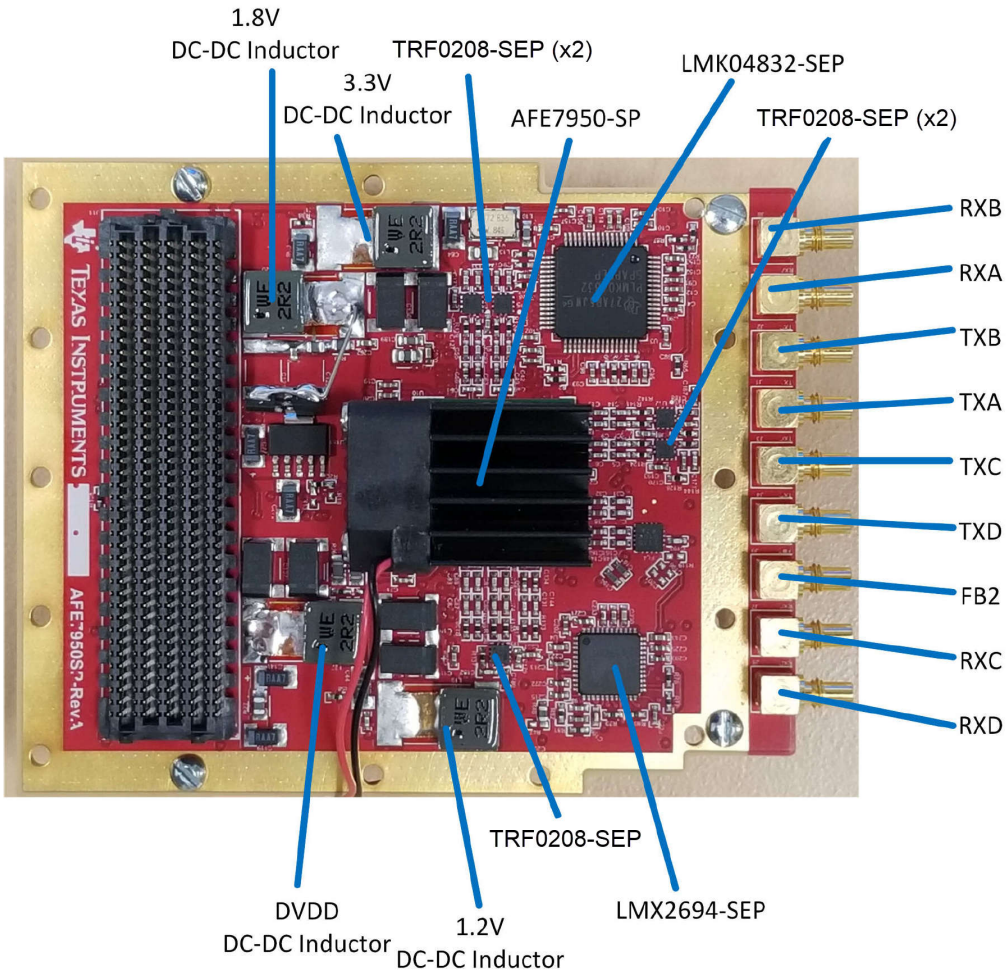


Figure 4-1. Reference Design Board Identification

4.3.3 FMC Interface Board Location Identification

Figure 4-2 identifies key connectors and ports on the FMC Interface board.

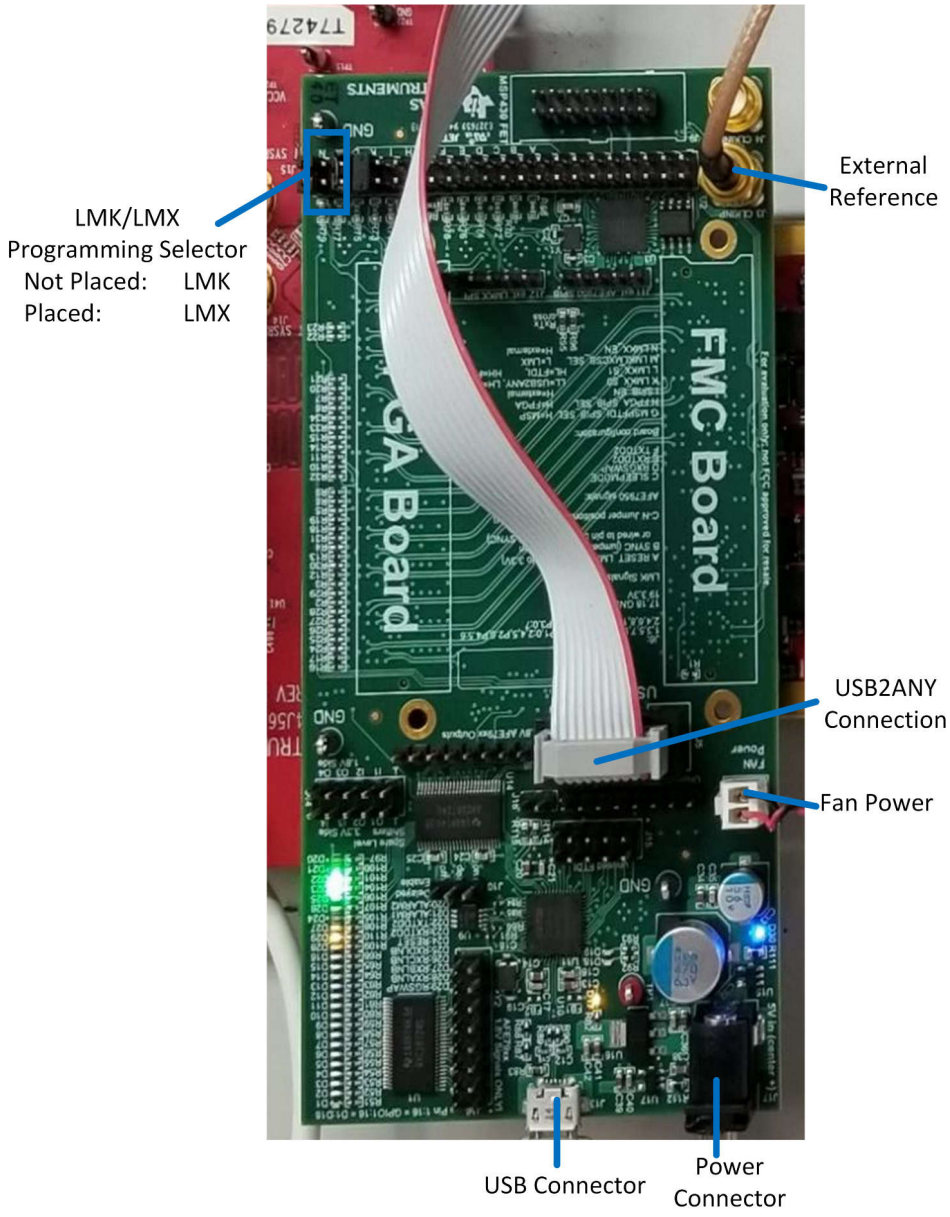


Figure 4-2. FMC Interface Board Identification

4.4 Documentation Support

1. Texas Instruments, *AFE7950 4T6R RF Sampling AFE with 12 GSPS DACs and 3 GSPS ADCs*, data sheet.

4.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

Russell Hoppenstein is a system engineer in the System Engineering Marketing (SEM) group supporting the Aerospace and Defense sector. He has over 20 years of semiconductor experience working with high-performance RF devices and RF sampling data converters for the communication and defense markets. He previously designed RF transceivers, active antenna systems, and linearized power amplifiers for the wireless infrastructure market. Russell earned his BSEE from the University of Texas at Austin and his MSEE from University of Texas at Arlington.

6 Revision History

Changes from Revision * (March 2024) to Revision A (November 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated *TIDA-010260 Block Diagram* to correct *TRF0208-SP/SEP* part number	2
• Added *TRF0208-SEP* section	4

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