Design Guide: TIDA-020047

Two-Device mmWave Cascade Reference Design for Automotive 4D Imaging Radar

Description

This automotive radar reference design is a cascaded 76-GHz to 81-GHz radar sensor module. This includes two-device cascaded array of AWR2243 devices and an AM2732R radar processor. In this cascaded radar configuration, a primary device distributes a 20-GHz local-oscillator (LO) signal to both the primary and secondary devices, allowing these two devices to operate as a single RF transceiver. This enables support for up to 6 transmit (TX) and 8 receive (RX) antenna elements, giving a total number of 48 virtual channels in the MIMO virtual array.

Resources

TIDA-020047	Design Folder
AWR2243, AM2732-Q1	Product Folder
LP876242-Q1, LM62460-Q1	Product Folder
DP83TC812-Q1, DP83TC811-Q1	Product Folder
TCAN1043A-Q1, TCAN1044A-Q1	Product Folder
TMP112-Q1, TPS78401-Q1	Product Folder
TPS61379-Q1, TPS7B8133-Q1	Product Folder

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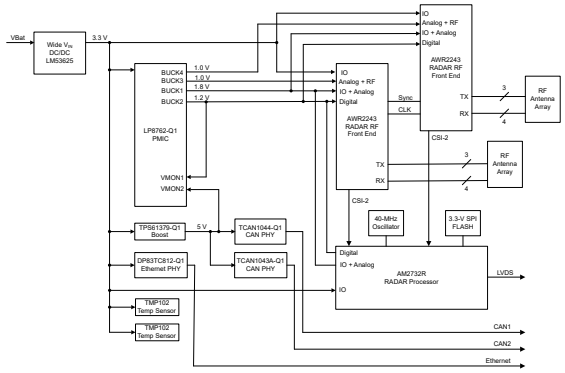
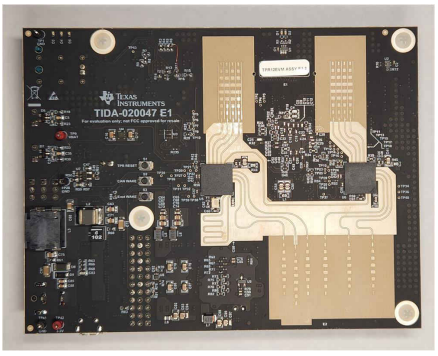
Features

- Imaging radar
- Longer-range TX beamforming and beamsteering
- High angular resolution MIMO
- Power Supply Optimized for Small Size and High Efficiency
- Two-device 76- to 81-GHz Automotive Radar Sensor Integrates DSP and MCU and Provides Object Data Over CAN-FD, Ethernet or LVDS
- Wide VIN 36-V OFF Battery Supply Tolerates up to 42 V
- Diagnostic and Monitoring Functions for ASIL B

Applications

- Imaging Radar
- Long Range Radar
- Medium or Short Range Radar





1 System Description

High resolution images of vehicle surroundings are a requirement for many automotive safety systems. This cascade radar reference design addresses these concerns by combining two 76- to 81-GHz radar transceivers, a radar processor, two CAN-FD PHYs, an Ethernet PHY and a low noise power supply. The only two connections that the system requires are the battery power input and CAN-FD or Ethernet for data output.

The radar section of this design utilizes a printed-circuit-board (PCB) etched antenna with 6 transmit elements and 8 receive elements. By using this antenna, a modulated chirp is transmitted and reflections are sampled into the onboard digital signal processor (DSP). With this information, the sensor can record distance, angle, and velocity measurements from objects within the antenna field of view. The design offers a feature to write out the object data to a central electronic control unit (ECU) on the CAN-FD bus at a rate of 5 Mb/s, raw data to the LVDS port, or any data up to 100 Mb/s over Ethernet PHY.

1.1 Key System Specifications

Detect and track objects (such as cars and trucks) up to 250 meters away with velocity of ±45 meters per second (m/s).

Antenna azimuth field of view ±75º with azimuth angular resolution of approximately 3.5º.

Demonstrates the following AWR2243 capabilities:

- TX phase shift
- Data compression
- HWA with Doppler division multiple access
- (DDMA) processing chain provided by mmWave SDK

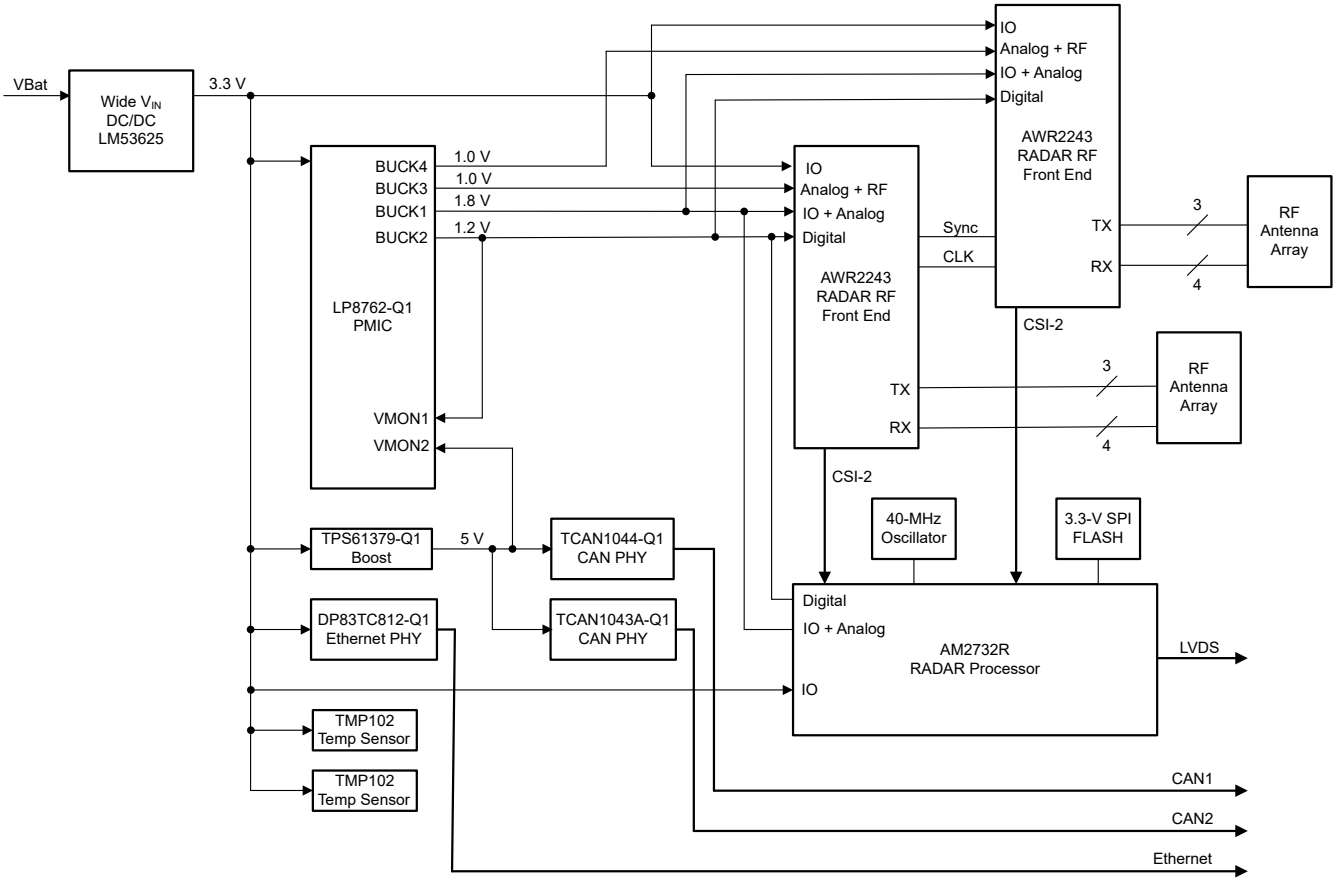
Table 1-1. Key System Specifications

FOV azimuth	**± 75 degrees**
FOV elevation	±10 degrees
Azimuth angle resolution	3.5 degrees
Max range detection (car)	250 meters at ± 30 degrees 100 meters at ± 75 degrees
Range resolution	1.07
Velocity resolution	0.09 m/s
Max velocity	± 45.6 m/s
Radar data cube (0.5 compression)	2MB

2 System Overview

The battery power connects to the 12-V input terminal, J10. The wide VIN buck, LM62460-Q1, is used to convert this 12-V input to a 3.3-V output. The LP876242-Q1 then takes the 3.3-V input and creates, 1.8-V, 1.2-V and 1.0-V rails. To maintan a low-noise supply, the 1-V rail is filtered to create a clean input rail for the radio frequency (RF) section of the radar.

2.1 Block Diagram



2.2 Design Considerations

In TX beamforming, beamsteering, and multiple-input, multiple-output/single-input, multiple-output (MIMO/SIMO) use cases, the larger number of antenna elements allows for higher signal-to-noise ratio (SNR) and superior angular resolution compared to a single-device sensor.

This application focuses on corner and front long-range radar systems for multiple functions such as adaptive cruise control (ACC), automated emergency braking (AEB), blind spot detection, front cross-traffic assist, and lane change assist. The design also demonstrates the TI compression engine and hardware accelerator (HWA) capabilities.

The Cascade Radar evaluation board, when combined with a compatible host/data capture board, contains everything needed to start evaluating a single-device, or 2-device cascaded radar solution.

2.3 Highlighted Products

2.3.1 Devices

2.3.1.1 AWR2243

The AWR2243 device is an integrated single-chip FMCW transceiver capable of operation in the 76- to 81-GHz band. The device enables unprecedented levels of integration in an extremely small form factor. AWR2243 is an ideal solution for low power, self-monitored, ultra-accurate radar systems in the automotive space.

The AWR2243 device is a self-contained FMCW transceiver single-chip solution that simplifies the implementation of Automotive Radar sensors in the band of 76 to 81 GHz. It is built on TI's low-power 45-nm RFCMOS process, which enables a monolithic implementation of a 3TX, 4RX system with built-in PLL and ADC converters. Simple programming model changes can enable a wide variety of sensor implementation (Short, Mid, Long) with the possibility of dynamic reconfiguration for implementing a multimode sensor.

2.3.1.2 AM2732R

The AM273x family of microcontrollers is a highly-integrated, high-performance microcontroller based on the Arm Cortex-R5F and a C66x floating-point DSP cores. The device enables Original-Equipment Manufacturers (OEM) and Original-Design Manufacturers (ODM) to quickly bring to market devices with robust software support, rich user interfaces, and high performance, through the maximum flexibility of a fully integrated, mixed processor solution.

With an integrated Hardware Security Module (HSM) and functional safety support built in, large, integrated RAM on die and a wide temperature range, the AM273x offers a safe, secure and cost-effective solution for many industrial and automotive applications

2.3.1.3 LP876242-Q1

The LP876242-Q1 device is designed to meet the power management requirements of the latest processors and platforms in various safety-relevant automotive and industrial applications. The device has four step-down DC/DC converter cores, generating four 1-phase outputs. The device settings can be changed by I2C-compatible serial interface or by a SPI serial interface.

The switching clock is forced to PWM mode and the phases are interleaved. The switching can be synchronized to an external clock and spread-spectrum mode can be enabled to minimize the disturbances.

The LP876242-Q1 device is a power-management integrated circuit (PMIC), available in a 32-pin, 0.5-mm pitch, 5.5-mm × 5-mm QFN HotRod package. The device is designed for powering embedded systems or system on chip (SoC) in Automotive or Industrial applications. All buck converters have the capability to sink up to 1 A, and support dynamic voltage scaling. Double buffered voltage scaling registers enable each BUCK to transition to different voltages during operation by SPI, I2C or state transition. A DPLL enables the BUCK converters to synchronizing to an external clock input, with phase delays between the output rails.

Two I2C interface channels or one SPI channel can be used to configure the power rails and the power state of the LP876242-Q1 device. I2C channel 1 (I2C1) is the main channel with access to the registers that control the configurable power sequencer, the states and the outputs of power rails, and the device operating states.

I2C channel 2 (I2C2), which is available through GPIO2 and GPIO3 pins, is dedicated for accessing the Q&A Watchdog communication registers. When the SPI is configured instead of the two I2C interfaces, the SPI can access all of the registers, including the Q&A Watchdog registers. An NVM option is available to enable I2C1 to access all of the registers as well, including the Q&A Watchdog registers.

LP876242-Q1 device has ten GPIOs each with multiple functions and configurable features. All of the GPIOs, when configured as a general-purpose output pin, can be included in the power-up and power-down sequence and used as enable signals for external resources. In addition, each GPIO can be configured as a wake-up input or a sleep mode trigger. The default configuration of the GPIO port comes from the NVM memory, and can be re-configured by software if the external connection permits.

The LP876242-Q1 device includes a Q&A watchdog to monitor software lockup, and a system error monitoring input (nERR_MCU) with fault injection option to monitor the lock-step signal of the attached MCU. The device includes protection and diagnostic mechanisms such as short-circuit protection, thermal monitoring

and shutdown. The PMIC can notify the processor of these events through the interrupt signal, allowing the processor to act in response.

2.3.1.4 LM62460-Q1

The LM6x4xx-Q1 buck regulator family are automotive-focused regulators providing either fixed or an adjustable output voltage which can be set from 1 V to 95% of expected input voltage. These regulators operate under a wide input voltage range of 3 to 36V and has transient tolerance up to 42 V.

2.3.1.5 TCAN1043A-Q1

The TCAN1043A-Q1 is a high-speed Controller Area Network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2016 highspeed CAN specification. The device supports both classical CAN and CAN FD data rates up to 8 megabits per second (Mbps).

The TCAN1043A-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a system via the INH output pin. This allows a low-current sleep state in which power is gated to all system components except for the TCAN1043A-Q1, while monitoring the CAN bus. When a wake-up event is detected, the TCAN1043AQ1 initiates system start-up by driving INH high.

The TCAN1043A-Q1 features an SWE timer that enables a safe transition to Sleep mode after 4 minutes (tINACTIVE) of inactivity in Standby mode. This ensures that the device is transitioned to low-power Sleep mode if the MCU fails to transition the device to Normal mode.

2.3.1.6 TCAN1044A-Q1

The TCAN1044A-Q1 is a high speed controller area network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2016 highspeed CAN specification.

The TCAN1044A-Q1 transceiver supports both classical CAN and CAN FD networks up to 8 megabits per second (Mbps). The TCAN1044A-Q1 includes internal logic level translation via the VIO terminal to allow for interfacing the transceiver I/Os directly to 1.8 V, 2.5 V, 3.3 V, or 5 V logic I/Os. The transceiver supports a low-power standby mode and wake over CAN compliant to the ISO 11898-2:2016 defined wake-up pattern (WUP). The TCAN1044A-Q1 transceiver also includes protection and diagnostic features supporting thermal-shutdown (TSD), TXDdominant time-out (DTO), supply undervoltage detection, and bus fault protection up to ±58 V.

2.3.1.7 DP83TC812-Q1

The DP83TC812-Q1 device is an IEEE 802.3bwcompliant automotive PHYTER™ Ethernet physical layer transceiver which can work with Unshielded Twisted Pair cable. The PHY supports TC10 sleep and wake features. It provides all physical layer functions needed to transmit and receive data over unshielded single twisted-pair cables. The device provides xMII flexibility with support for standard MII, RMII, RGMII, and SGMII MAC interfaces. The PHY also integrates a low pass filter on the MDI side to reduce emissions.

This device includes the Diagnostic Tool Kit, providing an extensive list of real-time monitoring tools, debug tools and test modes. Within the tool kit is the first integrated electrostatic discharge (ESD) monitoring tool. It is capable of counting ESD events on MDI as well as providing real-time monitoring through the use of a programmable interrupt. Additionally, the DP83TC812-Q1 includes a pseudo random binary sequence (PRBS) frame generation tool, which is fully compatible with internal loopbacks, to transmit and receive data without the use of a MAC. The device is housed in a 6.00-mm × 6.00-mm, 36-pin VQFN wettable flank package. This device is pin-2- pin compatible with DP83TG720 (1000BASE-T1). It is also form factor compatible with DP83TC811. This would allow for a single PCB layout to be used for DP83TC811, DP83TC812, DP83TC814, and DP83TG720.

2.3.1.8 TPS61379-Q1

The TPS61379-Q1 is a fully integrated synchronous boost converter with load disconnect function integrated. The input voltage covers 2.3 V to 14 V, while the maximal output voltage is up to 18.5 V. The switching current limit is 2 A typical. It consumes 25- µA quiescent current from VIN.

The TPS61379-Q1 employs the peak current mode control with the switching frequency programmable from 200 kHz to 2.2 MHz. The device works in fixed frequency PWM operation in medium to heavy load. There are two optional modes in light load by configuring the MODE pin: auto PFM mode and forced PWM to balance the

efficiency and noise immunity in light load. The switching frequency can be synchronized to an external clock. The TPS61379-Q1 uses the spread spectrum of the internal clock to be more EMI friendly at FPWM mode. In addition, there is an internal soft-start time to limit the inrush current.

The TPS61379-Q1 has various fixed output voltage versions to save the external feedback resistor. It supports the external loop compensation so that the stability and transient response can be optimized at wider VOUT/VIN ranges. It also integrates robust protection features including the output short protection, output overvoltage protection, and thermal shutdown protection. The TPS61379-Q1 is available in a 3-mm × 3-mm 16-pin QFN package with wettable flank.

2.3.1.9 TMP102-Q1

The TMP102-Q1 device is a digital temperature sensor ideal for NTC and PTC thermistor replacement where high accuracy is required. The device offers an accuracy of ±0.5°C without requiring calibration or external component signal conditioning. Device temperature sensors are highly linear and do not require complex calculations or lookup tables to derive the temperature. The on-chip 12-bit ADC offers resolutions down to 0.0625°C.

The 1.6-mm × 1.6-mm SOT563 package is 68% smaller footprint than an SOT23 package. The TMP102-Q1 device features SMBus, two-wire, and I 2C interface compatibility, and allows up to four devices on one bus. The device also features an SMBus alert function. The device is specified to operate over supply voltages from 1.4 V to 3.6 V with the maximum quiescent current of 10 µA over the full operating range.

The TMP102-Q1 device is designed for extended temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications. The device is specified for operation over a temperature range of –40°C to 125°C.

The TMP102-Q1 production units are 100% tested against sensors that are NIST-traceable and are verified with equipment that are NIST-traceable through ISO/IEC 17025 accredited calibrations.

3 System Design Theory

For systems with additional safety requirements, diagnostic and monitoring features have been included in this reference design.

- Imaging radar
- Watchdog: The LP876242-Q1 device includes a Q&A watchdog to monitor software lockup, and a system error monitoring input (nERR_MCU) with fault injection option to monitor the lock-step signal of the attached MCU.
  In this implementation, the SPI bus is used for the communication between the PMIC and the MCU. This is done using the two pins for I2C (SCK, SDI) and GPIO2 and GPIO3 (CS0, SDO). When the SPI is configured instead of the two I2C interfaces, the SPI can access all of the registers, including the Q&A Watchdog registers.
- Voltage Monitors (VMON): The voltage monitoring pins within the LP876242-Q1 have been connected to the 1V2_FILTERED and 5V rails. In the event of an under voltage or over voltage event, this allows the PMIC to monitor these rails and using SOC_nRESET_FROM_PMIC (GPIO10) issue a hard reset to the SOC. These inputs are low pass filtered to eliminate any short term events that would not adversely affect the operation of the system. The connection of these monitors is made directly at the connection to the radar. This avoids the situation where the ferrite bead in the power filters could fail and not be detected. The VMON thresholds and the actions taken during an OV/UV condition are configured in the Non-Volatile Memory (NVM) settings of the PMIC, and are re-configurable over SPI.
- Additional Voltage Monitoring: To monitor the VIN_RF1 and VIN_RF2 rails, they are connected to ADC inputs on the SOC. If the rails monitored by the PMIC are functioning correctly, the SOC will be powered and the ADC will be able to monitor the RF rails. The action(s) taken by the SOC during a failure are configurable in software.
- The watchdog monitors the correct operation of the MCU. This watchdog requires specific messages from the MCU in specific time intervals to detect correct operation of the MCU. When the watchdog detects an incorrect operation of the MCU, the LP876242-Q1 device pulls the SOC_nRESET_FROM_PMIC (GPIO10) pin low. This process triggers a restart of the SOC and FE1/FE2.

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

The Cascade Radar reference design includes:

- Two AWR2243 devices: an integrated single-chip FMCW transceiver.
- Power management network using a power management integrated circuit (PMIC) DC/DC supply (LP876242-Q1), wide-Vin Buck DC/DC supply (LM62460-Q1), and Boost DC/DC supply (TPS61379-Q1).
- Two CAN-FD transceivers (TCAN1043A and TCAN1044A), and Ethernet PHY (DP83TC812-Q1).
- The reference design also includes devices to assist with onboard emulation and UART emulation over a USB link with the PC and Ethernet Port.

4.2 Test Setup

4.2.1 Virtual Antenna Array

The two-chip cascade EVM consists of 6-TX channels and 8-RX channels as shown in Figure 4-1 giving a total number of 48 virtual channels in the MIMO virtual array. The arrangement of the channels is shown in Figure 4-2 where the MIMO array gives an aperture limited angle resolution of about 3 deg in the azimuth direction.

The antenna element design is shown in Figure 4-1.

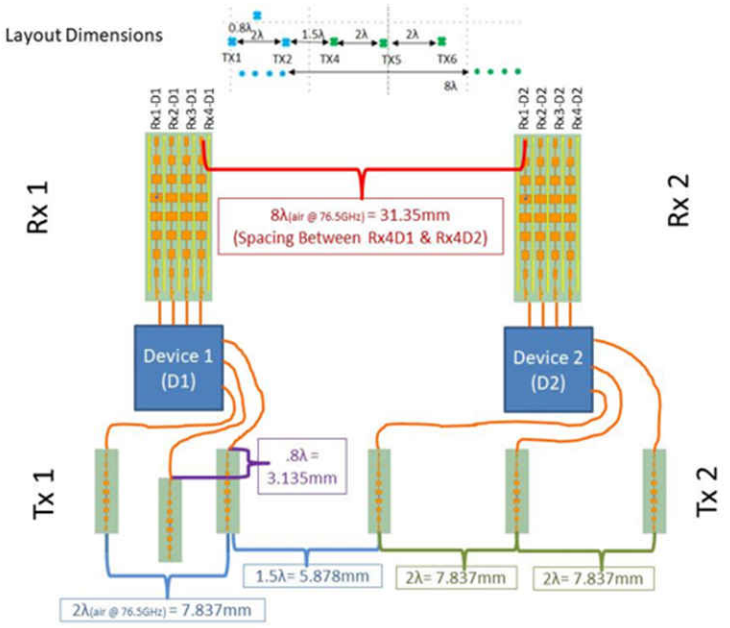


Figure 4-1. TX and RX Channel Spacings

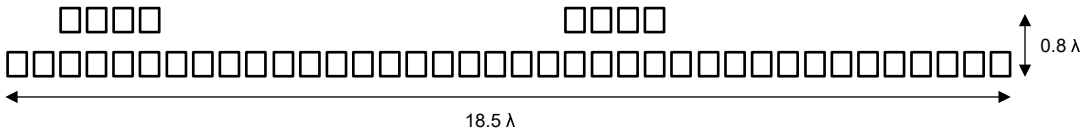


Figure 4-2. MIMO Virtual Array

4.3 Test Results

4.3.1 Angle Resolution Measurement

The azimuth angle resolution was measured by using two 10 dBsm corner reflectors placed in the same range-bin at a radial distance of about 9.5 meter from the radar. Boresight calibration is applied prior to angle estimation (for example, measurements from a single corner reflector placed at boresight are used to compensate for the inter-channel phase gain mismatch).

The angle estimation was performed using a 512-point FFT. The measured angular spectrum from the range-Doppler bin corresponding to the reflection of the corner reflectors is shown in Figure 4-3 where we can see the peaks corresponding to the two corner reflectors. The measured angular separation between the peaks is about 3.3 deg which is close to the theoretical angular resolution of about 3 deg. Higher angular resolution can be obtained by using more computationally extensive angle estimation methods such as Capon Beamformer or MUSIC.

Figure 4-3. Corner Reflectors

Angular spectrum from the range bin corresponding to the two corner reflectors is shown in Figure 4-4.

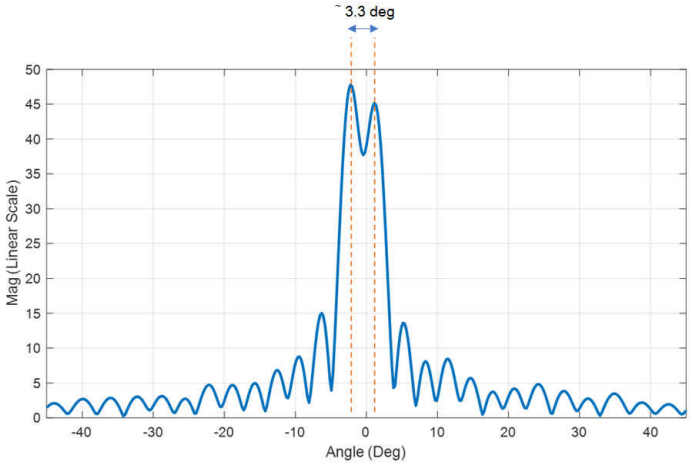


Figure 4-4. Angular Resolution Measurement

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-020047.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-020047.

5.1.3 PCB Layout Recommendations

5.1.3.1 20 GHz (FMCW) RF LO Sync

This reference design is based on TI's AWR2243 radar chip. Using the 20 GHz LO input and output paths, two of these chips are cascaded together and operated synchronously. This requires that the RF LO frequencies of each chip be synchronized. The AWR2243 synthesizer generates LO between 19 GHz and 20.25 GHz, depending on the programmed chirp RF output frequencies.

The AWR2243 that is designated as the primary, generates a common Local Oscillator (LO) signal (19 GHz to 20.25 GHz) to be shared across all the transmitters and receivers in the entire cascade system.

The primary AWR2243 is capable of supplying the shared LO signal on two different output pins through two different delay matched amplifiers. Either or both of these signals, FM_CW_CLKOUT and FM_CW_SYNCOUT, can be used as the source of the LO from the primary to the secondary device. To avoid skew between the LO signals used in both devices, the LO signal input into the primary needs to pass through a trace that is length-matched to the trace between the primary and the secondary devices. As shown in Figure 5-2, one LO signal output is routed with a trace between devices. Then, the other output LO signal from the primary device is looped back to the LO signal input on the primary device using a trace that is the same length.

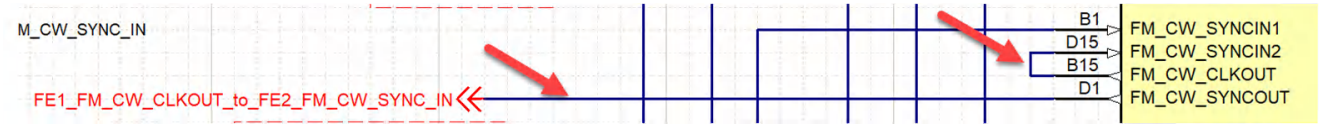


Figure 5-1. LO Clock Signals

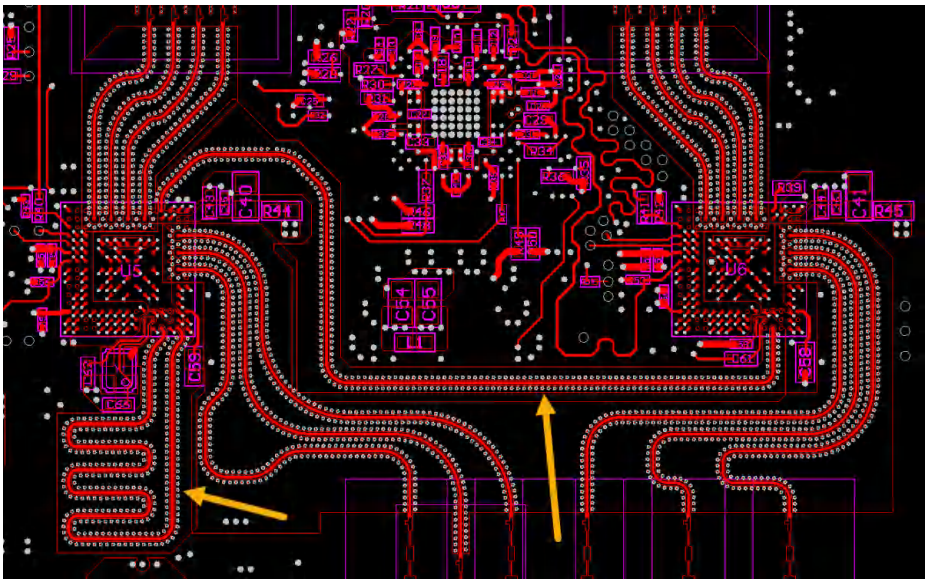
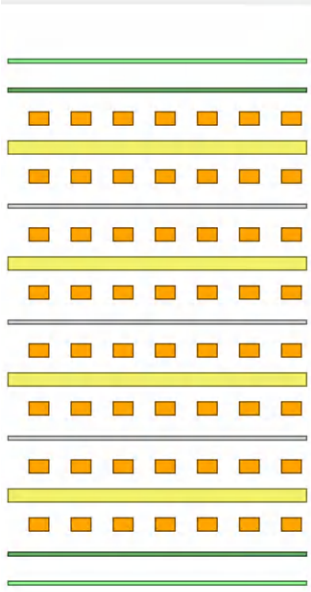


Figure 5-2. LO Clock Routing

5.1.3.2 PCB Layer Stackup

A normal FR4 board material results in unacceptable losses for the 77-GHz antenna included in the top two layers of this design. This design uses ceramic material from Rogers Corporation to meet the dielectric requirements. Additionally, the RO4000® LoPro® series of laminates from Rogers Corporation uses a reverse-treated foil for a smoother metal. This selection of material results in a lower variation in etched-feature dimensions. With wavelengths of less than 4 mm, these tolerances are very important. By routing the 20GHz LO clock (FM_CW) on the same layer as the antennas, only one RO4000 core is required.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Layer 1 - Top Lay...	Signal	Copper	1.6		
Dielectric 1	Dielectric	Core	5	RO3003	3
Layer 2 - GND	Signal	Copper	1.4		
Dielectric 2	Dielectric	Prepreg	5	RO4450F	4.2
Layer 3 - Signal (...	Signal	Copper	0.7		
Dielectric 3	Dielectric	Core	10.7	RO4835	3.66
Layer 4 - GND / ...	Signal	Copper	1.4		
Dielectric 4	Dielectric	Prepreg	5	370HR	4.2
Layer 5 - Signal	Signal	Copper	1.4		
Dielectric 5	Dielectric	Core	10	370HR	4.34
Layer 6 - PWR / ...	Signal	Copper	0.7		
Dielectric 6	Dielectric	Prepreg	5	370HR	4.2
Layer 7 - GND	Signal	Copper	1.4		
Dielectric 7	Dielectric	Core	5	370HR	4.34
Layer 8 - Bottom...	Signal	Copper	1.6		
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Bottom Overlay	Overlay				

Figure 5-3. PCB Layer Stackup

5.1.3.3 Board Photos

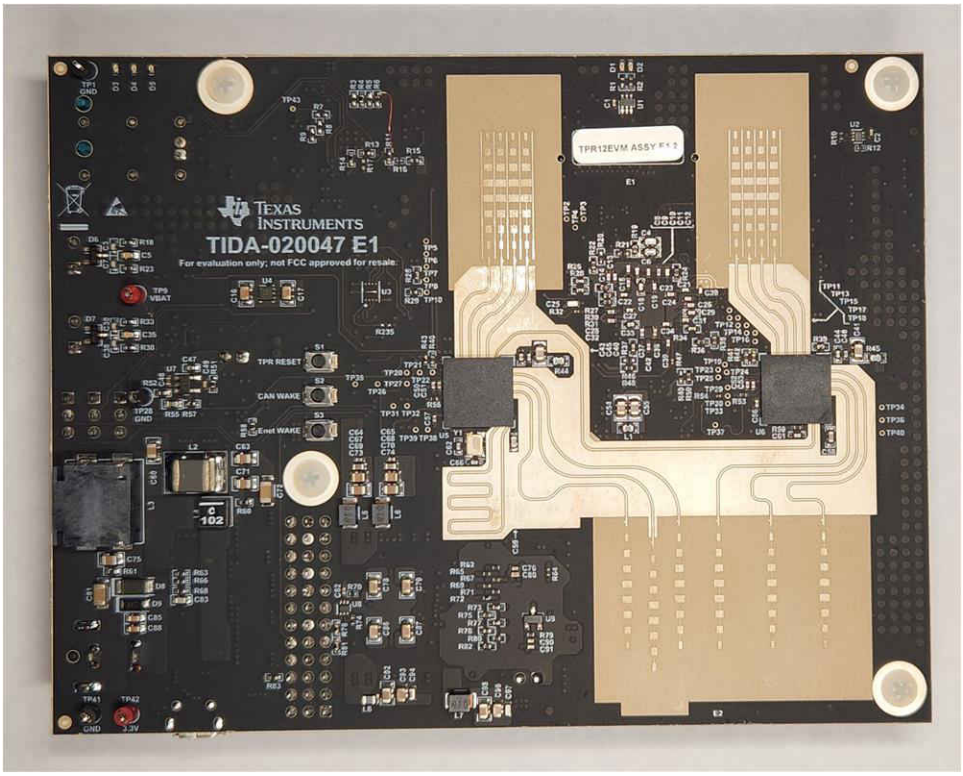


Figure 5-4. Board Side A

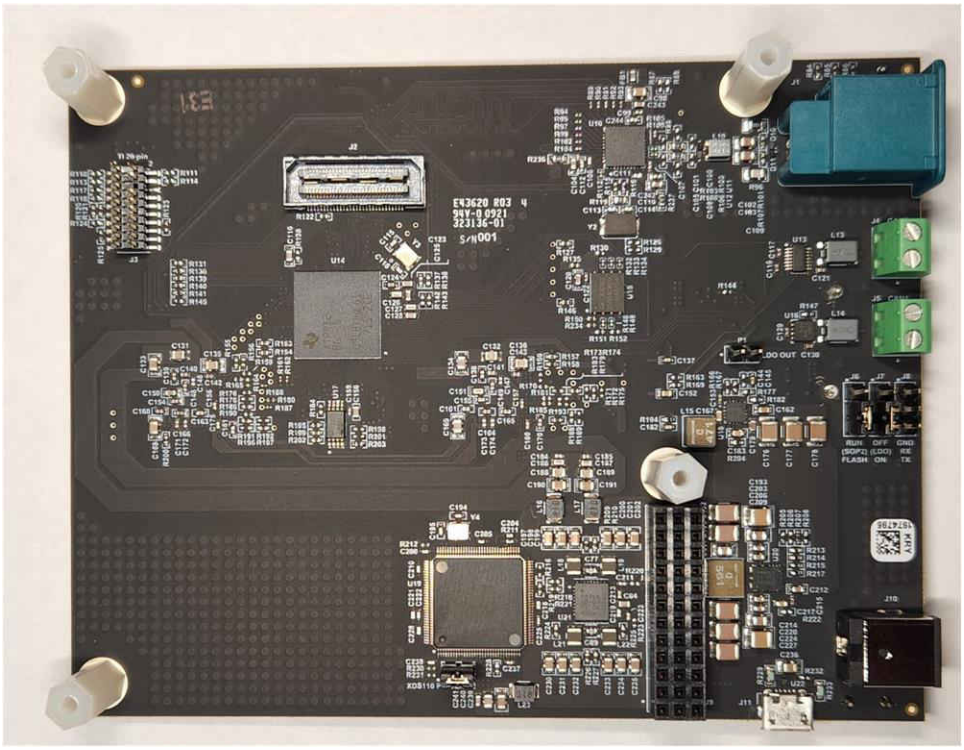


Figure 5-5. Board Side B

5.2 Tools and Software

Tools

DCA1000EVM	Real-time data-capture adapter for radar sensing evaluation module
MMWAVE-STUDIO	mmWave studio

Software

PROCESSOR-SDK-TDAX	Processor SDK for TDAx ADAS SoCs – Linux and TI-RTOS Support
MMWAVE-DEMO-VISUALIZER-CLOUD	

5.3 Documentation Support

1. Texas Instruments, *mmWave Device Firmware Package (DFP)*
2. Texas Instruments, *AM273x Technical Reference Manual*
3. Texas Instruments, *The Fundamentals of Millimeter Wave Radar Sensors*
4. Texas Instruments, *Programming Chirp Parameters in TI Radar Devices* application note

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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