TI Designs: TIDA-050012
Power DUO Source 200 W USB-C PD Reference Design

Description

This USB Power Delivery (PD) reference design will allow users to implement system that require more than 100 W as a power source while also highlighting the industries lowest RDSon solution. The design can output all four of the standard USB Type-C PD source voltages of 5 V, 9 V, 15 V, and 20 V. In standard Type-C PD operation, the design will output up to 20V/4A. When Texas Instruments Power DUO mode is enabled, the design will be able to output up to 20V/10A while simultaneously lowering the RDSon by a factor of two.

Resources

TIDA-050012	Design Folder
TIDA-050014	Design Folder
TPS65987D	Product Folder
LM3489	Product Folder
TPS62177	Product Folder

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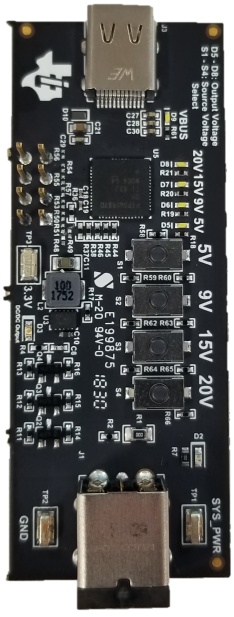
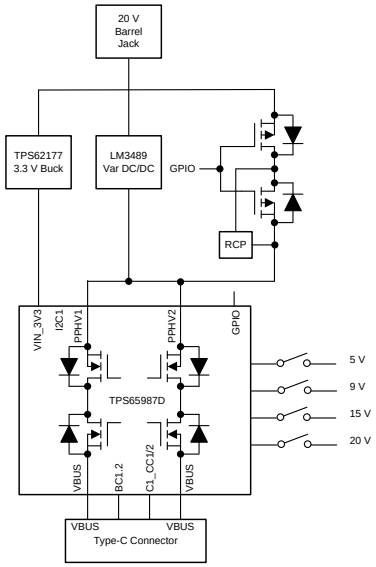
Features

- High Power USB Type-C PD Source
- Barrel Jack to Type-C: 5-V, 9-V, 15-V, or 20-V Charging up to 4 A
- Up to 20-V at 10 A through Texas Instruments Power Duo Mode
- Integrated power paths in PD Controller
- User selectable output voltage

Applications

- Notebooks and Laptops
- Personal Electronics
- Consumer AC/DC: USB Type-C AC/DC Notebook PC Power Adapters (60 W Minimum)
- Power Bank
- Notebook PC Power Adapters





1 System Description

This Design highlights how to implement a high powered USB Type-C PD Source device. This design can be referenced for various different end equipments, from PC Docks, Notebook PC Charger, Industrial chargers, Wall outlets, and many others. Through the use of a Texas Instruments USB Power Duo Mode, the TPS65987D PD adapter will close both of it's load switches in parallel to double the current carrying capability and reduce the effective RDSon by a factor of two. The design also highlights a feature of the TPS65987D called App Config by allowing users to select their Type-C PD Output voltage through push button switches. Additionally, this design goes through steps on how to implement a high powered DC/DC converter to offer the standard Type-C PD source voltages. Finally, the design also contains a P-FET bypass power path to route the input supply directly to the PD controller allowing for very high efficiency in a 20 V contract. The design also supports BC1.2 charging modes through the D+/D- USB 2.0 signals.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input Power Source	20-V Barrel Jack (230 W recommended for full-feature use)
Max Output Power	20-V at 10 A (200 W)
System Quiescent Current	3.4 mA
Typical Load Switch RDSon	29 mOhm
Power DUO Mode RDSon	14.5 mOhm

2 System Overview

2.1 Block Diagram

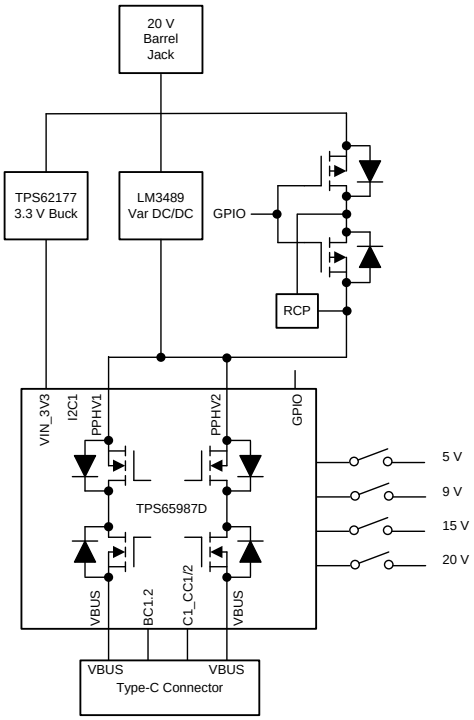


Figure 1. TIDA-050012 Block Diagram

2.2 Design Considerations

TIDA-050012 illustrates how to design a high current USB Type-C PD source device. This subsystem can be used in monitors, docks, dongles, wall chargers, power outlets, and so forth. Any system that is required to provide high power to a connected device can use the concepts in this design. If the end user will exceed 5 A of current, it is recommended to use a tethered cable instead of a Type-C receptacle. This would allow the user to develop their own high current cable and not be limited by the cables and connectors in the design.

2.3 Highlighted Products

The following sections highlight the TI integrated circuits used on this TI-Design and what their benefits are.

2.3.1 TPS65987D

The TPS65987D is a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation detection for a single USB Type-C connector. Upon cable detection, the TPS65987D communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65987D enables the appropriate power path and configures alternate mode settings for external multiplexers. The TPS65987D is fully configurable to fit in many different applications. In this design, the TPS65987D is included to highlight the support of a Texas Instruments Power Duo mode. Power Duo mode allows for the TPS65987D to close both of its power paths in parallel when operating as either a source or a sink. When this mode has been enabled, the effective RDSon of the TPS65987D is decreased by a factor of 2. Additionally, the current carrying capability is doubled.

The TPS65987D is the heart of this design and is used to control the LM3489 output voltage, the VBUS negotiation, VBUS voltage selection, PD Alternate Mode negotiation, and VBUS Over-current protection.

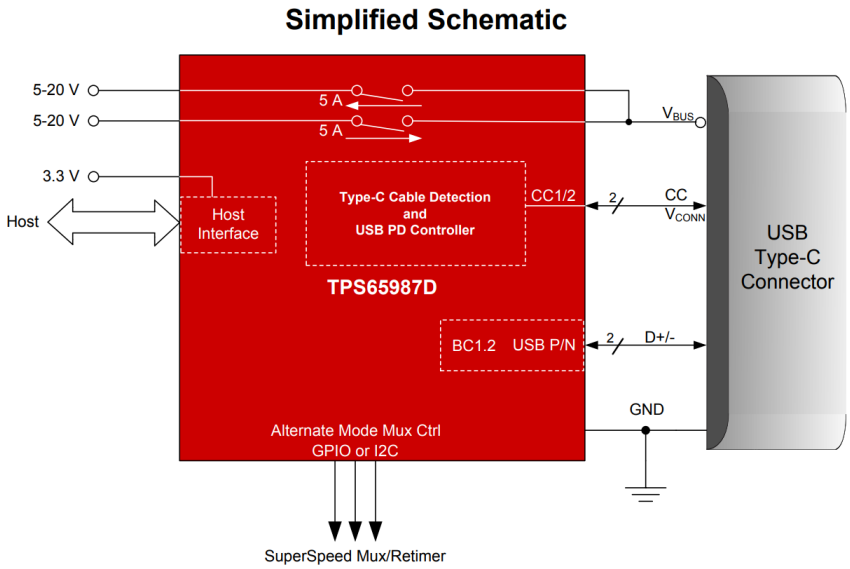


Figure 2. TPS65987D Simplified Schematic

2.3.2 LM3489

The LM3489 device is a high-efficiency PFET switching regulator controller that can be used to quickly and easily develop a small, cost-effective, switching buck regulator for a wide range of applications. The hysteretic control architecture provides for simple design without any control loop stability concerns using a wide variety of external components. The PFET architecture also allows for low component count as well as ultra-low dropout, 100% duty cycle operation. Another benefit is high efficiency operation at light loads without an increase in output ripple. A dedicated enable pin provides a shutdown mode drawing only 7 µA. Leaving the enable pin unconnected defaults to on.

Current limit protection can be implemented by measuring the voltage across the PFET's RDS(ON), thus eliminating the need for a sense resistor. A sense resistor may be used to improve current limit accuracy if desired. The cycle-by-cycle current limit can be adjusted with a single resistor, ensuring safe operation over a range of output currents.

The LM3489 is used to buck down the 20 V DC input to the 5-V, 9-V, 15-V, or 20-V Type-C PD voltages. The LM3489 has a max duty cycle of 100% allowing it to pass through the input voltage through the PFET.

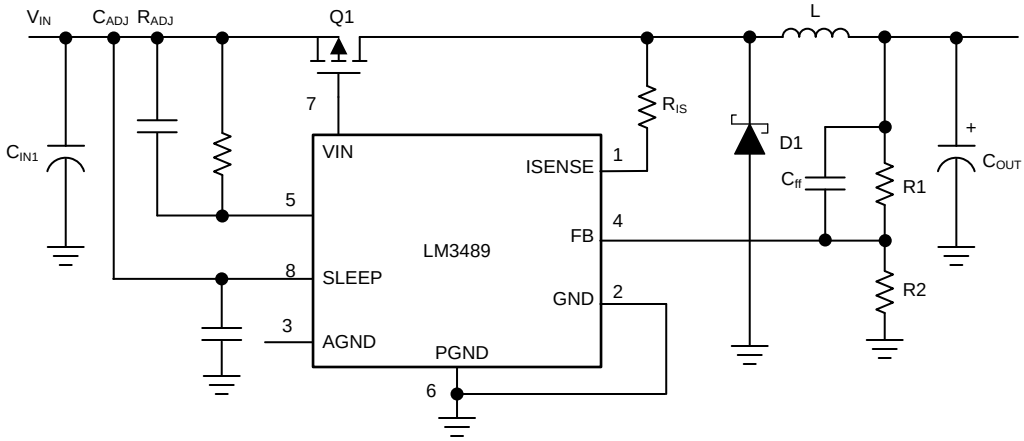


Figure 3. LM3489 Typical Application Circuit

2.3.3 TPS62177

The TPS62177 is a high efficiency synchronous step-down DC/DC converter, based on the DCS-Control™ topology.

With a wide operating input voltage range of 4.75 V to 28 V, the device is ideally suited for systems powered from multi cell Li-Ion as well as 12 V and even higher intermediate supply rails, providing up to 500-mA output current.

The TPS62177 automatically enters power save mode at light loads, to maintain high efficiency across the whole load range. It also features a sleep mode to supply applications with advanced power save modes like ultra low power micro controllers. The power good output may be used for power sequencing and/or power on reset.

The device features a typical quiescent current of 22 µA in normal mode and 4.8 µA in sleep mode. In sleep mode, the efficiency at very low load currents can be increased by as much as 20%. In shutdown mode, the shutdown current is less than 2 µA and the output is actively discharged.

The TPS62177, available in an adjustable and a fixed output voltage version, is packaged in a small 2-mm × 3-mm 10-pin WSON package.

In this design, the TPS62177 is used to convert the 20-V DC input voltage to a 3.3-V output voltage. This is used to power the TPS65987D and other accessories on the board.

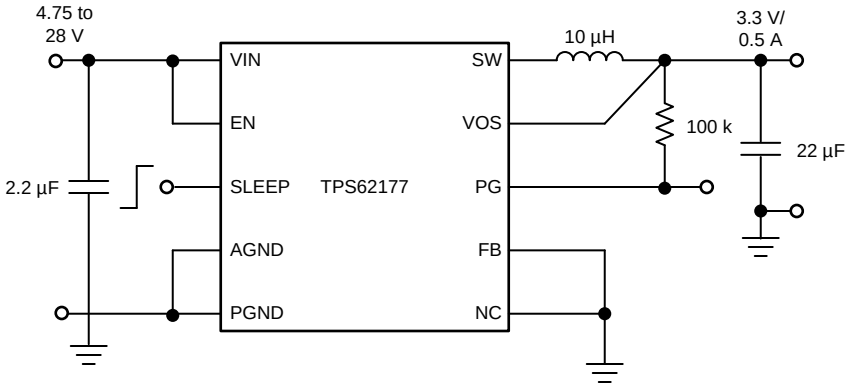


Figure 4. TPS62177 Typical Application Circuit

2.4 System Design Theory

The following sections will highlight subsystems on the TIDA-050012 board, discuss their features, and how they are implemented.

2.4.1 LM3489 DC/DC with Variable Output

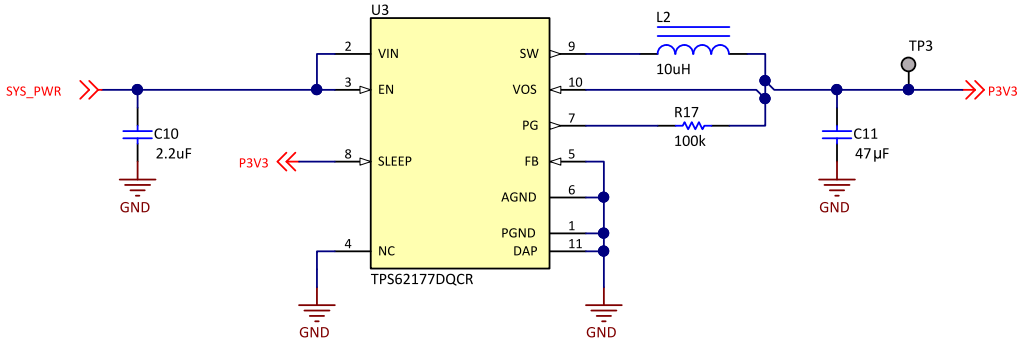


Figure 5. LM3489 Variable DC/DC Schematic

For high powered USB Type-C PD Source applications, a variable DC/DC is required as the source must be able to offer 5-V, 9-V, 15-V, and 20-V per the PD Specification. To do this, the feedback network of the LM3489 is altered through a series of FETs and resistors. The TPS65987D is used to control the feedback loop through GPIO options.

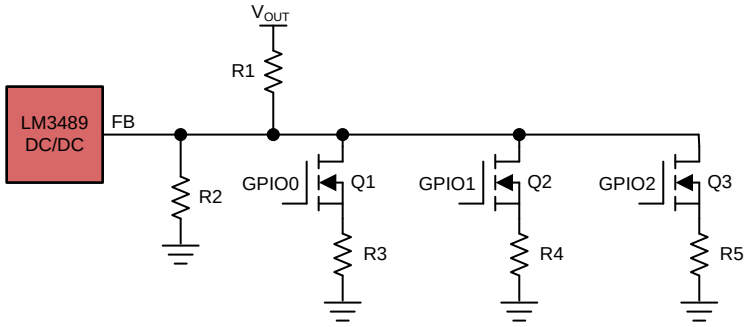


Figure 6. LM3489 Feedback Network

Figure 6 Shows how the feedback network of the LM3489 is implemented in this design. When all of the GPIO's are off, the feedback network just consists of R1 and R2 which will deliver an output voltage of 5 V. When a 9-V PD contract is negotiated, the TPS65987D will enable GPIO0 which would adjust the feedback network so that R2 in parallel with R3 is on the bottom of the divider network. The resistor value for R2 and R3 were selected so that their parallel resistance would deliver an output voltage of 9-V when R1 is at the top of the divider. The same theory applies for a 15 V and 20 V PD contract where either GPIO1 or GPIO2 will turn on respectively to set the output voltage of the LM3489 to the negotiated PD voltage.

Figure 5 highlights the schematic of the LM3489 on this design. Table 2 shows the values calculated for the feedback network and the corresponding output voltage that the LM3489 will deliver.

Table 2. LM3489 Feedback Network Values

PDO_3	PDO_2	PDO_1	Expected Output Voltage	Feedback (R1)	Feedback (R2)	Calculated Output Voltage
0	0	0	5 V	30k	9.53k	5.14-V
0	0	1	9 V	30k	4.59k	9.33-V
0	1	0	15 V	30k	2.64k	15.32-V
1	0	0	20 V	30k	1.79k	22.03-V

The TPS65987D is in control of the GPIOs for the feedback network of the LM3489. When connecting a Type-C PD device to this board, the TPS65987D will begin the PD negotiation contract. On initial connection, all devices will start with 5 V, this is why the base feedback is set to output 5 V. After 5 V is present on VBUS, the two connected devices will communicate over the CC line per the USB Type-C PD Specification. This design will always be the power source so it will send its Source Capabilities of 5-V, 9-V, 15-V, and 20-V to the connected device. The connected device will then select one of those voltages and return a Request message to the Source. The source will then accept this request and begin preparing the system. The source will toggle the correct GPIOs that match the requested output voltage to ensure the LM3489 is outputting the correct voltage. Once the voltage has stabilized, the source will send a PS Ready message indicating to the sink that its power supply is ready and that the sink may now begin to draw current.

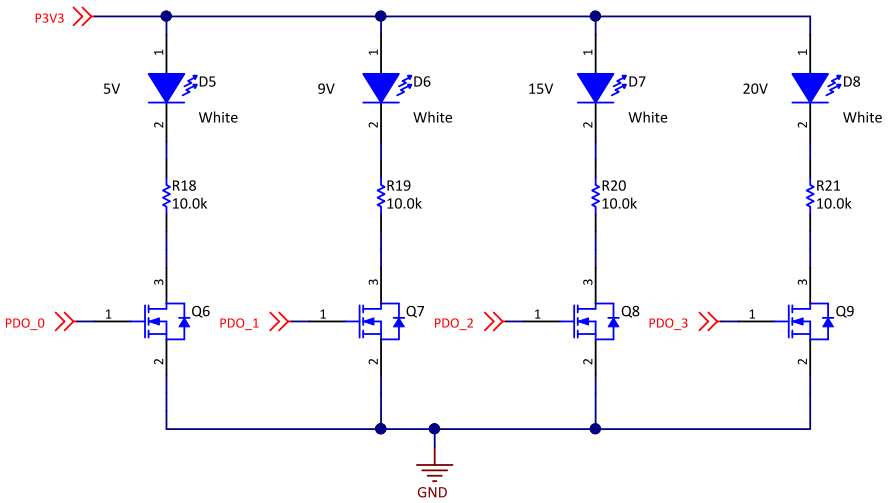


Figure 7. PDO LEDs Schematic

Figure 7 highlights the LEDs on this design that will show the user what type of source contract is currently active. This can help speed up debug and measurements as the actual VBUS voltage is not needed to be measured.

2.4.2 TPS62177 DC/DC Buck Regulator

The TPS62177 was used to generate a 3.3 V supply rail to power the TPS65987D as well as some indication LED's on the TIDA-050012 PCB. The datasheet was followed when creating the TPS62177 schematic.

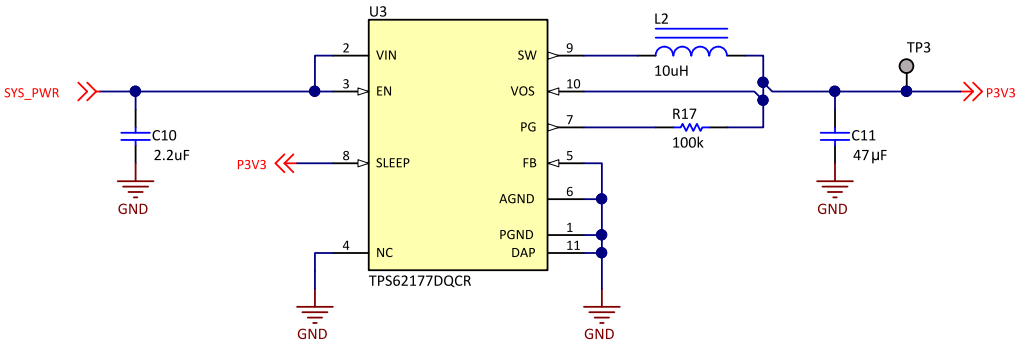


Figure 8. TPS62177 3.3 V Buck Regulator Schematic

2.4.3 TPS65987D PD Controller

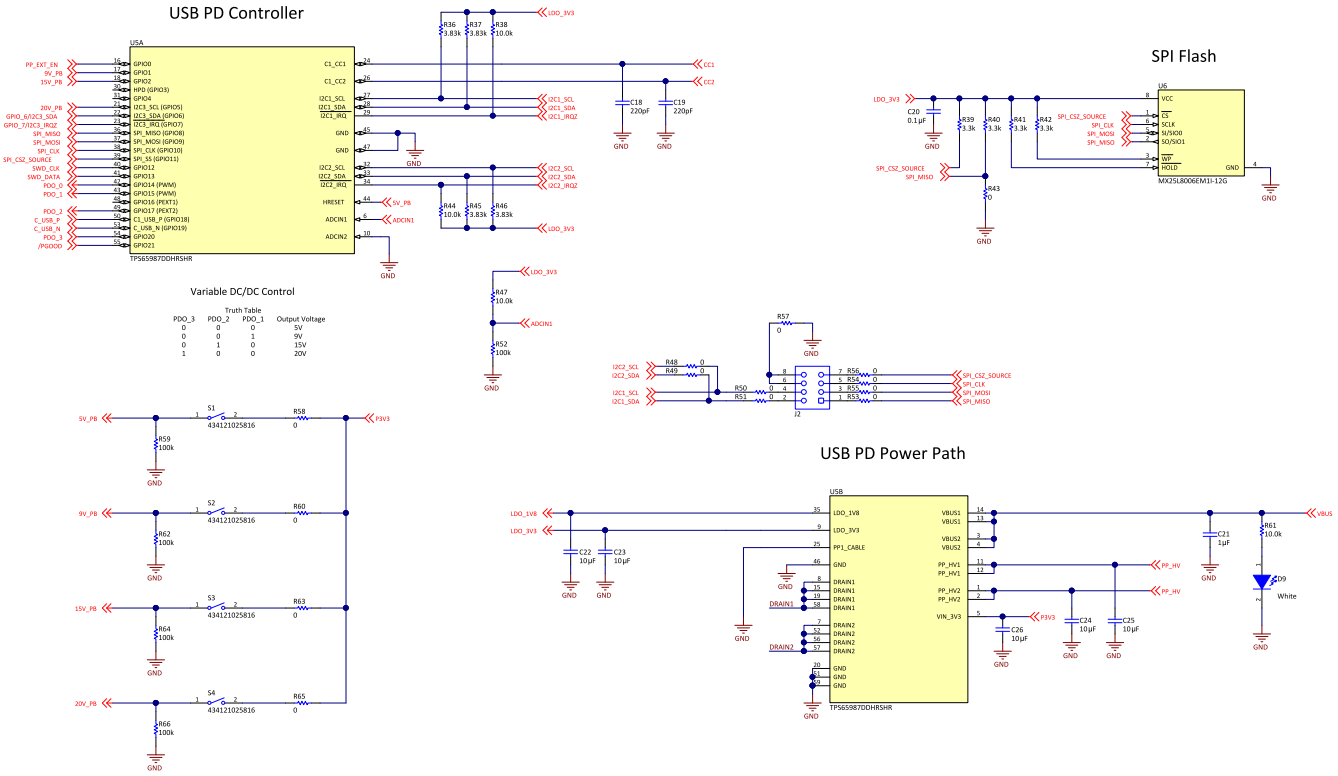


Figure 9. TPS65987D PD Controller Schematic

The TPS65987D is used to handle all of the USB PD communication when another device is connected to the Type-C Connector. The previous section walked through a basic PD negotiation process and how the TPS65987D is used to control the output voltage of the LM3489. It can be seen in the schematic that GPIO 15, 17, and 20 are used for the variable DC/DC control. GPIO 18 and 19 are used as the BC1.2 detection and advertisement pins. These are connected to the USB2.0 D+/D- lines on the Type-C connector so that the TPS65987D can advertise as a BC1.2 compliant charger.

The TPS65987D is using an external SPI-Flash in this design to hold the application code. In many systems, the TPS65987D can boot into a default configuration based on the pin strapping on the ADCIN1 and ADCIN2 pins. This would remove the requirement for an external SPI Flash. Additionally, the TPS65987D has the option of being booted from an external controller. In this scenario, the TPS65987D would receive the application code from the external controller upon boot. However, since this design does not have an external controller and is using a complex application code, an external SPI-Flash is used for flexibility. Upon booting, the TPS65987D will read back the application code from the SPI-Flash. The SPI-Flash is only accessed upon initial boot up and power on reset events.

This design also features an 8 pin header (J2) that connects to the SPI and I2C lines of the TPS65987D. This header can be used to update the application code on the SPI-Flash and to read back registers over I2C during run-time. The TIDA-050014 companion design contains an FTDI chip and this same 8-pin header. This allows the two boards to be stacked on top of one another so that TIDA-050014 can program TIDA-050012. This 8-pin header is highlighted in Figure 10.

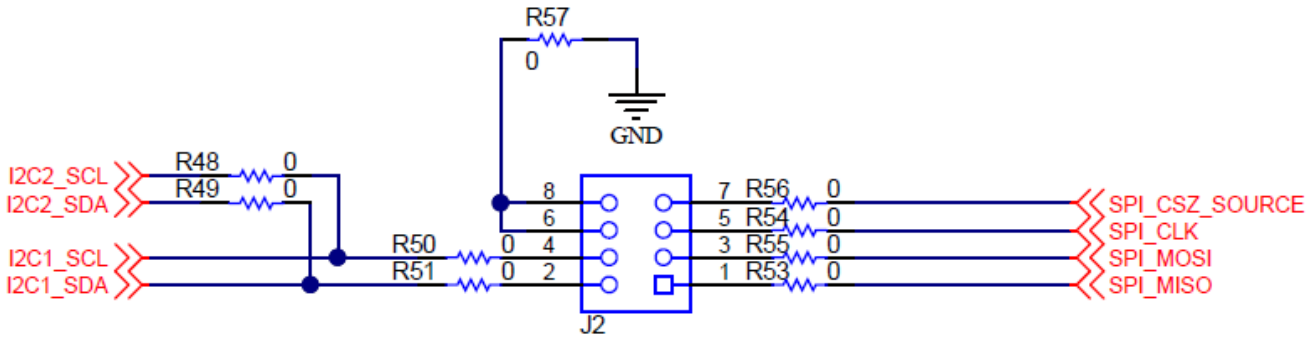


Figure 10. SPI/I2C 8-Pin Programming Header

There are four push button switches that are used to control the output voltage setting by the user. Each button is labeled with the corresponding output voltage that will be offered when the button is pushed. Initially, the TPS65987D will only advertise 5-V as it's only source capability. When for example, the 15-V button is pushed, the TPS65987D will change the configuration in the Source Capabilities register by using the App Config input GPIO events. In this case, the TPS65987D will add 9-V and 15-V to it's source capabilities and then re-send the Source Capabilities to the connected device so a higher voltage contract can be negotiated. If next, the user pushed the 20-V push button, the Source Capabilities register will be updated to add the 20-V PDO in addition to the 5-V, 9-V, and 15-V PDOs and resend the source capabilities PD message to allow for a higher voltage contract to be negotiated. Figure 11 highlights the circuitry used on the push-buttons. When the 5-V push button is pressed after a high voltage push button had been pressed, the TPS65987D will reset to only offering a 5 V PD Contract. GPIOs 1, 2, and 5 are used for the 9-V, 15-V, and 20-V push button inputs respectively.

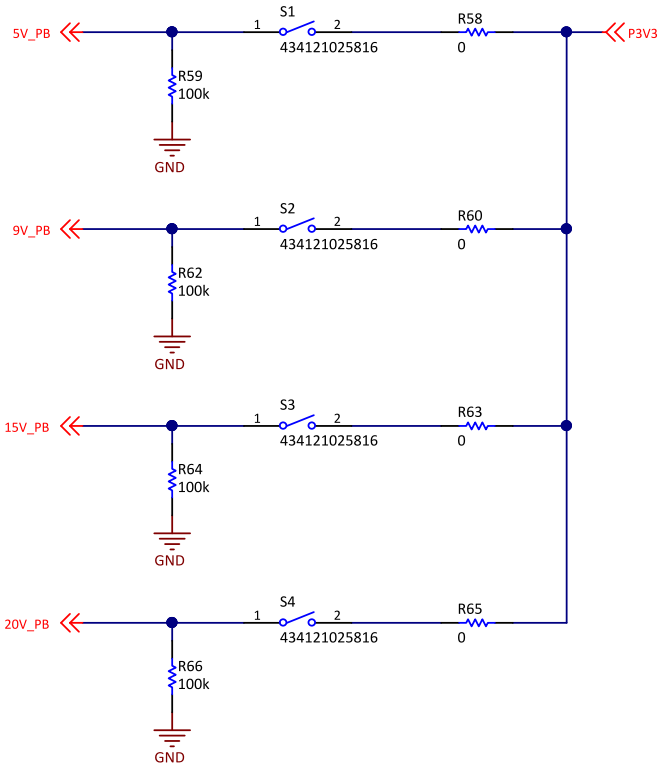


Figure 11. Selectable Output Voltage Push Button Schematic

As seen in Figure 9, the push button signals go into GPIOs of the TPS65987D. The App Config GPIO events are used to load different PDOs based on which button is pushed. For example, when the 9 V Push Button is pressed, the TPS65987D will advertise a 5 V and a 9 V Source Capability. Similarly, when the 20 V push button is pressed, the TPS65987D will advertise 5 V, 9 V, 15 V, and 20 V Source Capabilities. Finally, when the 5 V push button is pressed, the TPS65987D will reload its original configuration which only contains the 5 V source capability. The App Config GPIO event is explained in more detail in the TPS6598x GPIO Events Application Note. Also, the project file for this design can be referenced when using the TPS6598x Application Customization Tool.

When this power source board is paired with the TIDA-050014 Power Sink board, Texas Instruments Power Duo Mode can be enabled. This would allow for the TPS65987D to negotiate up to 200 W over a single Type-C cable. The TPS65987D can close both of its power paths in parallel to allow for double the current carrying potential and half the effective RDSon. Once a 20 V contract has been negotiated, the TPS65987D will toggle a GPIO which will enable a bypass PFET path that will directly pass the barrel jack supply to the PPHV pins of the TPS65987D. This allows for higher current loads since the loss from the DC/DC converter is removed.

2.4.4 External PFET Bypass Path

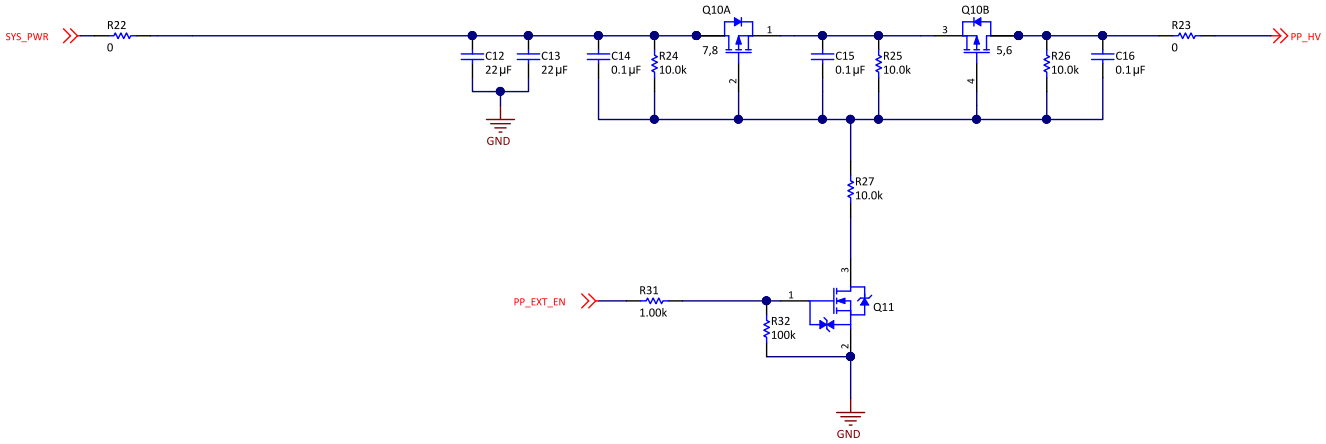


Figure 12. External Bypass Path

The TIDA-050012 reference design features an external bypass path using two PFET transistors. The bypass path is enabled once a 20 V PD contract has been entered. This would allow for the 20 V barrel jack source to be directly passed through to the PPHV pins of the TPS65987D to minimize the loss through the LM3489 DC/DC Convertor. Figure 12 highlights the schematic of the external PFET path used for this application.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

To fully test the TIDA-050012 board, the following items are required:

1. Windows PC with TPS6598x Application Customization Tool installed
2. TIDA-050014 Companion TI-Design board
3. High Current Type-C Cable
4. 230 W Barrel Jack Connector or High Powered Bench Supply capable of sourcing 20 V at 10 A
5. E-load or resistive load

3.1.1 Hardware

For use of this design, a high powered power source is required. The power source must be able to source at least 20 V at 10 A.

3.1.2 Software

The TPS6598x Application Customization Tool must be installed on the Windows PC used to interface with this design.

3.2 Testing and Results

3.2.1 Test Setup

The following sections will highlight how to program the TIDA-050012 board using the TIDA-050014 board. This section will also cover how to use this board, what each button does, and what each LED indicates.

3.2.1.1 Programming the TIDA-050012 Board

The utilities tool can be found by going to the TPS65987D product page on TI.com, which is at the following link. From there click the tools and software tab, and then click the link for the TPS6598x Configuration Tool.

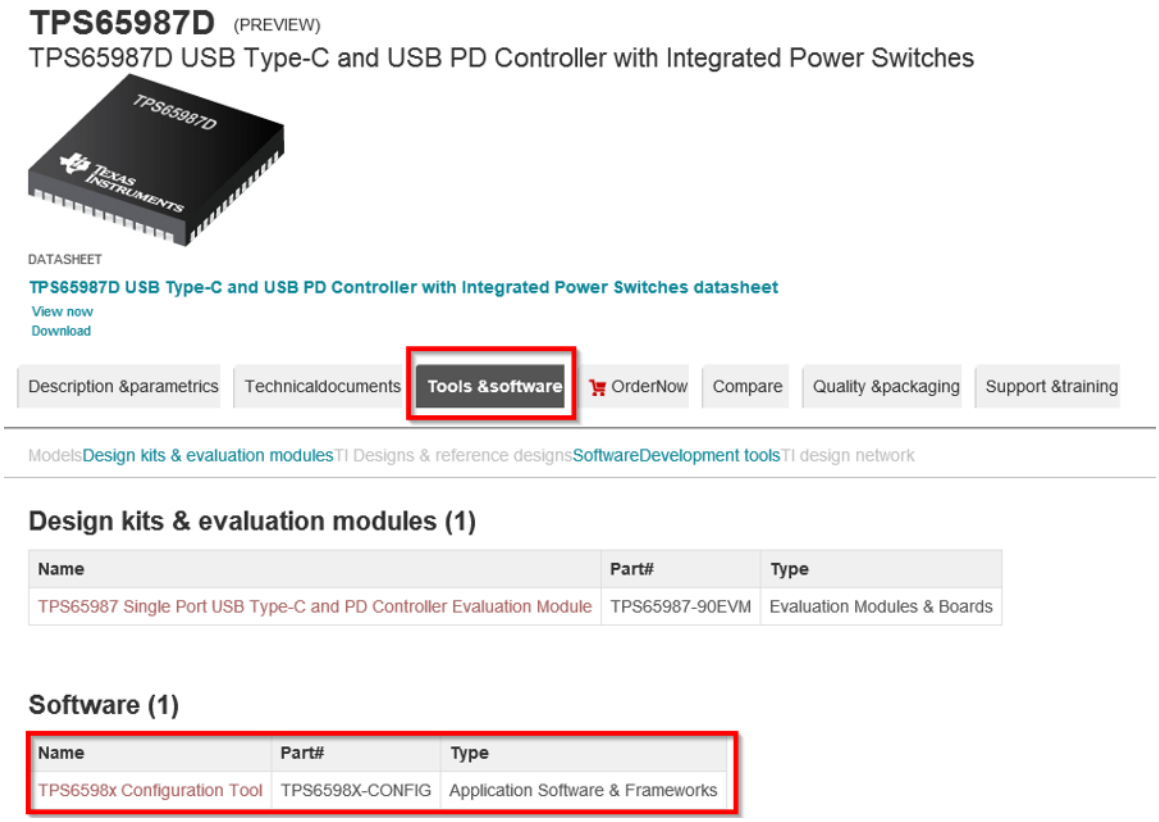


Figure 13. TPS65987D Product Page

From there, click the link next to TPS6598x-CONFIG that says “Get Software”. You will then have to fill out some information to get the link to the software download.

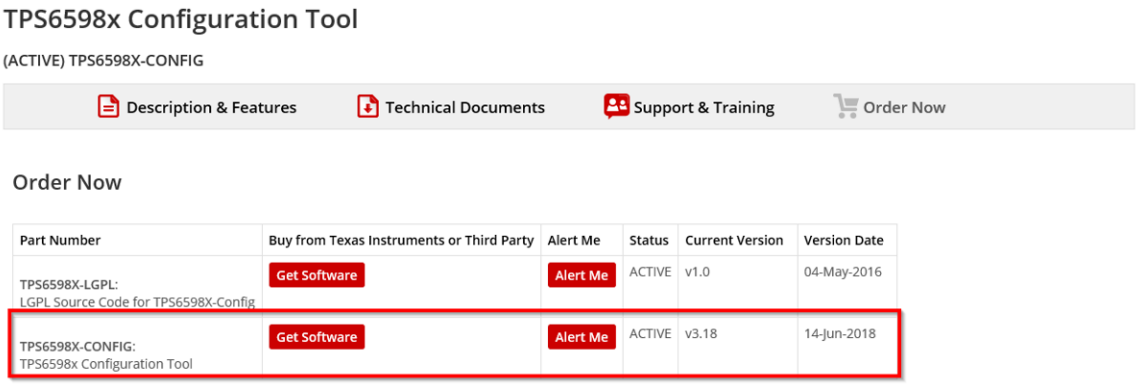


Figure 14. TPS6598x-Config Download Page

Once the download link has been clicked, you will be brought to a window for a 32 bit and 64 bit executable. Depending on the system you are using, click the correct executable. The executable will open, which will look like the following image.

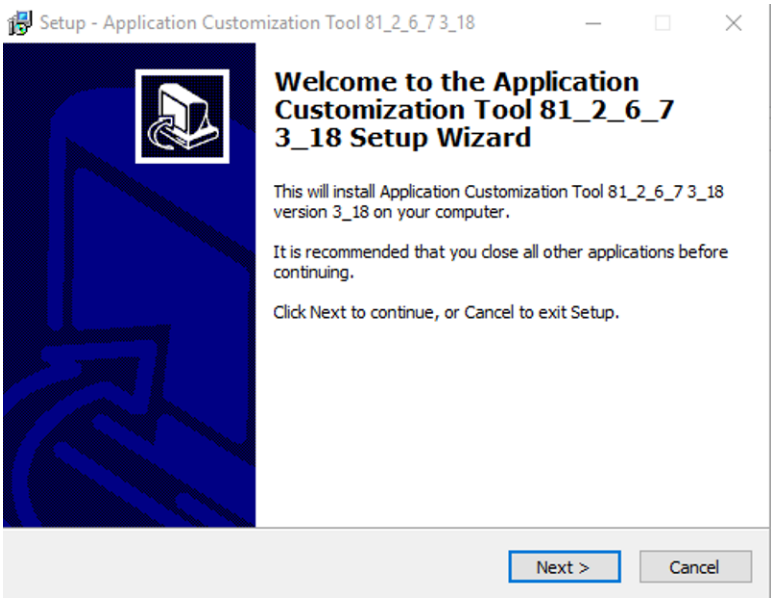


Figure 15. TPS6598x-Config Installation

Once the configuration tool has been downloaded, the program file for the source board will be flashed. This is done by first plugging in the barrel jack to power the source board, and then using a micro-usb to Type-A cable, connect the FTDI to a laptop for programming. Make sure that the jumper J202 is connected to SRC (right two pins). The cable connections and LEDs for this set up are shown below.

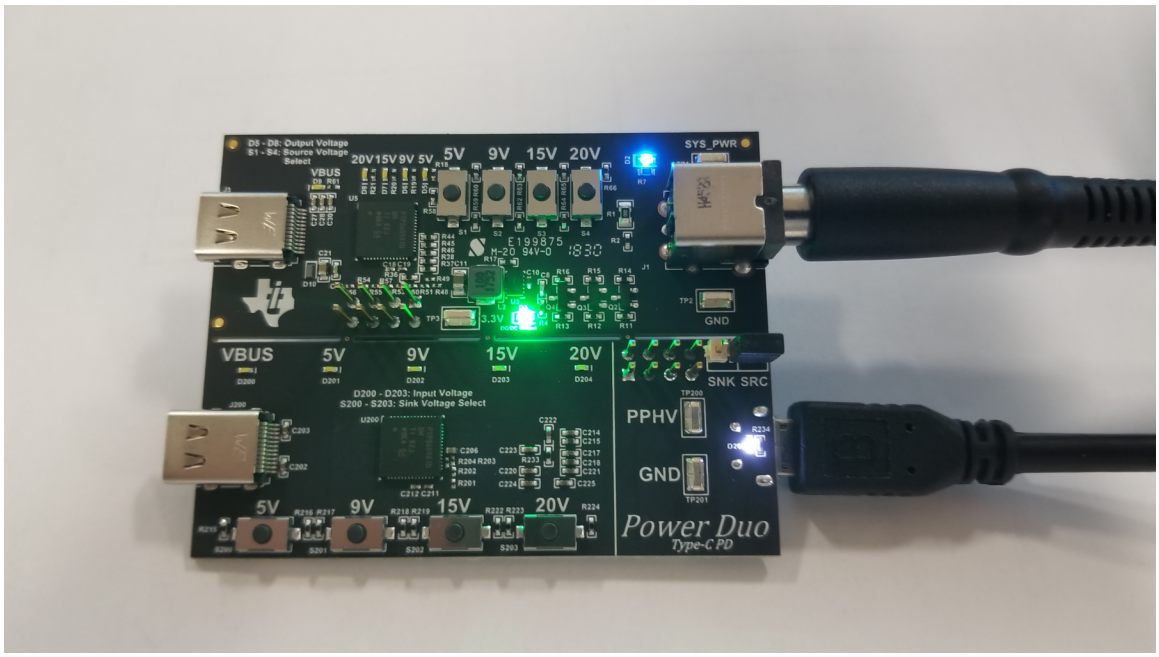


Figure 16. TIDA-050012 Source Board Programming

The next step is to flash the source.bin file onto the TIDA-050012 board. This is done by clicking the Binary tab, and then Flash from Binary File.

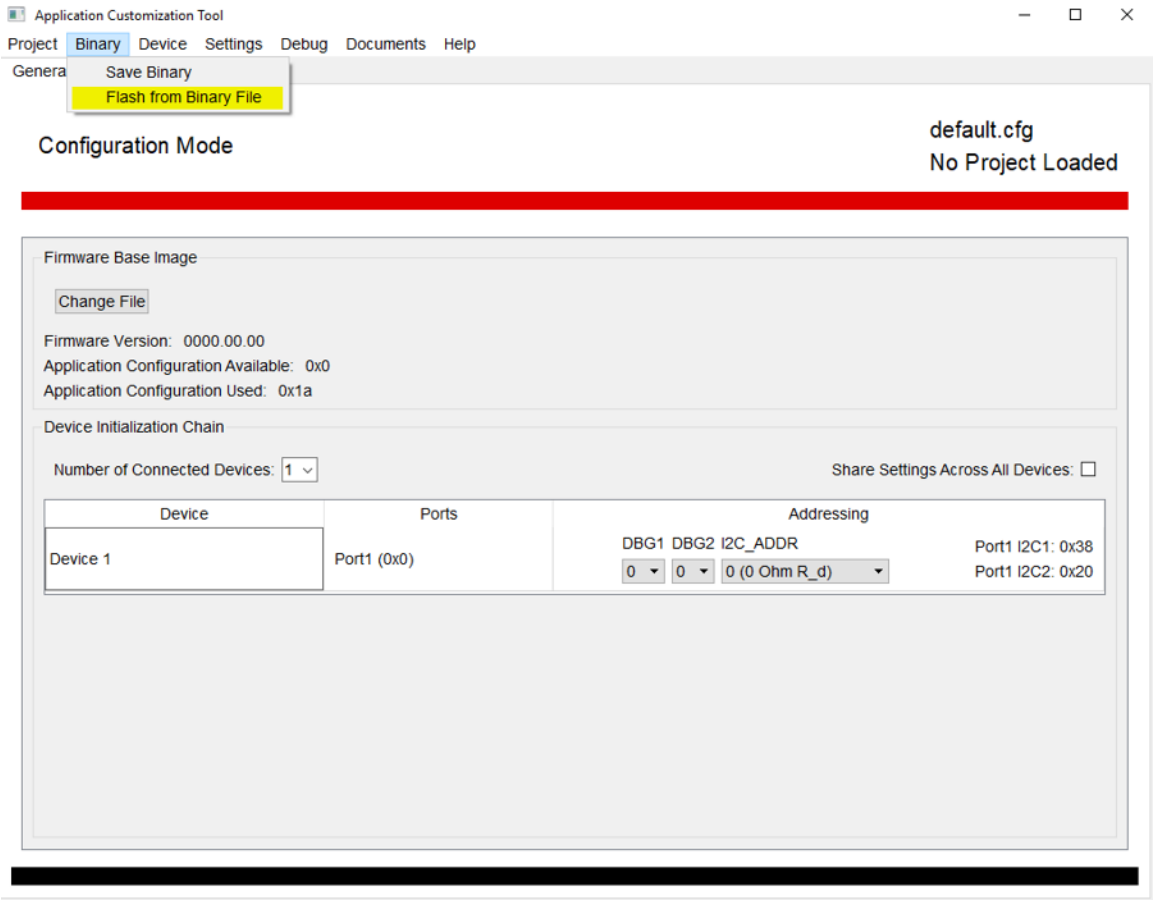


Figure 17. Flash From Binary File

From there, you will have to change the USB SPI Adapter from Aardvark to FTDI. Then click the change file button, and load the sink.bin file to be flashed. Press OK, and the file will begin flashing onto the EVM.

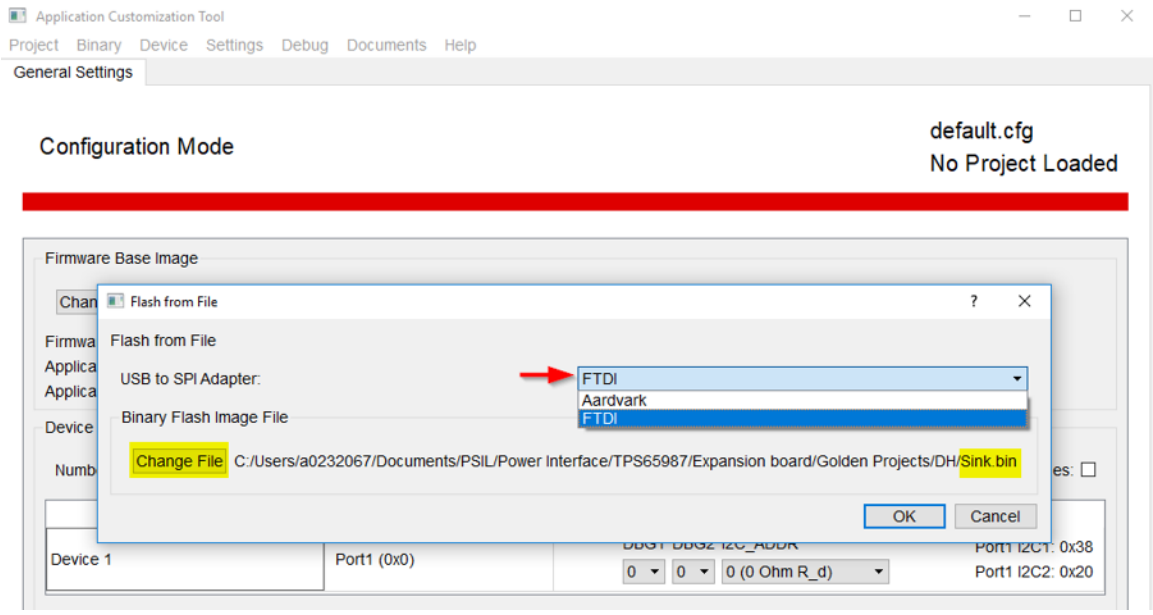


Figure 18. USB to SPI Adapter

Once this file has been flashed onto the source board, unplug the Micro-USB cable and then the barrel jack from the PCB. Move the jumper on J202 from the SRC setting to the SNK setting. Plug the barrel jack back in, and the image should be loaded onto the TIDA-050012 PD controller. Next, using a Type-C to Type-C cable, power the sink board from the source board. The cable connections and LEDs for this set up are shown in Figure 19.

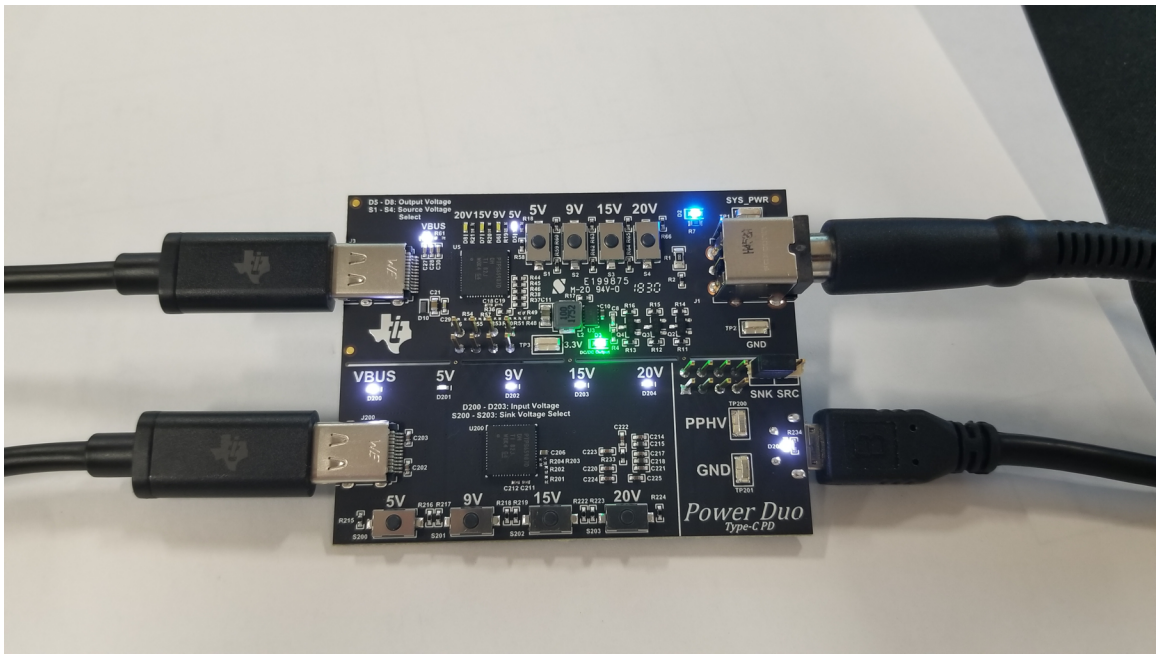


Figure 19. TIDA-050014 Programming

Next, the sink board program file needs to be flashed. You will follow the same setup as with the Source board, but instead of flashing source.bin you will flash sink.bin. Make sure that the header on J202 is now the SNK side (left two pins).

Once the binary file has been flashed, unplug the micro-usb and the barrel jack. Plug the barrel jack back in, and the image should not be loaded onto the TIDA-050014 PD controller. The LEDs should look similar to the image below.

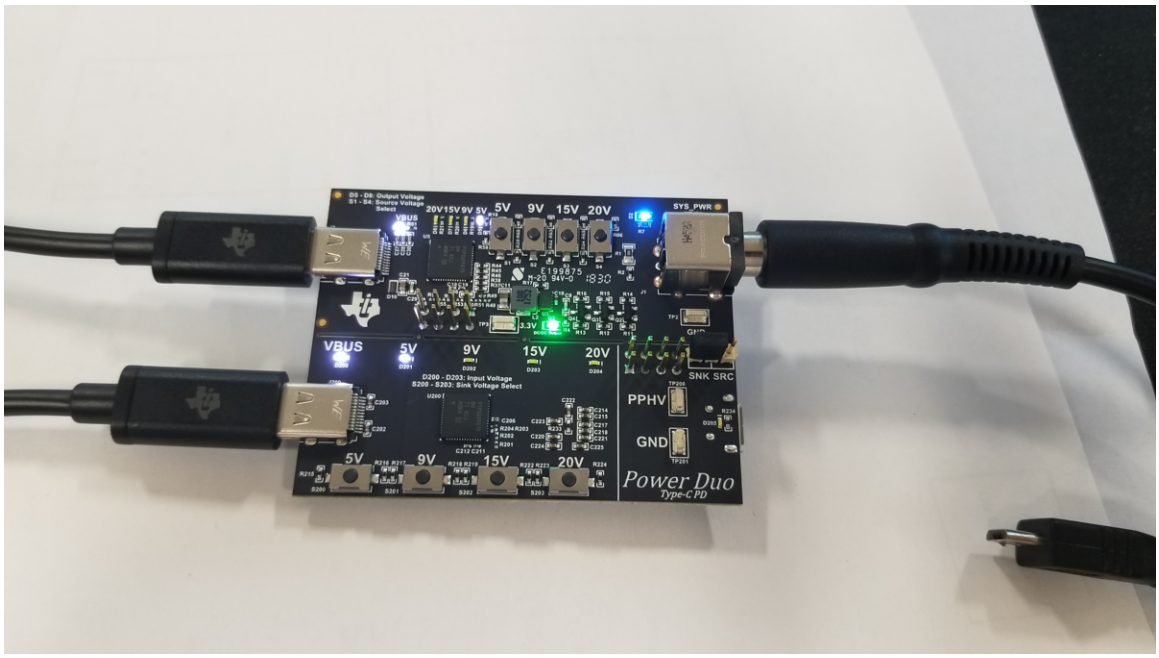


Figure 20. TIDA-050012 and TIDA-050014 Boards Programmed

NOTE: The TIDA-050012 and TIDA-050014 boards will come preprogrammed out of the box. If you would like to change any of the configurations, you can do so by using the TPS6598x Application Customization Tool and following the above mentioned steps.

3.2.1.2 Setting up the TIDA-050012 Board with a PD Device

To use the TIDA-050012 board, first connect a barrel jack supply to J1. This will power the device and get it ready for use. Once the device is powered, you can connect any Type-C PD device to it through a Type-C Cable. Upon initial connection, the TIDA-050012 board will only output 5 V on VBUS. This will be indicated through D5 being on. This LED is also labeled "5 V" in the silkscreen for clarity. If the attached sink device supports more than 5 V, you can use the push button switches S1 through S4 to select a higher voltage. S1, S2, S3, and S4 are labeled 5 V, 9 V, 15 V, and 20 V respectively in the silkscreen. If the attached sink device supports the voltage of the button pressed, it will negotiate the higher voltage and increase VBUS.

3.2.2 Test Results

The following sections will highlight the performance of the TIDA-050012 design.

3.2.2.1 RDSon

The effective RDSon was measured using Power Duo mode and in normal operation. The results are highlighted in Table 3 and Table 4. Each measurement was taken with various currents going through VBUS. The boards were left for 5 minutes before the voltage drop across the power path was measured to allow for the drop to reach a steady state.

Table 3. Rds_{on} Power Duo Mode Measurements

VBUS Voltage (V)	VBUS Current (A)	Voltage Drop across Power Path (mV)	Effective RDSon (mOhm)
20	1.5	21.48	14.32
20	2	28.16	14.08

Table 3. Rds_{on} Power Duo Mode Measurements (continued)

VBUS Voltage (V)	VBUS Current (A)	Voltage Drop across Power Path (mV)	Effective RDSon (mOhm)
20	3	44.42	14.81
20	4	58.12	14.53
20	5	76.32	15.26
20	6	97.43	16.24
20	7	120.36	17.19
20	8	145.32	18.17
20	9	175.76	19.53
20	10	216.78	21.68

NOTE: It can be expected that actual RDS_{on} will be a few milli-ohms lower than the results above. The results above do NOT take into account cable or trace resistance. This is a board level measurement. Additional thermal management is required on the PCB if exceeding 7 A in Power Duo Mode.

Table 4. Rds_{on} Single Power Path Measurements

VBUS Voltage (V)	VBUS Current (A)	Voltage Drop across Power Path (mV)	Effective RDSon (mOhm)
20	1.5	44.22	29.48
20	2	56.89	28.45
20	3	86.12	28.71
20	4	119.78	29.95
20	5	158.74	31.75

NOTE: When using one power path, do not exceed 5 A of current as this exceeds the ratings of the device. Please see TPS65987D datasheet for more information.

From the results above, it can be seen that the Power DUO Mode RDS_{on} is about half of the single power path RDS_{on}. This can be modeled as two FETs in parallel. The effective RDS_{on} when two of the same FETs are in parallel will be roughly half RDS_{on} of a single one.

3.2.2.2 VBUS Short to Ground in Power Duo Mode

Since the TIDA-050012 design will always be a power source, it needs to be able to protect against VBUS shorts to ground. The TPS65987D has been strenuously tested when operating using a single power path. These results can be found in the TPS6587D Power Path Performance and Protection application note.

This section will highlight how the TPS65987D performs when it is in Power Duo mode and there is a VBUS short to ground event. Note that the current on VBUS will spike higher when in Power Duo mode but the power paths should open just as quickly as when a single power path is used. The results of a VBUS short to ground when VBUS is 5 V is shown in Figure 21. The current through VBUS spikes to about 18 A and the power paths are able to open in about 20 us.

Figure 21. TIDA-050012 Hard Short at 5 V

Next, VBUS was raised to 9 V and then shorted to ground. The results of this test can be seen in Figure 22. Here, the current rises to about 28 A and the power paths are able to open in less than 20 us.

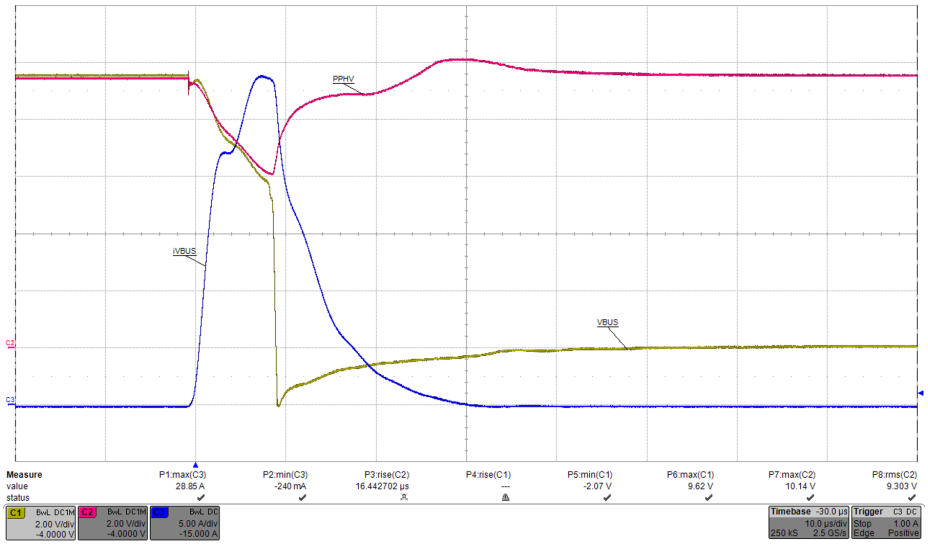


Figure 22. TIDA-050012 Hard Short at 9 V

VBUS was then increased to 15 V and shorted to ground. The results are highlighted in Figure 23. Here the current on VBUS spikes to about 34 A and the power paths are able to open in under 10 us.

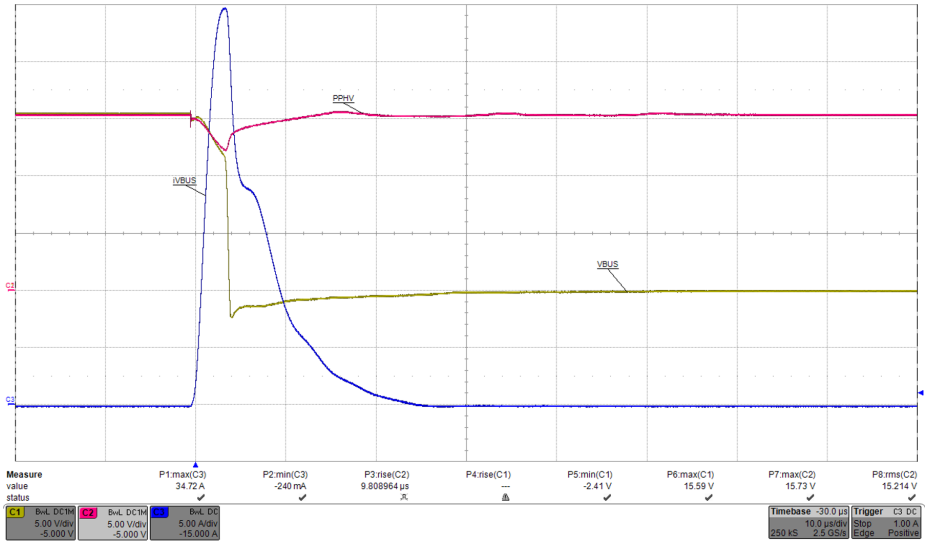


Figure 23. TIDA-050012 Hard Short at 15 V

Finally, VBUS was increased to 20 V and then shorted to ground. A VBUS short to ground with 20 V on VBUS is the most difficult to protect against since the current will spike very fast. The results of this test can be seen in Figure 24. The current spikes to about 43 A and the power paths are able to open in under 10 us to protect the system.

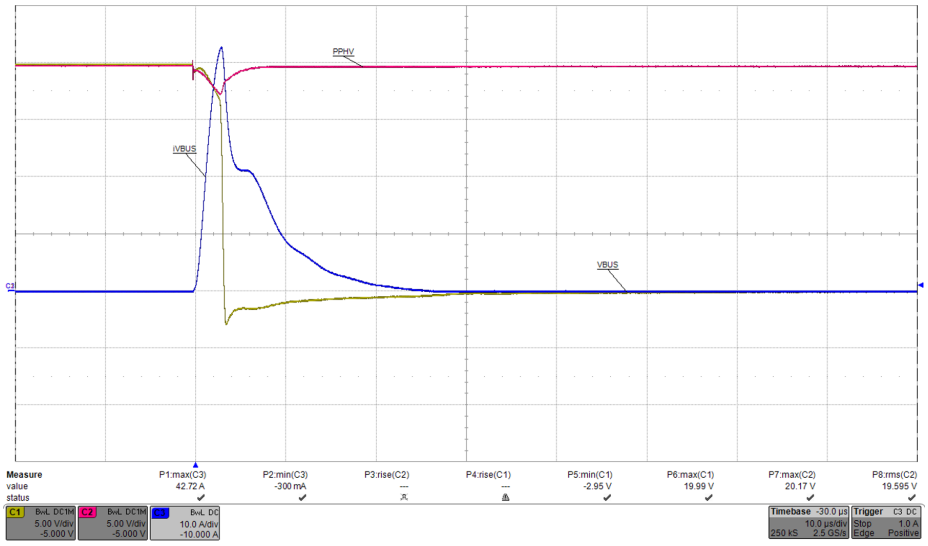


Figure 24. TIDA-050012 Hard Short at 20 V

3.2.2.3 200 W Over Type-C PD using Power Duo Mode

Once Texas Instruments' Power Duo mode is enabled, the TPS65987D closes both of its power paths and is able to carry up to 10 A over the USB Type-C connector. Figure 25 highlights an oscilloscope capture where the TIDA-050012 board is sourcing almost 200 W over the Type-C cable.

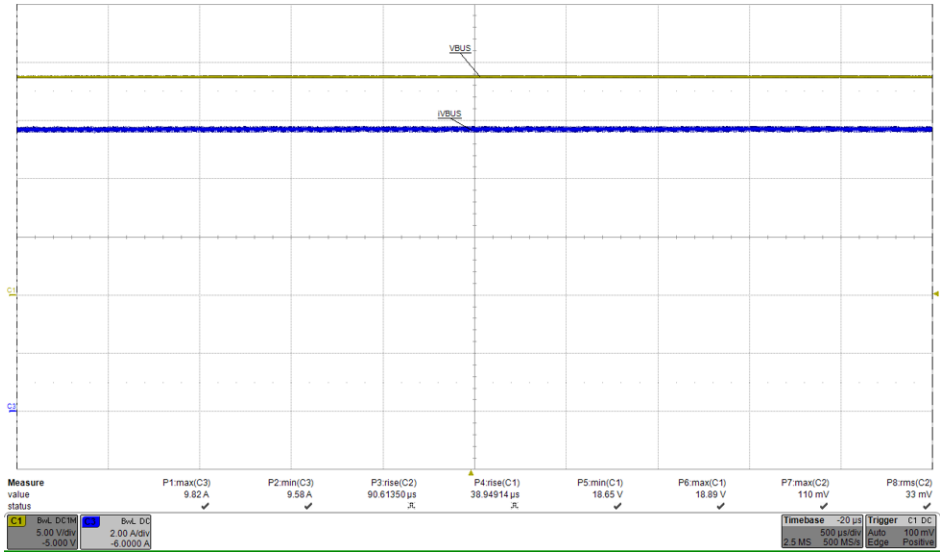


Figure 25. TIDA-050012 Outputting 20 V at 10 A

3.2.2.4 Efficiency

The efficiency of the TIDA-050012 board was measured to see how efficient the LM3489 asynchronous buck controller would regulate the Type-C PD VBUS output voltage. Figure 26 highlights the efficiency plot of the TIDA-050012 board with the different Type-C PD output voltages. The Y-axis of the plot highlights the efficiency in percentage and the X-axis represents the current load on the TIDA-050012 board. 20 V is the most efficient as it is directly passing the input voltage to VBUS through the external bypass path highlighted in Section 2.4.4.

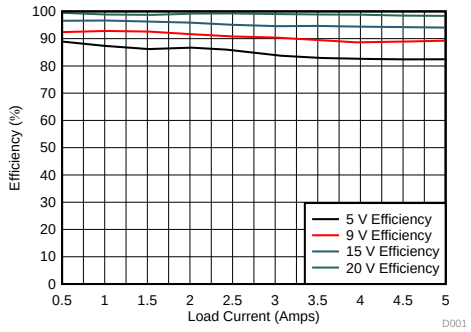


Figure 26. TIDA-050012 Efficiency

3.2.2.5 Power Loss

By using the results of the efficiency test, the power loss could be calculated at the different Type-C PD voltages. This is highlighted in Figure 27.

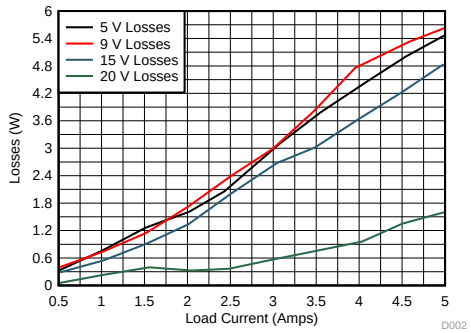


Figure 27. TIDA-050012 Power Loss

3.2.2.6 Voltage Regulation

The output voltage of the TIDA-050012 board was measured at different system loads at all 4 system output voltages. Figure 28, Figure 29, Figure 30, and Figure 31 highlight the voltage regulation for 5 V, 9 V, 15 V, and 20 V respectively.

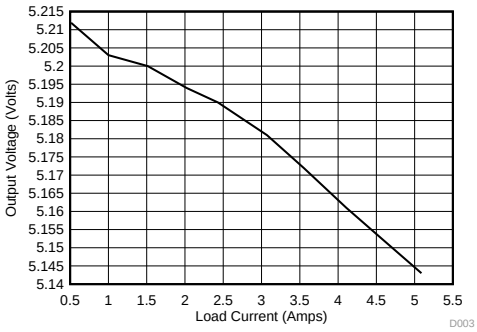


Figure 28. TIDA-050012 Voltage Regulation 5 V

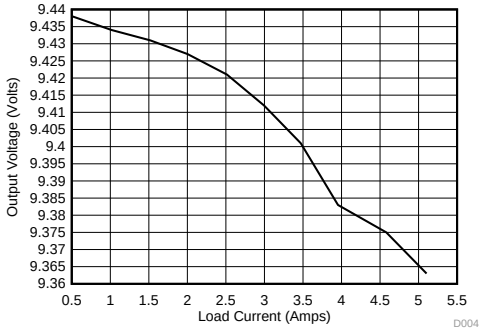


Figure 29. TIDA-050012 Voltage Regulation 9 V

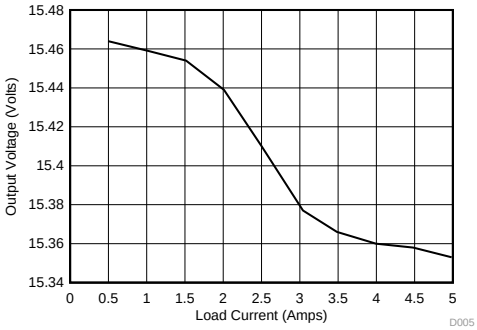


Figure 30. TIDA-050012 Voltage Regulation 15 V

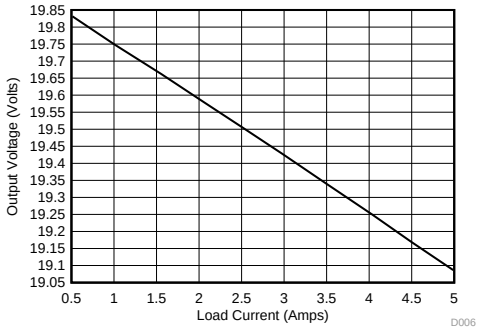


Figure 31. TIDA-050012 Voltage Regulation 20 V

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050012.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050012.

4.3 PCB Layout Recommendations

When designing a PCB that will carry high currents, it is crucial to ensure that enough copper is added into the high current paths of the PCB. For this design, the high current nets would be the nets connecting to the PPHV and VBUS pins of the TPS65987D. It is recommended to use a PCB layout calculator to find out how much copper to use given your design parameters.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050012.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-050012.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050012.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050012.

5 Software Files

To download the software files, see the design files at TIDA-050012.

6 Related Documentation

1. *TPS65987DDH Power Path Performance and Protection*

6.1 Trademarks

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7 Terminology

The terminology used in this design guide is all related to the USB Type-C and PD specifications. These specifications can be downloaded from the USB-IF website.

8 About the Author

Eric Beljaars is an Applications Engineer for Texas Instruments where he is responsible for supporting USB Type-C and PD controllers. Eric earned his bachelor of science in electrical engineering (BSEE) from The University of Oklahoma in Norman, OK.

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