TI Designs: TIDA-01537

Scalable Automotive HEV/EV 6s to 96s Lithium-Ion Cell Supervision Demonstrator Reference Design

Description

This reference design is a small-sized cell supervision demonstrator design for a centralized battery management system (BMS). Its configurable capacitive isolation daisy-chain solution enables monitoring and protecting cells ranging from 6-series to 96-series, which allows its use in BMS systems ranging from 24 V to 400 V. In hybrid or electric vehicles (HEV/EVs), a high-voltage lithium-ion battery stores the energy required for traction and housekeeping. The lithium-ion cells in the battery must be monitored while charging and discharging. This design provides a solution for monitoring lithium-ion cell voltages accurately and communicating the data externally via various interfaces such as CAN and bqStudio.

Resources

TIDA-01537	Design Folder
BQ79606A-Q1	Product Folder
TPS65381A-Q1	Product Folder
TMS570LS0432	Product Folder
TPS57160-Q1	Product Folder
TCAN1042HGV-Q1	Product Folder
ISO7742-Q1	Product Folder
SN6501-Q1	Product Folder

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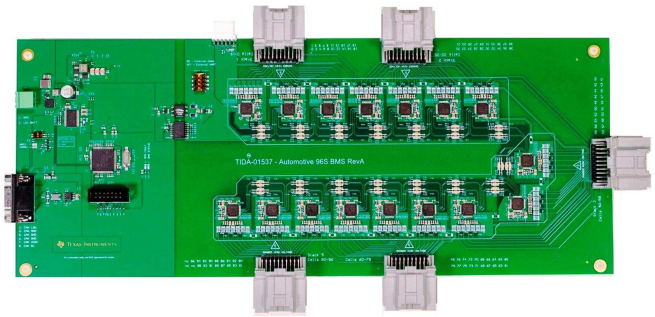
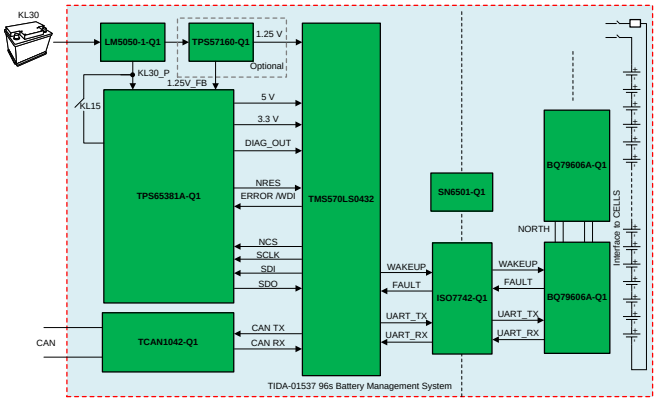
Features

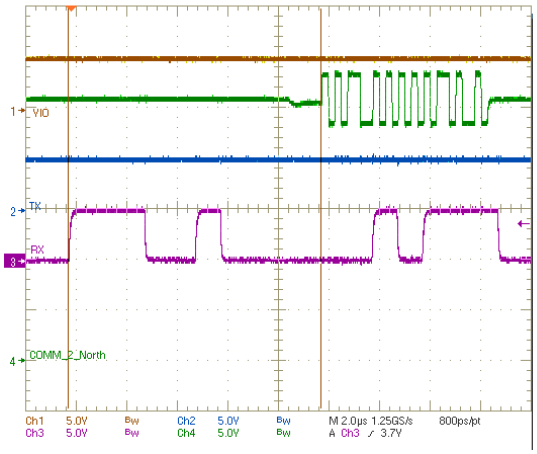
- Scalable cell supervision circuits from 6s to 96s
- Accurate cell voltage measurements
- Onboard PMIC diagnosis
- Onboard BQ79606A-Q1 diagnosis
- Onboard capacitive isolation
- Robust hot-plug performance
- 500 kbps external CAN communication

Applications

- HEV/EV Battery Management System
- Industrial Energy Storage Systems



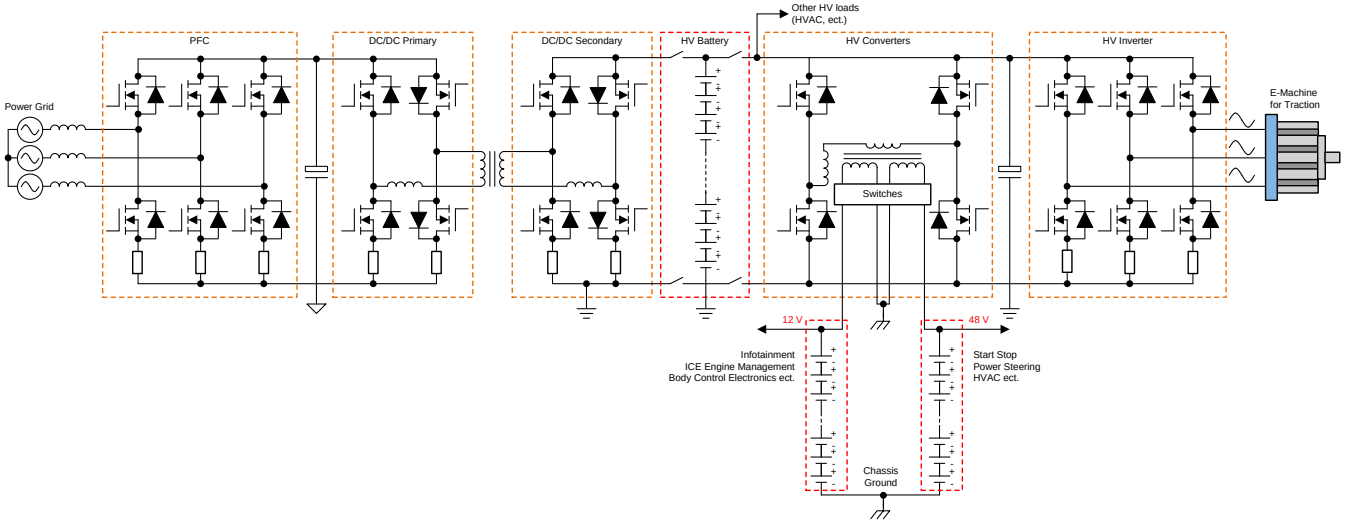




1 System Description

In response to the latest changes in global environmental conditions and efforts to reduce greenhouse gases, there is a need to have hybrid or electric traction units, which have very low or zero emissions. In a hybrid electric vehicle (HEV) or electric vehicle (EV), high-voltage batteries are used as storage elements to power the wheels. Onboard chargers or external DC converters are used to source the power, and high-voltage lithium-ion batteries are used to store that energy. DC/DC converters and motor control inverters are used to power the wheels and other subsystems such as heating, ventilating, and air conditioning (HVAC). All of these subsystems work on high voltages.

Figure 1. Battery Managements Systems in HEV/EV



The reliability of an electric powertrain is mainly dependent on its battery pack and inverter. DC/DC conversion and onboard charging support the structures for power transfer in a powertrain system. The battery cells and management systems play important roles in handling the reliability of the electric vehicle.

Mileage is one of the critical parameter in selling an electric vehicle. It can be accurately calculated by knowing the state of charge (SOC) and state of health (SOH) of your battery. Lithium-ion cells need to be closely monitored for accurate calculation of SOC and SOH. Voltage, temperature and current measurements are critical for SOC and SOH algorithms. Irrespective of type of algorithms such as coulomb counting, impedance spectroscopy, OCV, and others, voltage and current measurements of the cells are key parameters. Based on the type of chemistry used, all lithium-ion cells have operating voltage window. Overvoltage and undervoltage of the cells are key parameters that must be monitored closely during charging and discharging of the battery pack. Any deviation in the specification will hamper the health of the cells and battery pack. If there is a deviation in monitoring the battery cell voltages, it will impact the calculated driving range and safety of the vehicle.

Communication of battery management system integrated chips plays an important role in maintaining the integrity of signal and communicating the data of all cells to the main controller. Robust communication from top of the cell to the main controller is important to have the safety integrity in operation of the system. Battery management ICs need to have the capability to communicate down to the last cell in the stack. The communication of the system must be robust for all the dynamics of the electric vehicle. Critical reliability parameters such as hot plug, bulk current injection, and isolation strength are considered for daisy-chain communication while selecting a battery management integrated circuit.

The controller of the battery management system must maintain the algorithms to ensure the appropriate SOC and SOH of the battery pack. Communication must be established with external powertrain end equipment such as the inverter, DC/DC converter, onboard charger, and vehicle control units. This external communication is typically established using the CAN interface, and depending on the electric vehicle, there may be a need for more than one CAN interface.

1.1 Key System Specifications

Table 1. Key System Specifications

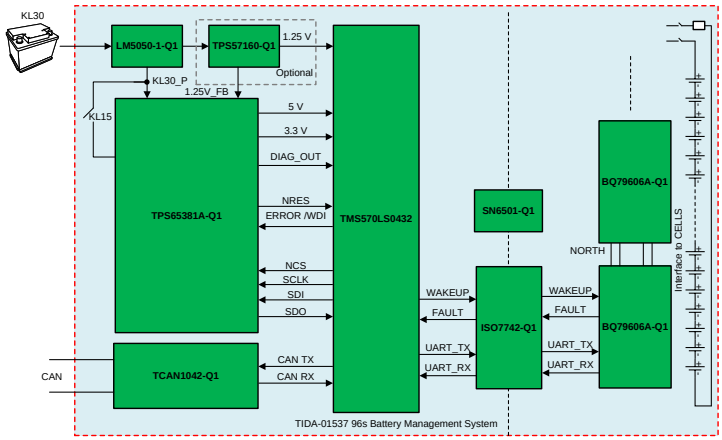
PARAMETER	SPECIFICATIONS	TYPICAL VALUE	UNITS
Daisy-chain delay of BQ79606A-Q1	South to north (room temperature)	3.26	µs
UART to daisy-chain delay	Start of daisy chain communication delay (room temperature)	6.28	µs
BQ79606A-Q1 shutdown-mode leakage current	Shut down mode (room temperature)	48.99(1)	µA
BQ79606A-Q1 sleep-mode leakage current	Sleep mode (room temperature)	144.47(1)	µA
BQ79606A-Q1 active-mode operating current	Active mode (room temperature)	6.4(1)	mA
1.25-V turn on delay	Delay from IGN high to > 90% of 1.25 V	23.52	ms
VDD5V and VDD3.3V Delay	Delay from IGN high to >90% of VDD5V and VDD3.3V	16.73	ms
Delta temperature in BQ79606A-Q1	Balancing current 150 mA, 10 minutes of continuous balancing for odd and even cells	25.6	°C

(1) Leakage current data shown here is measurement data on TIDA-01537, load conditions of LDO of BQ79606A-Q1 will have an impact on total leakage and operating currents.

2 System Overview

2.1 Block Diagram

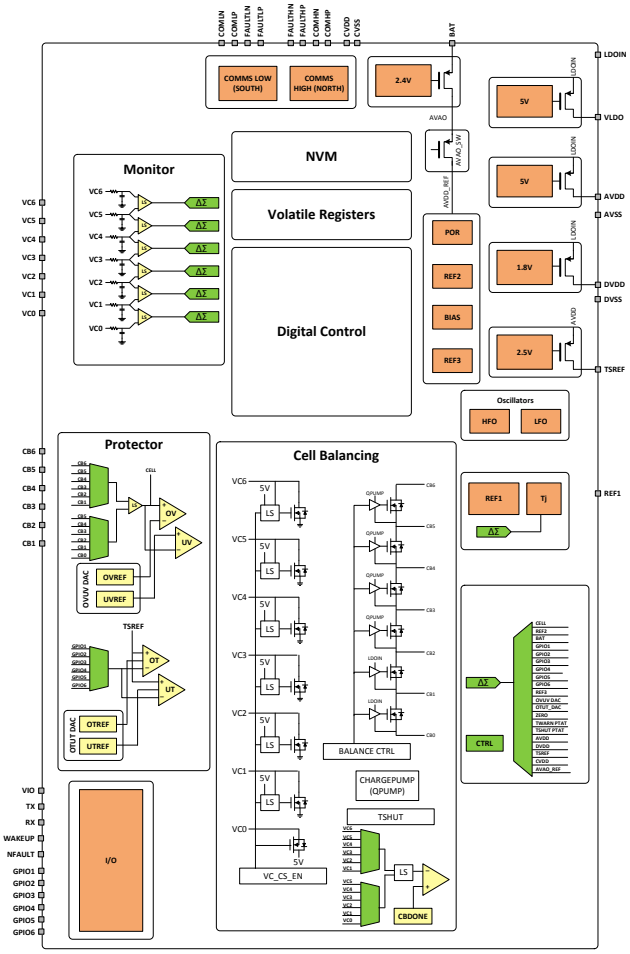
Figure 2. TIDA-01537 Block Diagram



2.2 Highlighted Products

2.2.1 BQ79606A-Q1

Figure 3. BQ79606A-Q1 Block Diagram



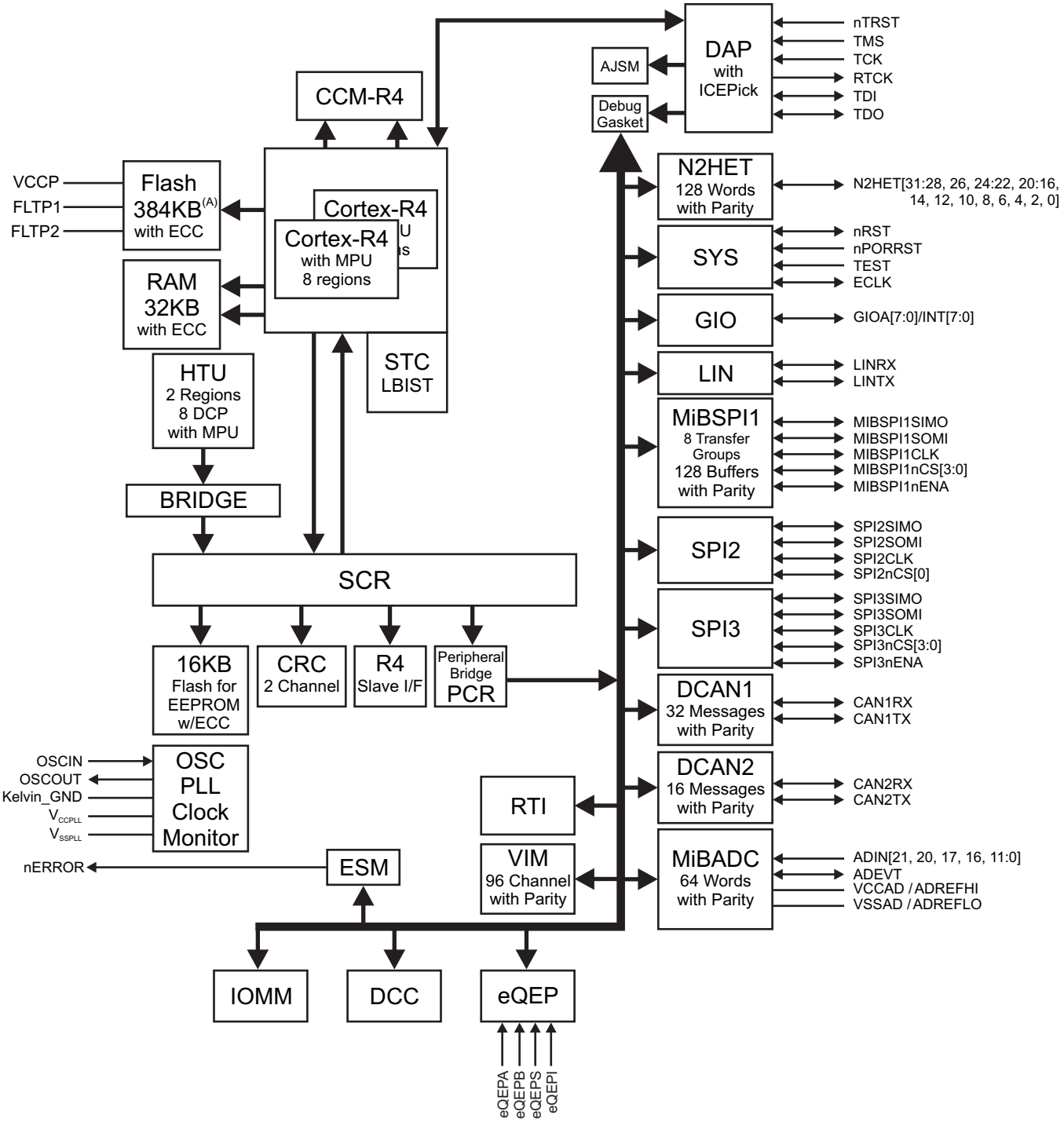
The BQ79606A-Q1 device provides simultaneous, high accuracy, channel measurements for three to six battery cells. With the inclusion of a daisy chain communication port, the BQ79606A-Q1 device is stack able (up to 51 devices) to support the large stack configurations found in battery packs for electrified automotive drive trains. Providing a Delta Sigma converter per cell input, the BQ79606A-Q1 allows simultaneous measurement of the battery voltages, providing a true snapshot of the voltage of the cells.

BQ79606A-Q1 features:

- Highly-accurate cell voltage measurements
- Monitor and communication functions: SafeTI™-26262 ASIL-D compliant
- Integrated cell-balancing MOSFETs up to 150 mA
- Integrated high-voltage AFE filter components
- Designed to pass BCI testing

2.2.2 TMS570LS0432

Figure 4. TMS570LS0432 Block Diagram



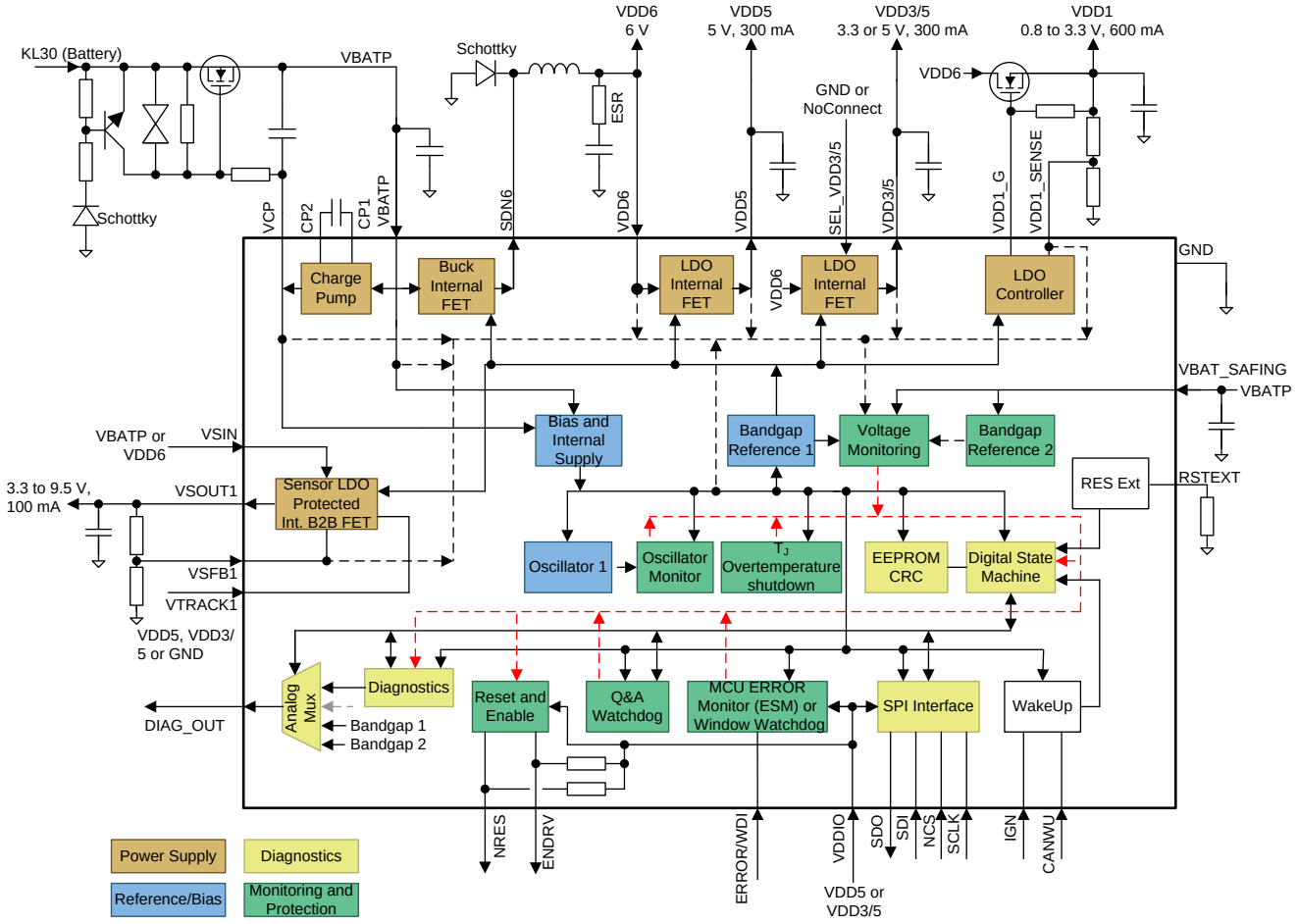
The TMS570LS0432 device is a high-performance automotive-grade micro controller for safety-relevant systems. The safety architecture includes dual CPUs in lockstep, CPU and Memory BIST logic, ECC on both the flash and the data SRAM, parity on peripheral memories, and loopback capability on peripheral I/Os. The CPU offers an efficient 1.66 DMIPS/MHz, and has configurations that can run up to 80 MHz, providing up to 132 DMIPS. The device supports the big-endian (BE32) format

TMS570LS0432 features:

- ARM® Cortex® R4 32-bit RISC CPU
- Dual CPUs Running in lockstep
- Error-signaling module with error pin
- Frequency-Modulated Phase-Locked Loop (FMPLL) With built-in slip detector
- Two CAN controllers (DCANs)
- Next generation high-end timer (N2HET) module

2.2.3 TPS65381A-Q1

Figure 5. TPS65381A-Q1 Block Diagram



The TPS65381A-Q1 device is a multi-rail power supply designed to supply micro controllers (MCUs) in safety-relevant applications. The TPS65381A-Q1 device integrates multiple supply rails to power the MCU, controller area network (CAN), or FlexRay, and an external sensor. An asynchronous-buck switch-mode power-supply converter with an internal FET converts the input supply (battery) voltage to a 6-V pre-regulator output. This 6-V pre-regulator supplies the other regulators 5 V, 3.3 V, and adjustable core supply. The device supports wake up from IGNITION or wake up from the CAN transceiver.

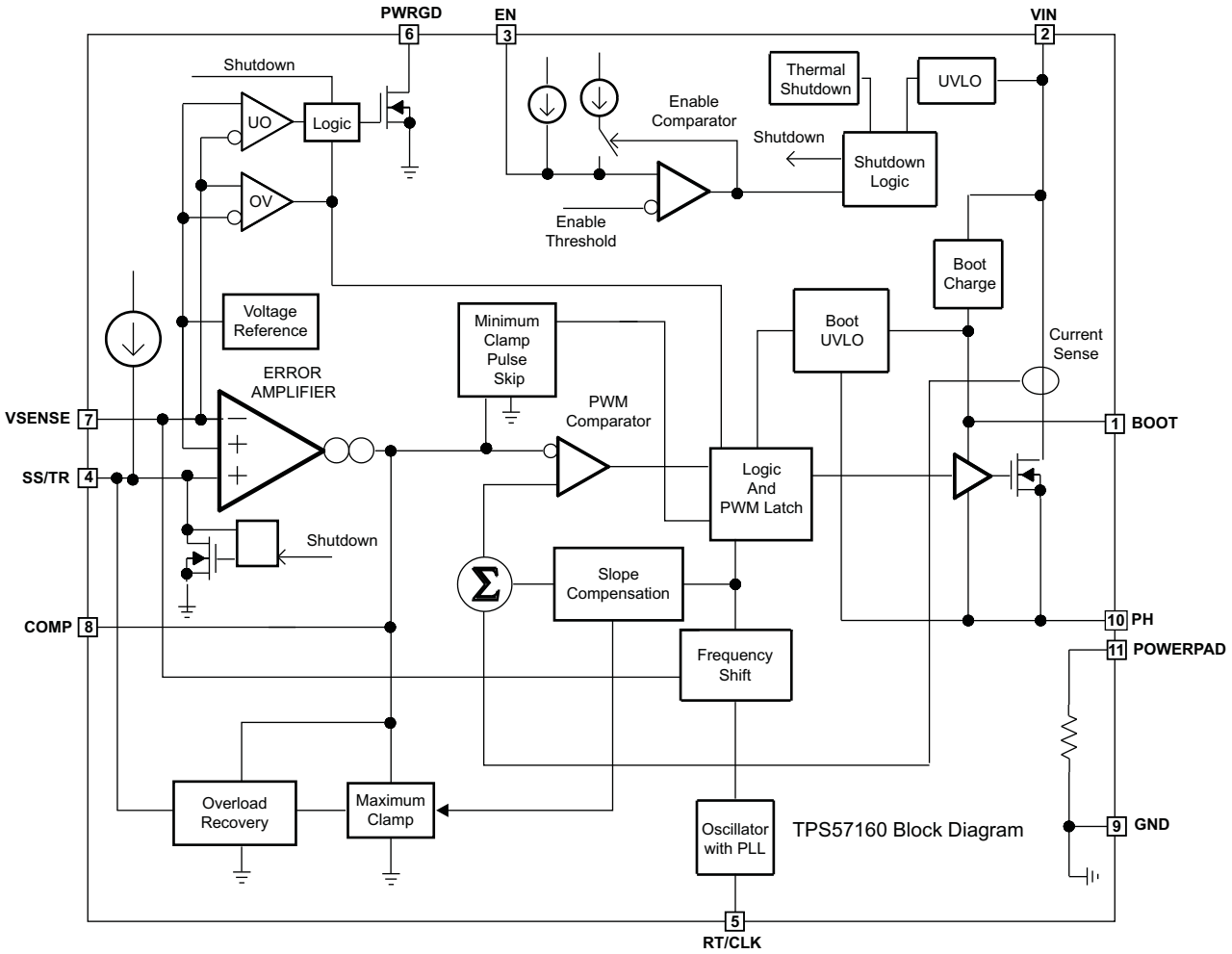
TPS65381A-Q1 features:

- 6-V asynchronous switch mode pre regulator with internal FET, 1.3-A output current
- Charge pump: Typically 12 V above battery voltage
- Independent undervoltage and overvoltage monitoring on all regulator outputs, battery voltage, and internal supplies
- All supplies with internal FETs protected with current-limit and over temperature shutdown
- Watchdog: Trigger mode (OPEN, or CLOSE window) or question and answer mode

- Diagnostic output pin allowing MCU to observe through a multiplexer internal analog and digital signals of the device

2.2.4 TPS57160-Q1

Figure 6. TPS57160-Q1 Block Diagram



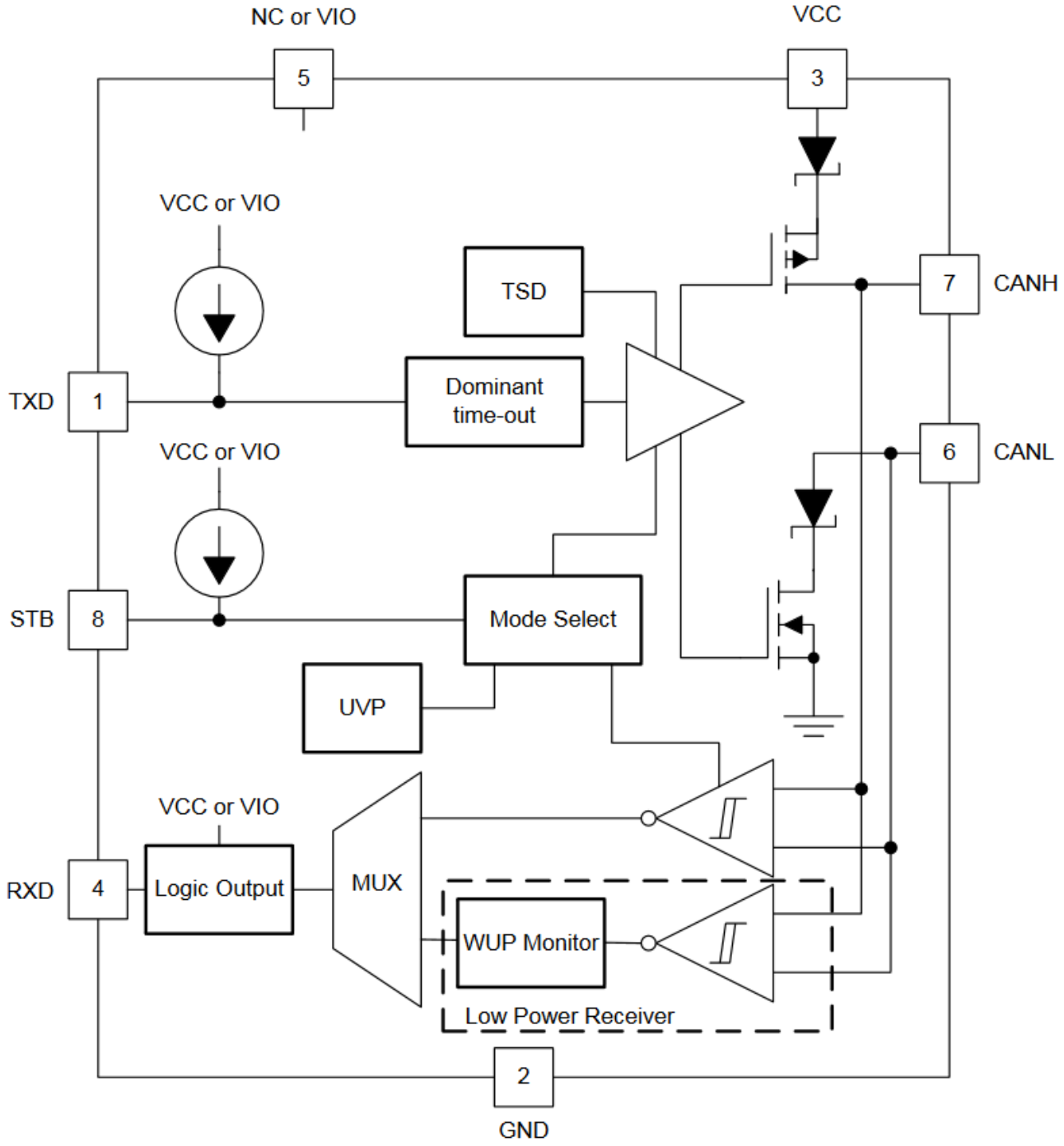
The TPS57160-Q1 device is a 60-V 1.5-A step-down regulator with an integrated high-side MOSFET. Current-mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the no load, input supply current to 116 µA. Using the enable pin, shutdown supply current is reduced to 1.5 µA. Undervoltage lockout is set internally at 2.5 V but can be increased using the enable pin. The output voltage startup ramp is controlled by the slow-start pin that can also be configured for sequencing or tracking. An open-drain power-good signal indicates the output is within 92% to 109% of the nominal voltage.

TPS57160-Q1 features:

- 3.5-V to 60-V input voltage range
- 200-mΩ high-side MOSFET
- 100-kHz to 2.5-MHz switching frequency
- Adjustable undervoltage lockout (UVLO) voltage and hysteresis
- Adjustable slow start, sequencing

2.2.5 TCAN1042-Q1

Figure 7. TCAN1042-Q1 Block Diagram



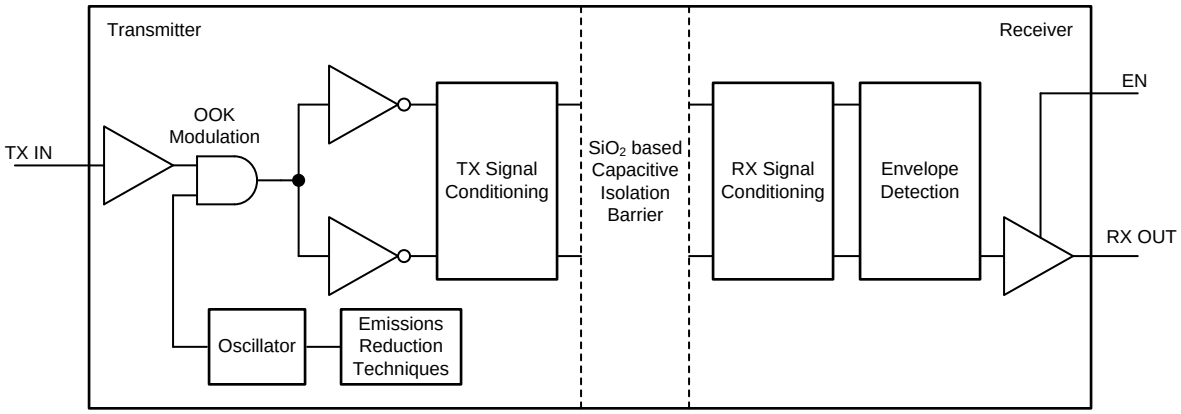
This CAN transceiver family meets the ISO11898-2 (2016) high-speed CAN physical layer standard. All devices are designed for use in CAN FD networks up to 2 Mbps (megabits per second). Devices with part numbers that include the "G" suffix are designed for data rates up to 5 Mbps, and versions with the "V" have a secondary power supply input for I/O level shifting the input pin thresholds and RXD output level. This family has a low power standby mode with remote wake request feature. Additionally, all devices include many protection features to enhance device and network robustness.

TCAN1042-Q1 features:

- I/O voltage range supports 3.3 V and 5 V MCUs
- Typical loop delay: 110 ns
- Ideal passive behavior when unpowered
- Bus fault protection: ±58 V (non-H variants) and ±70 V (H variants)
- Receiver common-mode input voltage: ±30 V
- Short and symmetrical propagation delay times and fast loop times for enhanced timing margin

2.2.6 ISO7742-Q1

Figure 8. ISO7742-Q1 Block Diagram



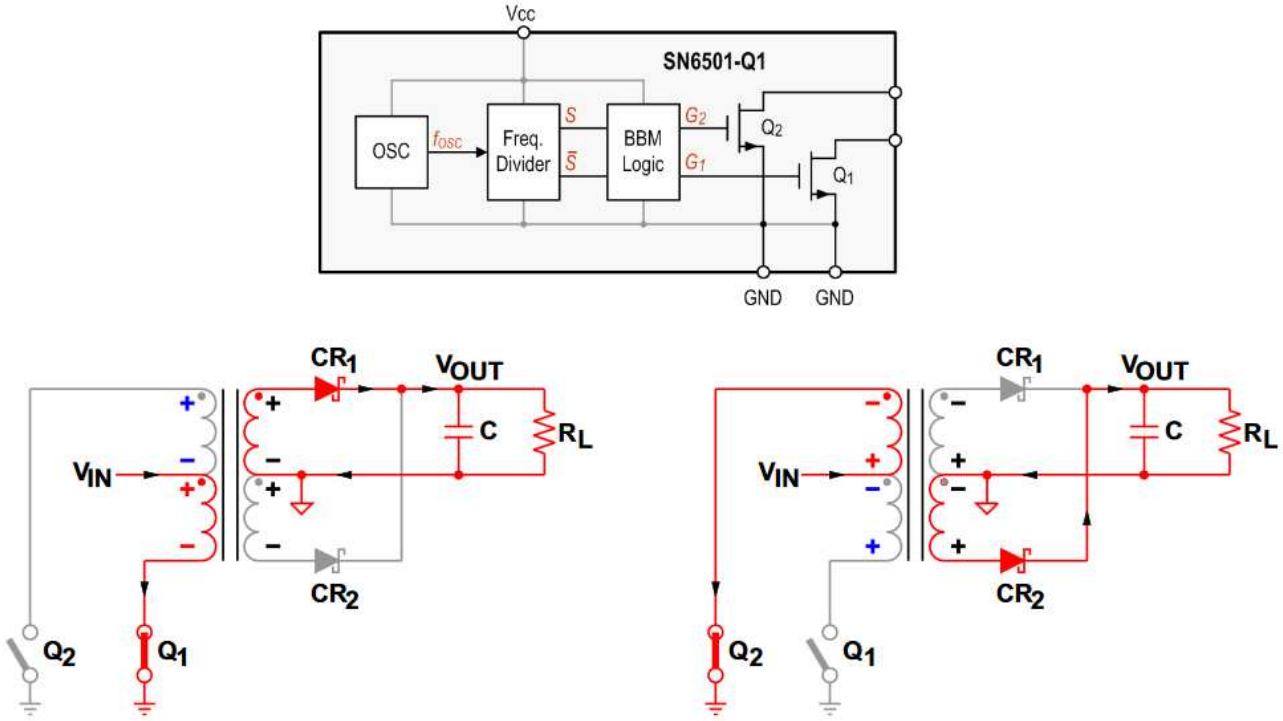
The ISO774x-Q1 devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by silicon dioxide (SiO2) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. The ISO7740-Q1 device has all four channels in the same direction, the ISO7741-Q1 device has three forward and one reverse-direction channels, and the ISO7742-Q1 device has two forward and two reverse-direction channels. If the input power or signal is lost, default output is high for devices without suffix F and low for devices with suffix F.

ISO774x-Q1 features:

- Signaling rate: Up to 100 Mbps
- Low propagation delay: 10.7 ns typical (5-V supplies)
- High CMTI: ±100 kV/µs typical
- Default output high and low options
- Isolation barrier life: > 40 years
- Wide-SOIC (DW-16) and QSOP (DBQ-16) package options

2.2.7 SN6501-Q1

Figure 9. SN6501-Q1 Functional Block Diagram



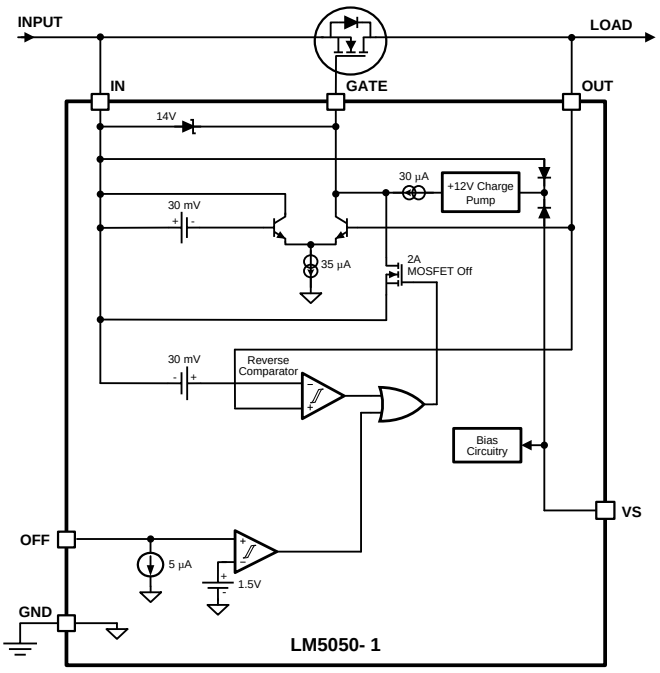
The SN6501-Q1 device is a monolithic oscillator, power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3-V or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on transformer turns ratio. The SN6501-Q1 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures break-before-make action between the two switches.

SN6501-Q1 features:

- Push-pull driver for small transformers
- 5-V supply: 350 mA (Max)
- 3.3-V supply: 150 mA (Max)
- Low ripple on rectified output permits small output capacitors
- Small 5-pin SOT-23 package

2.2.8 LM5050-1-Q1

Figure 10. LM5050-1-Q1 Block Diagram



The LM5050-1-Q1 high-side ORing FET controller operates in conjunction with an external MOSFET as an ideal diode rectifier when connected in series with a power source. This ORing controller allows MOSFETs to replace diode rectifiers in power distribution networks thus reducing both power loss and voltage drops. The LM5050-1/-Q1 controller provides charge pump gate drive for an external N-Channel MOSFET and a fast response comparator to turn off the FET when current flows in the reverse direction. The LM5050-1 and LM5050-1-Q1 can connect power supplies ranging from 5 V to 75 V and can withstand transients up to 100 V.

LM5050-1-Q1 features:

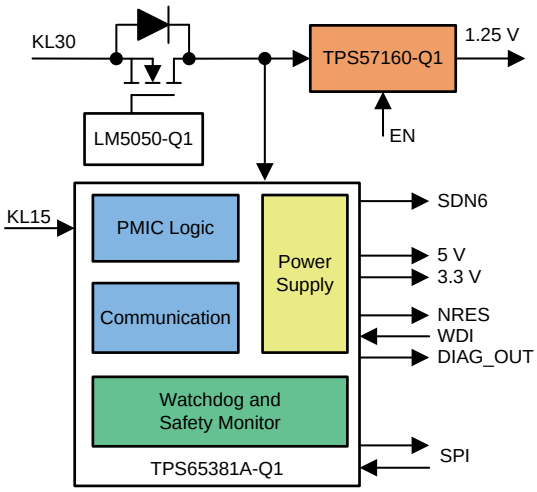
- 2-A peak gate turnoff current
- Fast 50-ns response to current reversal
- Minimum VDS clamp for faster turnoff
- Available in standard and AEC-Q100 qualified versions LM5050Q0MK-1 (up to 150°C T_J) and LM5050Q1MK-1 (up to 125°C T_J)
- Package: SOT-6 (thin SOT-23-6)

2.3 System Design Theory

2.3.1 Input Power

Every electronic unit working on the KL30 (12-V battery positive) line needs to have input power protection for all transients the specific to vehicle, OEM. The TIDA-01537 design has only reverse polarity protection, see TIDA-01167 for more info on input battery protection circuits.

Figure 11. TIDA-01537 Input Power

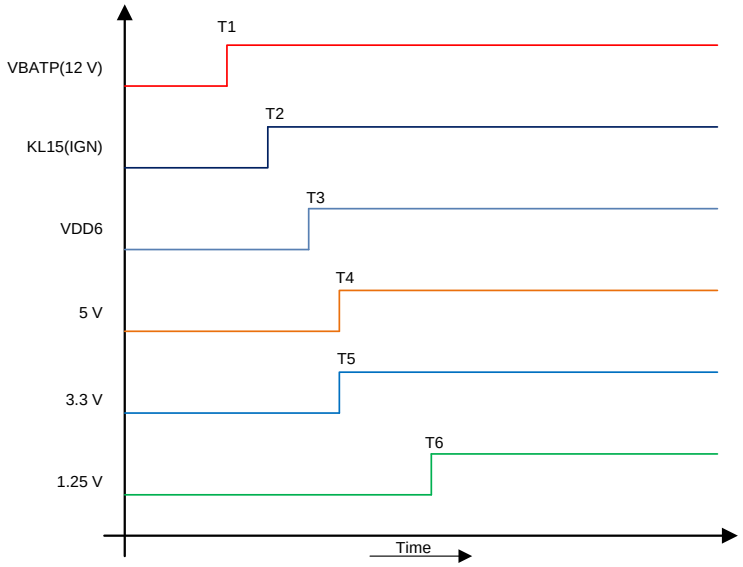


In the LM5050-1-Q1 device, a high-side MOSFET controller is used to support reverse-polarity protection. The LM5050-1-Q1 device has an internal charge pump and VDS monitor to support the application. There is a need to place a diode in a forward direction in between the GND of the LM5050-1-Q1 to the KL31 (battery ground). Choose the MOSFET based on the maximum load current from KL30. In the TIDA-01537 design, there are no power-hungry loads such as power relays, solenoids, and motors. Adopt the input power structure based on the maximum load and protection requirements such as peak transients, reverse polarity, and jump start conditions.

DC/DC (VDD6) from the TPS65381A-Q1 device can supply a maximum output current of 1.5 A–2.5 A. TPS65381-Q1 LDOs can generate 5 V, 3.3 V, and core voltage (1.x V). VDD5 supports up to 300 mA, the configurable LDO VDD3/5 can drain up to 300 mA maximum. The core supply is critical to most of the control units, the TPS65381A-Q1 device can support up to 600 mA. The TPS57160-Q1 is used to support microcontrollers which require more than a 600-mA core supply.

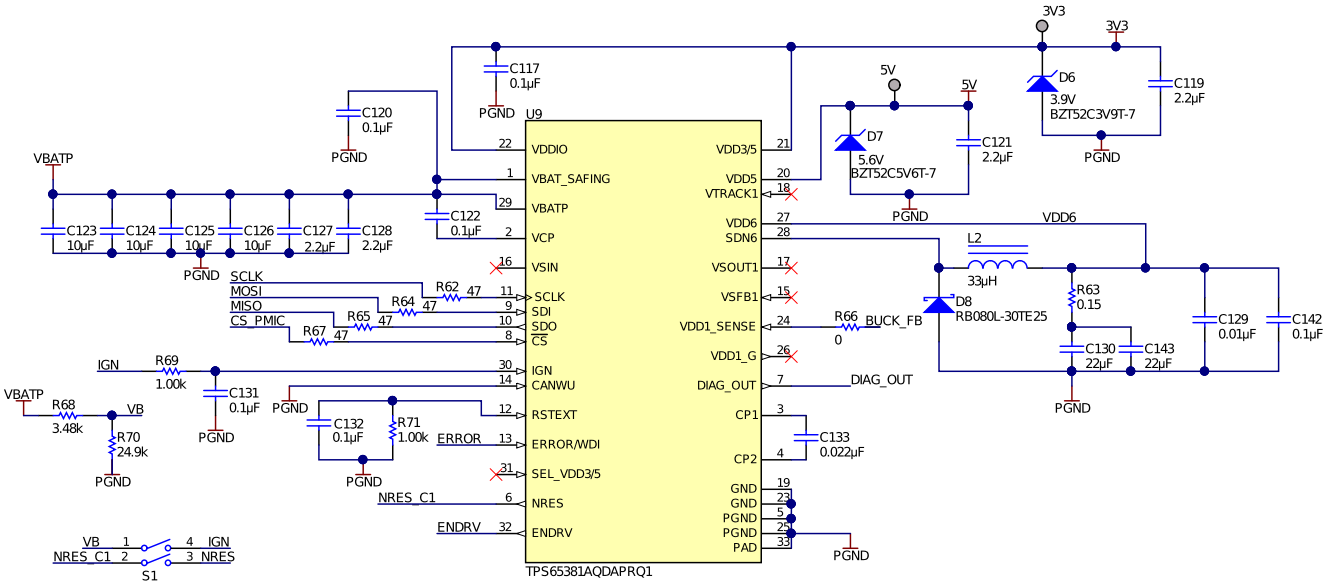
Figure 12 shows is the input power sequence on the 12-V side.

Figure 12. TIDA-01537 Input Power Sequence



T1 is the input power turned ON, with permanent supplied systems, VBATP is always 12 V. T2 is the ignition input to the TIDA-01537 or the battery management system. When the T2 is turned ON, the internal PMIC logic turns ON the internal high-side switching regulator for VDD6. The T3-T2 time delay mainly depends on the internal logic which is typically < 1 ms. T4 and T5 are mostly the same, 5 V and 3.3 V output starts ramping up once VDD6 is greater than its undervoltage threshold level. The typical delay of T4, and T5 from T3 mainly depends on VDD6 regulation. Typically, T2 to T5 should be less than 5 ms. The 3.3-V supply is used to enable the TPS57160-Q1 which starts regulating to generate the 1.25-V core supply. Based on the slow start, and frequency settings of the TPS57160-Q1, there is a typical delay of 5 ms (configurable and changes based on load) from T5 to T6.

Figure 13. TPS65381A-Q1 Schematic



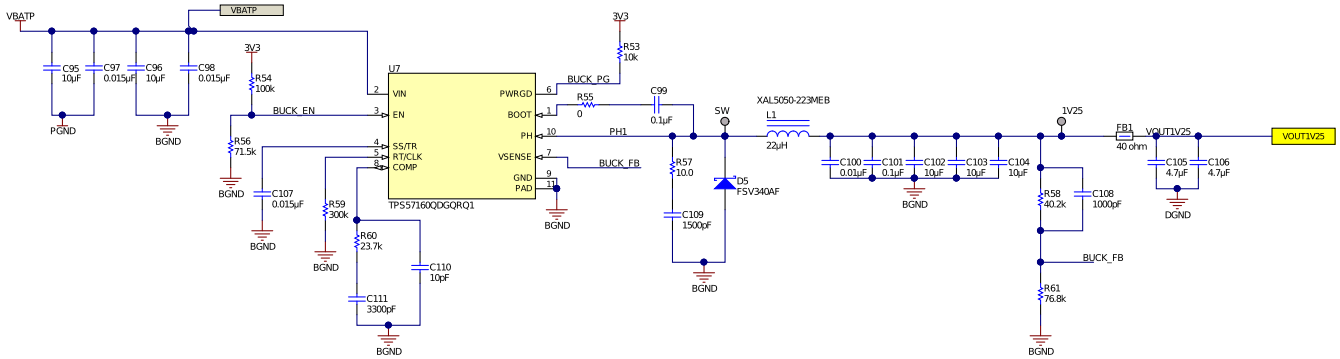
Switch S1 is used to emulate the ignition behavior onboard. The CAN wakup feature is not used in the TIDA-01537 design.

The TPS65381A-Q1 is a PMIC that generates regulated output voltages and plays an important role in handing the power sequence of electronic control units. It monitors and generates undervoltage and overvoltage flags for each output. Error flags can be multiplexed, or configured to generate a fault signal. The TPS65381A-Q1 has an independent voltage reference to monitor the output voltage, which also has a glitch filter to ensure the actual undervoltage and overvoltage flag.

The VDD6 switch-mode power supply operates with fixed-frequency (approximately 440 kHz), adaptive on-time control PWM. The control loop is based on a hysteretic comparator. The internal N-Channel MOSFET is turned on at the beginning of each cycle if the sensed voltage on the VDD6 pin is below the hysteretic comparator threshold. When the MOSFET is turned on, it is on for a minimum of 7% duty cycle (7% of fclk_VDD6). This MOSFET is turned OFF when the hysteretic comparator detects a voltage on the VDD6 pin above the threshold. The VDD6 regulator may skip pulses if the output voltage remains above the hysteretic comparator when the clock edge occurs. When the MOSFET is turned OFF, the external Schottky diode, D8, recirculates the energy stored in the inductor for the remainder of the switching period. The VDD6 regulator enters dropout mode (100% duty cycle) for a supply voltage below approximately 7 V on the VBATP pin.

A low-ESR ceramic capacitor is required for loop stabilization for 5 V and 3.3 V. This capacitor must be placed close to the pin of the device. These outputs are protected against shorts to ground by a current-limit. These outputs also limit output voltage overshoot during power up and during line or load transients

Figure 14. TPS57160-Q1 Schematic



The TPS57160-Q1 device is used as a buck from the KL30 battery supply to the core voltage (1.25 V). The TPS57160-Q1 uses an adjustable fixed frequency, peak current-mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is compared to the high-side power switch current. When the power switch current reaches the level set by the COMP voltage, the power switch is turned OFF. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level. The Eco-mode™ is implemented with a minimum clamp on the COMP pin.

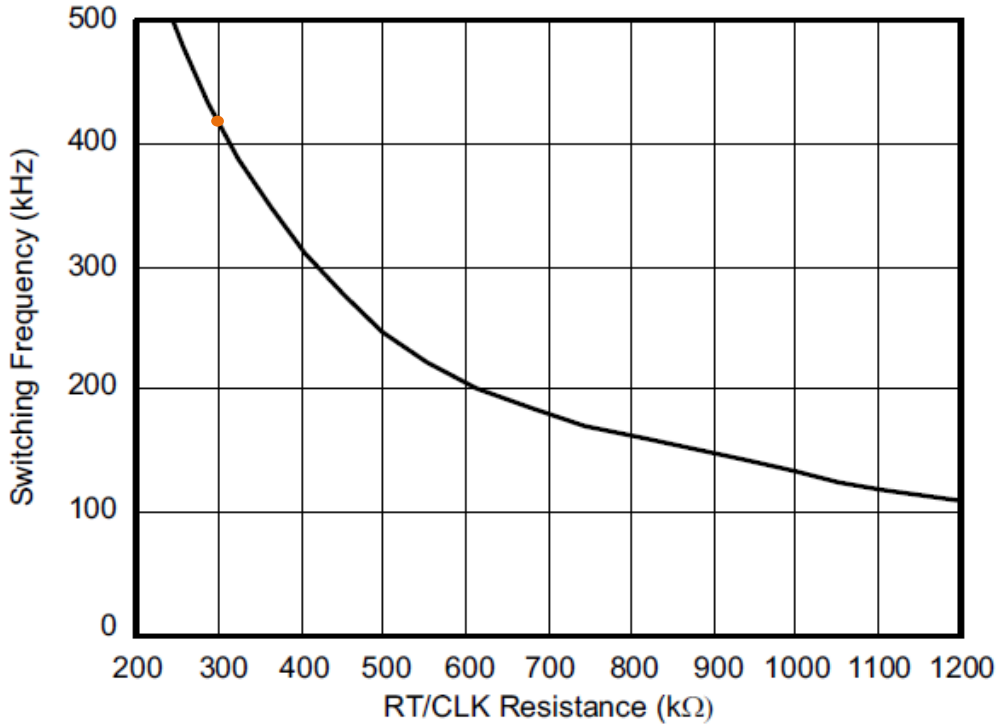
3V3 of TPS65381A-Q1 is used to enable the TPS57160-Q1, R54 and R56 are supporting potential divider to maintain enable threshold voltage of TPS57160-Q1 to be greater 1.25 V. The C107 capacitor is populated with 15 ηF which keep the slow start time approximately as 4.8 ms.

$$T_{SS\_U7} = \frac{C107 \times 0.8 \times V_{Ref\_U7}}{I_{SS\_U7}} \quad (1)$$

Use Equation 1 to calculate the slow start time, in vice versa it can also be used to set.

The resistor R59 is used to fix the frequency for U7. Figure 15 shows that if R59 is populated with 300 kΩ, the TPS57160-Q1 is operating at approximately 425 kHz.

Figure 15. CLK Setup TPS57160-Q1



Resistors R58 and R51 are the feedback potential divider resistors to set the output voltage. The TPS57160-Q1 has a trans-conductance amplifier for the error amplifier with an internal 0.8-V voltage reference. Tolerance of R58, R61 and internal voltage reference plays an important role in output voltage.

Components R60, C111, and C110 are populated to have type 2A compensation circuit. Values are populated to have a phase margin of 91.5° with a crossover frequency of approximately 34.67 kHz.

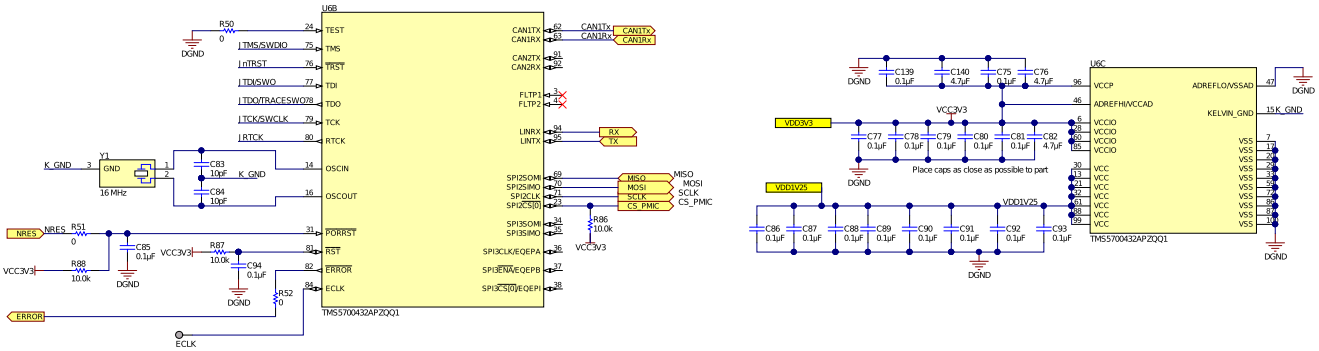
Power dissipation for the buck DC/DC converter mainly depends on load current and component selection. If the maximum load current is 500 mA ,the maximum input voltage is 18 V (excluding jump start). The power dissipation of the TPS57160-Q1 is around 50 mW. Significant power dissipation is seen in the forward diode, it can be around 200 mW where the forward diode drop is 0.4 V with an junction capacitance of 210 pF.

Choose L1 based on the frequency of operation, output ripple current, and maximum load (saturation current). Choose D5 because it has low power dissipation by having less junction capacitance with low forward voltage. The ESR of C102, C103, and C104 plays an important role in the output ripple of 1V25.

NOTE: See TPS65381A-Q1 and TPS57160-Q1 for more information of input power to electronic control units.

2.3.2 TMS570LS0432-Q1 and Interfacing Peripherals

Figure 16. TMS5700432A-Q1 Core Schematic



The TMS570LS0432/0332 device has 384KB and 256KB of integrated flash (respectively) and 32KB of data RAM. Both the flash and RAM have single-bit error correction and double-bit error detection. The flash memory on this device is a nonvolatile, electrically erasable, and programmable memory implemented with a 64-bit-wide data bus interface. The flash operates on a 3.3-V supply input (the same level as I/O supply) for all read, program, and erase operations. When in pipeline mode, the flash operates with a system clock frequency of 80 MHz. To operate the TMS570LS432-Q1 at 80 MHz, a Y1 16-MHz crystal oscillator with C83 and C84 load capacitors are placed with kelvin ground near to U6.

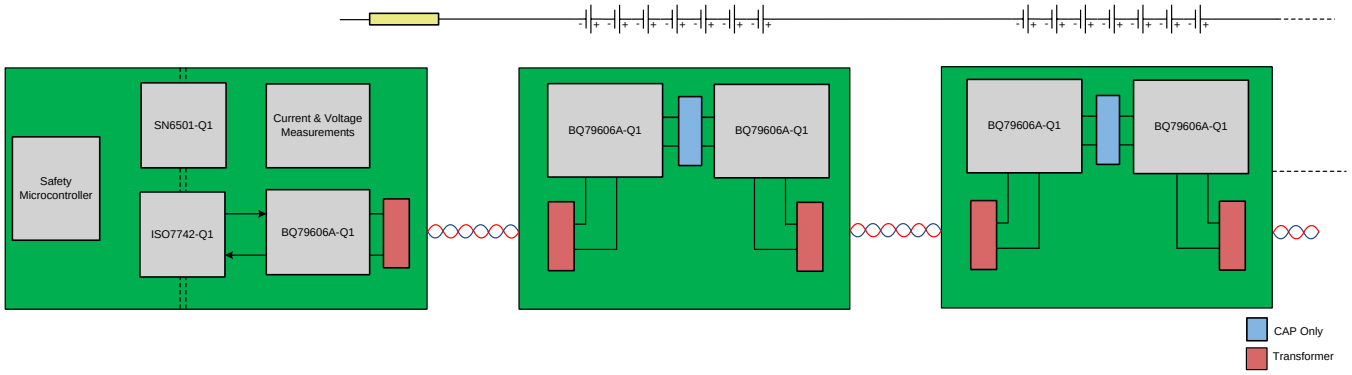
TPS65381A-Q1 is interfaced to TMS570LS432-Q1 with SPI for safety diagnosis. Follow *TPS65381A-Q1 Multirail Power Supply for Microcontrollers in Safety-Relevant Applications* and the TMS570LS432-Q1 data sheet for safety concepts when handling the system.

The BQ79606A-Q1 is interfaced with UART. More information for handling the TMS570LS432-Q1 is found in data sheet and safety manuals. Contact the local sales team for more information.

2.3.3 Interfacing BQ79606A-Q1

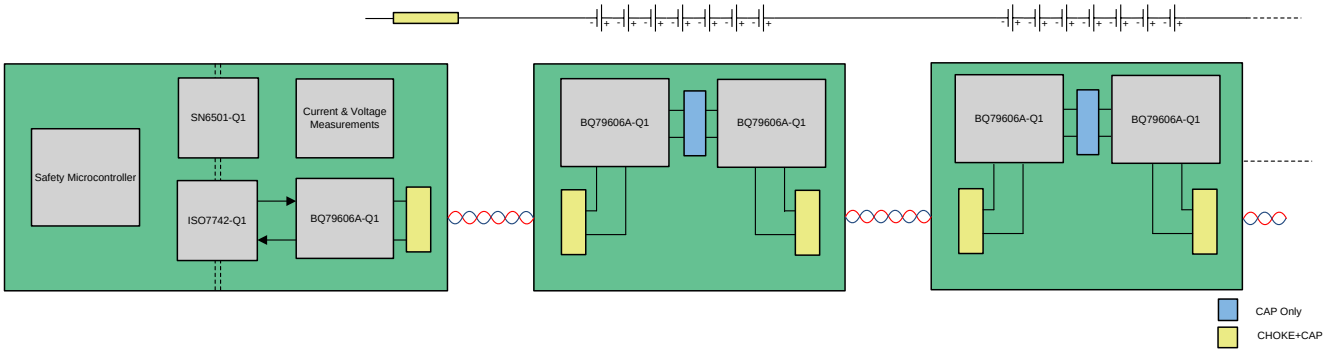
bq79606A-Q1 can support capacitor(CAP) isolation, it has capability to handle the isolation of onboard daisy chain communication. The BQ79606A-Q1 can be interfaced to the host controller and board-to-board in many ways. It depends on the overall architecture of the battery and isolation mechanism in the battery control units and cell supervision units.

Figure 17. Cell Supervision Units With CHOKE+CAP Isolation



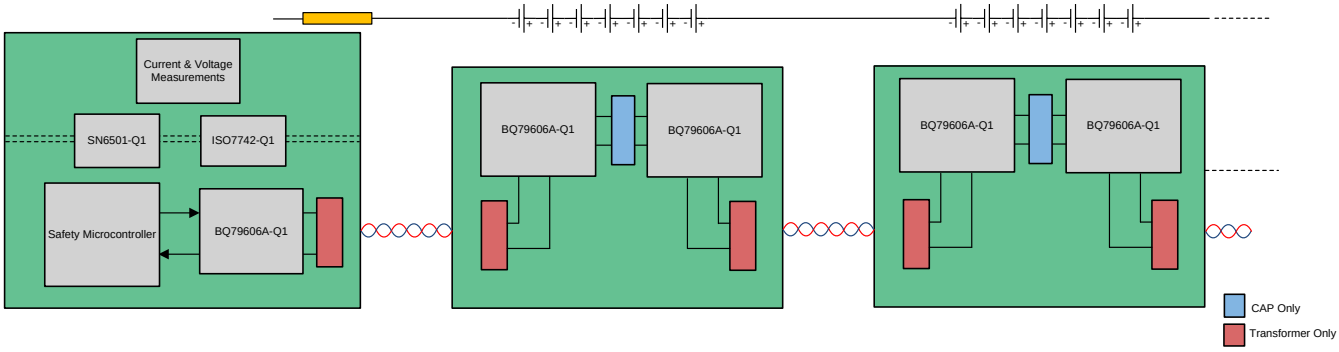
Choke + Cap Isolation is able to support reliable daisy-chain communication. The immunity of off-board communication is able to support various stress scenarios and hot plug of the cells and system. Dielectric strength of the capacitors is one of the important parameters to check for this solution. Based on the selection of components for capacitors and chokes, overall system cost will be lower compared to transformer isolated systems

Figure 18. Cell Supervision Units With Transformer Isolation Option 1



Transformer Isolation for board-to-board in Figure 18 helps in utilizing the BQ79606A-Q1 device for high-voltage measurements. The BQ79606A-Q1 on the first board (battery control unit) is isolated to the controller, which allows for high-voltage measurements. Transformer isolation is used for daisy-chain communication between the two cell supervision units.

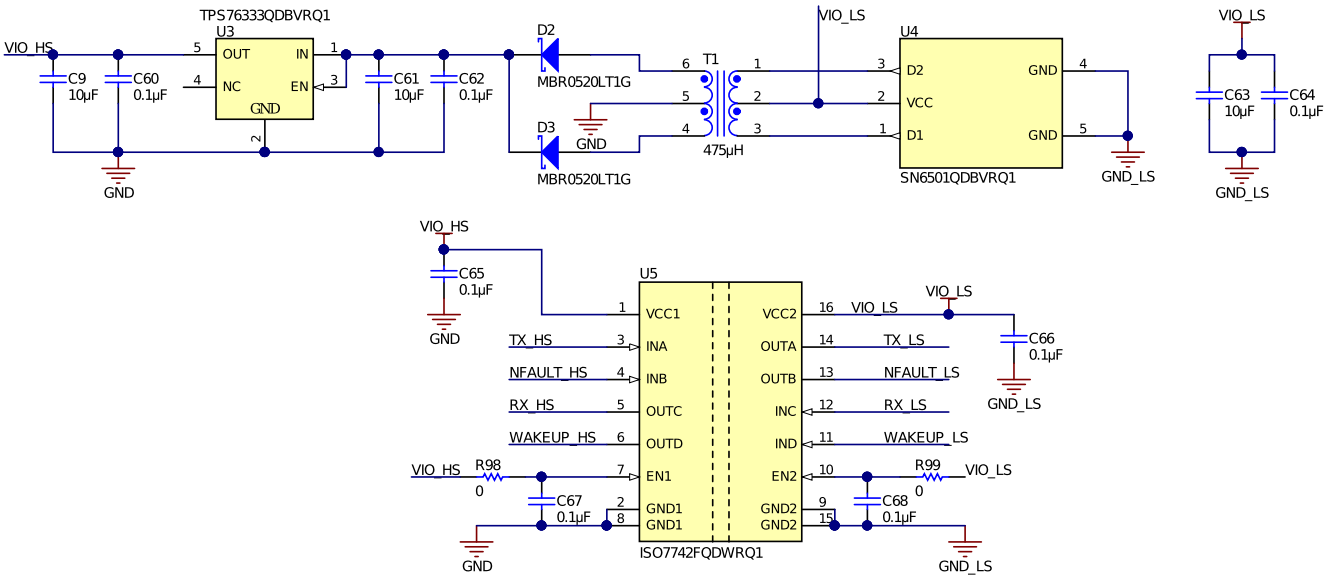
Figure 19. Cell Supervision Units With Transformer Isolation Option 2



The BQ79606A-Q1 can also be connected directly to the microcontroller with transformer isolation supporting daisy-chain communication. The BQ79606A-Q1 device can support both capacitive and transformer isolation. Transformer isolation gives superior reliability for hot-plug and bulk current injections.

The TIDA-01537 is a single board solution for 96s cells and communication to the TMS570LS0432 controller. The digital isolator ISO7742-Q1 is used to interface the BQ79606A-Q1 device.

Figure 20. Interface to BQ79606A-Q1



The SN6501-Q1 device is used to power the isolator on the high-voltage side. VIO_HS is connected to the VIO pin at the base of the BQ79606A-Q1. During deep sleep mode, VIO of base BQ79606A-Q1 is turned off, the SN6501-Q1 supports generating the VIO supply which powers up U5 ISO7742-Q1 to wake up the BQ79606A-Q1.The TPS76333-Q1 device is used to regulate the supply to 3.3 V.

Figure 21. BQ79606A-Q1 Interface Block Diagram

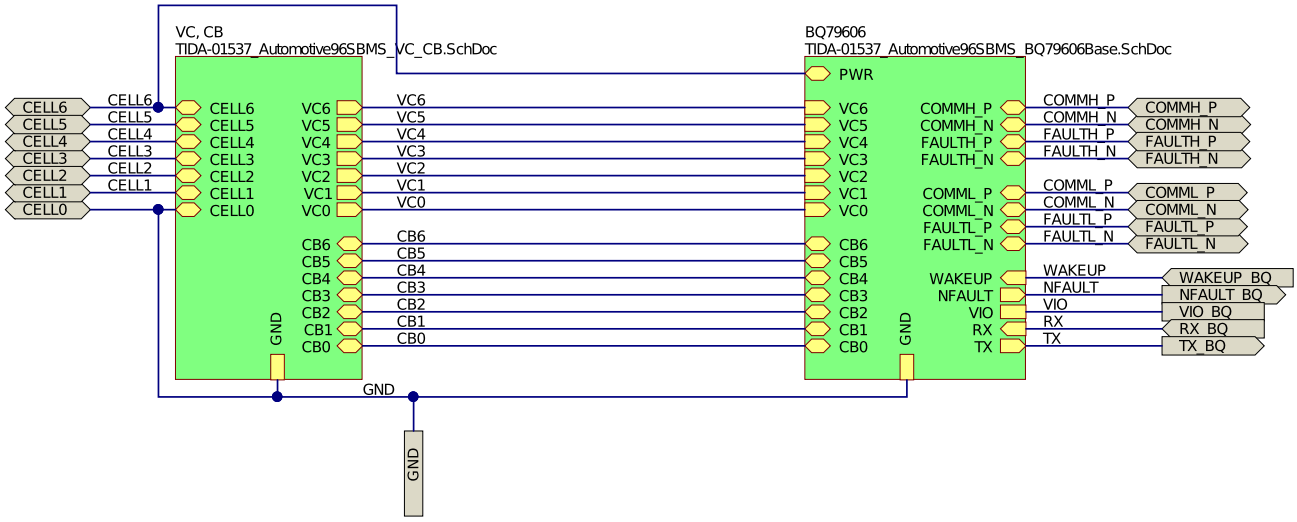
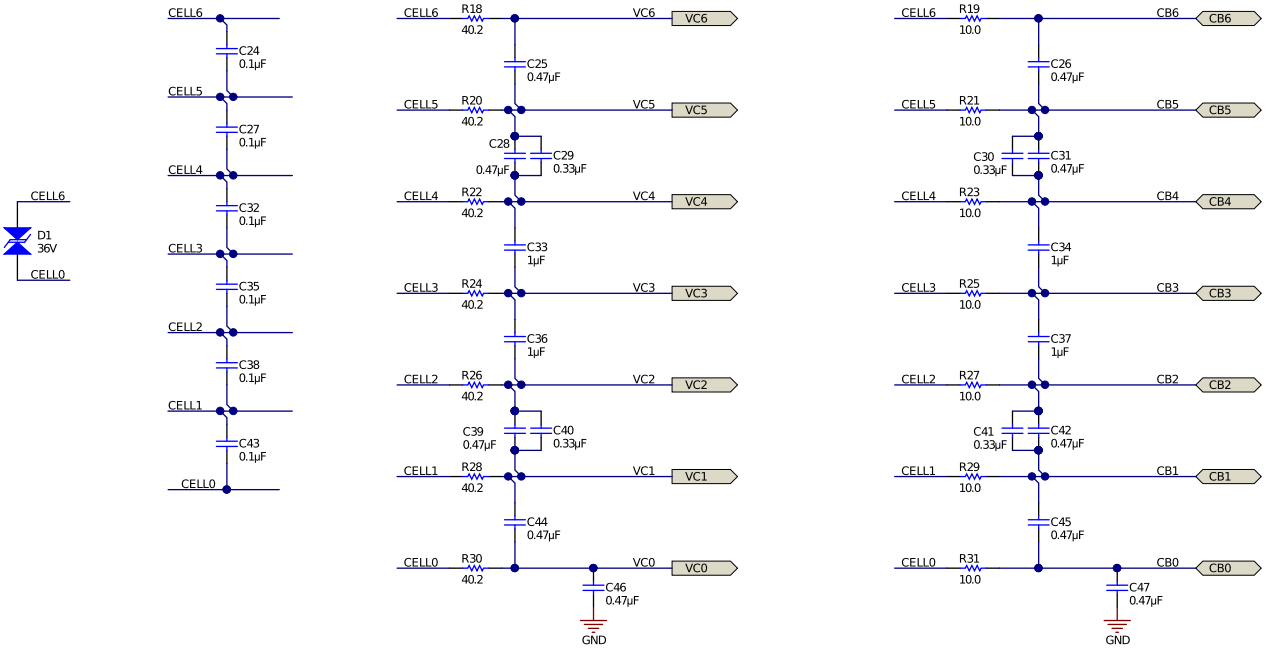


Figure 21 shows the BQ79606A-Q1 top-level block diagram. Input filter capacitors, the communication interface, and IC interface circuits are the building blocks for monitoring cell voltages, temperatures, and they transfer the data (*Monitor and Diagnosis*) via daisy chain and UART.

Figure 22. BQ79606A-Q1 Input Interface Circuit

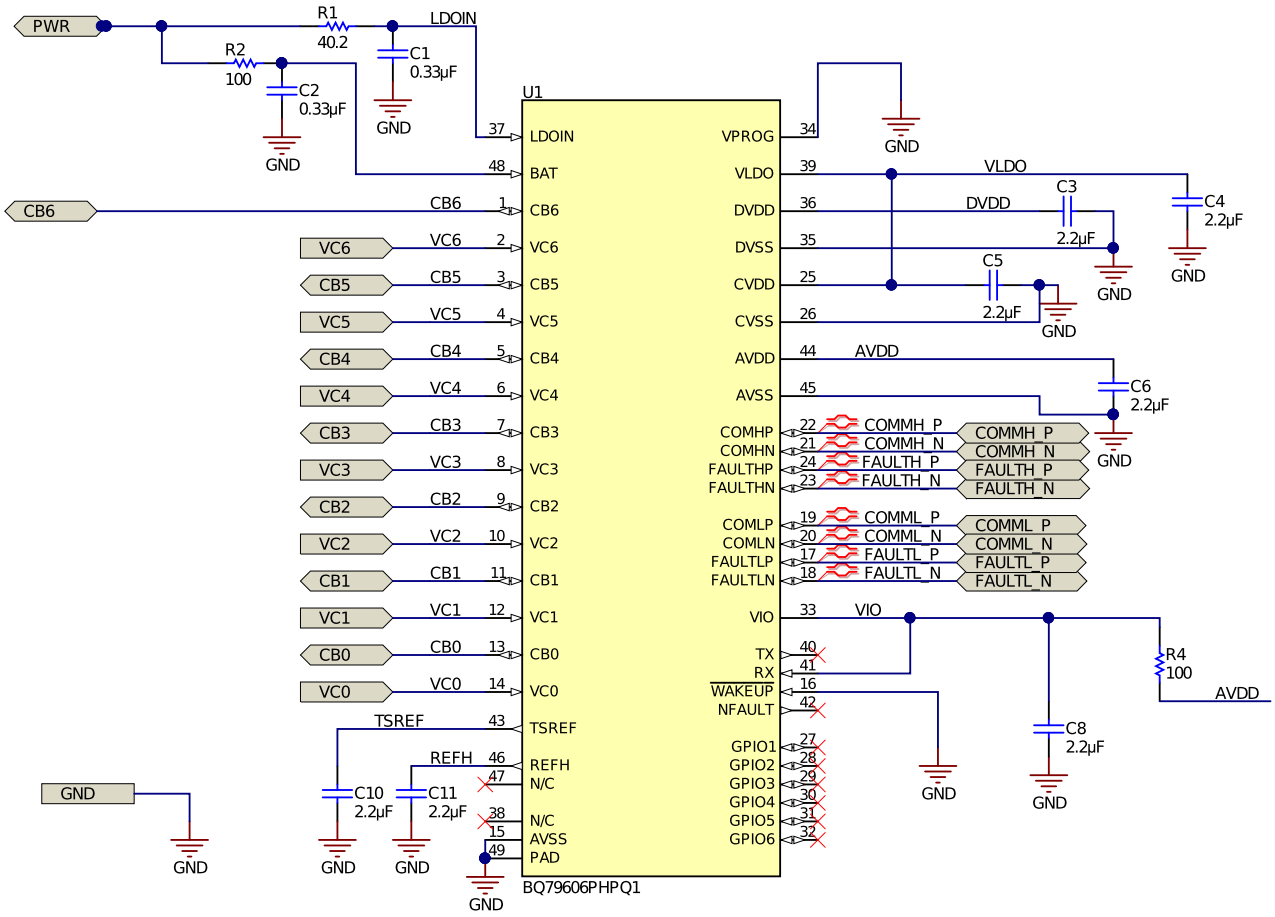


The BQ79606A-Q1 device has internal hot-plug diodes to withstand transients during hot plug, or random disconnections, This avoids the need for additional protection diodes for individual cells. D1_A provides additional protection for internal power and the LDO circuit. Capacitors C24, C27, C32, C35, C38, and C43 are differential filter capacitors. Components R30 and C46 make up the input low-pass filter for VC0. The input filter of the BQ79606A-Q1 internal ADC is fixed at 1.5 kHz. To improve the accuracy of BQ79606A-Q1 there is a single-pole digital filter in the BQ79606A-Q1 which can be configured from 1.2 Hz to 180.1 Hz.

Resistors R19, R21, R23, R25, R27, R29, and R31 are balancing resistors to support passive cell balancing with the BQ79606A-Q1. The BQ79606A-Q1 device supports up to 150-mA balancing current with an internal MOSFET, this saves cost on external MOSFETs.

D1_X is only a place holder on the board, it is not populated on the boards.

Figure 23. BQ79606A-Q1 Schematic



VLDO: External LDO and supplies communication

DVDD: Digital power supply

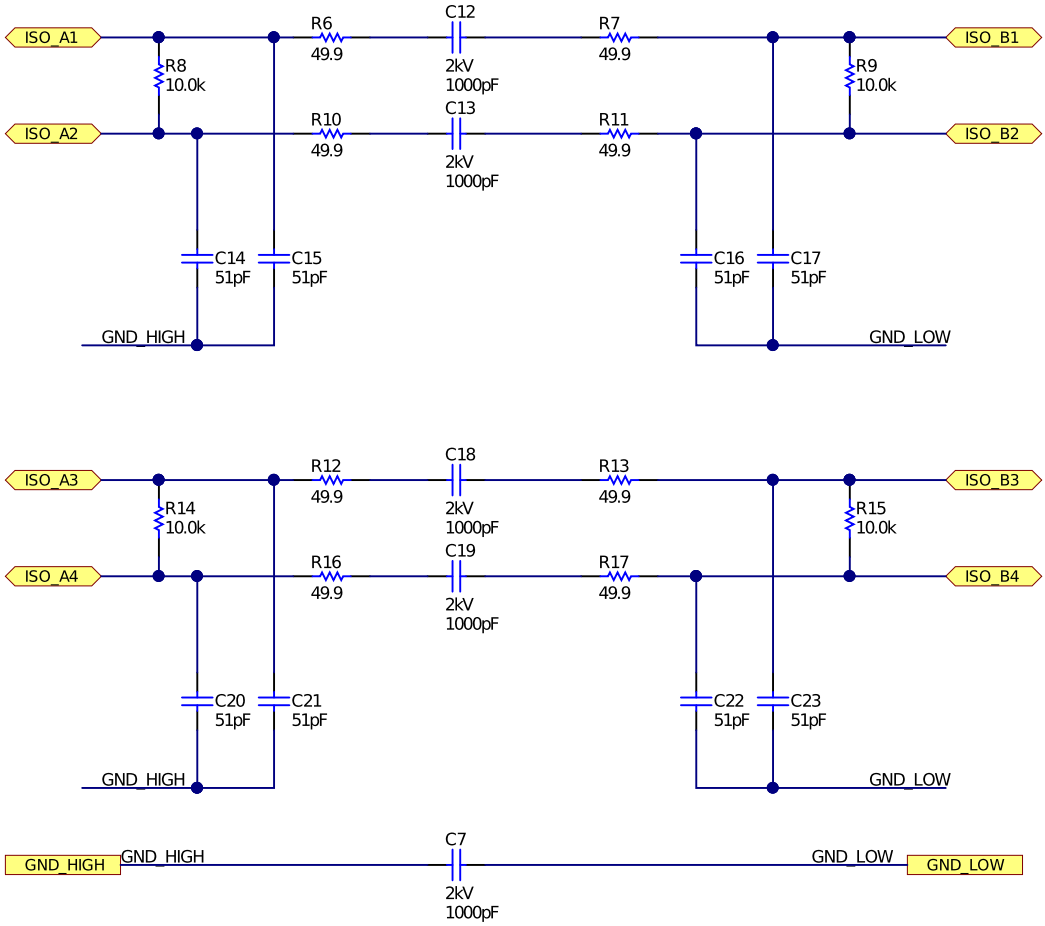
AVDD : Analog power supply and internal power supply of 5 V

CVDD: Communication Power Supply are different powering supplies supporting the functions of BQ79606A-Q1

BAT and LDOIN pins are main sources for the power and internal LDOs in BQ79606A-Q1

There is a need to have decoupling capacitors from these pins to GND/AVSS of BQ79606A-Q1. Typical decoupling capacitors for all LDO outputs should be less than 2.2 µF. R1_A, C1_A and R2_A, C2_A are components to support low-pass filter and hot-plug spikes for the BQ79606A-Q1. TSREF is bias for the NTC monitor. It can be used for the resistor divider for connecting the NTC temperature sensor. TSREF is an input pin, it cannot drive any loads. REFH/REF1: High-power bypass connections, It is an internal reference. There should not be any external load for REFH, a bypass capacitors should be placed very close to the pin.

Figure 24. Capacitive Isolation for BQ79606A-Q1



The BQ79606A-Q1 device is interfaced between two ICs with capacitive isolation. The BQ79606A-Q1 supports capacitive isolation, C12_B and C13_B are the isolating capacitors to support the daisy-chain communication. Capacitive isolation comes at a low cost and is efficient for isolated daisy-chain communication. It is very effective for onboard communication, based on external noises and OEMs, it can be extended to board-to-board communications as well. Resistors and capacitors need to have perfect termination of daisy-chain communication. Capacitors C14_B and C15_B support low-pass filters in combination to R6_B and R10_B, respectively.

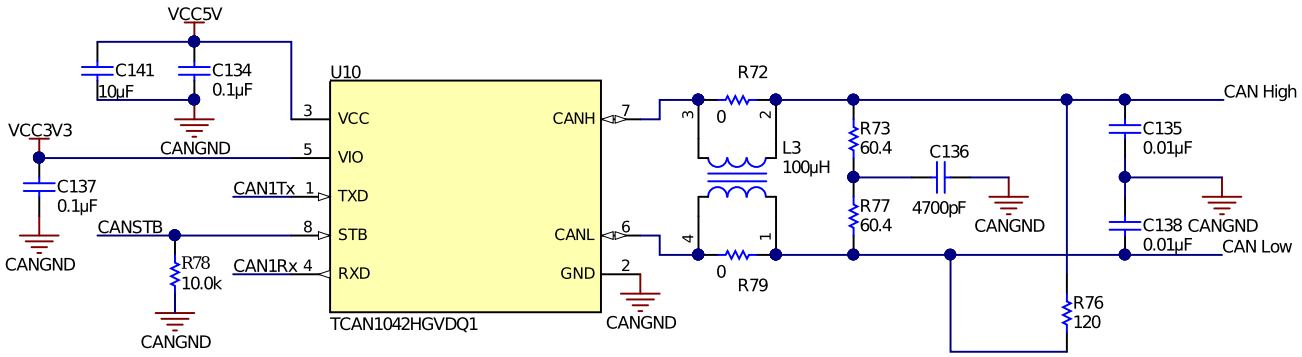
The BQ79606A-Q1 device has the fault line which can be used to update the failure status and also work as a heartbeat tone. The heartbeat tone is transmitted by the top-most BQ79606A-Q1 from north to south communication. If there is no heartbeat pulse in the given time, it can be considered that one of the BQ79606A-Q1 is not configured properly or not behaving as per the expectations. This failure can be a result of the loss of communication wires or disconnection of cells.

2.3.4 TCAN1042-Q1

A *Controller Area Network* (CAN) is widely used in the automotive industry to replace the complex wiring harness with a two-wire bus. It is highly immune to electrical interference and it has ability to self-diagnose and repair data errors. The evolution of automotive architectures and the need for efficient power train and vehicle control mechanisms increased the demand for the number of nodes in vehicles (both passenger and commercial). Improvement in safety architectures increases demand for internal diagnosis and data sharing between multiple nodes with faster response times. The number of nodes to transmit and the data

loads push the limits of the CAN baud rates while staying within its advantages of reliable robust communication. CAN flexible data rate (FD) is one such type of CAN communication, which gained popularity for its flexibility of retaining the features of basic CAN (no change to physical layer) and supports high data rates with little rise in system cost. The TCAN1042-Q1 is designed for CAN FD networks for data rates from 2 to 5 Mbps.

Figure 25. TCAN1042-Q1 in TIDA-01537



CAN FD is one of the commonly-used communication protocols in HEV/EV. The TIDA-01537 design is built by using TCAN1042-Q1 which support data rates up to 5 Mbps. R73 and R77 are the termination resistors populated for the TCAN1042-Q1. R76 is an optional resistor which can be populated onboard based on the external connections.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

Based on the type of tests, there are different setups and equipments used to test the TIDA-01537 design. For low-voltage tests of the TIDA-01537, a 10-W regulated lab power supply with 12-V output is required. An oscilloscope is required to capture the circuit behavior based on the type of test. High-voltage tests are performed on the TIDA-01537 design with the appropriate safety measures recommended by lab safety engineers. A safety box with an interlocking mechanism is required to perform high-voltage tests. High voltage can be created by using actual cells or a cell simulator or high-voltage power supply with appropriate potential dividers.

3.1.2 Software

3.1.2.1 TMS570 Initialization Sequence

The TMS570LS0432 micro controller (MCU) goes through a safety initialization sequence, where several of the diagnostic features are tested and enabled. These steps are done in the following sequence:

- Initialize clocks and Flash memory accesses
- Initialize CPU RAMs to all zeros
- Self-test on all other RAMs
- Verify correct operation of CPU RAM ECC checking and enable it
- Initialize all peripheral RAMs including the parity checking bits
- Verify correct operation of parity error detection and enable it
- Enable interrupts

3.1.2.2 Main Application

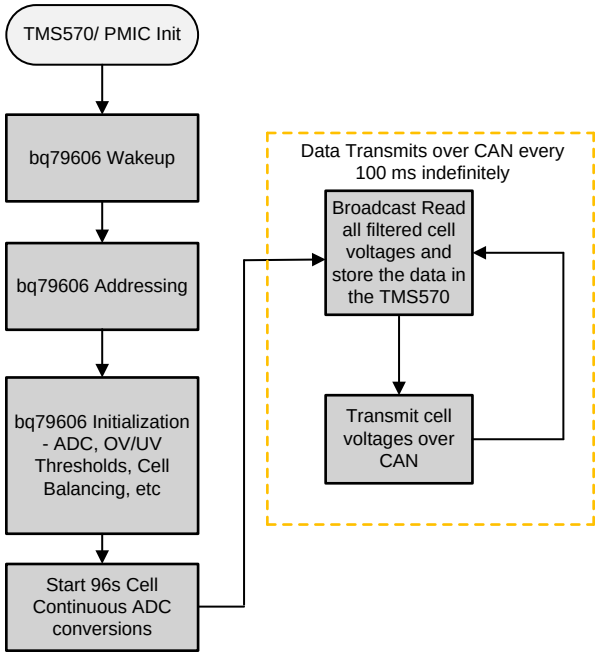
The main() function sets up the peripherals used in this application. This is done in the following sequence:

- Initialize the GIO ports:
  - GIOA.0 is used as an output pin
  - All other GIO pins are used as input pins
  - None of the GIO pins are configured to generate interrupts
- Initialize the CAN communication ports
  - CAN1 port is initialized for a baud rate of 500 kbps
- Initialize the dedicated SCI communication port
  - The LIN module on TMS570 is configured to be used in standard SCI mode
  - SCI port is initialized to communicate at 1 Mbps
  - This SCI port is used to communicate with the daisy-chained bq79606A parts via the isolation IC: ISO7742-Q1
- Initialize SPI2 module to communicate with the TPS65381A PMIC
  - CLK, SIMO, SOMI, nCS[0, 1, 2, 3] are configured as SPI-functional pins to be used in the communication
  - 1-MHz CLK frequency
  - 16-bit character length
- Initialize the TPS65381A PMIC
  - Setup timer task to service PMIC watchdog every 60 ms
  - Setup a task to run diagnostic checks on the PMIC

  - Setup a task to run diagnostic checks on the TMS570
- Wake up the bq79606A by creating a 10-ms wide pulse on GIOA.0

Figure 26 shows the flow chart for typical functions implemented in the TIDA-01537 software.

Figure 26. TIDA-01537 Software Flowchart

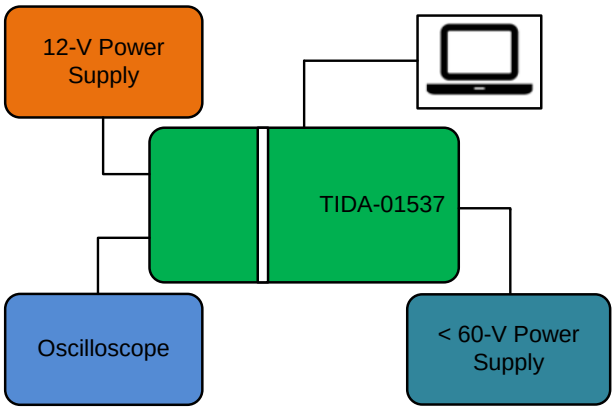


3.2 Testing and Results

3.2.1 Test Setup

Low-voltage tests are performed with basic setup and required safety precautions. Figure 27 shows the preliminary setup for low-voltage tests.

Figure 27. TIDA-01537 Low-Voltage Setup



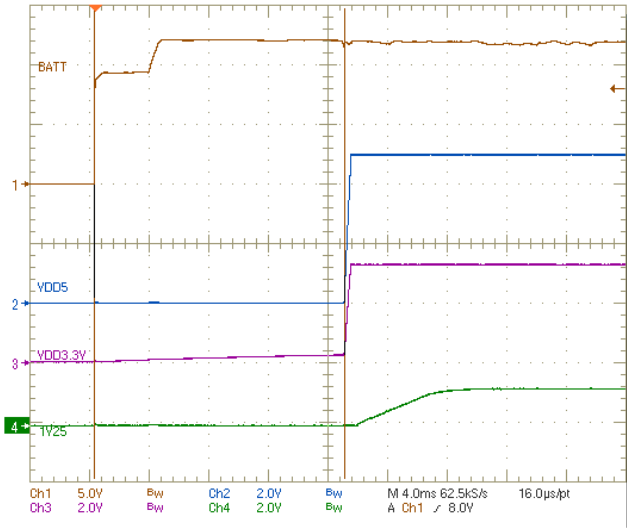
Low-voltage tests are done to check the basic performance of the TPS65381A-Q1 and TPS57160-Q1. The TMS570LS04362-Q1 is flashed and the performance of interface circuits operation is checked. The low-voltage setup is also used to check the performance of the initial two BQ79606A-Q1 devices.

3.2.2 Test Results

3.2.2.1 TIDA-01537 Power-up Sequence

Power-up sequence tests on the TIDA-01537 design show the performance of the TPS65381-Q1 and TPS57160-Q1. Use these tests to cross check the behavior expected in the data sheet and circuit design. Accurate assessment of the power-up sequence helps in estimating the bootup time of the TIDA-01537 device. Typically such performance is checked in any electronic control units to understand and define the system architecture.

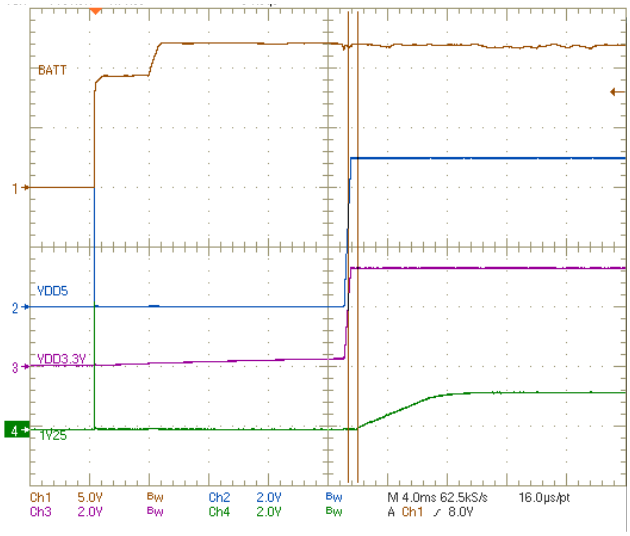
Figure 28. Startup Behavior TIDA-01537



CH1: BATT –12-V battery voltage
CH2: VDD5 - Internal 5 V
CH3: VDD3.3V - Internal 3.3 V
CH4: 1V25 - Internal 1.25 V

Typical Delay time of VDD5 and VDD3.3V from BATT = 16.8 ms

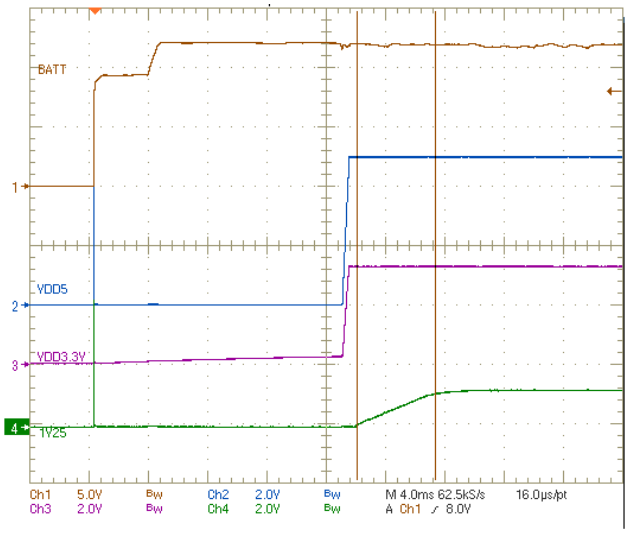
Figure 29. Delay of 1V25



CH1: BATT –12-V battery voltage
CH2: VDD5 - Internal 5 V
CH3: VDD3.3V - Internal 3.3 V
CH4: 1V25 - Internal 1.25 V

Typical Delay time of 1V25 from VDD3.3V = 640 µs

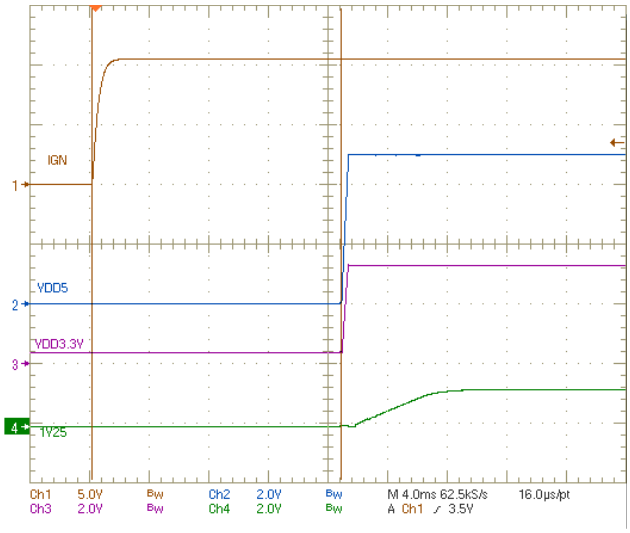
Figure 30. Rise Time of 1V25



CH1: BATT –12-V battery voltage
CH2: VDD5 - Internal 5 V
CH3: VDD3.3V - Internal 3.3 V
CH4: 1V25 - Internal 1.25 V

Typical Rise time of 1V25 = 5.28 ms

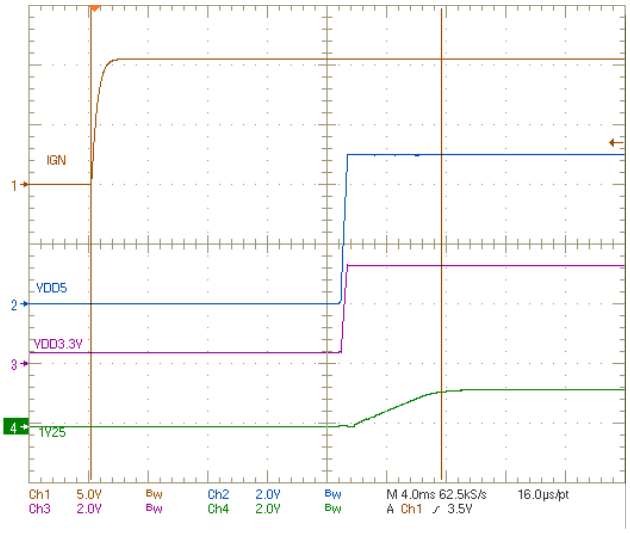
Figure 31. Delay Time of Internal VDD From Ignition



CH1: IGN -Ignition input of TIDA-01537
CH2: VDD5 - Internal 5 V
CH3: VDD3.3V - Internal 3.3 V
CH4: 1V25 - Internal 1.25 V

Typical delay time of VDD5 and VDD3.3V from IGN = 16.73 ms

Figure 32. Delay Time of 1.25 V From Ignition

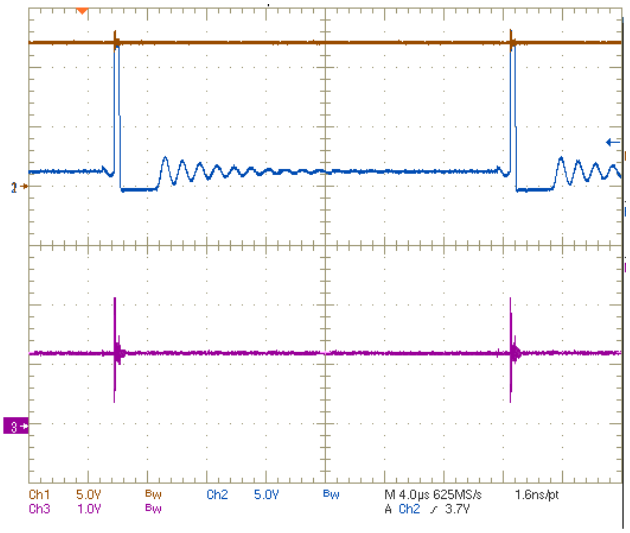


CH1: IGN -Ignition input of TIDA-01537
CH2: VDD5 - Internal 5 V
CH3: VDD3.3V - Internal 3.3 V
CH4: 1V25 - Internal 1.25 V

Typical delay time of 1.25 V from ignition = 23.52 ms

Performance of input power sequence is well within the design specification. It is in line with the description explained in Section 2.3.1.

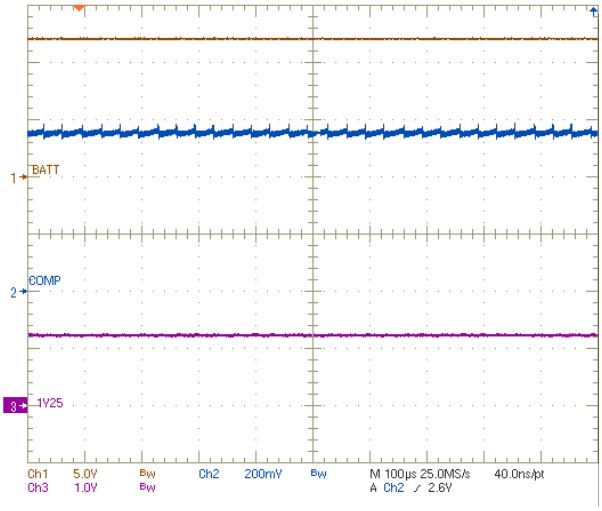
Figure 33. TPS57610-Q1 SW Behavior



CH1: BATT –12-V power supply
CH2: SW @ TPS57160-Q1
CH3: 1V25 - Internal 1.25 V

Typical time delay of pulse 1 to pulse 2 : 25 µs
Estimated frequency of TPS57610-Q1 = 400 KHz
Behavior of buck converter TPS57610-Q1 is as per design parameters mentioned in ??

Figure 34. TPS57610-Q1 Comp and Output Behavior

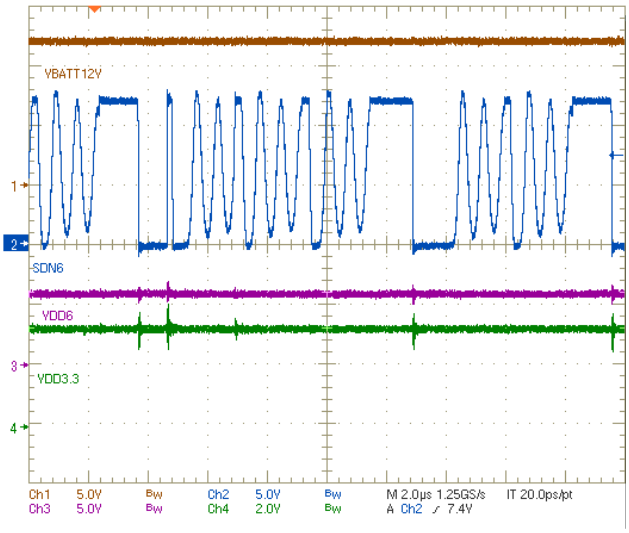


CH1: BATT –12-V power supply
CH2: COMP @ TPS57160-Q1
CH3: 1V25 - Internal 1.25 V

Peak to peak of COMP@TPS57160-Q1 = 55.66 mW
Mean output voltage = 1.23 V

The TPS57610-Q1 device is generating 1.25 V and works as per the designed frequency. The interfaced filter circuit behaves as expected in reducing the output ripple.

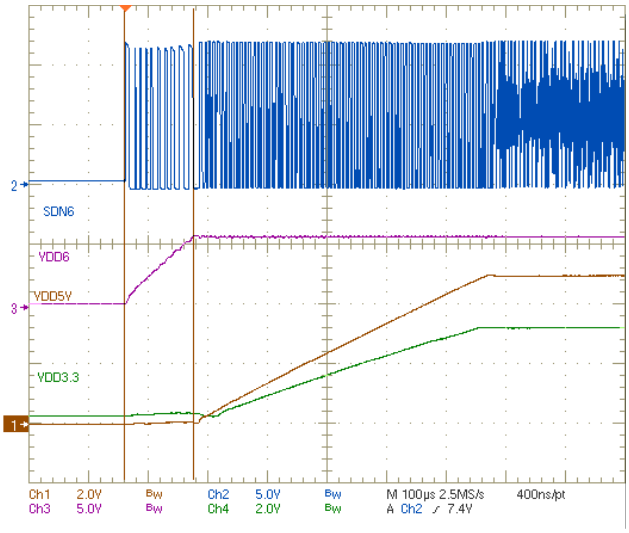
Figure 35. TPS65381A-Q1 Operating Behavior



CH1: IGN -Ignition input of TIDA-01537
CH2: SDN6 -TPS65381-Q1
CH3:VDD6 -TPS65381-Q1
CH4: VDD3.3 - Internal 3.3 V

Peak to peak of COMP@TPS57160-Q1 = 55.66 mW
Mean output voltage = 1.23 V

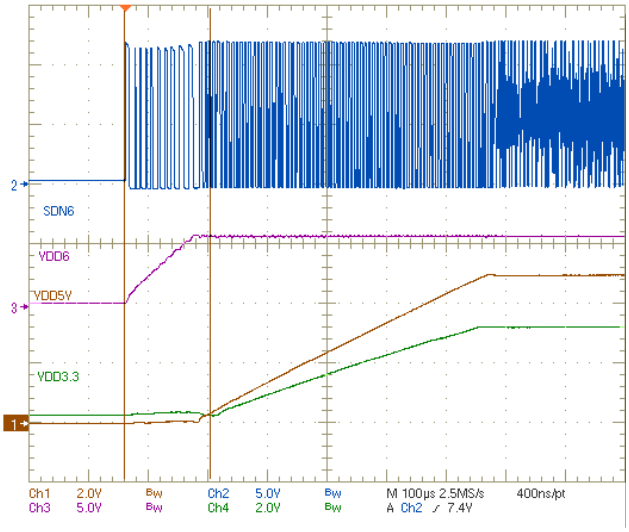
Figure 36. TPS65381A-Q1 Startup Behavior



CH1: VDD5V - Internal 5 V
CH2: SDN6 -TPS65381-Q1
CH3:VDD6 -TPS65381-Q1
CH4: VDD3.3 - Internal 3.3 V

Ramp-up time of VDD6 from SDN6 = 116 µs

Figure 37. TPS65381A-Q1 VDD6 Ramp-Up Behavior



CH1: VDD5V - Internal 5 V
CH2: SDN6 -TPS65381-Q1
CH3:VDD6 -TPS65381-Q1
CH4: VDD3.3 - Internal 3.3 V

Typical delay time of VDD5V and VDD3.3V from SDN6 = 144 µs

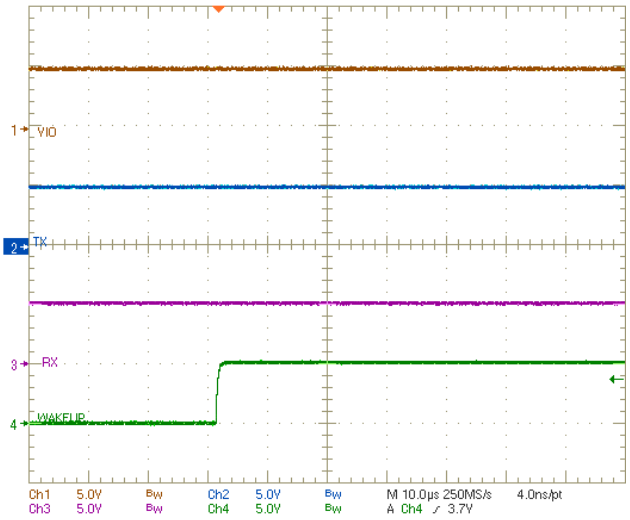
VDD6 is ramping up as expected based on the IGN signal to the TPS65381-Q1 device. Ramp-up behavior of VDD5V and VDD3.3V is inline to the description of the data sheet.

NOTE: Performance of the TPS65381A-Q1 device might vary with different loading conditions of the system.

3.2.3 BQ79606A-Q1 Circuit Behavior

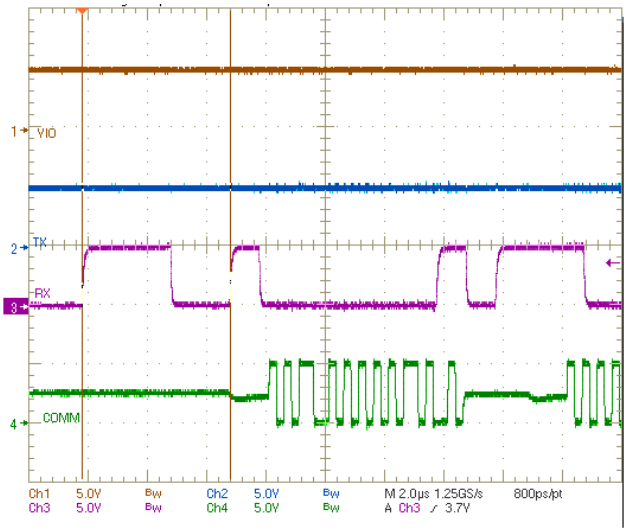
Preliminary tests are done on the TIDA-01537 to check the performance while interfacing BQ79606A-Q1s and external components required for *Battery Management Systems*. Different setups are used and listed accordingly for the tests on the TIDA-01537.

Figure 38. BQ79606A-Q1 UART Wakeup



CH1: VIO - Interface to host BQ79606A-Q1
CH2: TX - UART of BQ79606A-Q1
CH3: RX - UART of BQ79606A-Q1
CH4: WAKEUP - BQ79606A-Q1

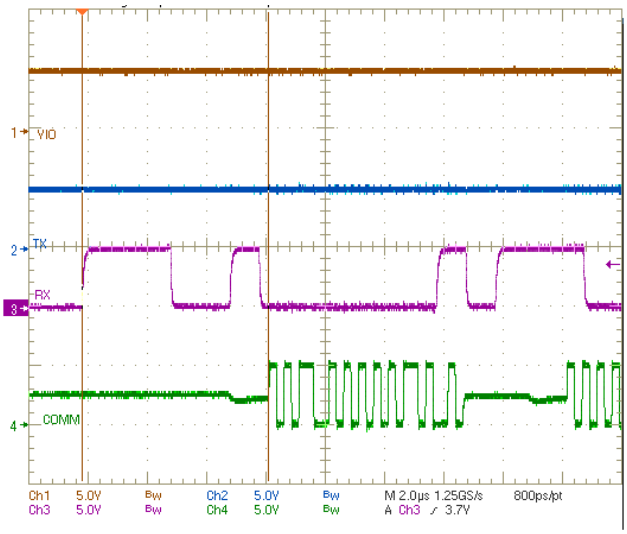
Figure 39. UART RX to Host BQ79606A-Q1



CH1: VIO - Interface to host BQ79606A-Q1
CH2: TX - UART of BQ79606A-Q1
CH3: RX - UART of BQ79606A-Q1
CH4: COMM - North COMM of host BQ79606A-Q1

Typical Delay to Initiate Daisy Chain Communication = 5 µs

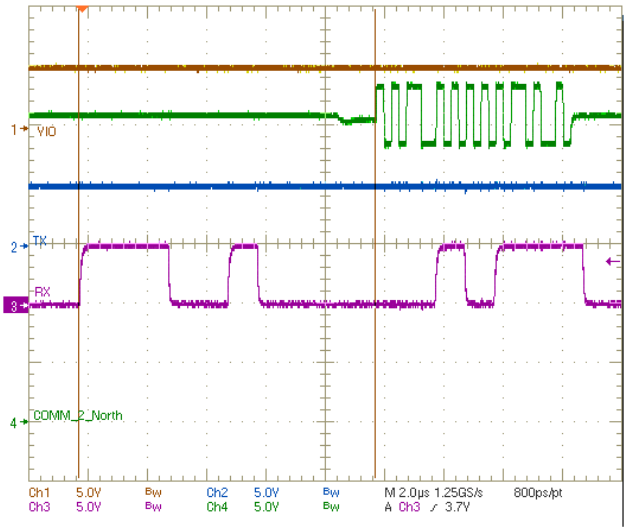
Figure 40. UART RX to Daisy-Chain Communication



CH1: VIO - Interface to host BQ79606A-Q1
CH2: TX - UART of BQ79606A-Q1
CH3: RX - UART of BQ79606A-Q1
CH4: COMM - North COMM of host BQ79606A-Q1

Typical delay to start initial daisy-chain communication = 6.28 µs

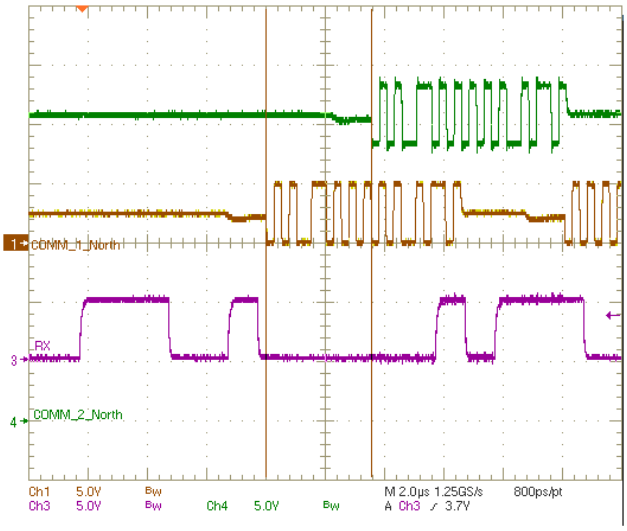
Figure 41. Daisy-Chain Communication From BQ79606A-Q1



CH1: VIO - Interface to host BQ79606A-Q1
CH2: TX - UART of BQ79606A-Q1
CH3: RX - UART of BQ79606A-Q1
CH4: COMM 2 North - North COMM of second BQ79606A-Q1

Typical daisy-chain transmission delay after second BQ79606A-Q1 = 10 µs

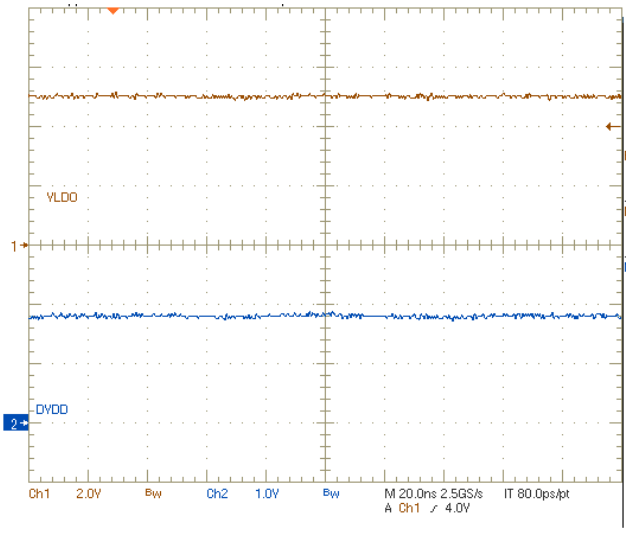
Figure 42. Daisy-Chain Communication BQ79606A-Q1



CH1: COMM 1 North - North COMM of host BQ79606A-Q1
CH3: RX - UART of BQ79606A-Q1
CH4: COMM 2 North - North COMM of second BQ79606A-Q1

Typical daisy-chain transmission delay by a BQ79606A-Q1 = 3.56 µs

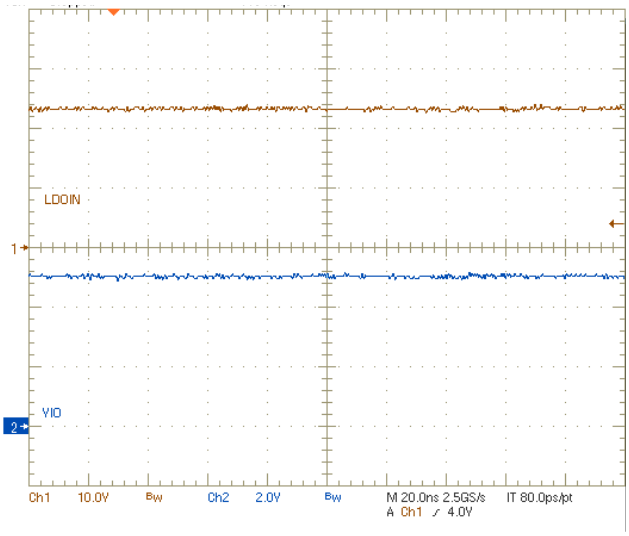
Figure 43. BQ79606A-Q1 VLDO Behavior



CH1: VLDO of BQ79606A-Q1
CH2: DVDD of BQ79606A-Q1

Typical VLDO voltage of BQ79606A-Q1 = 5.018 V
Typical DVDD voltage of BQ79606A-Q1 = 1.801 V

Figure 44. BQ79606A-Q1 LDOIN Behavior



CH1: LDOIN of BQ79606A-Q1
CH2:VIO of BQ79606A-Q1

Typical VIO voltage of BQ79606A-Q1 = 5.033 V

3.2.4 BQ79606A-Q1 Cell Balancing

Cell balancing is one of the critical activities for *Battery Management Systems*. The BQ79606A-Q1 device can support a passive cell balancing current of 150 mA. Tests are done on the TIDA-01537 to check the behavior of the BQ79606A-Q1.

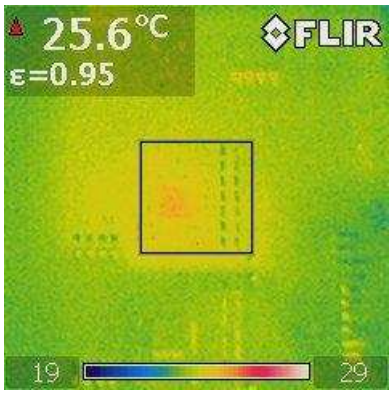
Specification:

- 150 mA balancing current
- 2 min odd cells, 2 min even cells
- 60 min timer for all cells

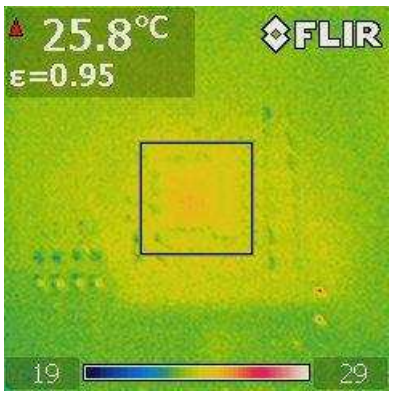
Procedure:

- Wakeup the device via TMS570LS432-Q1 or UART
- Capture the board temperature with a thermal camera
- Configure cell balancing to run even then odds with 2-min duty cycle and 60 min timer for each cell, and VCBDONE threshold of 3 V (external resistors set the cell-balancing current)
  - Configure 2 min duty cycle, keep balancing on fault and balance odd then even using the CB_CONFIG register
  - Configure the timer to 60 minutes in CB_CELL1_CTRL to CB_CELL6_CTRL registers
  - Set VCB_DONE threshold to 3 V in CB_DONE_THRESH register
  - Enable BAL_GO bit in CONTROL2 register to start balancing
  - Monitor CB_DONE status register to see the status of each cell being balanced
- Capture the board temperature with a thermal camera

Figure 45. BQ79606A-Q1 Cell Balancing-OFF State



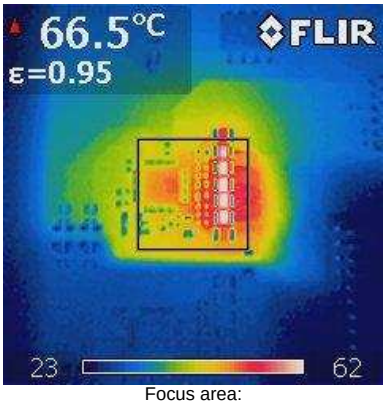
Focus area:
BQ79606A-Q1 + Balancing Resistors



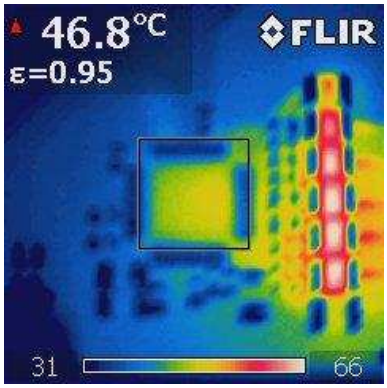
Focus area: only BQ79606A-Q1

Very low power dissipation in BQ79606A-Q1 during active mode (ADC running and cell balancing turned off)

Figure 46. BQ79606A-Q1 Cell Balancing - 1 min



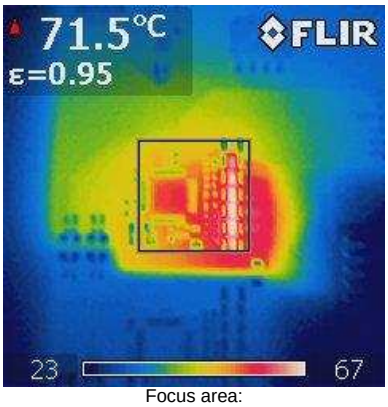
Focus area:
BQ79606A-Q1 + Balancing Resistors



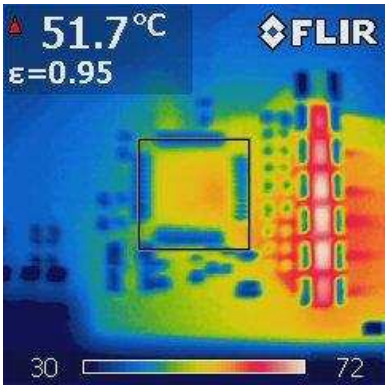
Focus area: only BQ79606A-Q1

Cell Balancing Turned ON = 1 min
Maximum board temperature = 66.5°C
Maximum BQ79606A-Q1 temperature = 46.8°C
Estimated ambient temperature = 31°C
Approximate Delta in BQ79606A-Q1 due to 150-mA cell balancing = 17.8°C

Figure 47. BQ79606A-Q1 Cell Balancing - 3 min



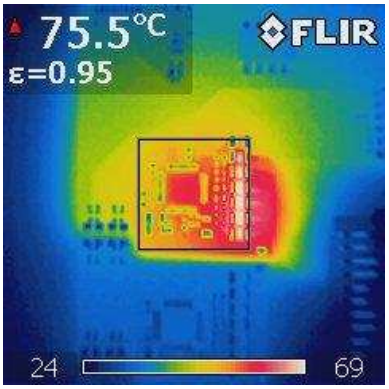
Focus area:
BQ79606A-Q1 + Balancing Resistors



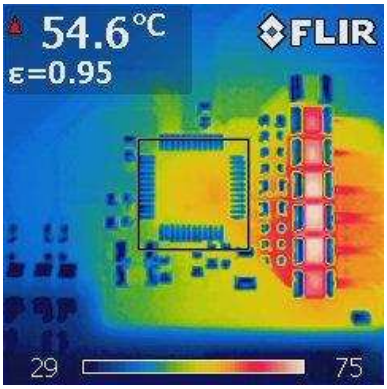
Focus area: only BQ79606A-Q1

Cell Balancing Turned ON = 3min
Maximum Board Temperature = 71.5°C
Maximum BQ79606A-Q1 Temperature = 51.7°C
Estimated ambient temperature = 30°C
Approximate delta in BQ79606A-Q1 due to 150-mA cell balancing = 21.7°C

Figure 48. BQ79606A-Q1 Cell Balancing - 10 min



Focus area:
BQ79606A-Q1 + Balancing Resistors



Focus area: only BQ79606A-Q1

Cell Balancing Turned ON = 10min
Maximum board temperature = 75.5°C
Maximum BQ79606A-Q1 temperature = 54.6°C
Estimated ambient temperature = 29°C
Approximate delta in BQ79606A-Q1 due to 150-mA cell balancing = 25.6°C

After 10 mins of cells balancing, the temperature is more or less constant at with a peak delta of 25.6°C from the ambient temperature. In most of the cases, power dissipation and maximum temperature in an IC and control units depends on many factors such as operating mode, PCB design, housing design, and ambient air flow.

3.2.5 BQ79606A-Q1 Leakage Current Tests

Setup:

Figure 49. Leakage Test Setup Block Diagram

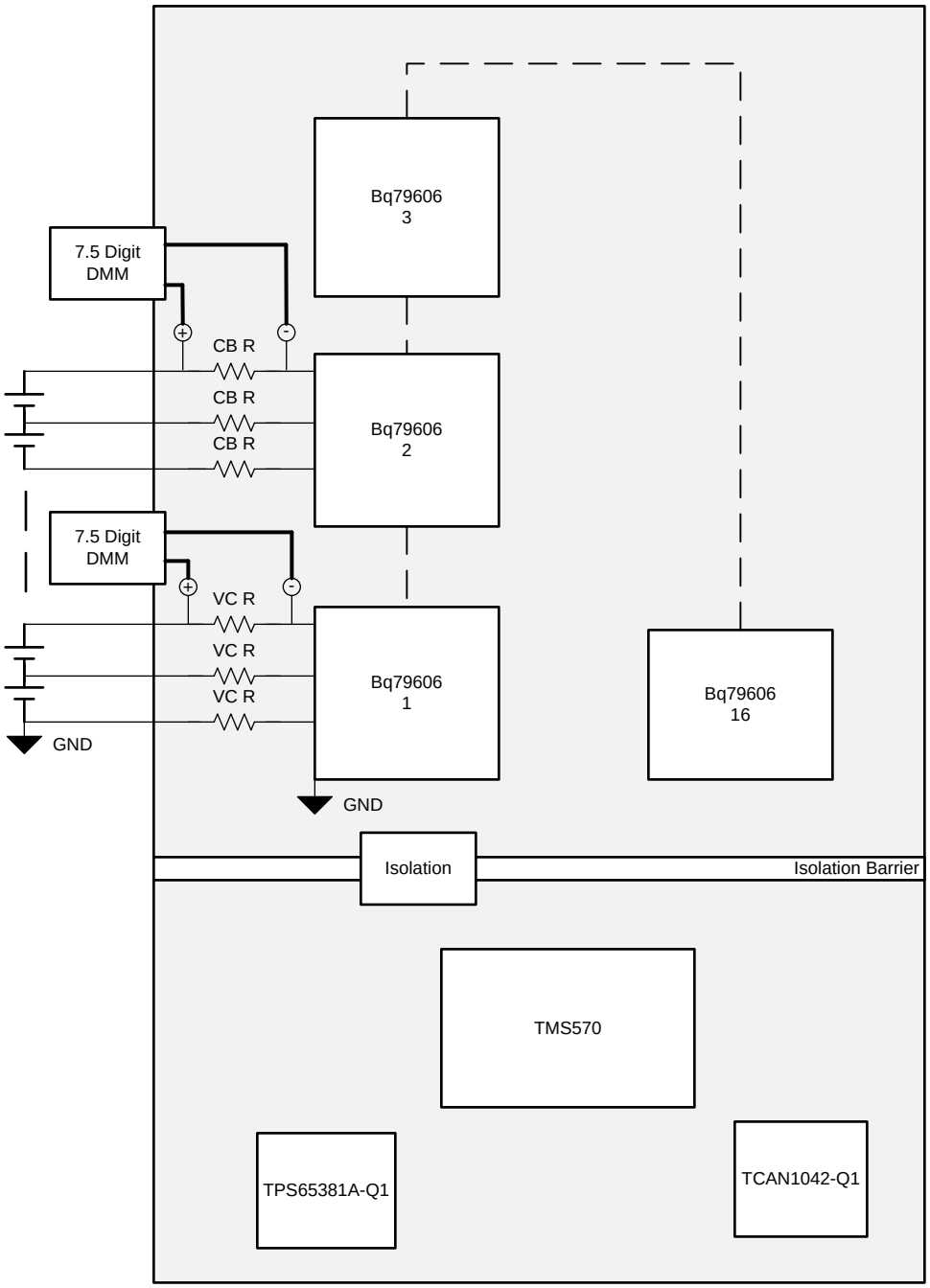
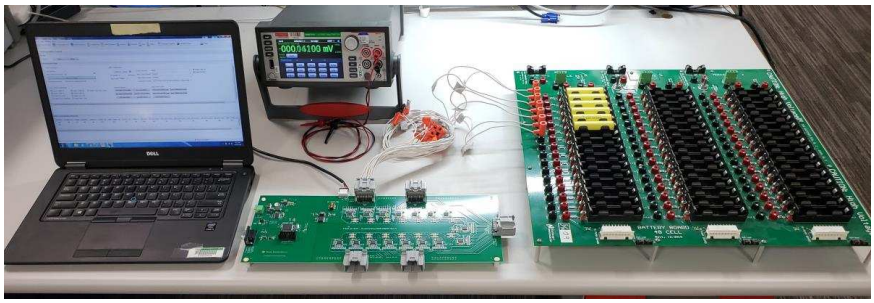


Figure 50. TIDA-01537 Leakage Lab Setup



Test Cases:

- bq79606A-Q1 in shutdown mode
- bq79606A-Q1 in sleep mode
- bq79606A-Q1 in active mode (ADC running)

Leakage Current Test Results:

Leakage currents are measured on the TIDA-01537 design during different test cases. A 7.5-digit multimeter is used to measure the leakage current flowing through the pins as Section 3.2.4 shows. Leakage current measurements are tabulated in Table 2.

Table 2. BQ79606A-Q1 Leakage Currents Active Mode

BQ79606A-Q1 PIN	ACTIVE MODE - ADC RUNNING (µA)					
EACH CELL VOLTAGE	2 V	3 V	3.5 V	4 V	4.5 V	5 V
BAT	30.790	31.400	31.550	31.670	32.030	32.209
LDOIN	6335.815	6355.711	6353.594	6350.158	6343.808	6341.044
VC6	1.273	1.664	1.860	2.046	2.243	2.418
VC5	1.249	1.670	1.856	2.063	2.254	2.445
VC4	1.212	1.619	1.813	2.019	2.205	2.398
VC3	1.110	1.495	1.690	1.888	2.083	2.252
VC2	0.933	1.310	1.848	1.992	2.136	2.267
VC1	0.552	1.244	1.573	1.841	2.403	2.355
VC0	0.749	1.171	1.367	1.558	1.771	1.962
CB6	0.006	0.010	0.013	0.010	0.002	0.009
CB5	0.011	0.006	0.016	0.017	0.006	0.016
CB4	0.010	0.004	0.004	0.006	0.013	0.013
CB3	0.017	0.016	0.014	0.011	0.005	0.002
CB2	0.004	0.004	0.019	0.010	0.003	0.007
CB1	0.006	0.006	0.002	0.008	0.005	0.007
CB0	0.007	0.008	0.006	0.002	0.006	0.006
Total	6373.746	6397.337	6397.224	6395.300	6390.974	6389.409

Table 3. BQ79606A-Q1 Leakage Currents Sleep Mode

BQ79606A-Q1 PIN	SLEEP MODE (µA)					
EACH CELL VOLTAGE	2 V	3 V	3.5 V	4 V	4.5 V	5 V
BAT	24.404	24.764	24.954	25.094	25.354	25.374
LDOIN	114.968	115.566	115.939	116.039	116.362	116.935
VC6	0.005	0.009	0.009	0.009	0.007	0.011
VC5	0.003	0.005	0.004	0.010	0.012	0.007
VC4	0.005	0.008	0.002	0.003	0.011	0.005
VC3	0.006	0.007	0.005	0.008	0.005	0.004
VC2	0.006	0.007	0.004	0.006	0.011	0.009
VC1	0.005	0.004	0.008	0.011	0.008	0.006
VC0	0.005	0.007	0.009	0.009	0.009	0.008
CB6	0.009	0.009	0.018	0.016	0.007	0.010
CB5	0.005	0.010	0.004	0.009	0.013	0.003
CB4	0.004	0.006	0.008	0.013	0.007	0.007
CB3	0.008	0.006	0.005	0.006	0.013	0.007
CB2	0.005	0.004	0.002	0.002	0.006	0.004
CB1	0.006	0.006	0.004	0.008	0.003	0.003
CB0	0.009	0.008	0.010	0.009	0.002	0.003
Total	139.452	140.426	140.984	141.252	141.829	142.396

Leakage currents are plotted in Figure 51 through Figure 54.

Figure 51. VC Leakage Current-ADC Running

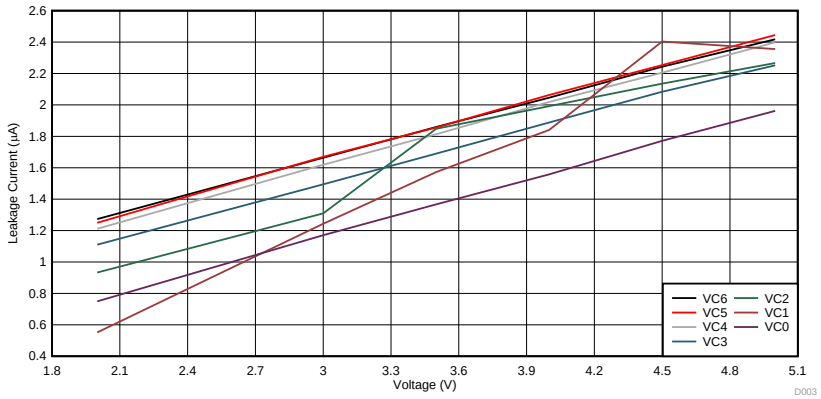


Figure 52. VC Leakage Current-Sleep Mode

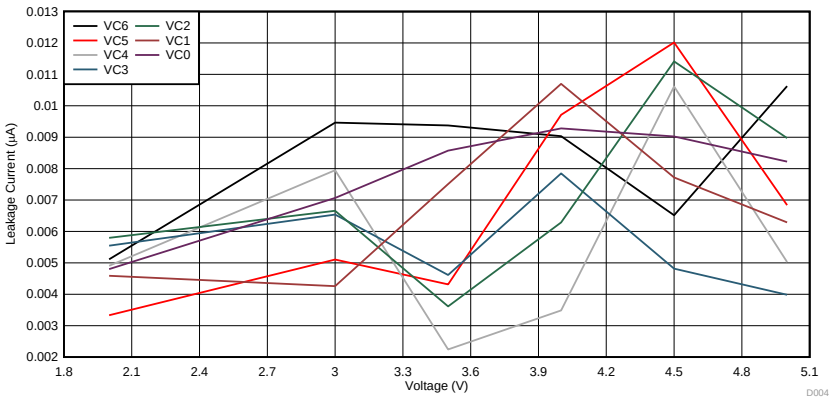


Figure 53. CB Leakage Current-ADC Running

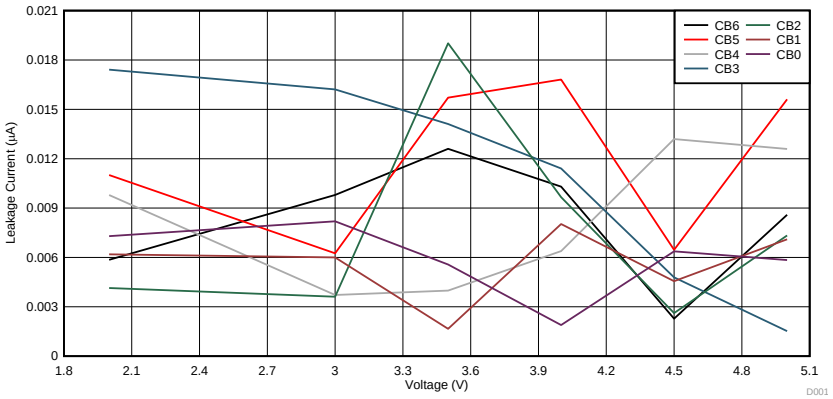
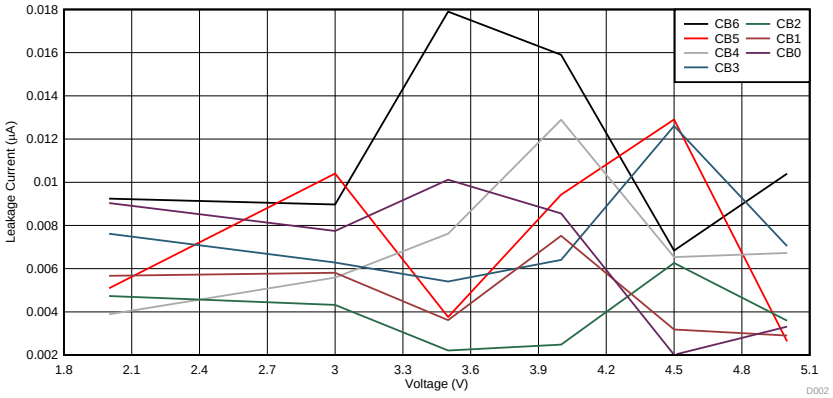


Figure 54. CB Leakage Current-Sleep Mode



The leakage current of the VCx and CBx pins is low in all operating modes of the BQ79606A-Q1 device.

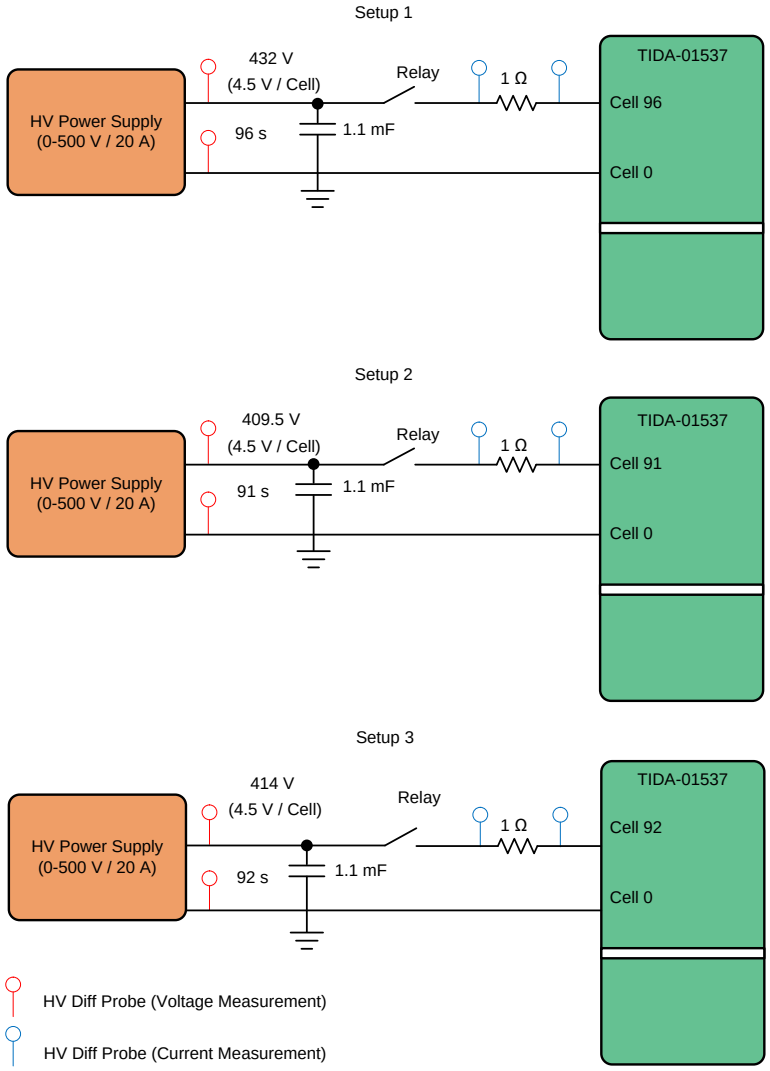
3.2.6 TIDA-01537 High Voltage Tests

3.2.6.1 Hot Plug Tests

The following equipment is used to perform the hot-plug tests:

- TIDA-01537 board
- Capacitor bank in parallel with HV power supply (1.1 mF)
- 1-Ω resistor (High Wattage)
- HV differential probe
- Oscilloscope
- 12-V supply (to control relay)
- HV power supply (to supply 4.5 V per cell)
- CANalyzer with Interfacing cable

Figure 55. TIDA-01537 Hot-Plug Setup



Precautions:

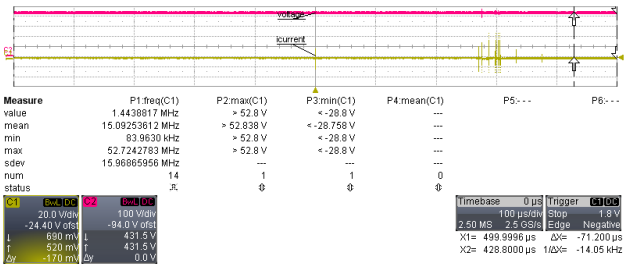
- Never touch the board when high voltage is turned ON
- High-voltage ground must be isolated with low-voltage ground and equipment
- Make sure the DC-Link capacitor is fully discharged before touching the HV lines, or the board
- The relay should be operated with the proper switch and safety instructions

Test Cases: The worst-case hot-plug scenarios were tested

- Cell 96-0 -> GND connected, relay for cell 96 (96s)
- Cell 91-0 -> GND connected, relay for cell 91 (91s)
- Cell 92- 0 -> GND connected, relay for cell 92 (92s)

Test Setup: General setups in Figure 55 were used for each test case, and a different cell was connected via relay. The input voltage was set to 4.5 V per cell and pre-charged a capacitor bank to supplement the power-supply current sourcing ability. A high-voltage differential probe was placed across the capacitor bank to measure the voltage, and an additional differential probe was placed across the 1-Ω resistor to measure the hot-plug current. The LeCroy Scope was triggered on the rising edge of the current spike, triggered by an AEV14012W relay supplied by a separate 12-V supply

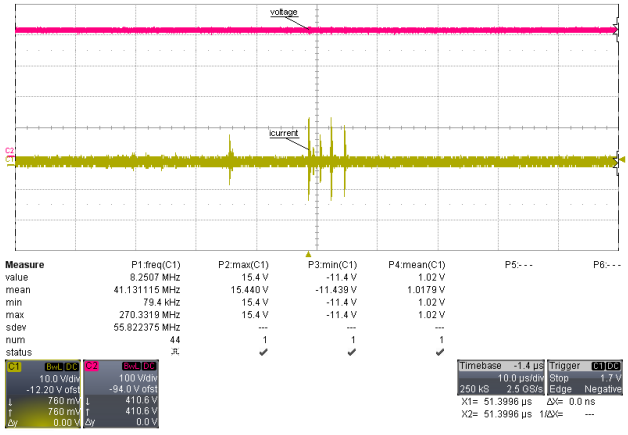
Figure 56. 96s Hot-Plug Tests Setup 1



CH1: High-voltage measurement
CH2: Hot-plug current measurement

Peak transient current measured for 96s hot plug = 52.8 A (52.8 V/1 Ω)

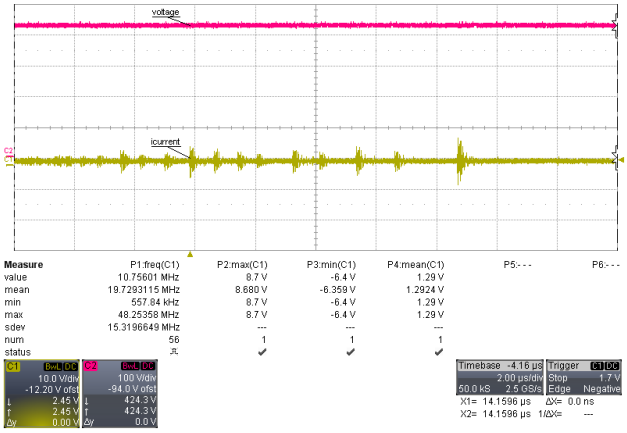
Figure 57. 91s Hot-Plug Tests Setup 2



CH1: High-voltage measurement
CH2: Hot-plug current measurement

Peak transient current measured for 91s hot plug = 15.44 A (15.44 V/1 Ω)

Figure 58. 92s Hot-Plug Tests Setup 3



CH1: High-voltage measurement
CH2: Hot-plug current measurement

Peak transient current measured for 91s hot plug = 8.68 A (8.68 V/1 Ω)

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01537.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01537.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01537.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01537.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01537.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01537.

5 Software Files

To download the software files, see the design files at TIDA-01537.

6 Related Documentation

1. Texas Instruments, *TMS570 Active Cell-Balancing Battery-Management Design Guide*
2. Texas Instruments, *TMS570LS04x/03x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual*
3. Texas Instruments, *Safety Manual for TPS65381-Q1 and TPS65381A-Q1 Multirail Power Supply Application Report*

6.1 Trademarks

General Texas Instruments High Voltage Evaluation (TI HV EMV) User Safety Guidelines

Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://ti.com/customer support for further information.

Save all warnings and instructions for future reference.

WARNING

Failure to follow warnings and instructions may result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety:
   a. Keep work area clean and orderly.
   b. Qualified observer(s) must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and non-conductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety:

   As a precautionary measure, it is always good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   a. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   b. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   c. Once EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.

3. Personal Safety
   a. Wear personal protective equipment e.g. latex gloves or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2018) to A Revision	Page
• Changed BQ79606-Q1 to BQ79606A-Q1 globally in design guide.	1

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