

Design Guide: TIDA-020000

Automotive 2.6-MP Camera Module Reference Design With POL PMIC, FPD-Link III, Supervisor, and POC



Description

This camera module reference design addresses the need for small cameras in automotive systems by combining a 2.6-megapixel (MP) imager with a 4-Gbps serializer while providing power supplies and voltage supervision for both devices in an ultra-small form factor. This design includes a high-speed serial interface to connect a remote automotive camera module to a display or machine vision processing system with a coaxial cable transmitting both data and power. Texas Instrument's 4-Gbps FPD-Link III SerDes technology used in this reference design enables the transmission of uncompressed 2.6-MP video data, bidirectional control signals, and power over coax (POC) using a single cable.

Resources

TIDA-020000	Design Folder
DS90UB953-Q1	Product Folder
TPS62162-Q1	Product Folder
TPS650002-Q1	Product Folder
TPS3703-Q1	Product Folder

Features

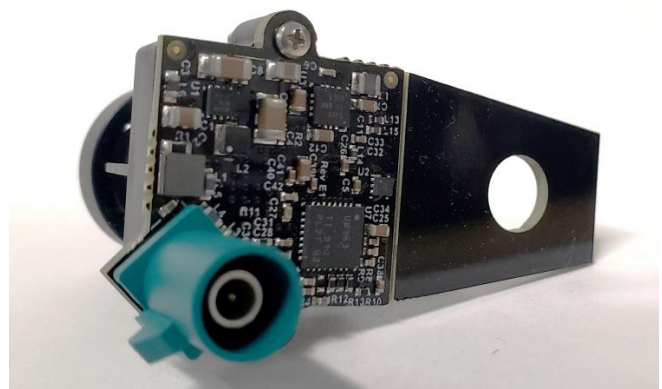
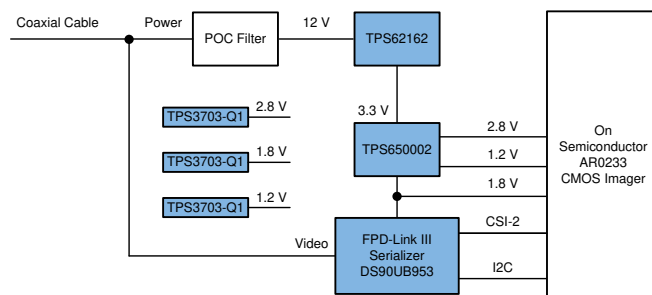
- Space-optimized design fits on single PCB 20 × 20 mm
- Power management integrated circuit (PMIC) used for additional power supply integration, allowing for both power supplies and voltage supervision in a small form factor
- 2.6-MP AR0233 image sensor from ON semiconductor providing up to 24-Bit MIPI CSI-2 HDR raw image data
- Single Rosenberger Fakra coaxial connector for digital video, power, control, and diagnostics
- Additional diagnostic capabilities to enable ASIL applications
- Includes design considerations and characterization test data

Applications

- ADAS vision systems
- Front camera
- Camera monitoring system (Mirror replacement)
- Surround view system



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1 System Description

For many automotive camera systems, small solutions are required. This reference design addresses these needs by combining a 2.6-megapixel (MP) imager with a 4-Gbps serializer and providing the necessary power supply for both. All of this functionality is contained on a 20×20-mm circuit board. The only connection required by the system is a single 50-Ω coaxial cable.

A combined signal containing the DC power, the FPD-Link front and backchannels enter the board through the FAKRA coaxial connector. The filter shown in Figure 1 blocks all of the high-speed content of the signal (without significant attenuation) while allowing the DC (power) portion of the signal to pass through inductor L5.

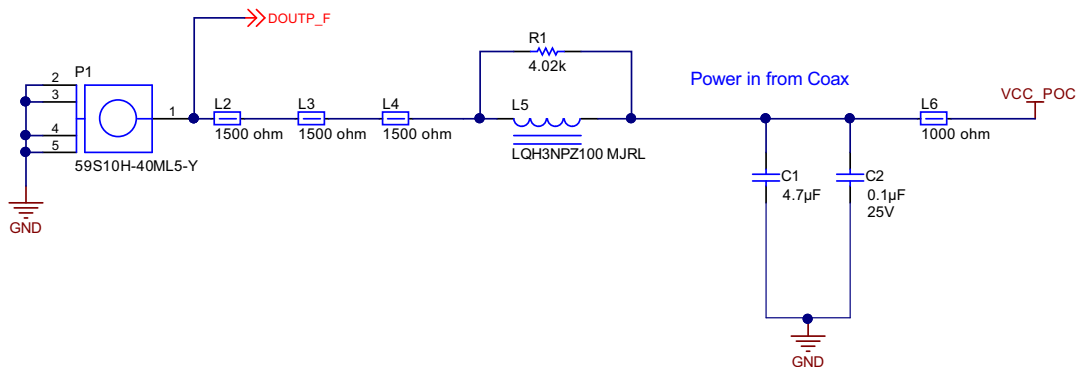


Figure 1. FPD-Link III Signal Path

The DC portion is connected to the input of the TPS62162-Q1 buck converter to output 3.3 V. The 1.8-V rail required by the serializer and the imager are created by the switching output of the TPS650002-Q1. The additional 2.8-V and 1.2-V rails required by the AR0233 imager are produced from the two LDO outputs of the TPS650002-Q1.

The high-frequency portion of the signal is connected directly to the serializer. This is the path that the video data and the control backchannel takes between the serializer and deserializer.

The output of the imager is connected through a four-lane MIPI CSI-2 interface to the serializer. Then the serializer transmits this video data over a single LVDS pair to the deserializer located on the other end of the coaxial cable.

On the same coaxial cable, there is separate low-latency, bidirectional control channel that transmits control information from an I²C port. This control channel is independent of video blanking period. It is used by the system microprocessor to configure and control the imager.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V _{IN}	Supply voltage	Power over coax (POC)	4	12	17	V
P _{TOTAL}	Total power consumption	V _{POC} = 12 V	—	0.72	—	W

2 System Overview

2.1 Block Diagram

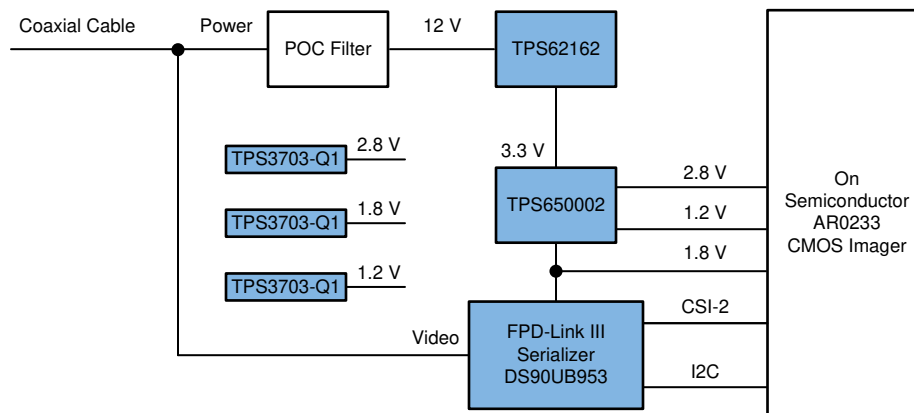


Figure 2. Camera Block Diagram

2.2 Highlighted Products

This reference design uses the following TI products:

- DS90UB953-Q1: the serializer portion of a chipset that offers an FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer and deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU).
- TPS62162-Q1: an automotive qualified step-down DC converter optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response.
- TPS650002-Q1: an automotive qualified single-chip power-management IC. This device combines a single 600-mA step-down converter with two 300-mA low-dropout (LDO) linear regulators. The step-down converter allows the use of a small inductor and capacitors to achieve a small solution size. The LDOs can operate with an input voltage range from 1.6 V to 6 V, thus allowing them to be supplied from the step-down converter.
- TPS3703-Q1: an automotive qualified integrated overvoltage and undervoltage window voltage detector with fixed voltage options and fixed reset time delay. This highly-accurate (0.7% max) voltage supervisor in small package (1.5 mm x 1.5 mm) is ideal for systems that operate on low-voltage supply rails and have narrow margin supply tolerances, especially in space constrain end equipments like remote automotive camera applications. Low threshold hysteresis options of 0.55% prevent false reset signals when the monitored voltage supply is in its normal range of operation.

Find more information on each device and why they were chosen for this application in the following subsections.

2.2.1 AR0233 Imager

Available from ON Semiconductor, this imager is a 1/2.5 in, 2.6-MP CMOS imager with high dynamic range (HDR). It is suitable for automotive systems and can provide a parallel 14-bit or four-lane MIPI CSI-2 output. Some additional features of the imager are:

- Supports image sizes: 2048x1280 at up to 45fps, 2048 x 1080 at up to 60fps
- Low power consumption
- Requires three voltage rails (2.8 V, 1.8 V, and 1.2 V)
- Can be configured using an I²C-compatible two-wire serial interface

2.2.2 DS90UB953-Q1

Using a serializer to combine 12-bit video with a bidirectional control signal onto one coaxial or twisted pair greatly reduces system complexity, cost, and cabling requirements. The CSI-2 input of the DS90UB953-Q1 mates well with the MIPI CSI-2 video output of the AR0233 imager. Once combined with the filters for the POC, video, I²C control, diagnostics, and power can all be transmitted up to 15 meters on a single inexpensive coaxial cable. For more information on the cable itself, see the [Cable Requirements for the DS90UB913A and DS90UB914A Application Report](#).

2.2.3 TPS62162-Q1

To keep the camera module small, the power supply must be small. The supply must also be efficient while not adding measurable noise to the video from the imager. Often, these two requirements stand in opposition. A switching power supply is more efficient than a linear regulator, but it can add noise to the system.

Camera sensor circuits usually are sensitive to noise at frequencies below 1 MHz, and in automotive applications staying above 2 MHz is desirable in order to avoid interference with the AM radio band. This means that the TPS62162-Q1 switching regulator operating at 2.25 MHz meets both requirements. This high switching frequency also helps to reduce the size of the discrete components in the circuit.

2.2.4 TPS650002-Q1

The TPS650002-Q1 power-management IC (PMIC) contains a single step-down DC/DC convertor with two LDO linear regulators, all providing excellent line and load transient performance with low quiescent current. The combination of these outputs on a single chip allows the 1.2-V, 1.8-V, and 2.8-V rails to be created in a very small space. The low output noise, high power-supply rejection ratio (PSRR) make the integrated LDOs ideal for this application and providing the 2.8-V noise sensitive analog rail.

2.2.5 TPS3703-Q1

The TPS3703-Q1 voltage supervisor adds an additional level of diagnostic functionality to the camera module by monitoring the 1.2-V, 1.8-V, and 2.8-V rails for the AR0233 imager and DS90UB953-Q1 serializer. The TPS3703-Q1 device has fixed voltage options from 500 mV to 5 V with a broad range of window thresholds from $\pm 3\%$ to $\pm 7\%$ of the nominal monitored voltage. The flexibility of threshold options for this supervisors makes it ideal for voltage monitoring in numerous automotive applications. The TPS3703-Q1 device does not require an external resistor divider for the threshold setting or external capacitor for reset time delay, this level of integration minimizes the total solution size and removes potential failures that come with discrete resistors and capacitors to help achieve a low system FIT rate (Failure in Time rate).

2.3 Design Considerations

The following subsections discuss the considerations behind the design of each subsection of the system.

2.3.1 PCB and Form Factor

This reference design is not intended to fit any particular form factor. The only goal of the design with regards to the PCB is to make as compact a solution as possible. The square portion of the board is 20 mm × 20 mm. The area near the board edge in the second image is reserved for attaching the optics housing that holds the lens.

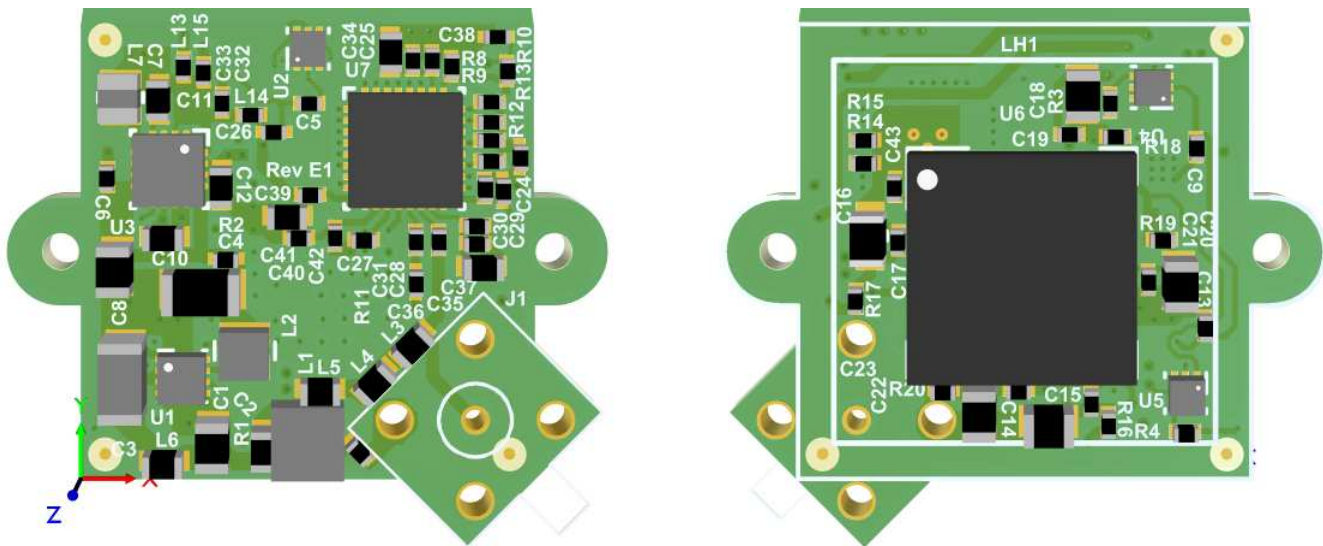


Figure 3. PCB Top and Bottom Views

2.3.2 Power Supply Design

2.3.2.1 POC Filter

One of the most critical portions of a design that uses POC is the filter circuitry. The goal is twofold:

1. Deliver a clean DC supply to the input of the switching regulators.
2. Protect the FPD-Link communication channels from noise coupled backwards from the rest of the system.

The DS90UB953-Q1 and DS90UB960-Q1 SerDes devices used in this system communicate over two carrier frequencies, 2 GHz at full speed ("forward channel") and a lower frequency of 25 MHz ("backchannel") determined by the deserializer device. The filter must attenuate this rather large band spanning both carriers, hoping to pass only DC.

For the POC design, to enable the forward channel and backchannel to pass uninterrupted over the coaxial cable, an impedance of > 2 k Ω across the 10-MHz to 2.2-GHz bandwidth is required. To accomplish this, an inductor is typically chosen for filtering the 10-MHz to 1-GHz range, while a ferrite bead is chosen for filtering the 1- to 2.2-GHz frequency band. This complete filter is shown by L2 in Figure 4. L1 is the same POC filter, but for the deserializer side of the FPD-Link III transmission.

In this camera design, it is imperative that this filter has the smallest footprint allowable. To accomplish this, the LQH3NPZ100MJRL 10- μ H inductor is chosen because it has a wide band impedance that filters from 10 MHz to 1 GHz. This eliminates the need for a solution that would typically require two inductors, one for the lower frequency and another for the higher frequency.

For the high-frequency forward channel filtering, inductors usually are not sufficient to filter above 1 GHz. This reference design uses three 1.5-k Ω ferrite beads in series with the 10- μ H inductor to bring the impedance above 2 k Ω across the 1- to 2.2-GHz range. This design uses three 1.5-k Ω ferrite beads because when in operation, the current through these devices reduces the effective impedance. Therefore three ferrite beads instead of two allows for more headroom across the whole frequency band. For good measure, this design uses a 4-k Ω resistor in parallel with the 10- μ H inductor to provide a constant impedance across the complete frequency band for impedance smoothing. With this approach, the solution size can be minimized on board for the POC inductor filtering. For more details, see the [Sending Power Over Coax in DS90UB913A Designs Application Report](#).

Lastly, in regards to filtering, ensuring that the FPD-Link signal is uninterrupted is just as important as providing a clean, noise-free DC supply to the system. To achieve this, AC coupling capacitors shown by the 0.033 μ F and 0.015 μ F are chosen to ensure the high-speed AC data signals are passed through but that the DC is blocked from getting on the data lines. A smaller capacitance is required for the DS90UB953-Q1 and DS90UB954-Q1 devices than previous generations, because they need to pass 4 Gbps of data while the previous generation only needed to pass the 2 Gbps of data seen on 1-MP cameras.

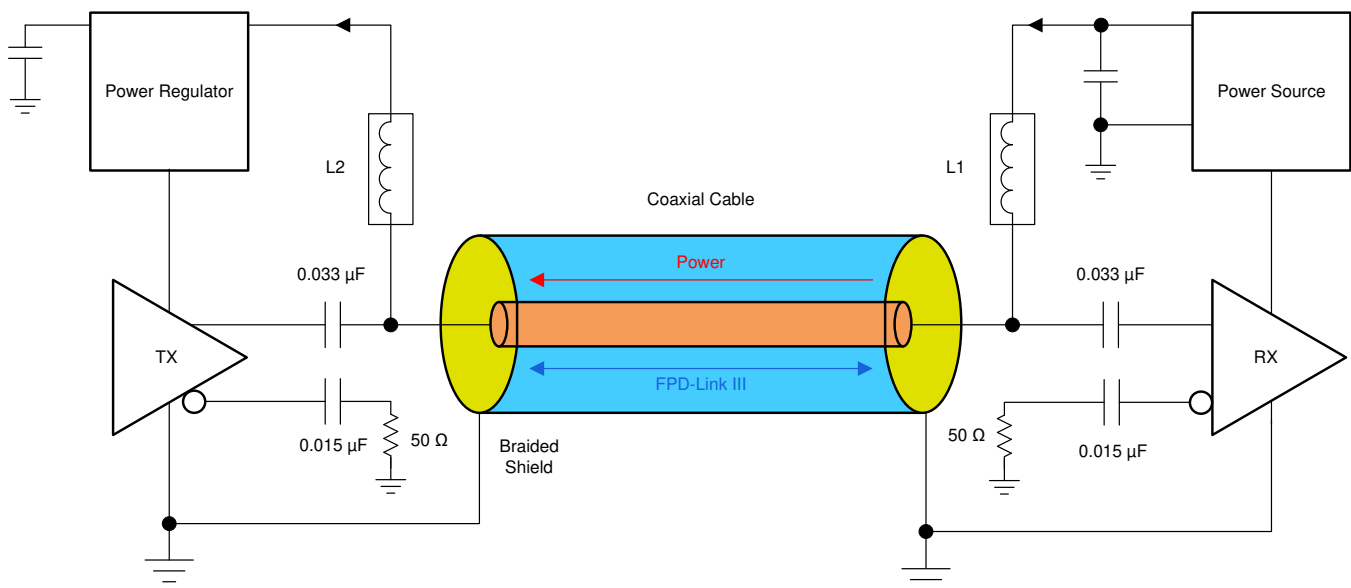


Figure 4. Power Over Coax

2.3.2.2 Power Supply Considerations

Because this reference design is targeted for automotive applications, there are a few considerations that restrict design choices. In addition, there are few systems-level specifications that shaped the overall design:

- The total solution size needs to be minimized to meet the size requirement of this design, which is less than 20 mm × 20 mm. This means choosing parts that integrate FETs, diodes, compensation networks, and feedback resistor dividers to eliminate the need for external circuitry.
- To avoid interference with the AM radio band, all switching frequencies need to be greater than 1700 kHz or lower than 540 kHz. Lower switching frequencies are less desirable in this case because they require large inductors and can still produce harmonics in the AM band. For this reason, this reference design looks at higher frequency switchers.
- All devices need to be AEC Q100 rated.

Before parts can be chosen, the input voltage range, required voltage rails, and required current per rail must be known. In this case, the input voltage is a pre-regulated 12-V supply coming in over the coaxial cable. This system has only two main devices, the imager and serializer, which consume the majority of the power; the current draw of the supervisors is insignificant and can be left out of these calculations. The requirements for these devices are shown in [Table 2](#):

Table 2. Power Budget

PARAMETER	VOLTAGE (V)	CURRENT (A)	POWER (W)
DS90UB953			
VDD-1.8	1.8	0.160	0.2880
AR0233			
VDD-1.2	1.2	0.192	0.2304
VDD_IO-1.8	1.8	0.001	0.0018
VAA-2.8	2.8	0.025	0.0700
RAIL TOTAL			
1.2-V rail	1.2	0.192	0.2304
1.8-V rail	1.8	0.353	0.6354
2.8-V rail	2.8	0.025	0.0700
3.3-V rail	3.3	0.218	0.7180

The 12-V supply over the coaxial is first stepped down to 3.3-V, which then supplies the rest of the system on the camera module. In this design, the 1.8-V rail also supplies the 1.2-V LDO of the TPS650002-Q1 device, which is reflected in the 1.8-V rail total. The 2.8-V rail requires 25 mA, the 1.8-V rail requires 355 mA, and the 1.2-V rail requires 192 mA. Based on these values, the 3.3-V supply needs to provide 218 mA to be able to power the 1.2-V, 1.8-V, and 2.8-V rails.

Because the input and output voltages, output current requirements, and total wattage consumption are known, calculate what the input current will look like with [Equation 1](#):

$$P_{OUT} = P_{IN} = I_{IN} \times V_{IN} \rightarrow 718 \text{ mW} = I_{IN} \times 12 \text{ V} \rightarrow I_{IN} = 59.8 \text{ mA} \quad (1)$$

These numbers give a good starting point for selecting the parts and topology for the regulators as well as inductor selections later on. However, this does not take into account the efficiencies of the power supplies and thus only provides an approximation.

As previously mentioned, the components in the power supply need to be Q100 rated, switch outside the AM band, and satisfy the voltage and current requirements as listed. Because the input voltage is a regulated voltage that will always be greater than any of the power rail needs, only choose from step-down converters and LDOs.

The key feature of the system is the small size, so integration of external circuitry is a high priority. Integrating FETs, compensation networks, and sometimes feedback, can significantly reduce total solution size. Many buck regulators integrate everything but the input/output capacitors and the inductor into very small packages.

To meet these small size requirements, the TPS65xxx PMIC (Power Management Multi-Channel IC) device family is a good candidate. These devices combine a single step-down converter with two LDO linear regulators in a small 3-mm x 3-mm package. For even further integration and design simplification, the TPS650002-Q1 device offers fixed output voltages: 1.8-V from the switching supply, with 2.8-V and 1.2-V from the LDOs.

Clearly the largest trade-off with using LDOs is that the efficiency drops significantly, increasing the total power consumption. This reference design is a lower-power design; however, in some situations a designer may sacrifice the efficiency to avoid the inherent noise and EMI issues associated with switching power supplies.

Ultimately, this reference design uses the TPS62162-Q1 device as a pre-regulator, and the TPS650002-Q1 PMIC to power the system. The TPS62162-Q1 switching supply steps down the 12-V POC input to 3.3-V. This 3.3-V rail then supplies power to the TPS650002-Q1 PMIC, which provides all voltage rails required for the system. For the TPS650002-Q1, the 1.8-V switching output is cascaded into the 1.2-V LDO, and the 2.8-V LDO is supplied by the 3.3-V system supply from the TPS62162-Q1 device. All of the power rails provided by the TPS650002-Q1 PMIC device are cascaded from the 3.3-V provided by the TPS62162-Q1 device. Functionally, the cascaded topology means that the output current is sufficient such that the TPS62162-Q1 device does not operate in discontinuous mode, allowing better predictions and control of the switching noise produced by the devices, as well as better efficiency.

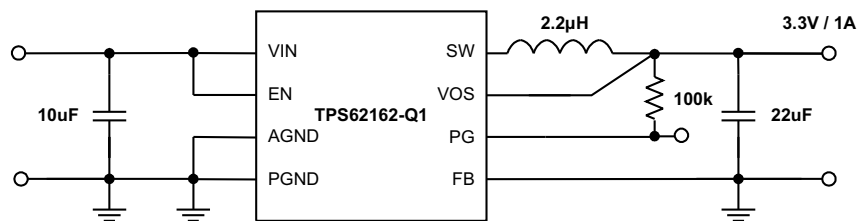


Figure 5. TPS62162-Q1 Typical Application Circuit

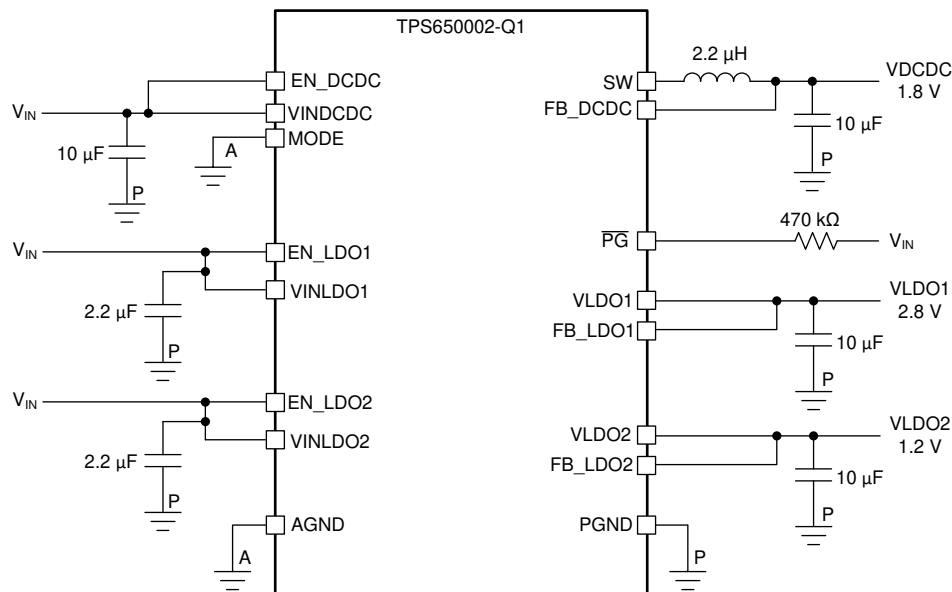


Figure 6. TPS650002-Q1 Typical Application Circuit

Component selection and design theory is found in the *Application Information* section of the device data sheets: [TPS6216x-Q1 3-V to 17-V 1-A Step-Down Converter with DCS-Control™](#) and [TPS65000-Q1 2.25-MHz Step-Down Converter With Dual LDOs](#).

2.3.2.2.1 Choosing the TPS62162-Q1 Output Inductor and Capacitor

As mentioned in [Section 2.3.2.2](#), the switching frequency of the converter must remain above 1700 kHz. This means that the converter must always operate in continuous mode. Because input voltage and output voltage are fixed and the output current is almost constant and can be predicted easily, the minimum inductance, L , for the converter to operate with continuous inductor current can be calculated using [Equation 2](#):

$$L_{\text{MIN}} = \frac{V_{\text{OUT}} \times (V_{\text{IN}(\text{MAX})} - V_{\text{OUT}})}{(2 \times V_{\text{IN}(\text{MAX})} \times I_{\text{OUT}} \times f)} = \frac{[3.3 \text{ V} \times (17 \text{ V} - 3.3 \text{ V})]}{(2 \times 17 \text{ V} \times 0.218 \text{ A} \times 2.25 \text{ MHz})} = 2.71 \text{ } \mu\text{H} \quad (2)$$

Because 2.7 μH is not a standard value and the design must use an inductor value above this, a higher value of 3.3 μH is chosen. The higher inductance value also helps minimize the voltage and current ripple of the output.

Due to the fact that this device is internally compensated, it is only stable for certain component values in the LC output filter. The application note on optimizing the output filter[6] has the chart of stable values shown in [Table 3](#). The value 3.3 μH is on this chart and with these recommended values, this reference design uses a 22- μF output capacitor and remains in the stable region of effective corner frequencies.

Table 3. Stability versus Effective LC Corner Frequency

NOMINAL INDUCTANCE VALUE	NOMINAL CERAMIC CAPACITANCE VALUE (EFFECTIVE = ½ NOMINAL)								
	4.7 μF	10.0 μF	22 μF	47 μF	100 μF	200 μF	400 μF	800 μF	1600 μF
EFFECTIVE CORNER FREQUENCIES (kHz)									
0.47 μH	151.4	103.8	70.0	47.9	32.8	23.2	16.4	11.6	8.2
1.00 μH	103.8	71.2	48.0	32.8	22.5	15.9	11.3	8.0	5.6
2.2 μH	70.0	48.0	32.4	22.1	15.2	10.7	7.6	5.4	3.8
3.3 μH	57.2	39.2	26.4	18.1	12.4	8.8	6.2	4.4	3.1
4.7 μH	47.9	32.8	22.1	15.1	10.4	7.3	5.2	3.7	2.6
10.0 μH	32.8	22.5	15.2	10.4	7.1	5.0	3.6	2.5	1.8
	Recommended for TPS6213x, TPS6214x, TPS6215x, TPS6216x, and TPS6217x								
	Recommended for TPS6213x, TPS6214x, and TPS6215x only								
	Stable without Cff (within recommended LC corner frequency range)								
	Stable without Cff (outside recommended LC corner frequency range)								
	Unstable								

With the inductance value chosen, the design now needs an inductor with a proper saturation current. This is going to be the combination of the steady-state supply current as well as the inductor ripple current. The current rating needs to be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. Calculate the inductor ripple current from [TPS6216x-Q1 3-V to 17-V 1-A Step-Down Converter with DCS-Control™](#) using [Equation 3](#):

$$\Delta I_{L(\text{max})} = V_{\text{OUT}} \times \left(\frac{1 - \frac{V_{\text{OUT}}}{V_{\text{IN}(\text{max})}}}{L(\text{min}) \times f_{\text{SW}}} \right)$$

where:

- $I_L(\text{max})$ is the maximum inductor current
 - ΔI_L is the peak-to-peak inductor ripple current
 - $L_{(\text{min})}$ is the minimum effective inductor value
 - f_{SW} is the actual PWM switching frequency
- (3)

The parameters for this reference design using the TPS62162-Q1 are:

- $V_{\text{OUT}} = 3.3 \text{ V}$
- $V_{\text{IN}(\text{max})} = 17 \text{ V}$
- $L_{(\text{min})} = 3.3 \text{ } \mu\text{H}$

- $f_{SW} = 2.25$ MHz

These parameters yield an inductor current of $\Delta I_L = 360$ mA. The maximum current draw of the system through this regulator is 270 mA. Finally, [Equation 4](#) gives the minimum saturation:

$$L_{SAT} \geq I_{OUT(MAX)} + \frac{\Delta I_L(max)}{2} = 270 \text{ mA} + \frac{360 \text{ mA}}{2} = 450 \text{ mA} \quad (4)$$

The TPS62162-Q1 on this design uses a Coilcraft® XPL2010-332MLB, which has a saturation current of 700 mA with a 10% drop-in inductance. This part comes in a very small 1.9-mm x 2.0-mm package.

2.3.2.2.2 Choosing the TPS650002-Q1 Output Inductor and Capacitor

Similar to the TPS62162-Q1, this device is internally compensated, and is only stable for certain component values in the LC output filter. The TPS650002-Q1 has internal loop compensation to work with a specific output filter corner frequency, with $L = 2.2$ μ H and $C_{out} = 10$ μ F as the recommended value. This design uses these recommended inductor and capacitor values. If selecting different values, the product of $L \times C_{out}$ must be constant while selecting a smaller inductor or increasing capacitor value.

Once the inductance value is chosen, we again need to determine the saturation requirement of the inductor by combining the steady-state supply current and the inductor ripple current. The current rating needs to be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. Calculate the inductor ripple current from [TPS65000-Q1 2.25-MHz Step-Down Converter With Dual LDOs](#) using [Equation 5](#):

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f}$$

where:

- f = Switching Frequency (2.25-MHz typical)
 - L = Inductor Value
 - ΔI_L = Peak-to-peak Inductor Ripple Current
- (5)

The parameters for this design using the TPS650002-Q1 are:

- $V_{OUT} = 1.8$ V
- $V_{IN} = 3.3$ V
- $L = 2.2$ μ H
- $f_{SW} = 2.25$ MHz

These parameters yield an inductor current of $\Delta I_L = 166$ mA. The maximum current draw through this regulator is 353 mA. Finally, [Equation 6](#) gives the minimum saturation current:

$$L_{SAT} \geq I_{OUT(MAX)} + \frac{\Delta I_L(max)}{2} = 353 \text{ mA} + \frac{166 \text{ mA}}{2} = 436 \text{ mA} \quad (6)$$

The TPS650002-Q1 on this design uses a Murata® LQM2MPN2R2NG0, which has a rated current of 900 mA at an ambient temperature of 125°C. This part comes in a very small 1.6-mm x 2.0-mm package.

The LDOs on the TPS650002-Q1 are a bit simpler to design for as they do not require any output inductor. The only considerations for these LDOs are sizing the capacitance of the ceramic output capacitors. For the TPS650002-Q1 LDO outputs on this design, the recommended capacitance values of 10 μ F are used for both the 2.8-V and 1.2-V rails. The capacitor can benefit from using a X5R or X7R capacitor for better performance over a wider temperature range.

2.3.3 Voltage Monitoring and Diagnostics (TPS3703-Q1)

This design uses supervisors to monitor the regulation of all three power rails (1.2 V, 1.8 V, and 2.8 V). If needed, the output of these supervisors can be utilized as part of a functional safety implementation. The supervisor outputs are routed to GPIO pins on the DS90UB953-Q1 serializer. This allows them to be transmitted over the backchannel on the coaxial cable to the deserializer. These signals can then be outputted to GPIO pins on the deserializer side, and read by an MCU or processor.

The TPS3703-Q1 device has open-drain, active-low outputs. This means that the output requires a pullup resistor, and the signal is high when the voltage is within the specified window. When the monitored voltage falls out of regulation, the output is then pulled low. The use of open-drain outputs allows the outputs of multiple supervisors to be tied together directly and create an OR logic, where the signal will be pulled low if either supervisor detects voltage out of regulation. This design takes advantage of this fact in order to reduce the number of GPIOs used on the DS90UB953-Q1 serializer. The two TPS3703-Q1 supervisors, monitoring the 1.2-V and 1.8-V digital rails, are tied together. This allows for the TPS3703-Q1 device, monitoring the sensitive 2.8-V analog rail, to have its own GPIO pin. This results in one GPIO dedicated to monitoring both digital rails, and a second GPIO dedicated to monitoring the analog rail for the imager.

Once these signals are received on the deserializer side, an MCU or processor can then send commands over the coaxial cable back to the camera module. For example, one of the GPIO pins on the DS90UB953 serializer is tied to the reset pin of the AR0233 imager, and could be used to reset the imager device. The serializer is also capable of being reset through the 'RESET_CTL' register (Address 0x01), which can be accessed over I2C communications from the deserializer side. If the MCU is controlling the power supply providing the power over coax voltage, this signal could also be used to cycle the power to the entire camera module.

3 Hardware, Testing Requirements, Test Results

3.1 Required Hardware

This reference design needs only one connection to a system with a compatible deserializer over the FAKRA connector as shown in [Figure 7](#).

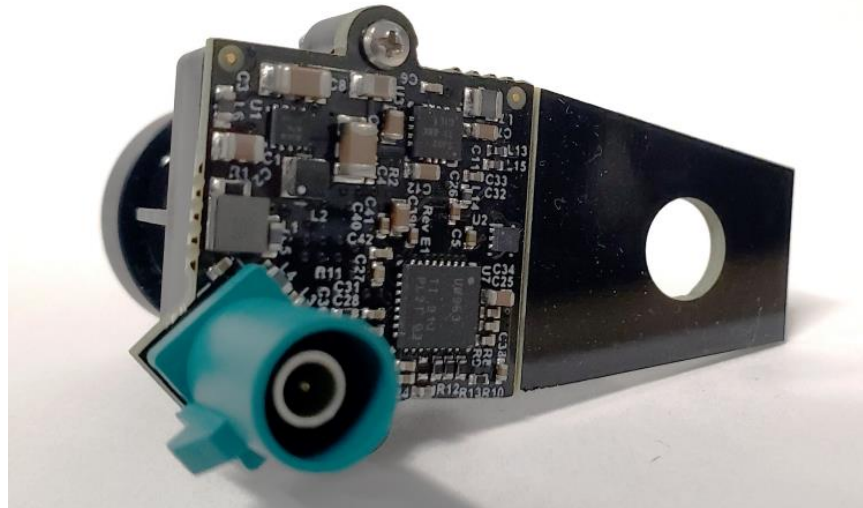


Figure 7. Getting Started With the Board

3.1.1 Video Output Hardware Setup

[Figure 8](#) shows the setup to test the video output of the camera module on this reference design. This reference design includes an AR0233 image sensor, which connects to the DS90UB953-Q1 serializer over CSI-2 and I²C interfaces. The DS90UB953-Q1 serializer then connects through POC to a DS90UB960-Q1 quad deserializer. Note that for test setup, only one channel is used from the DS90UB960-Q1 device.

To enable video output from the DS90UB960-Q1 device, the EVM is connected to the CSI-2 Samtec connector on the TDA3x EVM. The TDA3x EVM enables video output by writing all the backchannel I²C setting configurations for the AR0233, DS90UB953-Q1, and DS90UB960-Q1 devices. When these writes are completed, Vision SDK software enables video output to an HDMI-connected monitor.

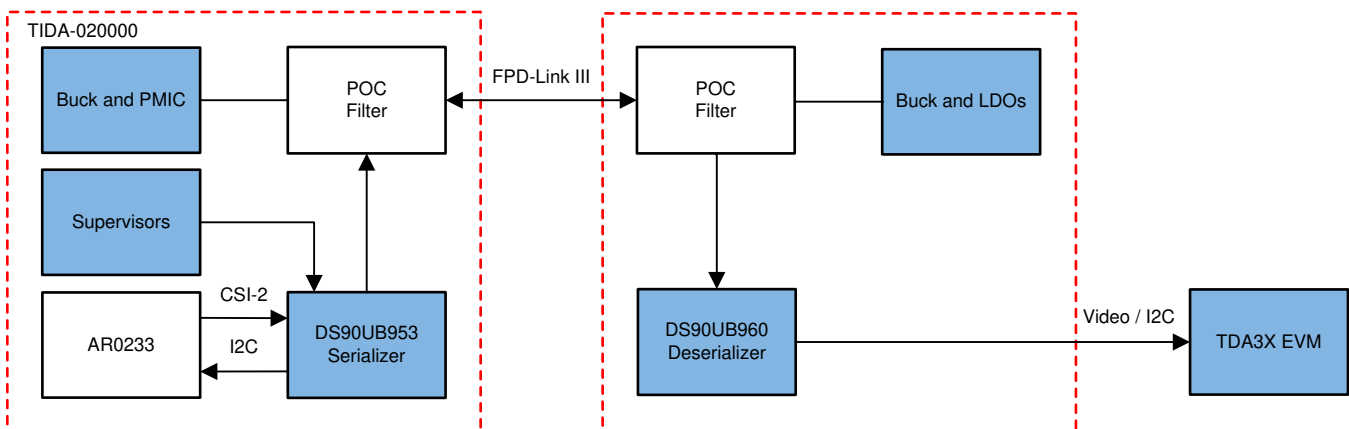


Figure 8. Block Diagram of Video Output Setup

3.1.2 FPD-Link III I²C Initialization

With the setup in [Figure 8](#) connected, the TIDA-01323 design is supplied input power and this is delivered to the POC supply for the camera power of this reference design and also is used to step down to 1.8 V and 1.1 V for the DS90UB960-Q1 supplies. Now the AR0233, DS90UB953-Q1, and DS90UB960-Q1 devices have power. Lastly, by connecting the TDA3x EVM to the TIDA-01323 design, the I²C writes for initialization can begin. Note that the following writes are only showing one channel camera and may not be the mode wanted for specific multi-camera mode. For example, each camera requires its own port initialization using address 0x4C for that specific port. The writes to initialize the DS90UB960-Q1 deserializer and DS90UB953-Q1 serializer are as follows:

- Deserializer slave I²C address 0x7A (8-bit) or 0x3D (7-bit):
 - Register 0x4C with 0x01: Enables write enable for Port 0
 - Register 0x58 with 0x5D: I²C passthrough enabled and backchannel frequency select
 - Register 0x5C with 0xE8: Sets serializer alias to 0xE8 (8-bit) or 0x74 (7-bit)
 - Register 0x5D with 0x80: Sets slave ID for imager to 0x80 (8-bit) or 0x40 (7-bit)
 - Register 0x66 with 0x80: Sets slave alias for imager to 0x80 (8-bit) or 0x40 (7-bit)
 - Register 0x6D with 0x7C: Configures port to coaxial mode and FPD III to CSI mode
 - Register 0x32 with 0x01: Enables TX write enable for port 0 and port 1
 - Register 0x33 with 0x03: Enables DS90UB960-Q1 CSI output and sets to 2 lane mode
 - Register 0x21 with 0x03: Sets round robin forwarding for CSI0 and CSI1
 - Register 0x20 with 0x00: Forwarding enabled for all ports and ports forwarded to CSI-2 Port 0
- Serializer slave I²C address 0xE8 (8-bit) or 0x74 (7-bit):
 - Register 0x06 with 0x21: Sets HS_CLK_DIV and DIV_M_VAL for CLKOUT from DS90UB953-Q1 to AR0233
 - Register 0x07 with 0x2A: Sets DIV_N_VAL for CLKOUT from DS90UB953-Q1 to AR0233
 - Register 0x0E with 0x3C: Sets GPIO0 and GPIO1 as outputs, and GPIO2 and GPIO3 as inputs on DS90UB953-Q1
 - Register 0x0D with 0x01: Pulls RESET pin on AR0233 high to bring imager out of reset

3.1.3 AR0233 Initialization

Once the FPD-Link III setup is done for the DS90UB953-Q1 and DS90UB960-Q1 devices, the I²C initialization can now be done on the AR0233. For these writes, see the AR0233 data sheet for register settings. There are many register settings listed, but as long as the DS90UB953-Q1 and DS90UB960-Q1 FPD-Link III parts are configured, the I²C backchannel allows for the AR0233 to be accessed at address 0x80 in 8-bit addressing or 0x40 in 7-bit addressing.

3.2 Testing and Results

3.2.1 Characterization Test Setup

For the following tests to verify power supply and I²C communication, the camera is connected to [TIDA-01323](#), a quad 2-MP FPD-Link III hub which utilizes the DS90UB960-Q1 deserializer. The [TIDA-01323](#) then connects to the [TDA3XEVM](#).

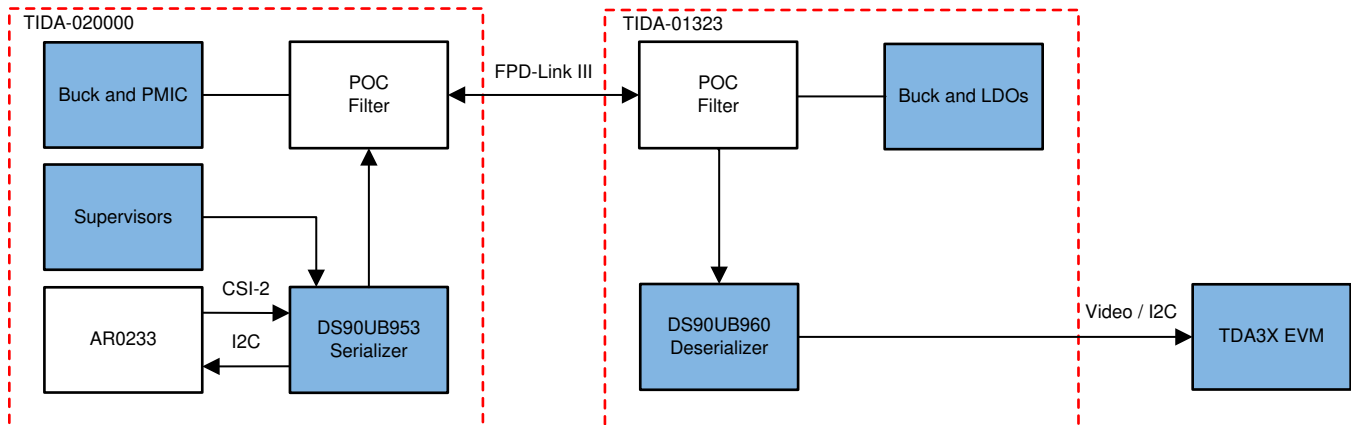


Figure 9. Block Diagram of Characterization Test Setup

3.2.1.1 Power Supplies Startup

Figure 10 shows the probe setup to measure the power sequence turnon for the system power, measuring 12-V input from POC and the 3.3-V supply to the system.

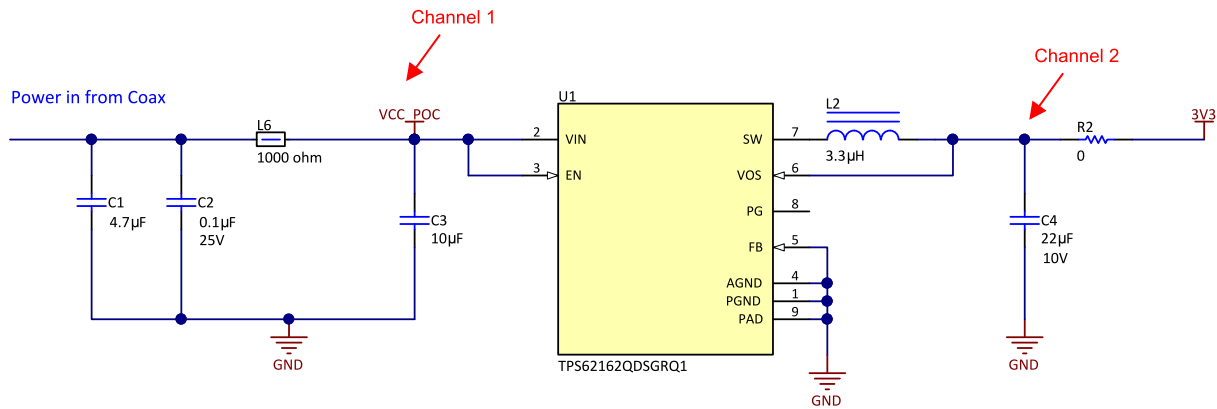


Figure 10. Measuring System Power Supply

Figure 11 shows the probe setup to measure the power sequence turn on for the point-of-load power, measuring the 3.3-V system supply, 2.8-V supply to imager, 1.8-V to the imager and serializer, and 1.2-V to the imager.

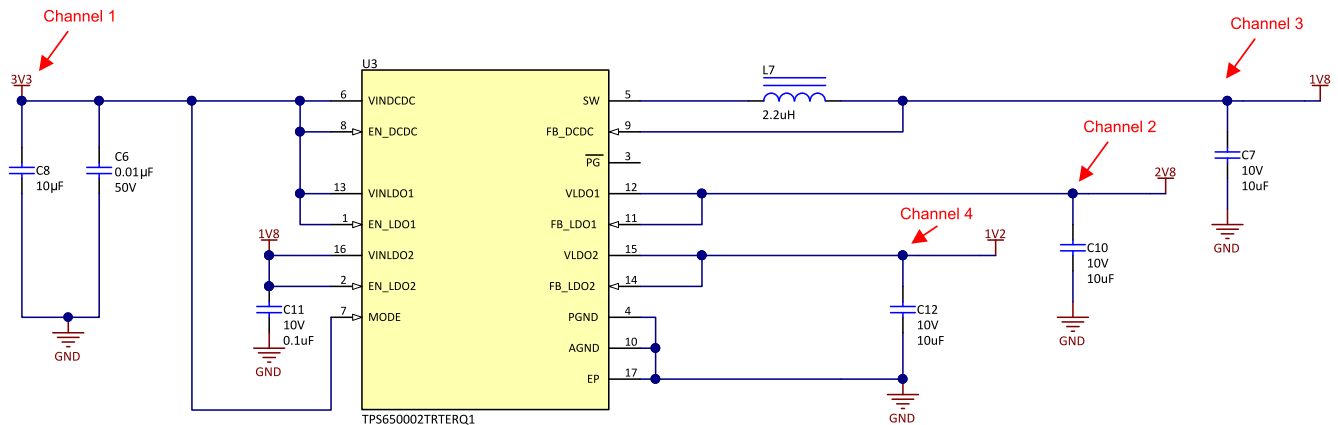


Figure 11. Measuring Point-of-Load Power Supplies

3.2.1.2 Power Supply Startup—1.8-V Rail and Serializer PDB Setup

For the serializer to be initialized after the 1.8-V power supply comes up, an RC time constant delay is added to the 1.8-V power supply of the DS90UB953-Q1 serializer. This ensures that the PDB reset line goes high only after the supply is high.

3.2.1.3 Setup for Verifying I²C Communications

For this test, a logic analyzer with I²C decode is used to monitor the I²C traffic on the buses. The two buses of interest are:

1. I²C connection from serializer to imager (shown as I2C_camera)
2. I²C connection from microprocessor to deserializer (shown as I2C_uC)

Connections are made to both the clock and data lines of each bus as shown in Figure 12.

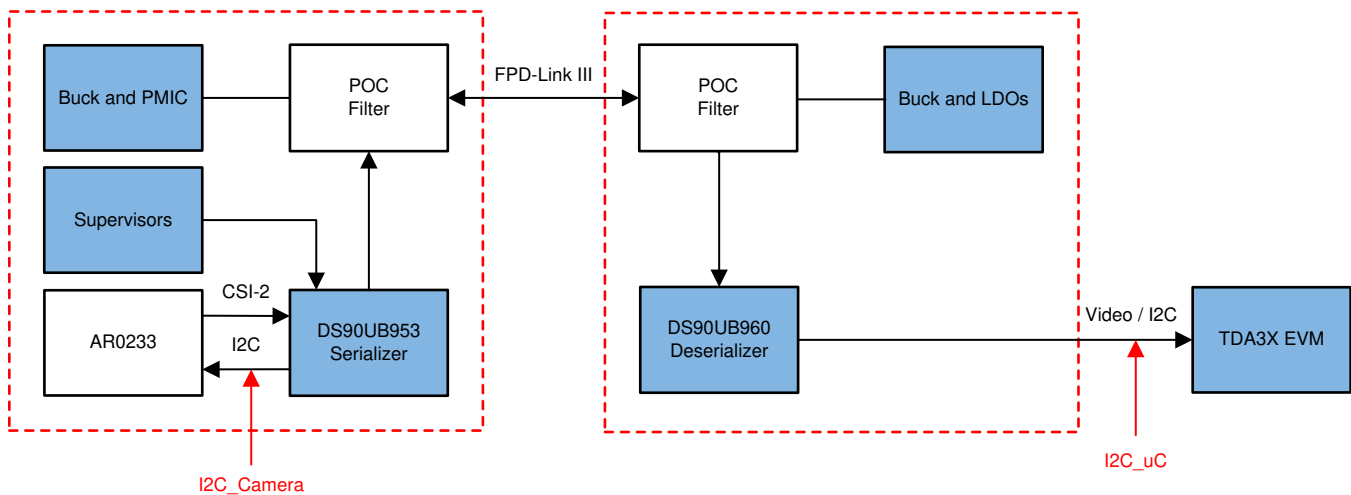


Figure 12. Setup for Monitoring I²C Transactions

3.2.2 Characterization Test Data

The following sections show the test data from verifying the functionality of the camera design.

3.2.2.1 Power Supplies Startup

Power startup behavior for the input power supply, and a 3.3-V system supply is shown in Figure 13. The startup sequence shows that when the 12-V input reaches turnon voltage for the TPS62162-Q1 device, the 3.3-V supply starts turning on.

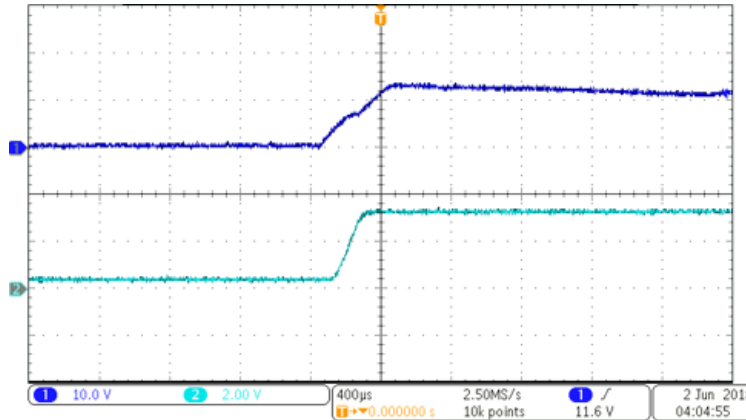


Figure 13. System Power Supply Startup

The same behavior is exhibited for the 2.8-V, 1.8-V, and 1.2-V supplies, which start turning on when the 3.3-V output has reached the minimum input needed for the switching supplies and LDOs of the TPS650002-Q1 device. Figure 14 shows the 3.3-V system supply followed by the 2.8-V analog rail from the LDO, the 1.8-V rail from the switching supply, and finally the 1.2-V rail from the second LDO.

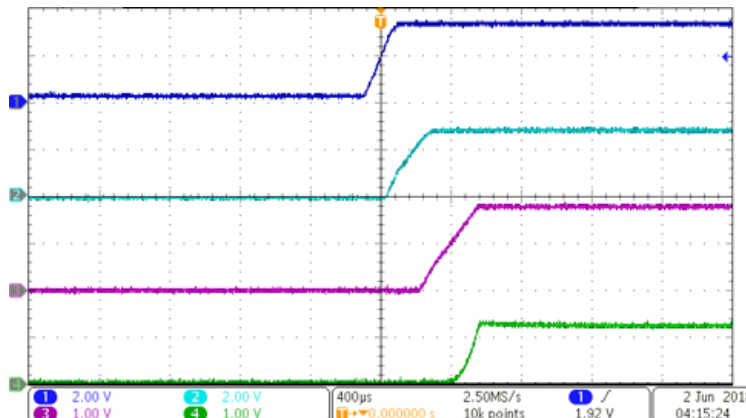


Figure 14. Point-of-Load Power Supply Startup

3.2.2.2 Power Supply Startup—1.8-V Rail and PDB

The only startup requirement is that the PDB pin of the serializer remains low until all power supplies stabilize to their final voltages. Figure 15 shows the power supply startup.

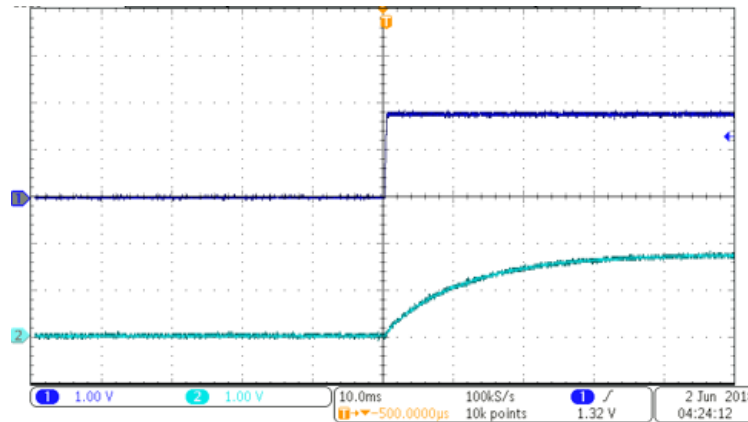


Figure 15. Serializer Power-Up Sequence

NOTE: Channel 1 (blue) 1.8 V; Channel 2 (turquoise) PDB

Figure 15 shows that PDB comes to $V_{DD} \times 0.65$ in 10 ms because of the 1- μ F delay capacitor on the PDB pin. This delay is more than sufficient for the PDB pin, which is required to come up only after the 1.8-V supply is stable.

3.2.2.3 Power Supply Voltage Ripple

To achieve a quality output video stream, the output voltage ripple on the AR0233 and DS90UB953-Q1 supplies must be low so that it does not affect the integrity of the high-speed CSI-2 data and internal PLL clocks. Measurements for 3.3-V, 2.8-V, 1.8-V, and 1.2-V rails are shown in Figure 16, Figure 17, and Figure 18, respectively. The key rails that are significant to impact on the imager are the 2.8-V and 1.2-V rails because 2.8 V is the analog rail and 1.2 V is the VDD rail for the imager. As measured, the 2.8-V and 1.2-V rails have less than a 1% ripple. The 1.8-V rail is significant to the serializer, as it supplies the VDD and VDD_PLL rails. The 1.8-V rail has great voltage ripple performance at 0.5%. The 3.3-V rail powers the entire system and also has excellent ripple performance of 0.4%. The voltage ripple on all rails is low enough for video output to be successfully transmitted.

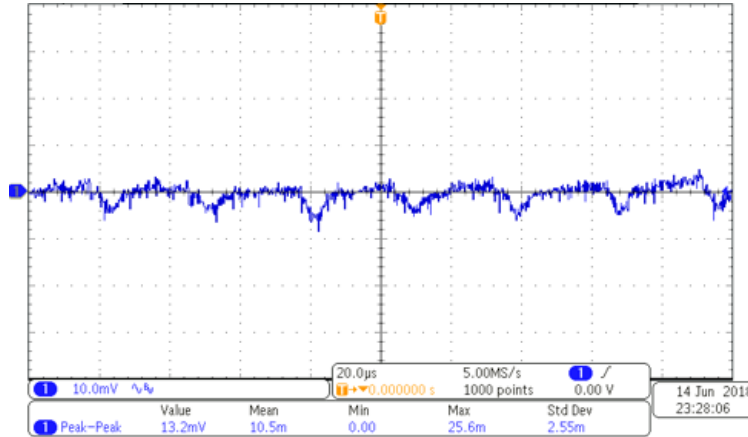


Figure 16. 3.3-V Output Voltage Ripple

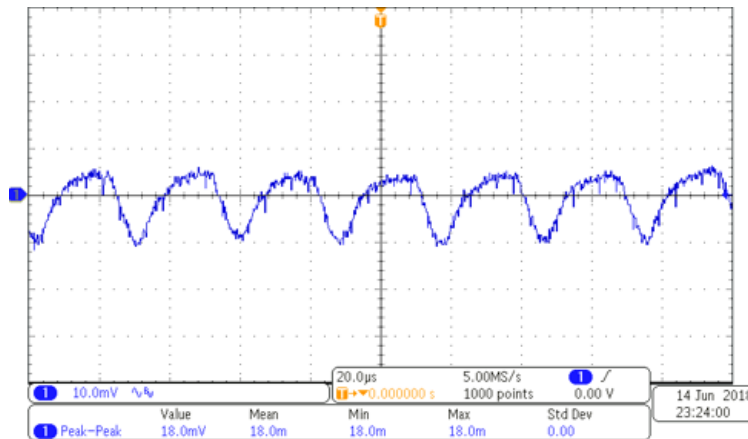
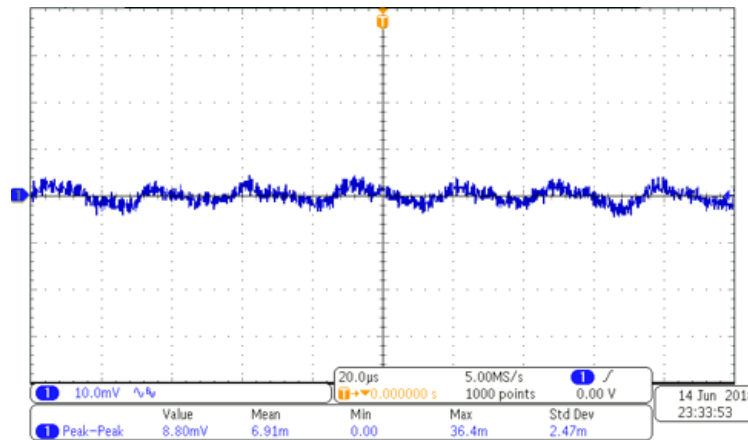
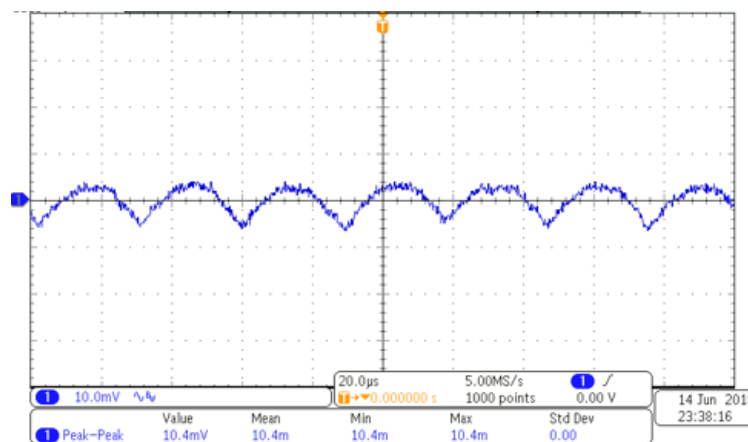


Figure 17. 2.8-V Output Voltage Ripple


Figure 18. 1.8-V Output Voltage Ripple

Figure 19. 1.2-V Output Voltage Ripple

3.2.2.4 Power Supply Load Currents

The last measurements to take in regard to the power supplies on the camera module are the load currents for the system supply, and the load currents on the AR0233 imager. These measurements verify total power consumption of the camera module as well as the load current for each individual rail on the AR0233 imager. For the following test data, each rail is drawing the specific load current outlined for the serializer and imager. All load current measurements are taken while a video output stream is present.

Figure 20 and Figure 21 show the 12-V and 3.3-V load currents measured on this reference design. The 12-V load current is the total input load for the camera module and measures at 55 mA. With this amount of current, the total input power consumption of the camera module is 660 mW. The 3.3-V system voltage from the TPS62162-Q1 is measured to be drawing 172 mA.

These values give both the input and output currents and voltages for the TPS62162-Q1 device, providing an estimate of the efficiency for this switching supply. The input power already mentioned is 660 mW from the 12-V power over coax. For the output power, using measured voltages of 3.29 V on the board and 172 mA, the total output power is 566 mW. To calculate system efficiency, the output power is divided by the input power to get 86%. With the larger step-down from 12 V to 3.3V and a fairly low load current, 86% efficiency is reasonable.

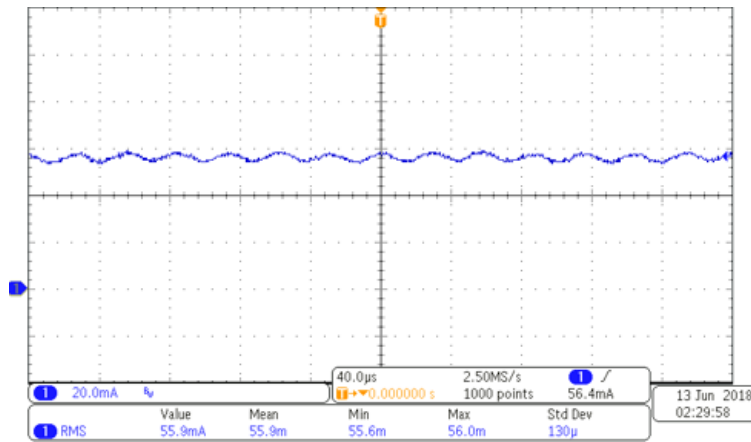


Figure 20. 12-V Input Load Current

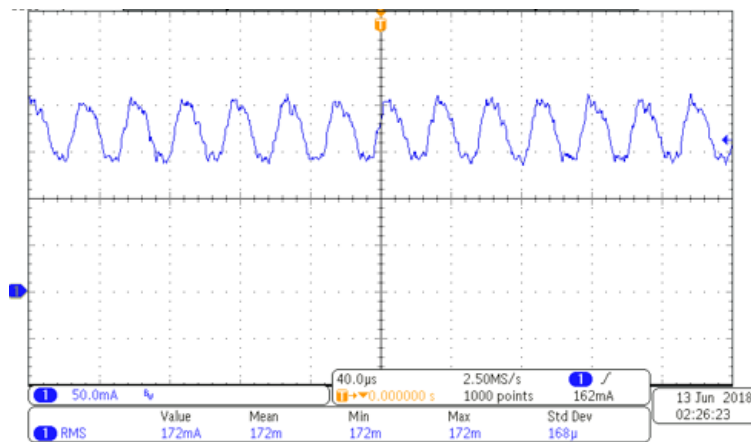


Figure 21. 3.3-V Output Load Current

Figure 22 through Figure 26 show the current measurements for each individual rail on the AR0233 imager. Each rail shows a periodic waveform that corresponds with the frame rate of the imager running at 30 fps during these tests, with the exception of the VDD_IO rail which is not affected by the frame rate. The 2.8-V load supplies the VAA and VAA_PIX analog rails, which consume 22 mA and 6 mA, respectively. The 1.8-V load supplies the VDD_IO rail, which consumes 13 mA. Finally, the 1.2-V load supplies the VDD and VDD_PHY rails, which consume 107 mA and 11 mA, respectively.

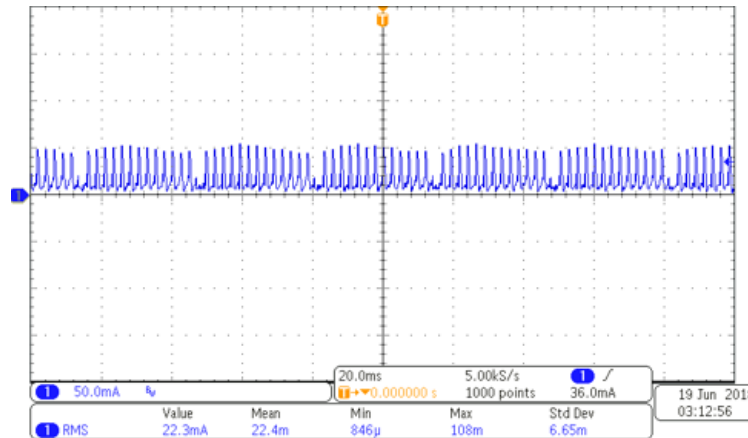


Figure 22. 2.8-V VAA Load Current

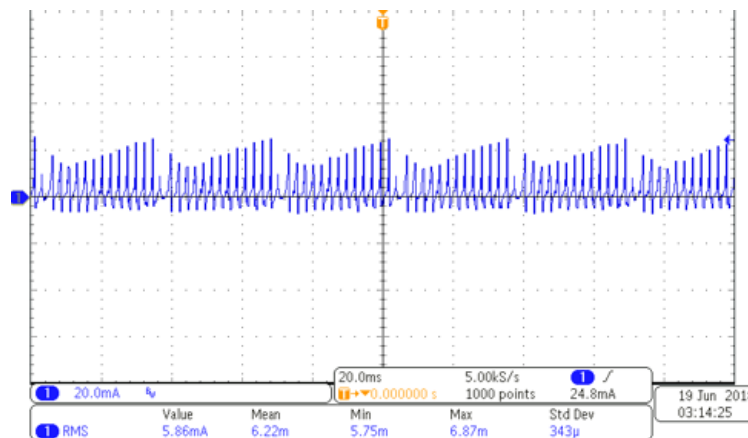


Figure 23. 2.8-V VAA_PIX Load Current

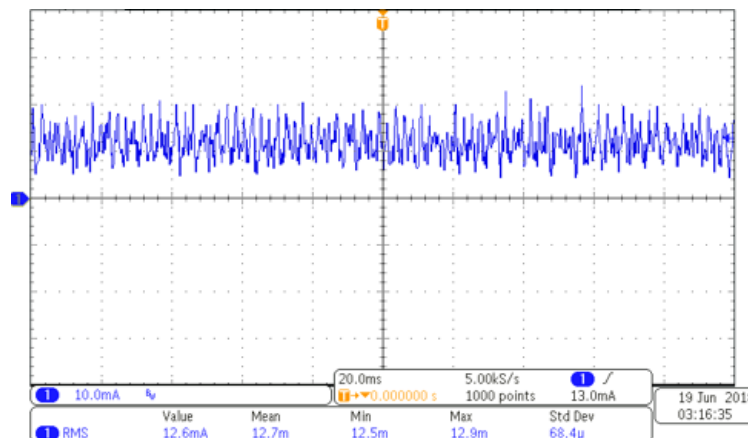


Figure 24. 1.8-V VDD_IO Load Current

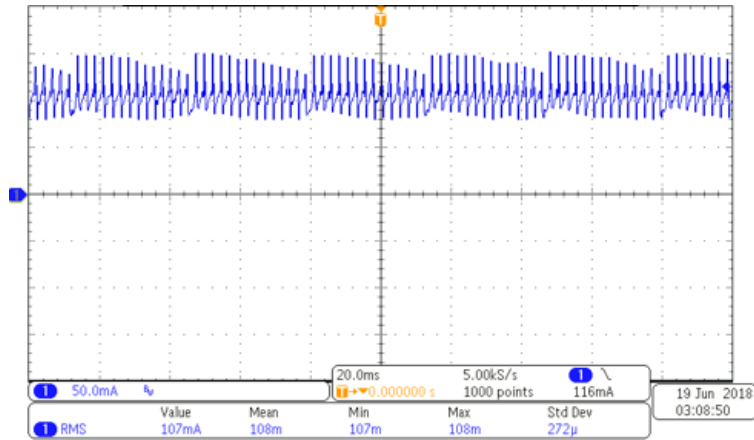


Figure 25. 1.2-V VDD Load Current

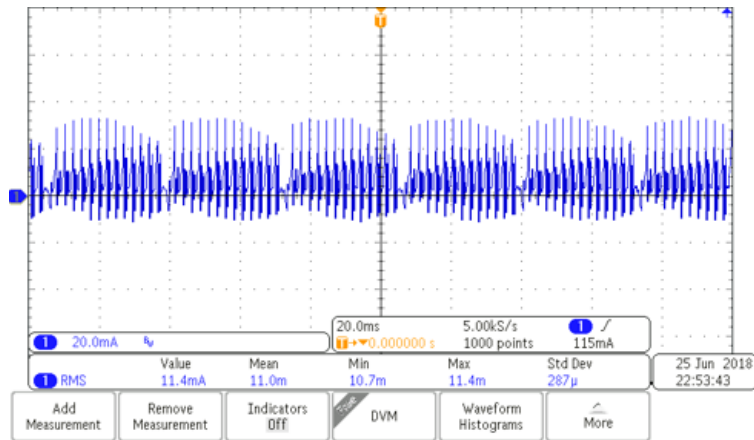


Figure 26. 1.2-V VDD_PHY Load Current

3.2.2.5 I²C Communications

Now that the power supplies are up and running, the I²C communication between the processor and the AR0233 imager over the FPD-Link III backchannel can be confirmed. Figure 27 shows a read I²C communication from the TDA3x EVM to the AR0233 imager on this reference design.

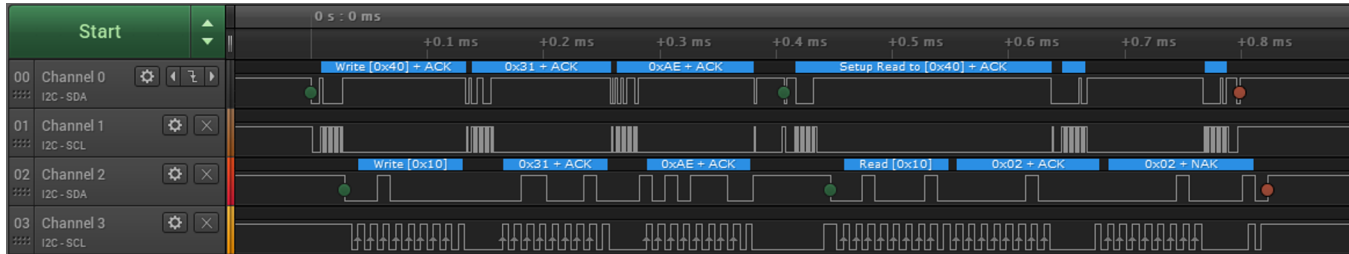


Figure 27. I²C Transactions

Channel 00 and 01 is the read I²C transactions at the processor and is measured at the deserializer side between the host microprocessor and the DS90UB960-Q1 device. The read is to the imager, which is at slave alias address 0x40. The read to the imager is for its register 0x31AE with data 0x0202, which shows the imager is set up to operate CSI in 2-lane mode.

Channel 02 and 03 are the I²C transactions at the camera, measured on the reference design SCL and SDA lines connecting the DS90UB953 and the AR0233 devices. This shows that the read initiated from the master and measured at the deserializer is successfully getting across the FPD-Link III connection and reading the imager on the camera module.

By acknowledging the I²C read, the imager has confirmed that it is present and at the correct slave address.

3.2.2.6 Return Loss Performance

Return loss testing measures the amount of the signal reflected and returned back to the transmitter as a ratio of return power to input power. Excessive reflected signals may cause interference with the FPD-Link III communications and result in a higher bit error rate so, in theory, the results need to be as low as possible.

TI offers some specifications for the DS90UB953 to help enforce a good bit error rate. These specifications are listed as less than -10 dB at 2 GHz for the forward channel, and less than -20 dB at 20 MHz for the back channel. The TIDA-020000 meets these specifications with results of -12.98 dB at 2 GHz and -25.57 dB at 20 MHz, as Figure 28 shows.

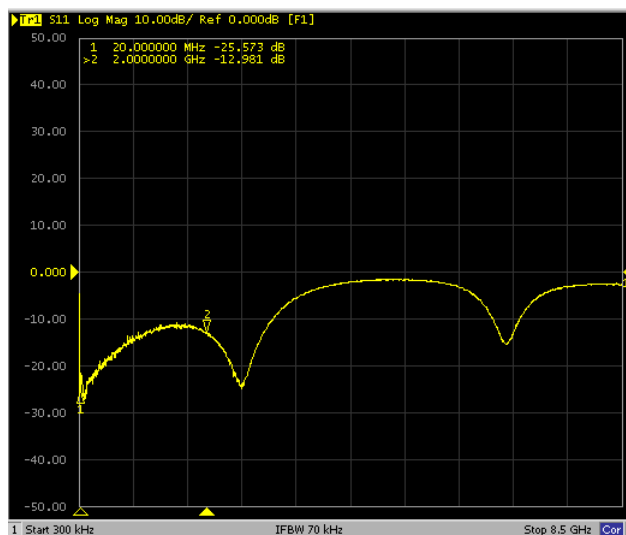


Figure 28. Return Loss Test Results

3.2.2.7 Thermal Performance

Thermal images were taken with the camera module running and streaming video after 1 minute, and then again after 60 minutes, shown in Figure 29 and Figure 30.

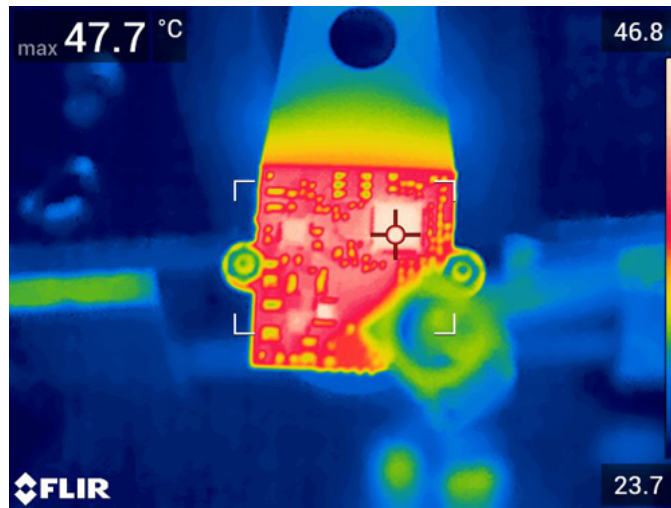


Figure 29. Thermal Performance at 1 Minute

After 1 minute, the highest temperature rise on the board is indicated by the DS90UB953-Q1 serializer, which rose 24°C above ambient to 47.7°C.

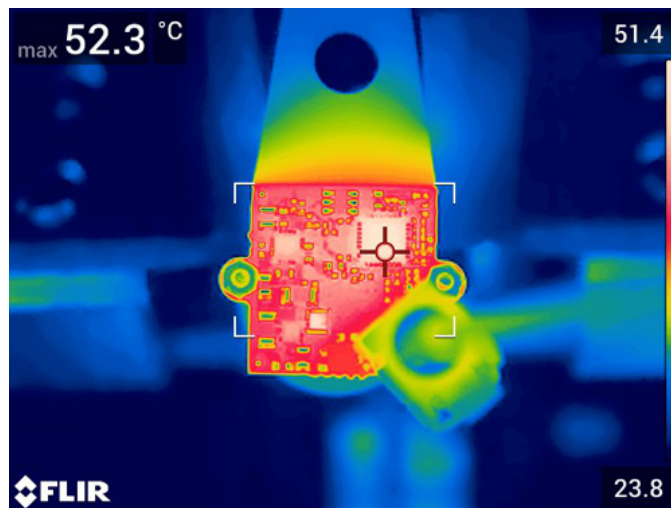


Figure 30. Thermal Performance at 60 Minutes

After 60 minutes, the highest temperature rise on the board is still represented by the DS90UB953 serializer, rising 28.6°C above ambient to 52.3°C. The TPS650002-Q1 PMIC reached a maximum temperature of 49.8°C (26°C above ambient), and the TPS62162-Q1 reached a maximum of 48.9°C (25.2°C above ambient).

4 Design Files

4.1 Schematics

To download the schematics, see the design files at [TIDA-020000](#).

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-020000](#).

4.3 PCB Layout Recommendations

4.3.1 Switching DC/DC Converters

During part placement and routing, it is helpful to always consider the path current will be taking through the circuit. The green line in [Figure 31](#) shows the current path from the coaxial cable in through the POC filter, inductor L1, and capacitors C1 and C2, and then out to the ferrite bead, L6, input capacitor, C3, to U1, or the TPS62162-Q1 device. The yellow line follows the 3.3-V output of the switcher to the output inductor L2 and output capacitor C4. Any return currents from the input capacitor C3 or the output capacitor C4 are joined together at the top left of U1 before they are connected to the ground plane. This is shown inside the blue circle. This reduces the amount of return currents, and thereby, voltage gradients in the ground plane. This may not be noticeable in the performance of the converter, but it will reduce its coupled noise into other devices.

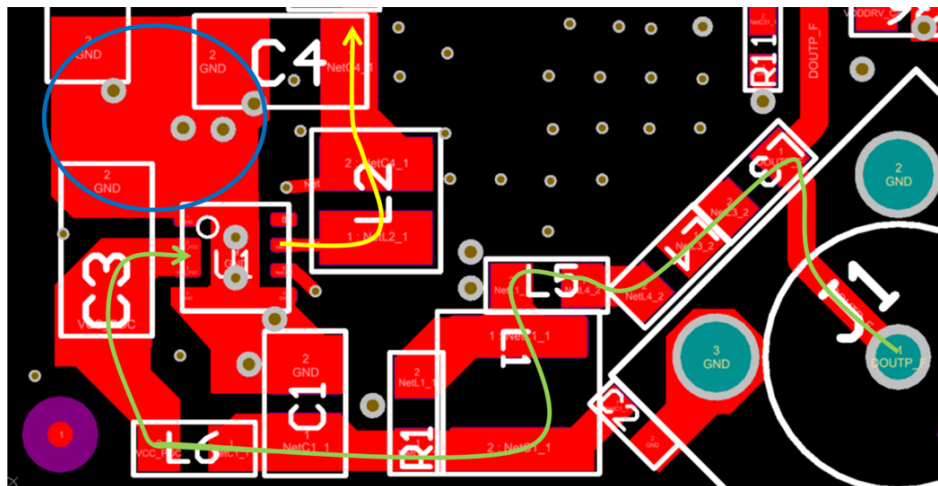



Figure 31. Routing Traces Around Switching Converters

4.3.2 PCB Layer Stackup Recommendations

The following are PCB layer stackup recommendations. Because automotive is the target space, there are a few extra measures and considerations to take, especially when dealing with high-speed signals and small PCBs:

- Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines
- If using a four-layer board, layer 2 must be a ground plane. Because most of the components and switching currents are on the top layer, this reduces the inductive effect of the vias when currents are returned through the plane.
- An additional two layers are used in this board to simplify BGA fan out and routing. [Figure 32](#) shows the stackup used in this board:



The diagram shows a cross-section of a PCB layer stackup. From top to bottom, it consists of: a green Top Overlay layer, a green Top Solder layer, a yellow Layer 1 - Top Layer (Signal), a grey Dielectric 1 layer, a yellow Layer 2 - GND (Signal), a grey Dielectric 2 layer, a yellow Layer 3 - PWR (Signal), a grey Dielectric 5 layer, a yellow Layer 4 - Signal, a grey Dielectric 4 layer, a yellow Layer 5 - Signal/GND (Signal), a grey Dielectric 3 layer, a yellow Layer 6 - Bottom Layer (Signal), a green Bottom Solder layer, and a green Bottom Overlay layer.

Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Coverlay	Surface Material	0.4	Solder Resist	3.5
Layer 1 - Top Layer	Signal	Copper	1.4		
Dielectric 1	Dielectric	Prepreg	12.6	370HR	4.2
Layer 2 - GND	Signal	Copper	1.4		
Dielectric 2	Dielectric	Core	8	370HR	4.2
Layer 3 - PWR	Signal	Copper	1.4		
Dielectric 5	Dielectric	Prepreg	12.6	370HR	4.2
Layer 4 - Signal	Signal	Copper	1.4		
Dielectric 4	Dielectric	Core	8	370HR	4.2
Layer 5 - Signal/GND	Signal	Copper	1.4		
Dielectric 3	Dielectric	Prepreg	12.6	370HR	4.2
Layer 6 - Bottom Layer	Signal	Copper	1.4		
Bottom Solder	Solder Mask/Coverlay	Surface Material	0.4	Solder Resist	3.5
Bottom Overlay	Overlay				

Figure 32. Layer Stackup

4.3.3 Serializer Layout Recommendations

High-speed CSI-2 routing is an important design aspect for the DS90UB953-Q1 device on this reference design. Layout considerations for trace impedance and length matching must be a high priority for good signal quality of the high-speed video data. For the CSI-2 traces, crosstalk can easily happen with high-speed signals, so it is important on this camera module design that the traces are away from the FPD-Link III RX traces to reduce coupling.

Trace impedance is one critical aspect to the CSI-2 lane routing. Route the differential pairs for CLK and DATA with a controlled 100- Ω differential impedance ($\pm 20\%$). For trace impedance to be within specifications and within range of each other, the length and width of the trace plays a factor in this. To achieve tight impedance specifications, length specifications also need to be strict within the positive to negative differential pair length and pair to pair length. If the length is not matched at these high data switching speeds, the data can arrive at the serializer at different times and cause issues of synchronization between data and clock. The length difference between the positive and negative differential pair trace should be within 5 mils of each other. For length matching between each CSI-2 lane pair, the difference must be kept within 25 mils.

The last key points to address with CSI-2 routing is crosstalk and reflections. To reduce the effects of crosstalk between lanes, spacing between each differential lane must be at least three times the signal trace width. In addition, keep vias and bends on the traces to a minimum. The vias must ideally be two or fewer to minimize stubs that cause reflections. Bends must be as equal as possible in the number of left and right bends, and the angle of the bend must be greater than or equal to 135 degrees. When these layout considerations are followed, the video data integrity can be maintained. If for any reason there are high-speed concerns on the CSI-2 lane design, debug tools are available to run video data over the 1, 2, or 4 lanes. The imager must be set to output over the specified number of data lanes, and the DS90UB953 device can then be set to the correct number of lanes in register 0x02.

5 Differential Pairs (5 Highlighted)		
Designator	Average Length (mil)	Longest Signal Length (mil)
CSI0_CLK	1040.91	1044.125
CSI0_D0	1045.844	1047.516
CSI0_D1	1056.45	1031.149
CSI0_D2	1051.333	1040.801
CSI0_D3	1049.198	1050.349

10 Nets (0 Highlighted)	
Name	Routed Length (mil)
CSI0_CLK_N (-)	1040.473
CSI0_CLK_P (+)	1041.347
CSI0_D0_N (-)	1045.086
CSI0_D0_P (+)	1046.601
CSI0_D1_N (-)	1038.398
CSI0_D1_P (+)	1074.502
CSI0_D2_N (-)	1039.155
CSI0_D2_P (+)	1063.511
CSI0_D3_N (-)	1047.52
CSI0_D3_P (+)	1050.876

Figure 33. CSI-2 Differential Trace Routing

Decoupling capacitors need to be located very close to the supply pin on the serializer. Again, this requires that the user consider the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor. Due to space constraints, ideal placement is not always possible. Smaller value capacitors that provide higher frequency decoupling must be placed closest to the device.

Figure 34 shows the supply current from C43 in yellow. The green line is the return path. The cross-sectional area of this loop is very small.

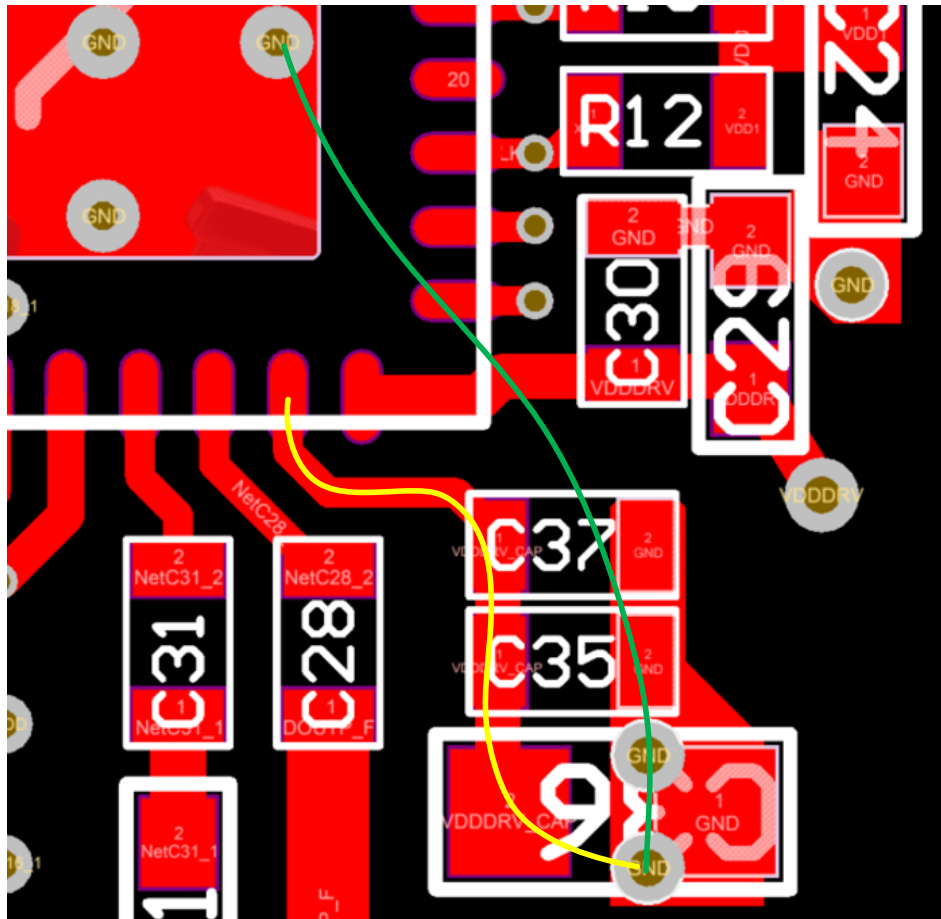


Figure 34. Decoupling Current Loop

For this application, a single-ended impedance of $50\ \Omega$ is required for the coaxial interconnect. Whenever possible, this connection must also be kept short. The routing of the high-speed serial line is shown in Figure 35, highlighted by the yellow line. The total length of the yellow line is about 3/8 inch.

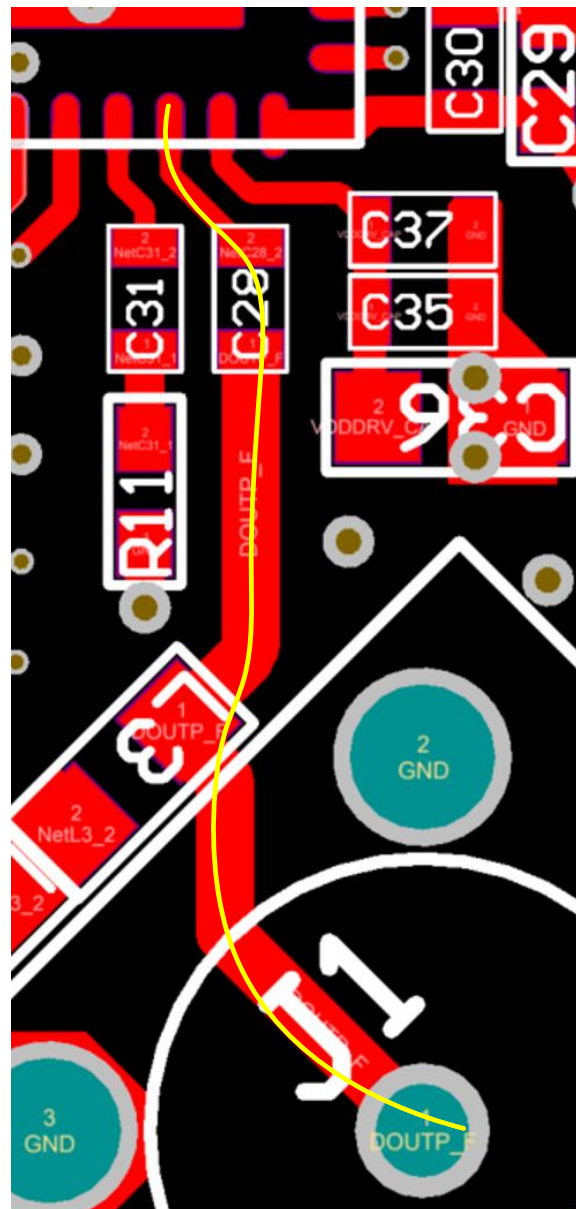


Figure 35. High-Speed Serial Trace

4.3.4 Layout Prints

To download the layer plots, see the design files at [TIDA-020000](#).

4.4 Altium Project

To download the Altium project files, see the design files at [TIDA-020000](#).

4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-020000](#).

5 Related Documentation

1. Texas Instruments, [DS90UB953-Q1 MIPI CSI-2 FPD-Link III Serializer for 2-MP/60-fps Cameras and RADAR Data Sheet](#)
2. Texas Instruments, [TPS6216x-Q1 3-V to 17-V 1-A Step-Down Converter with DCS-Control™ Data Sheet](#)
3. Texas Instruments, [TPS65002-Q1 2.25-MHz Step-Down Converter With Dual LDOs Data Sheet](#)
4. Texas Instruments, [TPS3702-Q1 High-Accuracy, Overvoltage and Undervoltage Monitor Data Sheet](#)
5. Texas Instruments, [Sending Power Over Coax in DS90UB913A Designs Application Report](#)
6. Texas Instruments, [Cable Requirements for the DS90UB913A and DS90UB914A Application Report](#)
7. Texas Instruments, [Optimizing the TPS62130/40/50/60/70 Output Filter Application Report](#)

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