TI Designs: TIDA-01349

IPM Interface Reference Design for Inverters Using Single-Package Six-Channel Digital Isolator

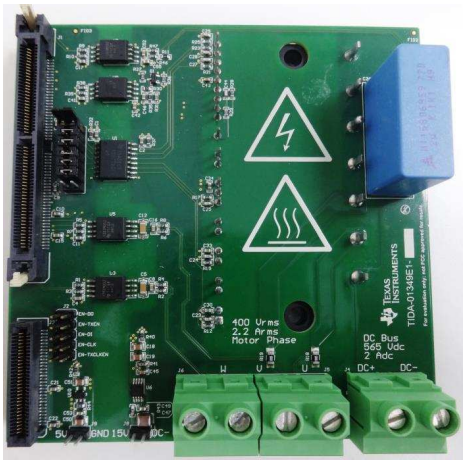
Description

This reference design realizes a three-phase inverter subsystem for AC inverter drives and servo drives using an intelligent power module (IPM). Reinforced isolation is present between the microcontroller (MCU) and the IPM-based power stage. The PWM signals are isolated using the single-package, six-channel digital isolator, ISO7760. In-phase current sensing is done in two motor phases using the isolated delta-sigma modulator, AMC1303M0520. DC bus voltage feedback and module temperature feedback is provided to the MCU through isolated delta-sigma modulators, AMC1303M2520. This reference design is controlled by a C2000™ MCU.

Resources

TIDA-01349	Design Folder
ISO7760	Product Folder
AMC1303M0520	Product Folder
AMC1303M2520	Product Folder
TLV760	Product Folder
TPS7A4201	Product Folder
TPS706	Product Folder
TMDSCNCD28379D	Tool Folder

TI E2E™ Community — ASK Our E2E™ Experts

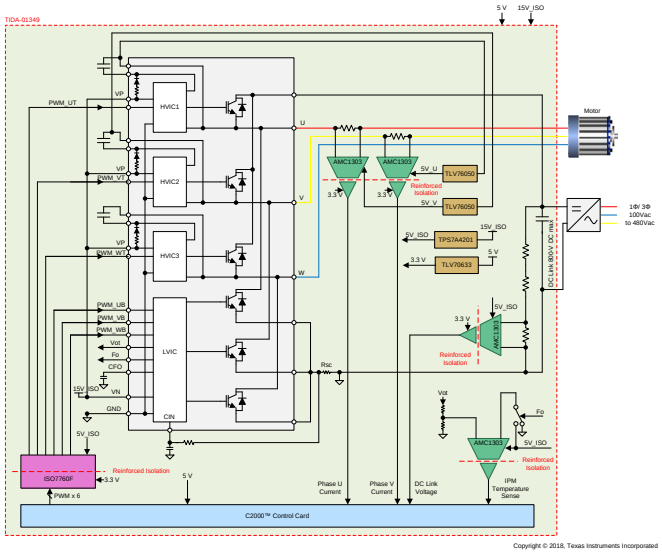


Features

- Power Stage Suited for 200-V to 480-V AC Drives With Continuous Current Rating up to 5 A_{RMS} and Peak Current Rating of 10 A_{PK} Using a 1200-V, 15-A IPM
- Reinforced Isolation Between Controller and Power Stage
- Single-Package Reinforced Isolator ISO7760 for Six PWM Signals Reduces BOM Count and PCB Footprint When Compared to Multiple Optoisolators
- Excellent Propagation Delay Matching of Isolator Channels Allows for Smaller Dead Time, Resulting in Reduced Inverter Output Distortions and Better Efficiency
- PWM Isolator With Very Low Current Consumption and Self Heating Allows Powering From 15-V IPM Supply With Small Footprint LDO
- IEC 61800-3 EMC Immunity for EFT up to 4 kV on Motor Power Cable

Applications

- Servo CNC and Robotics
- AC Inverters and VF Drives



1 System Description

Three-phase inverter power stages are the fundamental building blocks in industrial motor drive applications like pumps, compressors, robotics, machine tools, and CNC machines. The inverter converts a DC voltage into a variable frequency and power AC output to drive the motor. For inverter applications where space is a constraint, the inverter power stage must have a small form factor. For small compact inverters, using an IPM saves space significantly.

The IPM is an highly integrated inverter power stage. The gate drivers are integrated inside the module, and only external digital PWM signals are required to control the IPM. The IPM also provides diagnostic features like undervoltage protection on the gate drive power supplies, shoot-through detection in the phase half bridges, and overtemperature detection. The inverter PCB BOM count, gate drive subsystem design, and PCB routing complexity can be greatly minimized. In general, there are three main types of IPM from the PWM input perspective as shown in Figure 1.

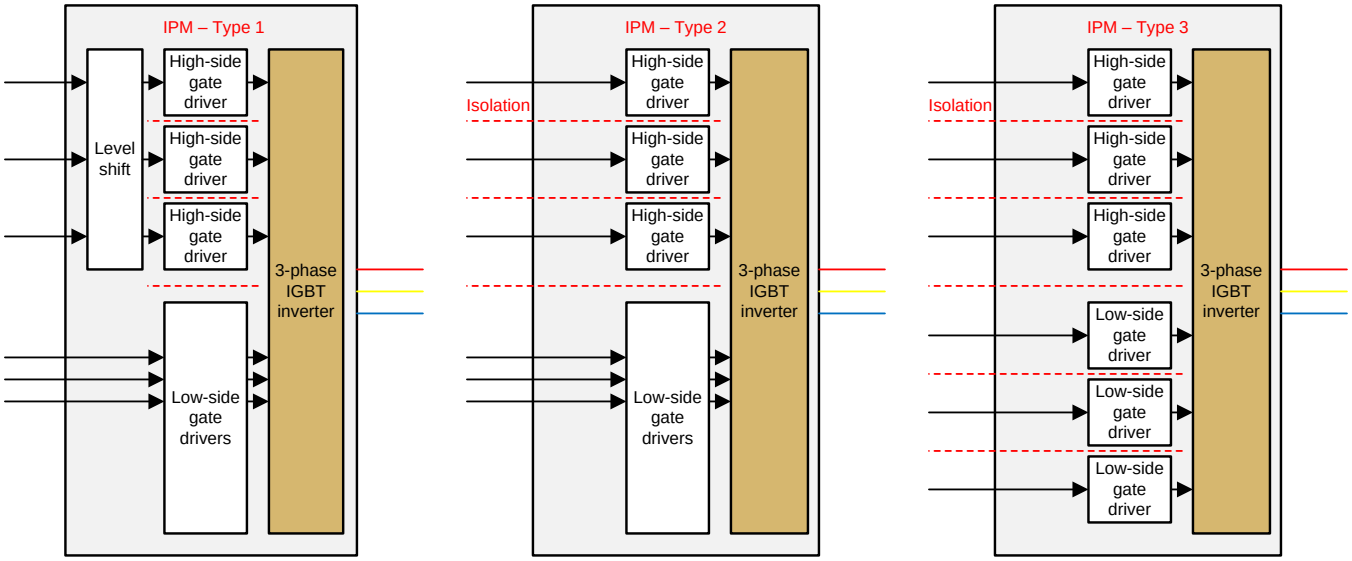


Figure 1. IPM Types—PWM Input Perspective

For the type 1 IPM, all the input PWM signals have a single reference. The high-side PWM signals are level shifted inside the module. For the type 2 IPM, the low-side PWM inputs have a single reference, but the high-side PWM signals are isolated from each other. For the type 3 IPM, all six input signals are isolated from each other. Type 3 IPMs are used typically for high-power inverters.

When all the input PWM signals of IPM have a single reference (type 1 IPM), then a six-channel isolator can be used as shown in the left half of Figure 2. The six-channel digital isolator uses only one device when compared to six optoisolator devices as shown in the right half of Figure 2. The six-channel digital isolator saves space significantly. Additionally, the input stage of the digital isolator is CMOS based, which requires much lesser drive current when compared to the LED input stage of the optocoupler. This enables driving the digital isolator directly from an MCU without any external buffers. The superior propagation delay and delay matching between multiple channels of the digital isolator enables reducing dead-time distortions. The capacitive technology-based digital isolators have a typical common-mode transient immunity (CMTI) of 100 kV/µs, which make them highly robust solutions to implement PWM isolation in inverters.

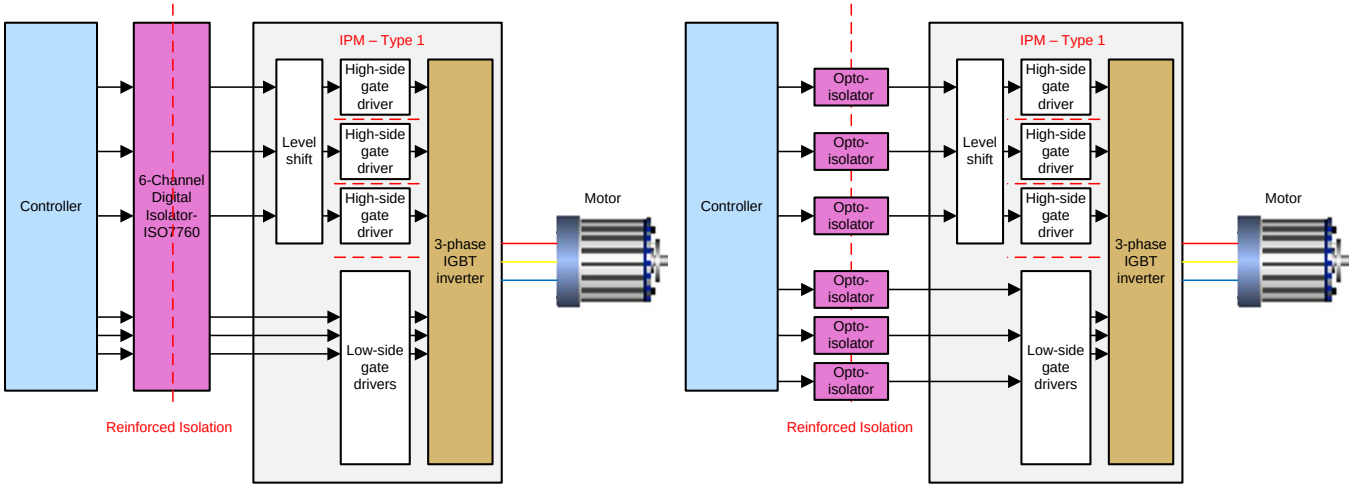


Figure 2. Using Six-Channel Digital Isolator

This reference design shows the functionality of the three-phase inverter implemented using an IPM. A six-channel digital isolator based on capacitive technology is used for PWM isolation, and isolated delta-sigma modulators are used for phase current, DC bus voltage, and module temperature sensing. This design guide shows the following test results:

- PWM propagation delays across isolation barrier
- Isolator thermal picture at maximum PWM frequency
- Switch node voltage at various switching conditions
- EFT on power interface to show robustness of PWM isolator

1.1 Key System Specifications

Table 1. Key System Specifications

SUBSECTION	PARAMETER	SPECIFICATION	COMMENT
Inverter	DC bus input voltage	200- to 800-V_{DC}	
	Continuous output current rating	5 A_{RMS}	
	Output frequency	0 to 100 Hz	
	PWM switching frequency	4 to 20 kHz	Output power has to be derated with a higher switching frequency.
	IPM used	1200-V, 15-A, six-pack inverter DIPIPM module with integrated gate drivers and analog temperature output	Part number: PSS15SA2FT
Motor phase current sensing	Linear measurement range	± 10 A_{PK} (typ)	Shunt resistor used is 5 mΩ. Resolution depends on the order of the SINC filter and OSR configured in software.
	Full scale range	± 12.8 A_{PK} (typ)	
DC bus voltage sensing	Linear measurement range	0 to 800 V_{PK} (typ)	Resolution depends on the order of the SINC filter and OSR configured in software.
	Full scale range	0 to 1027 V_{PK} (typ)	
IPM temperature sensing	Linear measurement range	100°C (typ)	Resolution depends on the order of the SINC filter and OSR configured in software.
	Full scale range	131°C (typ)	
Protection	DC bus voltage	Overvoltage and undervoltage detection	User software implementation
	Module temperature	Overtemperature shutdown and derating the output power delivered	User software implementation
	Isolation	5000 V_{RMS} withstanding isolation voltage as per UL 1577	Digital isolators are used for PWM signals and isolated ΔΣ modulators for current, voltage and temperature sensing
Interface connectors	MCU interface	180-pin dual in line edge connector socket for C2000 control cards	See Table 2 for pin assignments on the connector.
	Power	15 V	For powering the IPM control supply and LDO, which generates the secondary-side supply of DC-referenced isolators
		5 V	For powering the C2000 control card and LDO, which generates the primary side of isolators.
	Position feedback	Digital encoder	10-pin header. See schematics for pin assignments on the connector J2. Can use TIDA-00172, TIDA-00179 reference designs
PCB information	PCB layer stack	4 layer	2-oz external layers, 1-oz internal layers
	Laminate	FR4, high Tg	
	PCB thickness	1.6 mm	
	PCB size	110 mm × 110 mm	

2 System Overview

2.1 Block Diagram

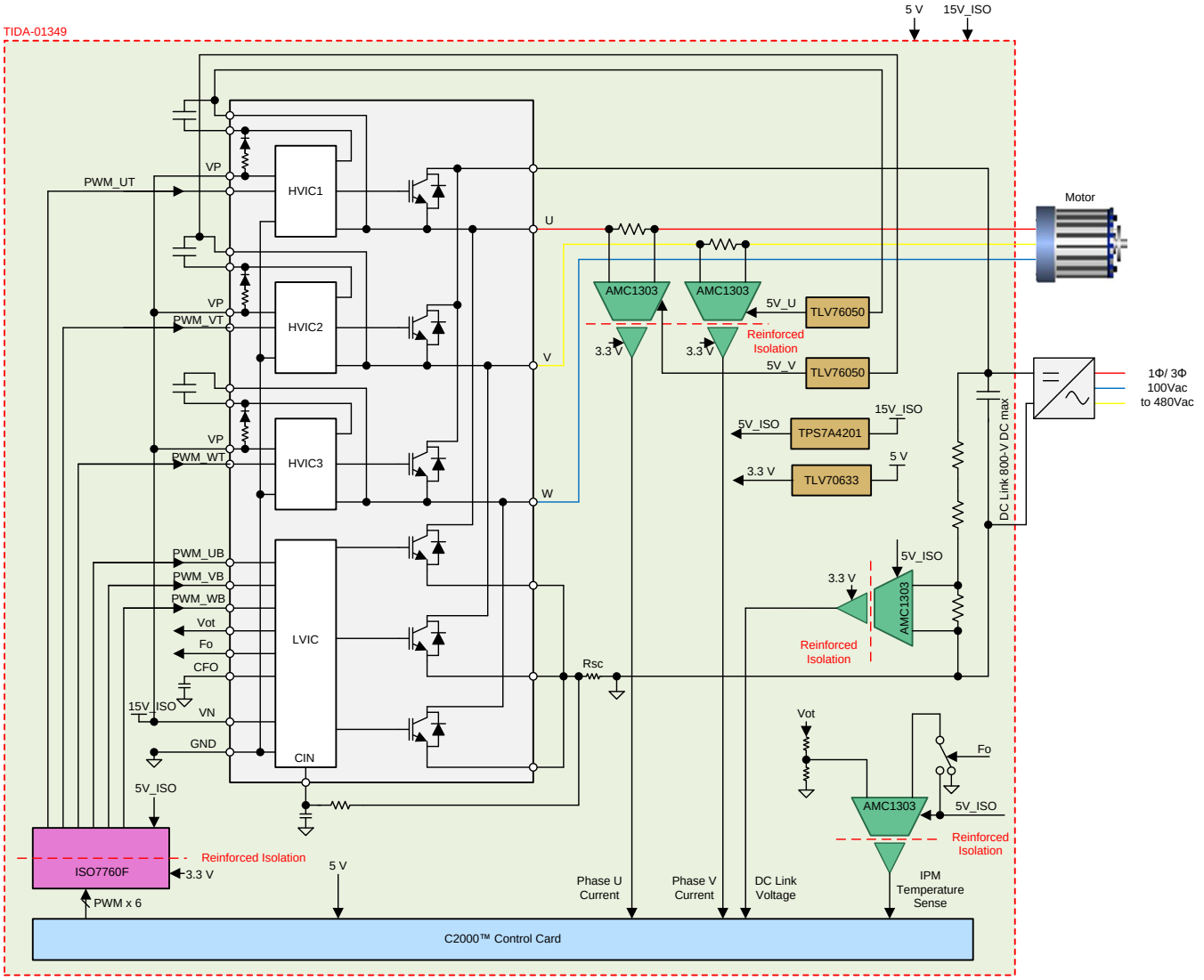


Figure 3. Block Diagram of TIDA-01349

The inverter section is implemented using an IPM. The IPM has integrated inside it three IGBT-based half bridges. A low-voltage IC (LVIC) inside the IPM drives the three low-side IGBT gates, and three individual high-voltage ICs (HVICs) drive the three high-side IGBTs. The LVIC and HVIC control circuits and low-side IGBT gates are powered by a single 15-V rail. The high-side IGBT gates are driven by individual isolated supplies. The isolated supplies are generated by bootstrapping the low-side 15-V rail. The high-voltage bootstrap diode and bootstrap capacitor inrush limiting resistor are integrated inside the IPM. Only the bootstrap capacitors have to be added externally. The high-voltage DC bus input to the board must be provided externally.

For the IPM used in this reference design, all six PWM signals are referenced to the DC link negative. The high-side PWM signals are level shifted inside the IPM. The PWM signals are reinforced isolated using the single-package, six-channel digital isolator, ISO7760F. The primary side is powered from 3.3 V to make the isolator inputs compatible to a 3.3-V I/O MCU. The secondary side is powered by a 5-V supply to make the isolator outputs compatible to the 5-V inputs of the IPM.

In-phase current sensing is done on two of the motor phases using shunt resistors. The 20-MHz, ±50-mV input range of the AMC1303 is used for sensing the voltage drop across the shunt resistors. The primary side is powered with 3.3 V. The secondary side of each current sense AMC1303 is powered by an isolated 5-V supply, which is derived from the corresponding bootstrap capacitors using the TLV76050 LDO.

Inverter DC bus voltage sensing is done using a high-impedance voltage divider network and the 20-MHz, ±250-mV version of the AMC1303 modulator. The IPM has an analog temperature sensor integrated inside it. The temperature sensor output is scaled down using a voltage divider network and fed into the input stage of the AMC1303 modulator. The primary side is powered from GND referenced 3.3 V and the secondary side powered by DC-referenced 5 V.

The primary-side ground referenced 3.3 V is generated using the TPS70633 LDO from the external 5-V input to the board. The DC-referenced 5 V is generated from the external 15-V reinforced isolated input to the board using the TPS7A4201 LDO.

The IPM has diagnostic features to detect short circuit in the low-side IGBTs and undervoltage on the control power supplies of the IPM. Whenever a short circuit event occurs, the low-side IGBTs are turned off and the fault pin is pulled low for a configurable time period. UVLO protection is applicable on both the high-side and low-side gate drive supplies of the IGBT. On UVLO detection, the IGBTs do not switch even on application of PWM signals. The fault pin is continuously low in case of undervoltage detection; the fault pin responds to UVLO only on the low side. The fault signal is transmitted across the isolation barrier by multiplexing it along with the temperature signal.

2.2 Highlighted Products

2.2.1 ISO7760

The ISO776x devices are high-performance, six-channel digital isolators isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic-input and logic-output buffer separated by a silicon dioxide (SiO_2) insulation barrier. The DW package used in this reference design has an isolation rating of 5000 V_{RMS} as per UL 1577. The device with an F suffix ensures that the PWM outputs are low in case of floating PWM inputs to the isolator. Through innovative chip design and layout, the electromagnetic compatibility of the ISO776x family of devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

For the three-phase inverter, the low propagation delay (11 ns) and channel-to-channel delay matching of the isolator enables reducing dead time. A lower dead time helps reduce distortions, enabling smoother running motors and higher efficiency. The low power consumption reduces device self heating. High CMTI of ±100 kV/µs enables robust operation in the presence of high dv/dt on the switch nodes. The high EMC immunity of the isolators is crucial in the noisy inverter switching environment. The capacitive isolation technology has a lifetime of > 40 years.

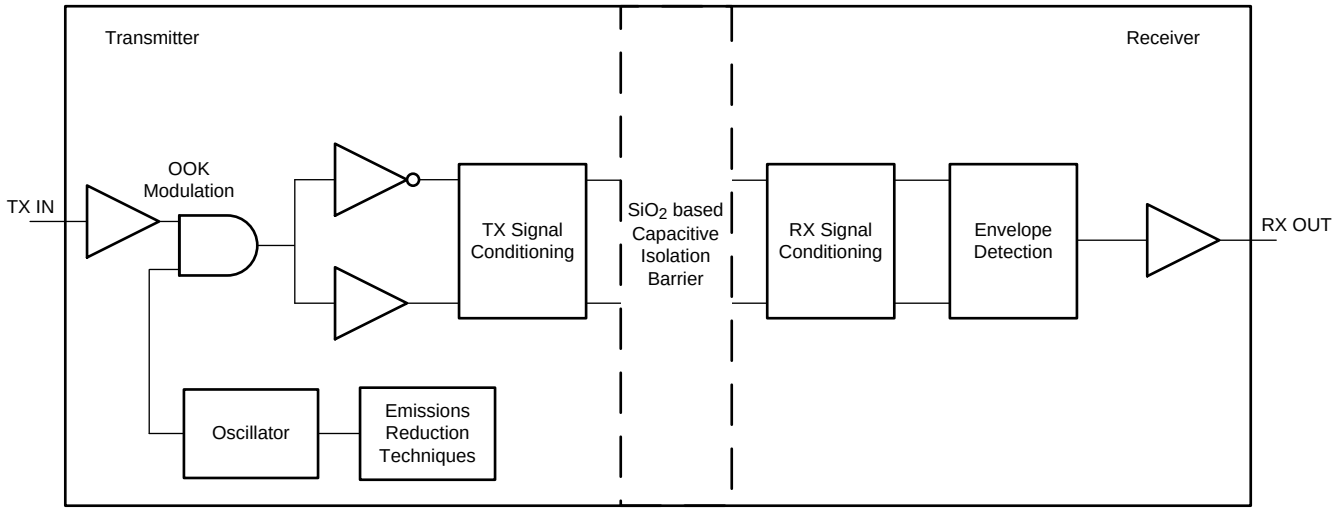


Figure 4. Functional Block Diagram of One Channel of ISO7760

2.2.2 AMC1303M2520, AMC1303M0520

The AMC1303 is a family of precision delta-sigma (ΔΣ) modulators with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{pk} according to DIN V VDE V 0884-11 and UL 1577 standards.

The input of the AMC1303 is optimized for direct connection to shunt resistors or other low voltage-level signal sources. The ± 50-mV input voltage range version of the device is used for shunt-based in-phase motor current sensing in this reference design. The lower voltage drop across the shunt resistor allows for significant reduction of power dissipation in the resistor. This decreases the self heating of the resistor helping minimize the drift in measurement due to its thermal coefficient.

For voltage sensing the ± 250-mV input voltage range version of the device is used. This improves the measurement accuracy by decreasing the effect of noise on the input signal when high impedance resistor divider networks are used for down converting the measured voltage signals to the input voltage range of the AMC1303.

High transient immunity of ± 100 kV/µs (typ) enables accurate measurements as the shunt voltage sensing is done in an environment of fast switching transients. System level diagnostic features of the device help improve the safety of the inverter. The AMC1303 is synchronized to an internally generated clock which helps simplify routing between the modulator and the controller and eliminates sample and hold time issues.

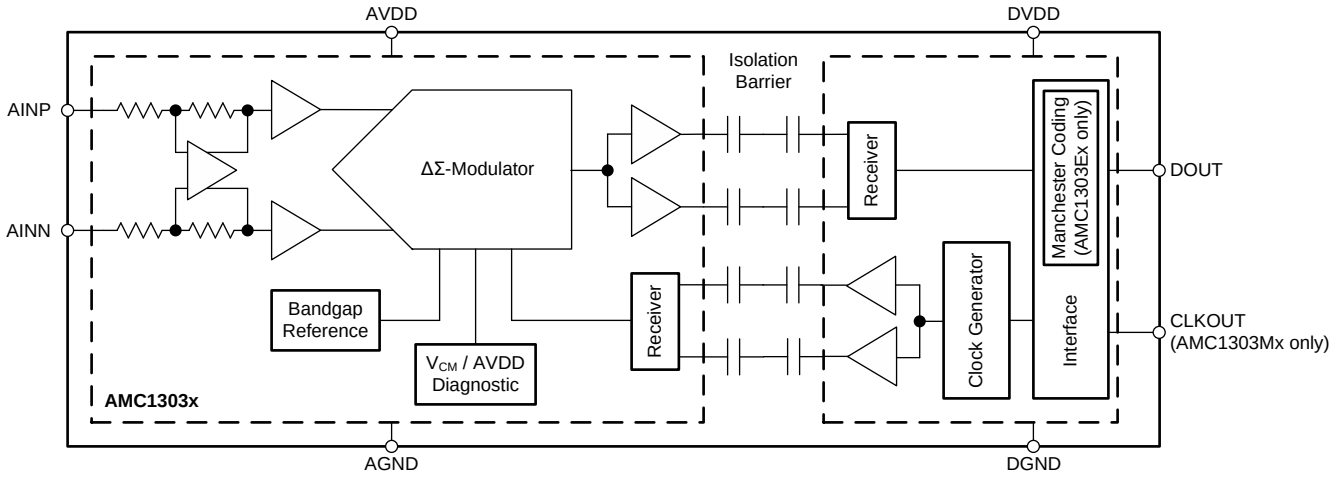


Figure 5. Functional Block Diagram of AMC1303x

2.2.3 TLV760

The TLV760 is an integrated linear-voltage regulator featuring operation from an input as high as 30 V. The TLV760 has a maximum dropout of 1.2 V at the full 100-mA load across its operating temperature. The TLV760 is available in 3.3 V, 5 V, 12 V, and 15 V. The SOT-23 packaging of the TLV760 series allows the device to be used in space-constrained applications. The TLV760 is designed to bias digital and analog circuits in applications that are subject to voltage transients and spikes up to 30 V. The device has robust internal thermal protection, which protects itself from potential damage caused by conditions like short to ground, increases in ambient temperature, high load, or high dropout events.

This reference design uses the 5-V version of the TLV760 to power the high-voltage side of the current sensing ΔΣ modulators. The 5 V is generated from the 15-V bootstrap power supplies of the high-side gate drivers. The small form factor enables a compact solution and immunity to voltage transients is important as the LDO operates on the switch node as a reference.

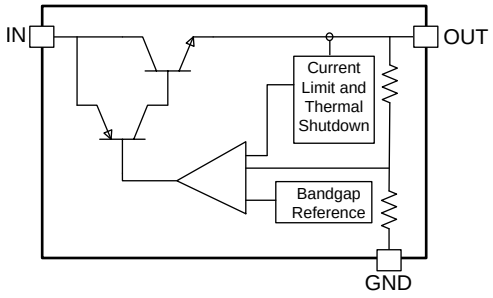


Figure 6. Functional Block Diagram of TLV760

2.2.4 TPS7A4201

The TPS7A4201 device is a high-voltage-tolerant linear regulator that offers the benefits of a thermally-enhanced package (MSOP-8) and is able to withstand continuous DC or transient input voltages of up to 28 V. The device has an internal thermal shutdown and current limiting to protect the system during fault conditions. The MSOP-8 package has an operating temperature range of T_J = –40°C to +125°C. The device is ideal for generating low-voltage supply from intermediate voltage rails in industrial applications as it can supply a well regulated voltage rail during fast voltage transients. This translates to a simpler and more cost effective electrical surge protection circuit.

This reference design uses the TPS7A4201 to generate the 5-V rail from the 15-V rail to power the secondary side of the DC-referenced isolators.

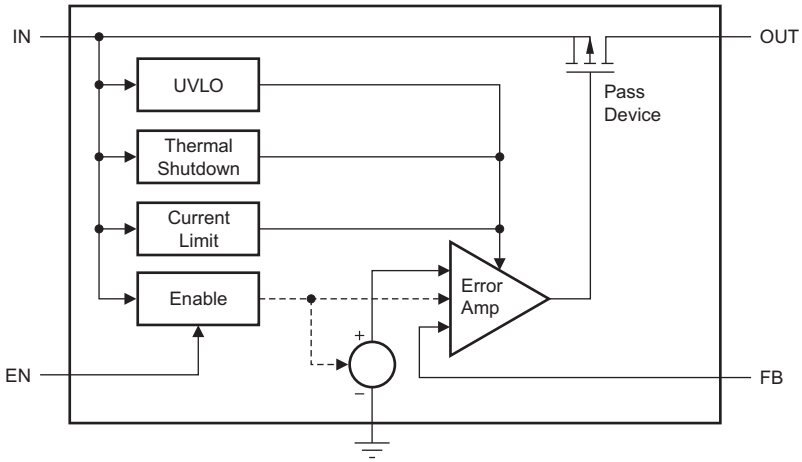


Figure 7. Functional Block Diagram of TPS7A4201

2.2.5 TPS706

The TPS706 series of linear voltage regulators are available in fixed output voltages of 1.2 V to 5 V. These devices have thermal-shutdown, current-limit, and reverse-current protection for added safety. The devices are available in WSON-6 and SOT-23-5 packages. This reference design uses the TPS706 to generate the 3.3-V rail from the 5-V rail to power the primary side of the isolating devices.

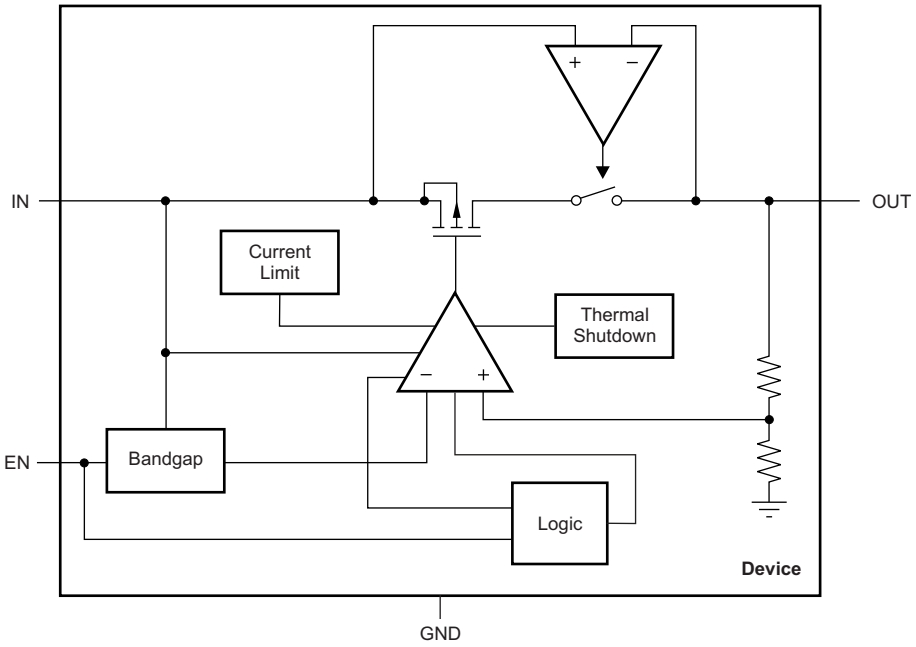


Figure 8. Functional Block Diagram of TPS706

2.3 System Design Theory

2.3.1 Three-Phase Inverter

This reference design uses an IPM to implement the three-phase inverter (see Figure 9). The inverter has a nominal output current rating of 5 A_{RMS} and a peak current rating of 10 A_{PK}. This reference design uses the 1200-V, 15-A IPM, PSS15SA2FT.

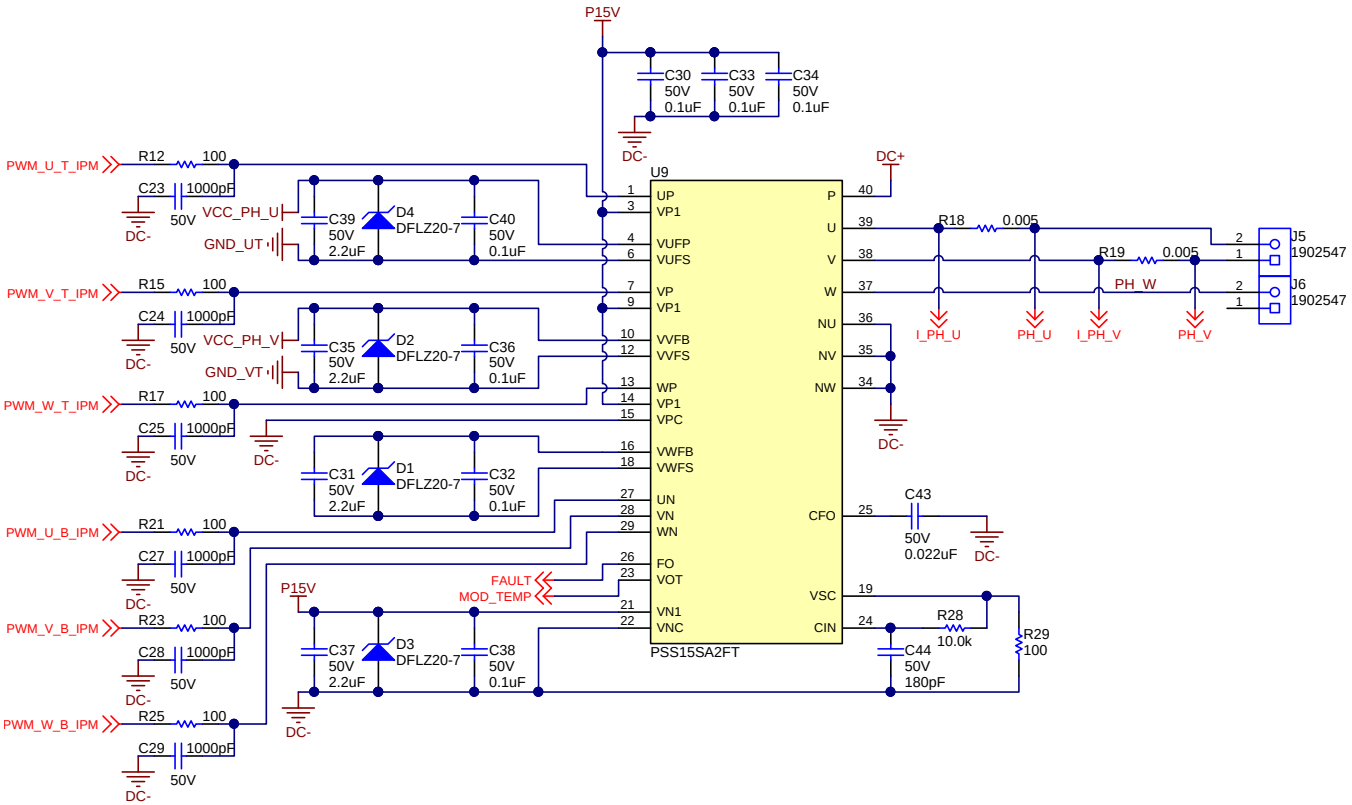


Figure 9. Schematic of Three-Phase Inverter Using IPM

A single 15-V IPM control power supply is required for biasing the internal control circuits of the IPM and for driving the low-side IGBT gates. This power supply is provided through connector J8 and connected across pins VN1 and VNC of the IPM. C37 is the bulk capacitor that provides the peak currents for driving the low-side IGBTs inside the IPM without causing much ripple on the 15-V rail. C38 is the noise decoupling capacitor and D3 is used for surge protection. VP1 is the control supply for the HVICs, and there is one VP1 pin for each of the three phases. C30, C33, and C34 are noise decoupling capacitors on VP1 pins. The power supplies for the high-side gate drive are generated by bootstrapping the 15-V control supply. The high-voltage bootstrap diode and inrush limiting resistor for the bootstrap capacitor are integrated inside the IPM. C31, C35, and C39 are the bootstrap capacitors. D1, D2, and D4 are used for surge protection. C40, C36, and C32 are the noise decoupling capacitors.

The IPM has a short-circuit protection feature for the low-side IGBTs. This feature works by detecting a small sense current, which is divided at the low-side IGBT from the phase current. This current is passed across sense resistor R29. The voltage drop across the sense resistor is then fed into the CIN pin of the IPM through an RC filter comprised of R28 and C44. When short circuit is detected, the IPM shuts down the low-side IGBTs and outputs the fault signal. In this reference design, R29 is 100 Ω, which sets the short circuit trip level at 25.5 A (min). The RC filter has a time constant of 1.8 µs to filter out noise spikes. Fault is an active low signal. The capacitor C43 on the CFO pin decides the time for which the fault signal goes low. The relation between fault pulse width t_{FO} and capacitor C43 is given by Equation 1. In this design, the time is set at 2.4 ms by selecting a 0.022-µF capacitor.

$$C\,43 = t\,FO \times 9\,.\,1 \times 10 - 6 \quad (1)$$

The fault signal is also triggered when UVLO is detected on the 15-V control power supply of the IPM. The IPM also has an analog temperature output signal (MOD_TEMP), which can be used to protect the module from overtemperature.

2.3.2 PWM Signal Isolation

The IPM used in this reference design has all its input PWM signals referred to DC-. The high-side PWM signals are level shifted inside the IPM, which allows the design to use the single six-channel PWM isolator ISO7760F. The F version has integrated pulldown resistors on the input, which ensures that the outputs are low in case the inputs are floating. The primary side is powered by a 3.3-V rail to make it compatible with a 3.3-V I/O controller. C1 is the noise decoupling capacitor. The secondary side is powered with a 5-V rail. The IPM selected in this reference design requires a 5-V I/O. C2 is the noise decoupling capacitor on the 5-V rail. Both the primary and secondary side are reinforced isolated from each other with a creepage spacing of 8 mm at minimum. The device has a withstanding isolation voltage rating of 5000 V_{RMS} as per UL 1577 and a maximum isolation working voltage of 1414-V DC as per DIN V VDE V 0884-11:2017-01.

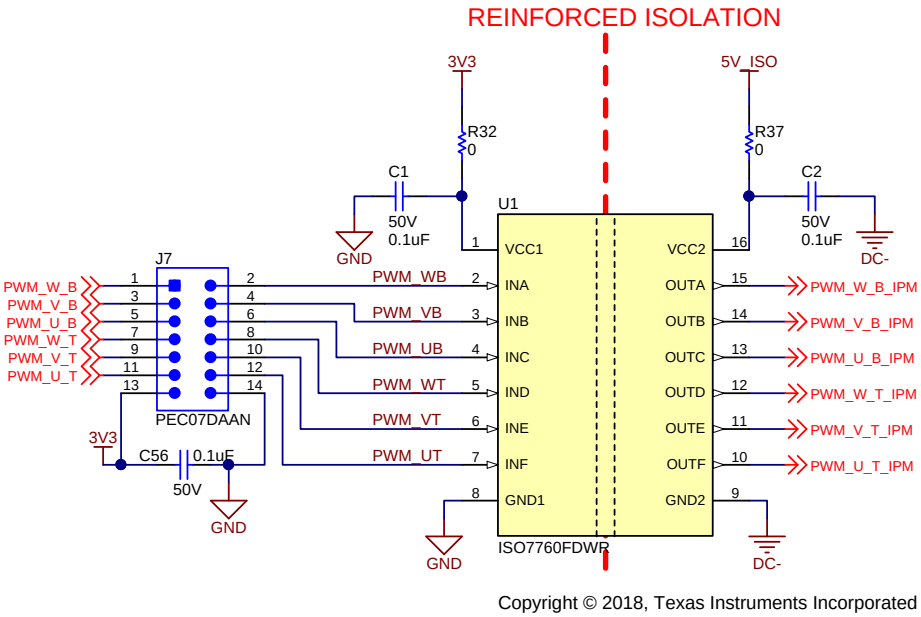


Figure 10. Schematic of PWM Signal Isolation Using ISO7760F

A 7×2 header J7 is provided for an optional add-on card. This add-on card provides the feature for PWM input interlocking. In case the add-on card is not used, the header pins must be jumpered to connect the PWM signals directly from the MCU to the ISO7760F. Figure 11 shows the circuit on the add-on interlock card. A pulldown resistor is required on each of the inputs to the XOR gates. These resistors ensure that the outputs of the interlock card are stable and not oscillating when the MCU PWM outputs are in the high impedance state. The logic shown in Equation 2 is used for PWM interlocking, which ensures that the high-side and low-side PWM output signals are low in case both the PWM inputs are high. This situation can occur due to errors in software.

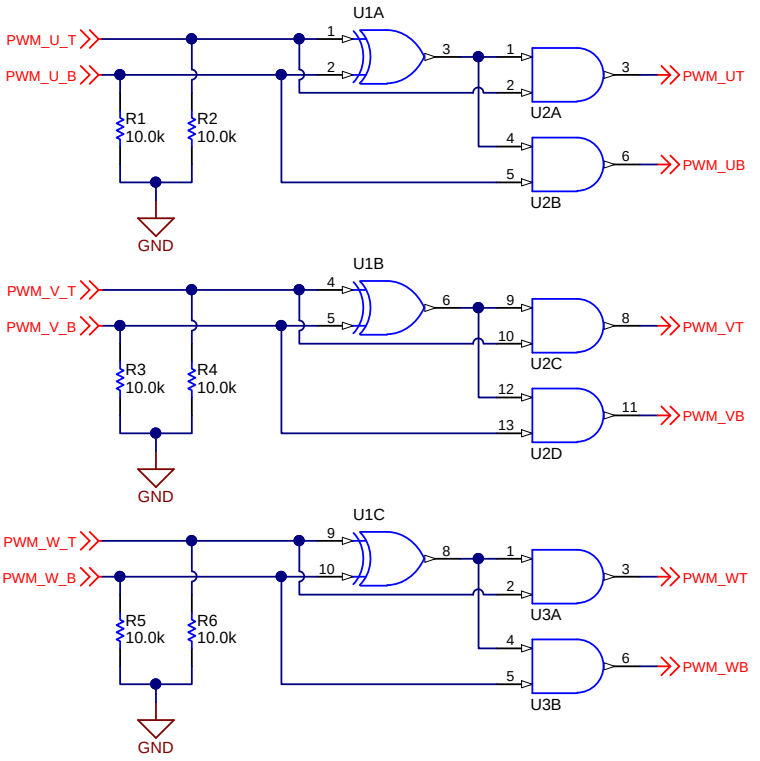


Figure 11. Schematic of PWM Input Interlocking Circuit

$$Y_T = (X_T \oplus X_B) X_T \quad Y_B = (X_T \oplus X_B) X_B \tag{2}$$

where:

- Y_T = PWM output of the interlock card for the top switch
- Y_B = PWM output of the interlock card for the bottom switch
- X_T = PWM input to the interlock card for the top switch
- X_B = PWM input to the interlock card for the bottom switch

2.3.3 DC Bus Voltage Sensing

This reference design is made to be operated from a DC bus voltage of up to 800-V DC as limited by the IPM. This covers most of the low-voltage drives with a grid voltage input up to 480-V AC. The DC bus voltage is applied to connector J4. The rectifier stage for generating the DC bus voltage from grid AC and bulk capacitors are not placed on the PCB and have to be connected externally, or a current limited high-voltage DC source can be used. A 2-µF, 1.1-kV film capacitor is placed close to the IPM DC bus input. The capacitor minimizes the loop area for the high-frequency switching currents. This helps minimize switch node overshoots and high frequency ringing, which in turn help reduce EMI.

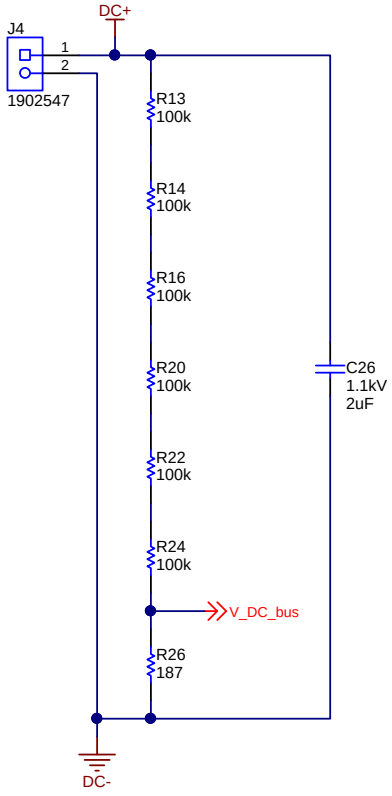


Figure 12. Schematic of Resistor Divider Network for Scaling DC Bus Voltage

The DC bus voltage feedback is necessary for over- and undervoltage protection as well as for regulating the PWM duty cycles to maintain a constant RMS voltage to the motor. A voltage divider is used to down convert the DC bus voltage to the input voltage range of the delta-sigma modulator. This reference design uses the AMC1303M2520 version, which has a linear input voltage measurement range of ± 250 mV. The scaling factor of the divider is calculated in Equation 3.

Scaling_factor = R 26 R 26 + R 13 + R 14 + R 16 + R 20 + R 22 + R 24 = 187 187 + 600 k = 0 . 000312 V DC_bus = (DC +) × Scaling_factor (3)

The 0-mV to 250-mV section of the ± 250-mV input range of the delta-sigma modulator is capable of measuring 0 to 800 V with a scaling factor of 0.000312. The resistors R13, R14, R16, R20, R22, and R24 are each rated for 200 V and will be derated by 33% in case of the maximum DC bus voltage of 800 V. The maximum power dissipated across each resistor is 0.18 W when DC bus voltage is 800 V. Each resistor is rated for 0.25 W.

Figure 13 shows the AMC1303 circuit used for sensing the scaled voltage. R46, R47, and C52 form the differential input filter. R11 is used to correct for the offset voltage due to the input bias current flowing through R26. C55 is the secondary-side supply noise decoupling capacitor. On the primary side, C17 is the noise decoupling capacitor. R9 and R10 are termination resistors on the data and clock lines. The data and clock lines are fed into the SDFM peripheral of the C2000 MCU. The SDFM is configured with OSR and SINC filter order for the required resolution.

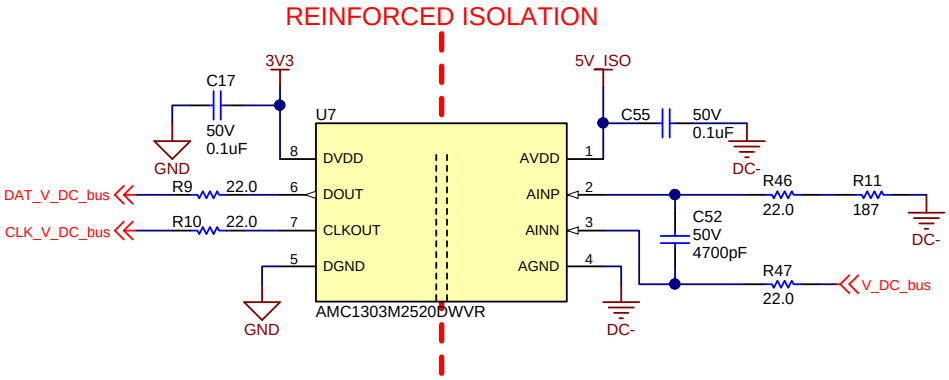


Figure 13. Schematic of DC Bus Voltage Sensing Using AMC1303M2520

2.3.4 Motor Phase Current Sensing

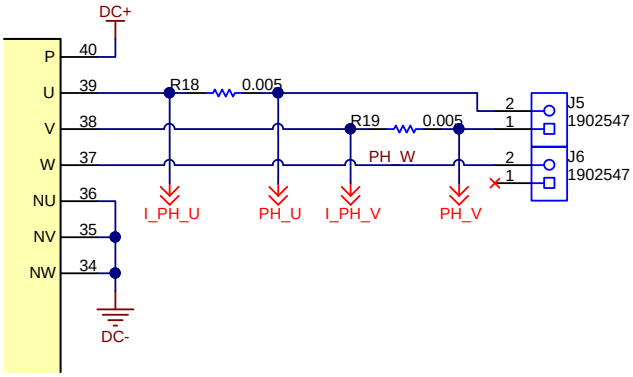


Figure 14. Schematic of Shunt Resistors for In-Phase Motor Current Measurement

Motor current is sensed in two of its phases (Phases U and V). The third phase current (Phase W) can be derived from the other two phase currents assuming a balanced load condition. Current sensing is in-phase shunt resistor based. The voltage drop across the resistor is measured using a delta-sigma modulator. This reference design uses the ± 50-mV input voltage range of the AMC1303M0520 device. The smaller input voltage range enables the use of a smaller shunt resistor, resulting in lower power dissipation in the resistor. This reference design has a peak inverter output current rating of ± 10 A_{PK} . The shunt resistor value can be calculated using Equation 4. R18 is selected to be 5 mΩ and a 1%, 1-W rated resistor is selected. The ± 50-mV input voltage is the specified linear differential full-scale measurement range of the delta-sigma modulator. The peak differential input voltage range before clipping the output is ± 64 mV. This range enables extending the measurement range to ± 12.8 A_{PK} although with lesser accuracy than specified.

Value of shunt resistor, R18 = Input voltage range of U3 Peak current value to be measured = 50 m 10 = 5 mΩ
Peak power dissipation in R18 = 10 × 10 × 5 mΩ = 0.5 W (4)

Figure 15 shows the circuit configuration for measuring current using the AMC1303M0520. R2, R4, and C8 form the input differential filter. This filter prevents high frequency noise on the input from getting aliased on the measured frequency range. R1 and R3 are termination resistors on the data and clock output lines. For the AMC1303x product series, the clock is generated internally inside the device. This design uses the 20-MHz clock version. The data and clock lines are connected to the SDFM peripheral of the C2000 MCU. The SDFM is configured with OSR and SINC filter order for the required resolution.

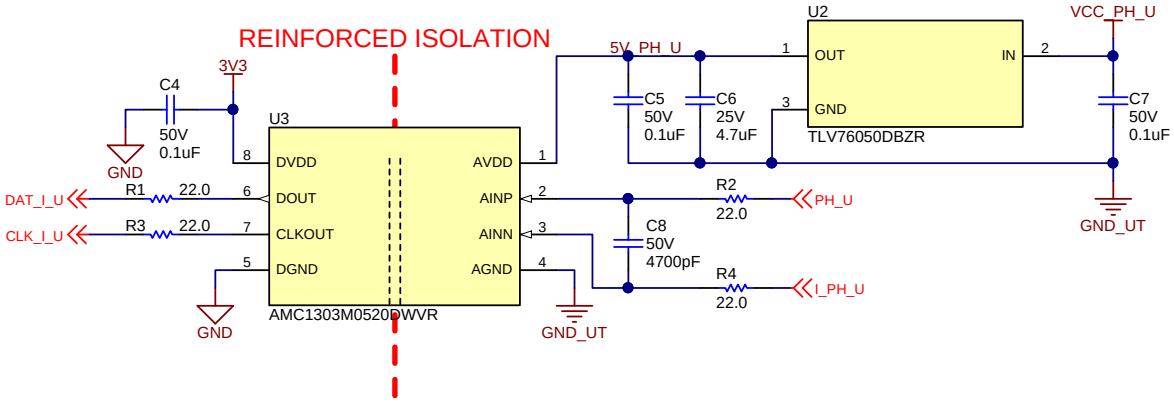


Figure 15. Schematic of Delta-Sigma Modulator Circuit for Current Measurement

The primary-side DVDD is powered from 3.3 V. C4 is the supply noise decoupling capacitor. The secondary-side AVDD is powered from a 5-V supply, which is referenced to the switch node of the phase in which current is being measured. For Phase U, the reference is GND_UT, which is the reference pin of bootstrap capacitor C39 (see Figure 9). The LDO U2 converts the 15-V supply across the bootstrap capacitor to 5 V. C7 is the LDO input supply noise decoupling capacitor and C6 is the output capacitor for the LDO. C5 is the supply noise decoupling capacitor for the delta-sigma modulator.

2.3.5 IPM Temperature Sensing

The IPM used in this reference design has an analog temperature feedback signal. The signal is proportional to the temperature of the LVIC integrated inside the IPM. The heat generated at the IGBT and free-wheeling diode transfers to the LVIC through mold package and inner and outer heat sink. Temperature feedback is used to protect against module over temperature and derate the output current of the inverter. Figure 16 plots temperature versus feedback signal amplitude.

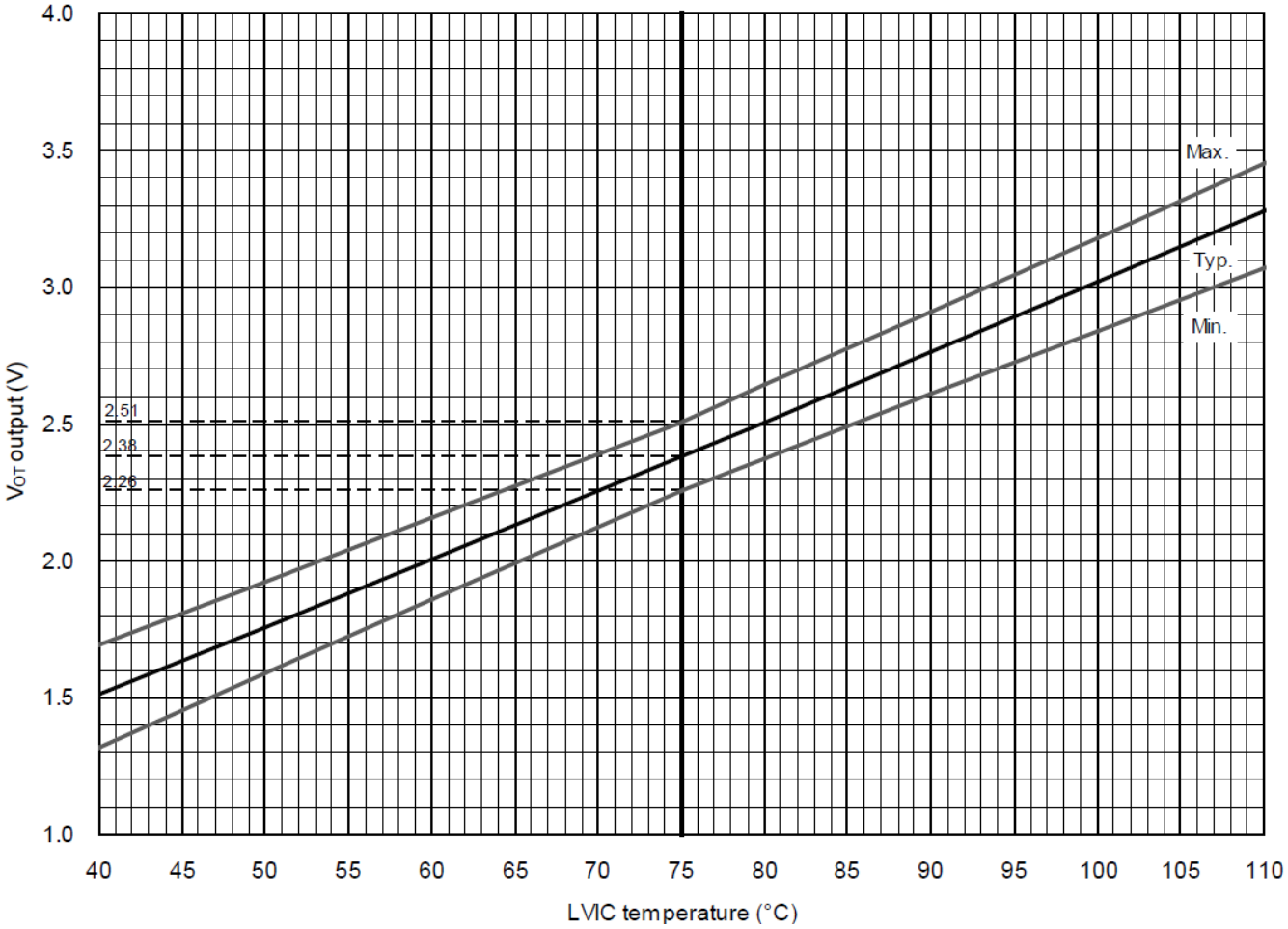


Figure 16. Temperature of LVIC vs V_{OT} Output Characteristics

The AMC1303M2520 is used for temperature sensing. The V_{OT} (temperature sense) output of the IPM is scaled to 250 mV, which is the specified linear full-scale positive range of the modulator using a voltage divider network comprising of R35 and R31. The scaling factor is set to 0.0834, which means that the 250-mV input to the modulator corresponds to a V_{OT} output voltage of 3 V. From Figure 16, this corresponds to a 100°C temperature reading.

The secondary side of the modulator is powered from 5 V. C42 is the supply noise decoupling capacitor. The primary side is powered by the 3.3-V rail and C41 is the decoupling capacitor. R38 and R39 are termination resistors used on data and clock outputs of the modulator. The modulator generates a clock signal with a frequency of 20 MHz.

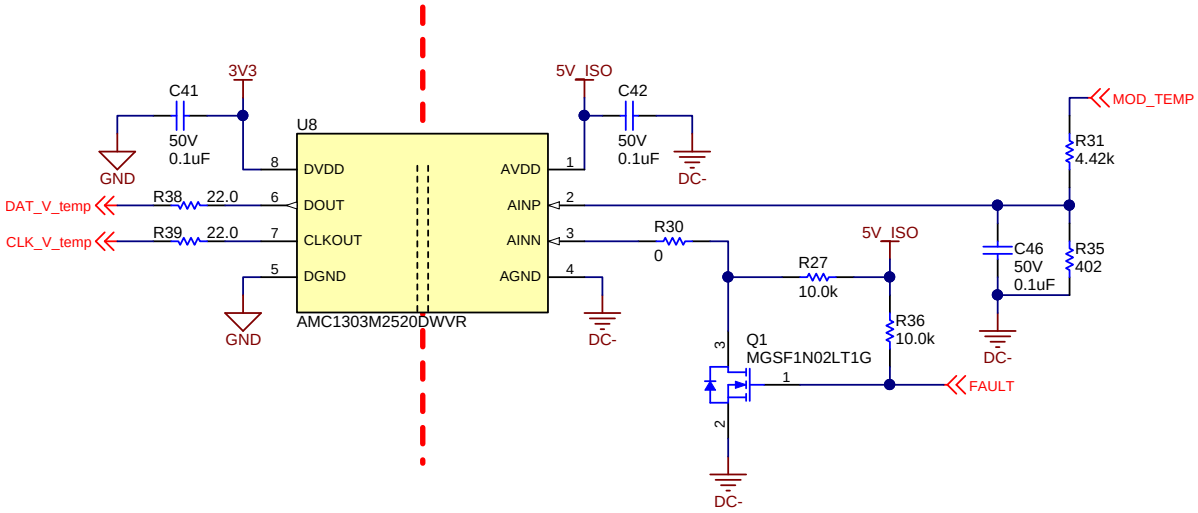


Figure 17. Schematic of Temperature Measurement Circuit

2.3.6 IPM Fault Signal Feedback

The IPM used in this reference design has integrated diagnostic features to detect short circuit in the low-side IGBTs and undervoltage on the control power supplies. The Fo (fault) pin of the IPM is open drain. If a short-circuit event occurs, then the Fo pin is pulled low for the time period specified by Equation 1. The Fo pin remains continuously low in case of UVLO event. A separate single-channel isolator is required to transmit this signal to the MCU. In this reference design, the fault signal is multiplexed with the temperature sense signal to save a digital isolator channel.

As shown in Figure 17, the MOSFET Q1 connects the AINN pin of the temperature sense modulator to DC-. The fault signal is open drain and active low. In the default state, the gate of Q1 is pulled up to 5 V through R36, which turns on Q1, connecting AINN to DC-. The modulator can measure the temperature signal normally. When the fault signal is triggered, the gate of Q1 is pulled low, which turns off Q1, and the AINN pin is connected to 5 V through R27. This causes the differential input voltage (AINP - AINN) to exceed the negative full-scale measurement range of the modulator, forcing the output to be continuously zero with a bit toggle every 128 bits (see the Output Behavior in Case of a Full-Scale Input section of the AMC1303x data sheet). The controller can decode from this bitstream that a fault has occurred.

2.3.7 Power Supply Rails

This reference design uses four main power supply rails. The 5-V rail is input to the primary low-voltage control side through J9. This rail powers the C2000 MCU control card. The TPS70633 LDO generates the 3.3-V rail from the 5-V rail. The 3.3-V rail powers the primary-side supply of the digital isolator, the delta-sigma modulators and the add-on interlock card. C50 is the input bulk capacitor and C53 is the noise decoupling capacitor for the LDO U10. The enable pin is pulled up to 5 V through R44. In this design, the LDO is always kept on. C51 is the output capacitor of the LDO.

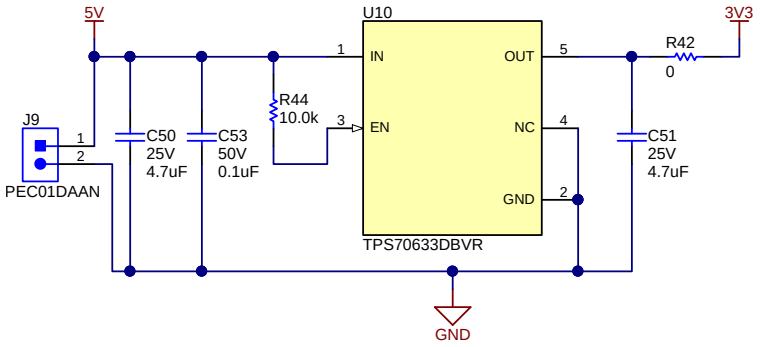


Figure 18. 5-V to 3.3-V Conversion Using TPS70633

The 15-V rail on the secondary high-voltage side is powered through connector J8. This rail powers the IPM control circuits. This rail has to be reinforced isolated from the primary-side supply. The TPS7A4201 LDO generates 5 V from 15 V. C47 is the input bulk capacitor and C49 is the supply noise decoupling capacitor. The enable pin is pulled to 15 V through R43. In this design, the LDO is always on. C19 and C18 are the output capacitors. R41 and R45 form the feedback network, setting the output voltage to 5 V. The pad of the device package is connected to DC- plane, which further improves the package thermal performance.

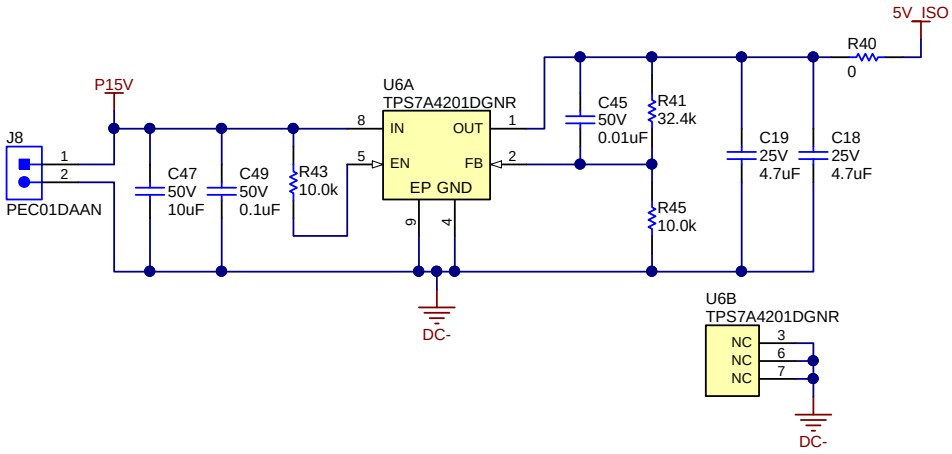


Figure 19. 15-V to 5-V Conversion Using TPS7A4201

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

Figure 20 shows the top view of the PCB. J4 connects the DC bus voltage, and J5 and J6 connect the three motor phase terminals. The 5-V supply is connected to J9. This supply powers the control card and the control side circuitry. The reinforced isolated 15-V supply is connected to J8. This supply powers the IPM control circuits. J3 is a provision to connect external digital encoders in case motor shaft position feedback is required. J7 connects an optional PWM interlock add-on card. If this card is not used, then the header pins are connected together with shorting jumpers as shown in Figure 20. A dual in-line edge connector socket is used for the 180-pin C2000 MCU control card. The dual core Delfino™ F28379D control card is used for testing this reference design.

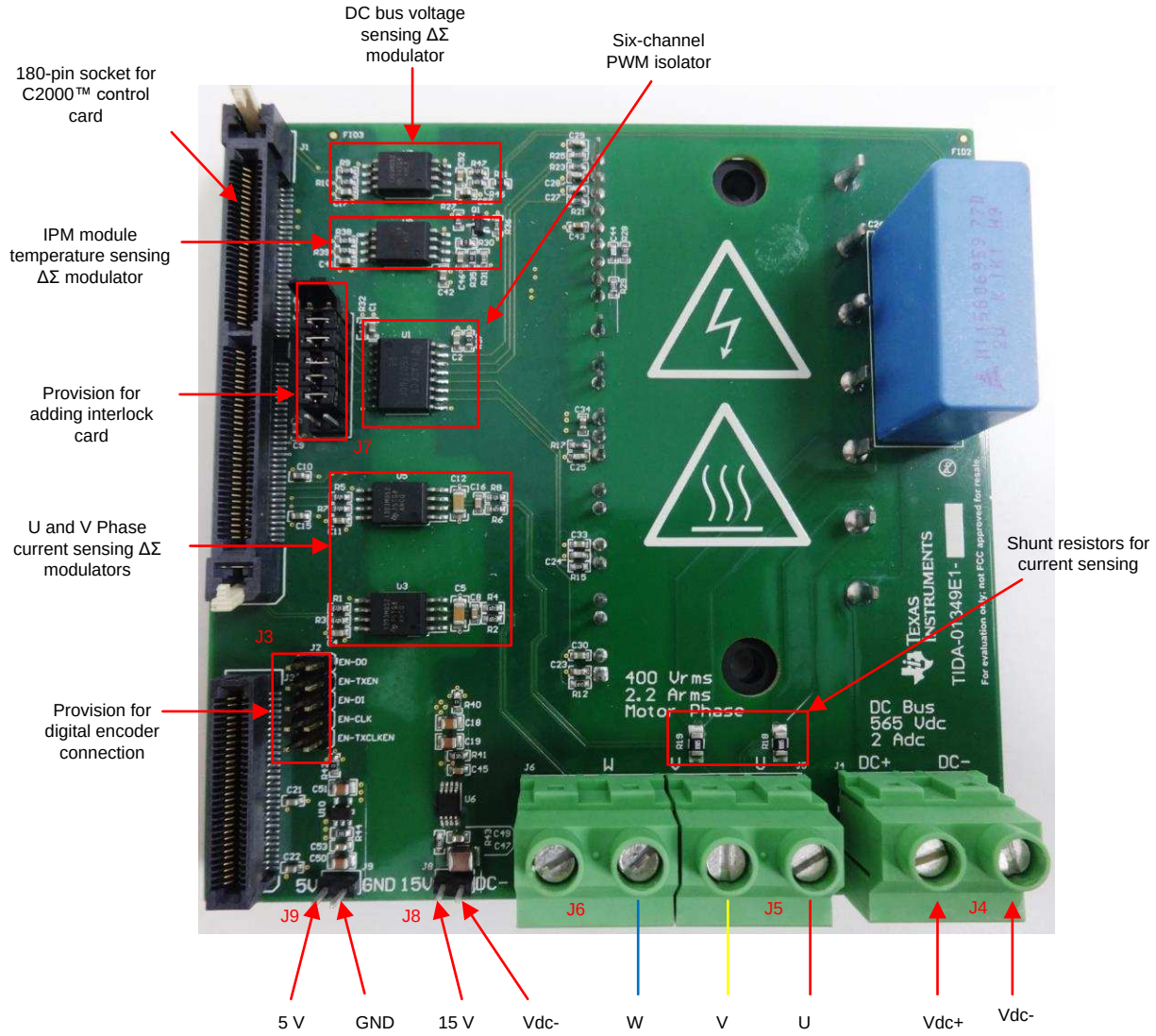


Figure 20. Top View of TIDA-01349 PCB

Figure 21 shows the high-voltage inverter side and the low-voltage controller side with the reinforced isolation barrier in between. The creepage and clearance distance across the barrier is 8 mm at minimum. The wide body digital isolator for the PWM signals and the isolated ΔΣ modulators for current, voltage, and temperature feedback signals are placed across the isolation barrier.

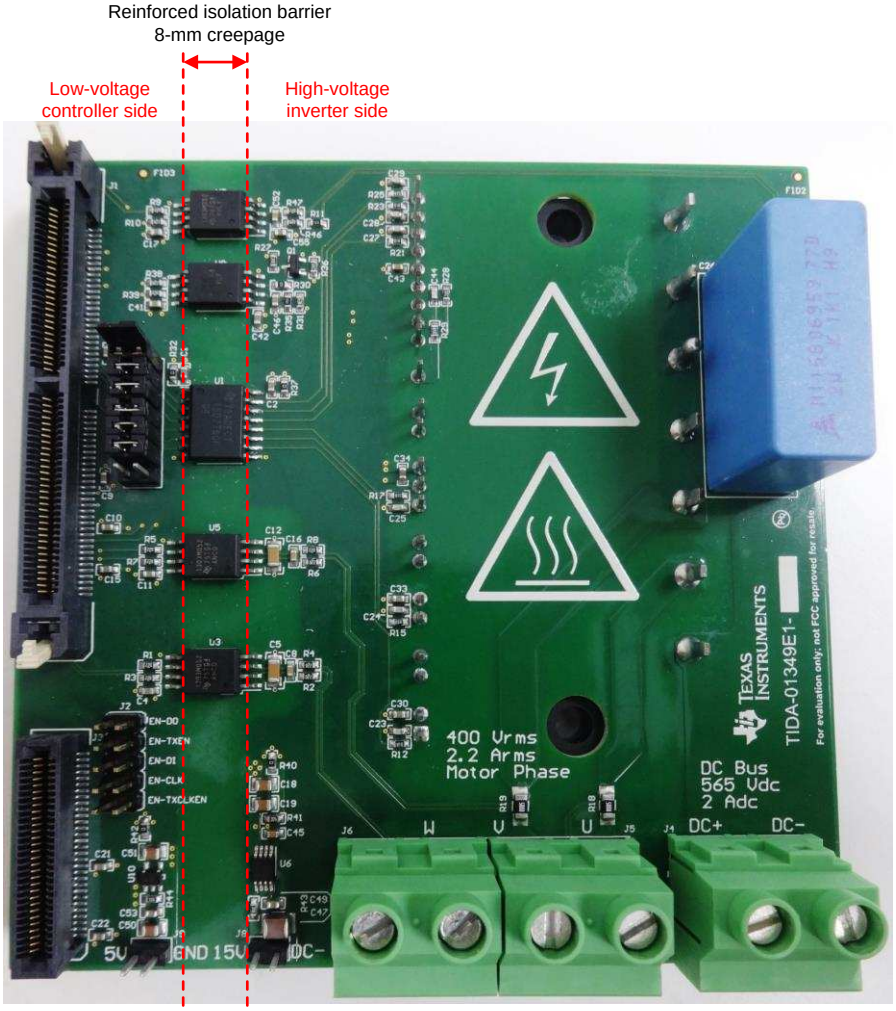


Figure 21. High-Voltage Inverter Side, Control Side, and Reinforced Isolation Barrier

Figure 22 shows the bottom view of the PCB. The metal pad of the IPM must be connected to a heat sink. A thermally conductive heat sink compound is applied between the IPM metal pad and the heat sink surface for reducing air gaps at the contact surface. The module is then tightly screwed to the heat sink as shown in Figure 23. Choose an appropriate heat sink based on the maximum continuous power to be dissipated.

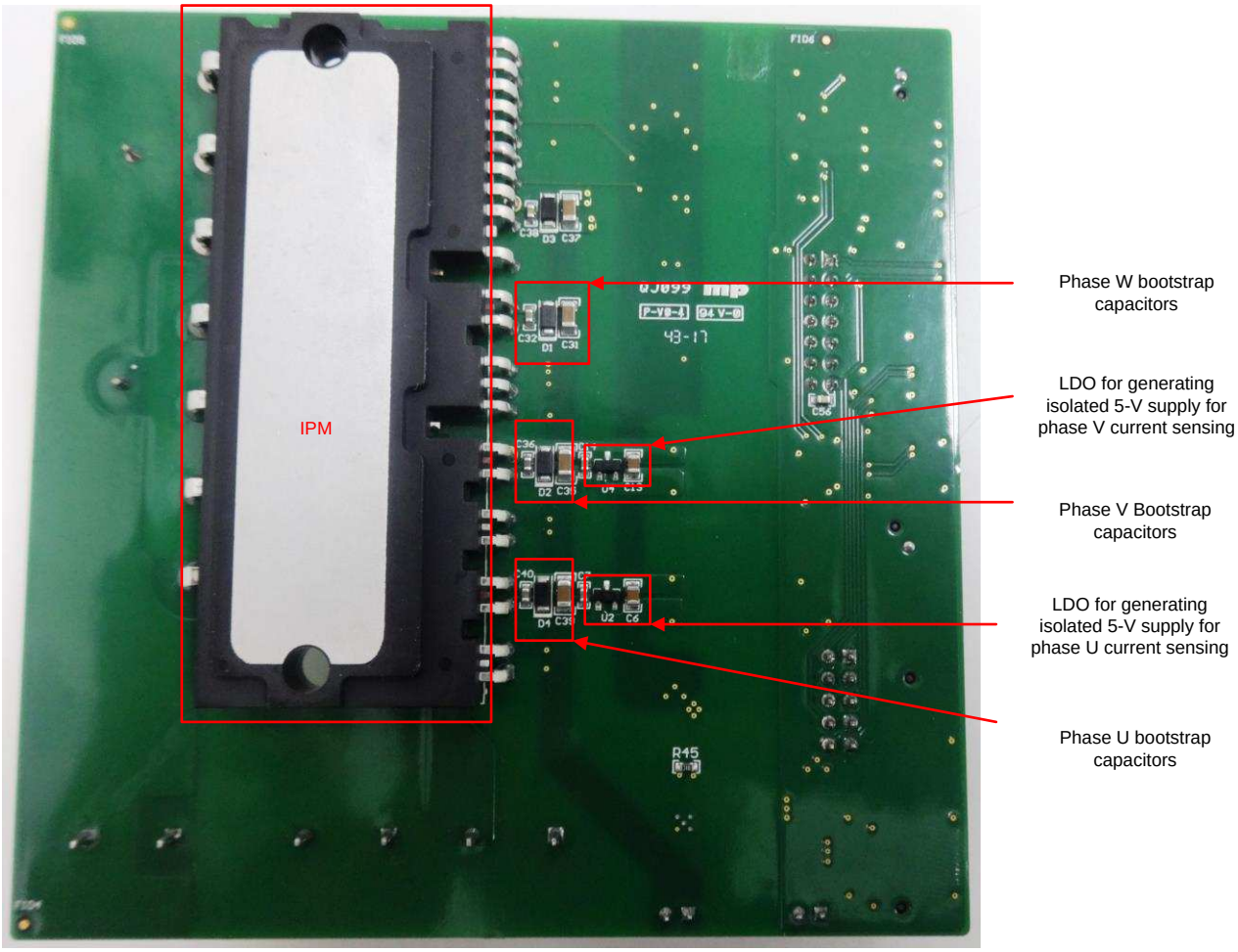


Figure 22. Bottom View of TIDA-01349

Figure 23. IPM Interface to Heat Sink

3.1.2 Controller Interface Socket

The 180-pin control card is mounted in the dual in-line socket J1 and J3 as shown in Figure 24. Table 2 describes the pin functions used on this PCB.

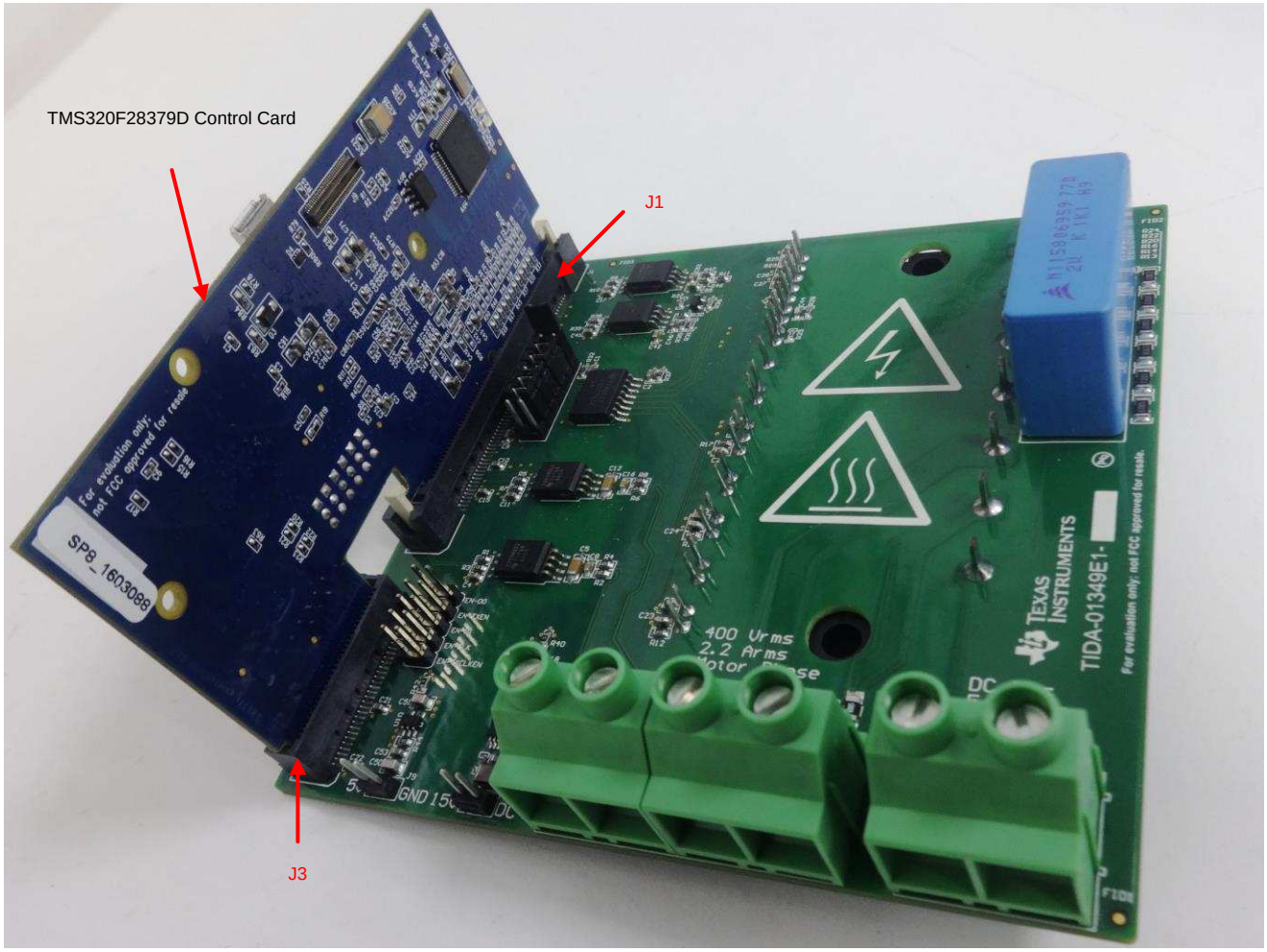


Figure 24. Control Card Connection to TIDA-01349

Table 2. TIDA-01349 Interface to Control Card

TIDA-01349 PINOUT	C2000 CONTROL CARD PINOUT	PIN NO		C2000 CONTROL CARD PINOUT	TIDA-01349 PINOUT
	JTAG-EMU1	1	2	JTAG-EMU0	
	JTAG_TMS	3	4	JTAG-TRSTN	
	JTAG_TCK	5	6	JTAG-TDO	
GND	GND	7	8	JTAG-TDI	
	ADC1 (and/or DACA)	9	10	GND	GND
	ADC1 (and/or DACB)	11	12	ADC2	
GND	GND	13	14	ADC2	
	ADC1 (and/or CMPIN+)	15	16	GND	GND
	ADC1	17	18	ADC2	
GND	GND	19	20	ADC2	
	ADC1 (and/or CMPIN+)	21	22	GND	GND
	ADC1	23	24	ADC2	

Table 2. TIDA-01349 Interface to Control Card (continued)

TIDA-01349 PINOUT	C2000 CONTROL CARD PINOUT	PIN NO		C2000 CONTROL CARD PINOUT	TIDA-01349 PINOUT
	ADC (and/or CMPIN+)	25	26	ADC2	
	ADC	27	28	ADC	
GND	GND	29	30	ADC	
	ADC	31	32	Rsv	
	ADC	33	34	ADC	
GND	GND	35	36	ADC	
	ADC	37	38	GND	GND
	ADC	39	40	ADC	
	Rsv	41	42	ADC	
	VREFLO on certain MCU	43	44	Rsv	
	VREFHI on certain MCU	45	46	GND	GND
	GND	47	48	5V0	5V
PWM_W_T	PWM1A	49	50	PWM3A	PWM_U_T
PWM_W_B	PWM1B	51	52	PWM3B	PWM_U_B
PWM_V_T	PWM2A	53	54	PWM4A	EN-CLK
PWM_V_B	PWM2B	55	56	PWM4B	
	PWM5A	57	58	PWM7A or TZ1	
	PWM5B	59	60	PWM7B or TZ2	
	PWM6A	61	62	PWM8A or TZ3	
	PWM6B	63	64	PWM8B or TZ4	
GND	GND	65	66	Rsv	
	SPISIMOA	67	68	QEP1A (McBSP-MDXA)	
	SPISOMIA	69	70	QEP1B (McBSP-MDRA)	
	SPICLKA	71	72	QEP1S (McBSP-MFSXA)	
	SPISTEA	73	74	QEP1I (McBSP-MCLKXA)	
EN-DO	CAP1 or SPISIMOB	75	76	SCIRXA/UARTRXA	
EN-DI	CAP2 or SPISOMIB	77	78	SCITXA/UARTTXA	
	CAP3 or SPICLKB	79	80	CANRXA	
	CAP4 or SPISTEB	81	82	CANTXA	
GND	GND	83	84	5V0	5V
	I2CSDAA	85	86	GPIO	EN-TXEN
	I2CSCLA	87	88	GPIO	
	GPIO	89	90	GPIO	EN-TXCLKEN
	GPIO	91	92	GPIO	
	GPIO	93	94	GPIO	
	GPIO	95	96	GPIO	
GND	GND	97	98	5V0	5V
DAT_I_V	SD-D1	99	100	QEP2A or GPIO	DAT_V_TEMP
CLK_I_V	SD-C1	101	102	QEP2B or GPIO	CLK_V_TEMP
DAT_I_U	SD-D2	103	104	QEP2S or GPIO	
CLK_I_U	SD-C2	105	106	QEP2I or GPIO	
DAT_V_DC_bus	SD-D3	107	108	GPIO (McBSP-MCLKRA)	
CLK_V_DC_bus	SD-C3	109	110	GPIO (McBSP-MFSRA)	
GND	GND	111	112	5V0	5V
	Rsv	113	114	Rsv	
	Rsv	115	116	Rsv	
	Rsv	117	118	Rsv	

Table 2. TIDA-01349 Interface to Control Card (continued)

TIDA-01349 PINOUT	C2000 CONTROL CARD PINOUT	PIN NO		C2000 CONTROL CARD PINOUT	TIDA-01349 PINOUT
	Rsv	119	120	Device Reset (Active low)	
	GPIO	121	122	GPIO	
	GPIO	123	124	GPIO	
	GPIO	125	126	GPIO	
	GPIO	127	128	GPIO	
	GPIO	129	130	GPIO	
	GPIO	131	132	GPIO	
	GPIO	133	134	GPIO	
GND	GND	135	136	Rsv	
	GPIO	137	138	Rsv	
	GPIO	139	140	Rsv	
	GPIO	141	142	Rsv	
	GPIO	143	144	Rsv	
	GPIO	145	146	Rsv	
	GPIO	147	148	Rsv	
	GPIO	149	150	Rsv	
	GPIO	151	152	Rsv	
	GPIO	153	154	Rsv	
	GPIO	155	156	Rsv	
GND	GND	157	158	5V0	5V
	GPIO	159	160	GPIO	
	GPIO	161	162	GPIO	
	GPIO	163	164	GPIO	
	GPIO	165	166	GPIO	
	GPIO	167	168	GPIO	
	GPIO	169	170	GPIO	
	Rsv	171	172	Rsv	
	Rsv	173	174	Rsv	
	Rsv	175	176	Rsv	
	Rsv	177	178	Rsv	
GND	GND	179	180	5V0	5V

3.1.3 Software

This reference design is tested using software modified from the application report *Sensored Field Oriented Control of 3-Phase Permanent Magnet Synchronous Motors Using TMS320F2837x*. The incremental build level 2 is used as the baseline. The software can be found in controlSUITE™. For questions on controlSUITE, visit the E2E forum: https://e2e.ti.com/support/microcontrollers/c2000/

3.2 Testing and Results

The focus of the tests is to evaluate the functionality and performance of the PWM isolation subsystem for the three-phase IPM-based inverter using the ISO7760 isolator.

3.2.1 Test Setup

Figure 25 shows the test setup used for characterizing the reference design. The F28379D 180-pin control card is mounted in the socket on the reference design board. External DC supplies power the primary-side 5-V rail and the secondary-side 15-V rail. Both these power supplies must be reinforced isolated from each other. The external high-voltage DC supply is connected to the inverter DC bus. The power-on sequence for this reference design is 5 V, 15 V, and then the DC bus voltage; the power-off sequence is the opposite. The controller is connected to the laptop through USB, which is running the motor control software in Code Composer Studio™ (CCS).

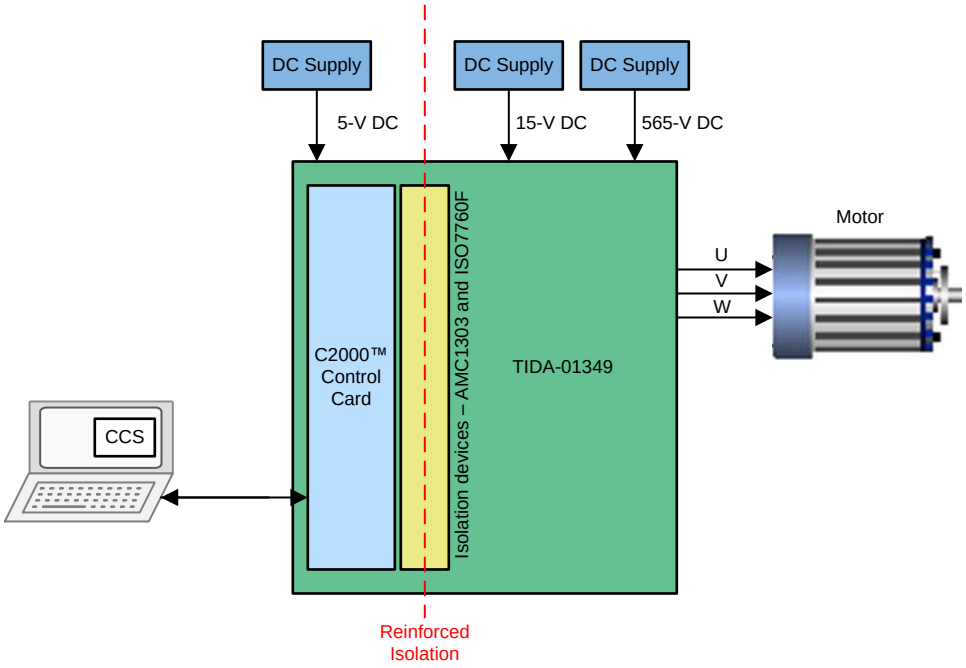


Figure 25. Test Setup

3.2.2 Test Results

3.2.2.1 PWM Propagation Delay and Channel-to-Channel Propagation Delay Matching

The ISO7760F has a propagation delay of 11 ns (typical) and a channel-to-channel output skew of < 4 ns. The propagation delays are measured according to the convention shown in Figure 26. The low-PWM propagation delays enable decreasing dead time and reducing phase voltage distortions.

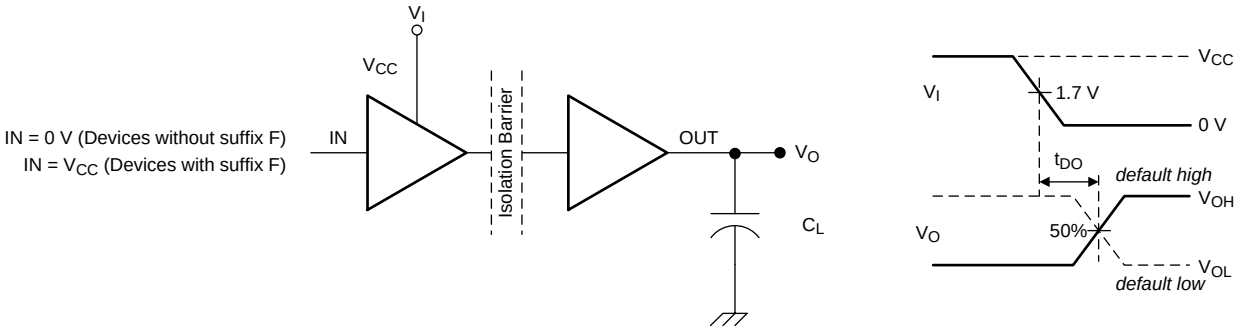


Figure 26. Propagation Delay Measurement Convention

The propagation delay waveforms are captured on the reference design. Figure 27 to Figure 31 show the input and output PWM signals of the top channel of Phase U. This test uses a PWM switching frequency of 8 kHz with a 50% duty cycle. Note that all the waveforms in this section are captured with an IPM PWM input load.

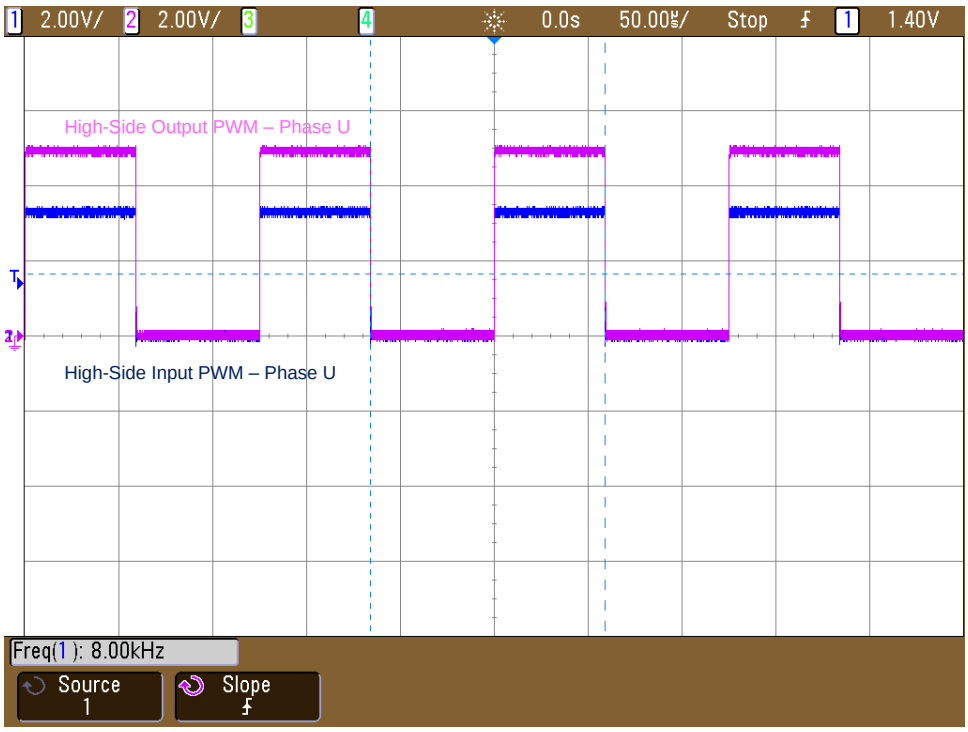


Figure 27. Input and Output PWM Waveforms of ISO7760F

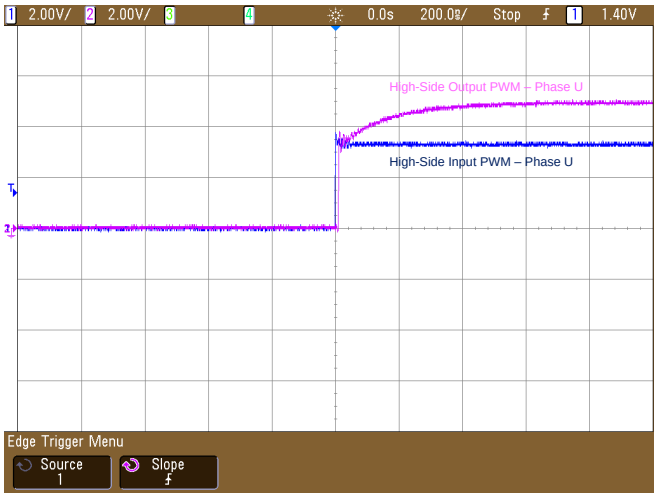


Figure 28. Rising Edge of PWM Signal—Propagation Delay

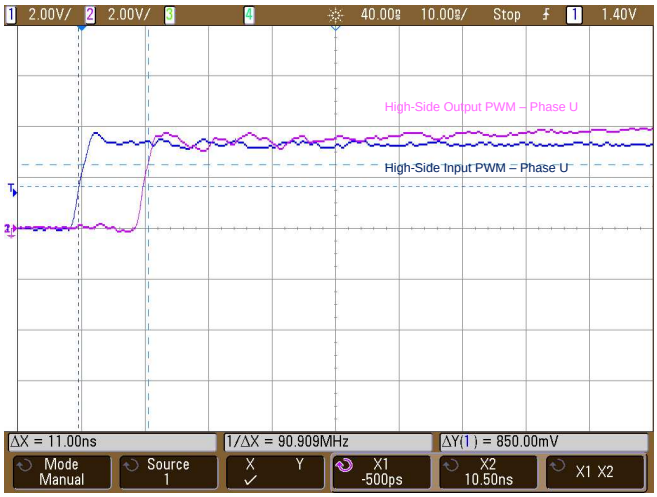


Figure 29. Rising Edge of PWM Signal Zoomed (Measured 11 ns)

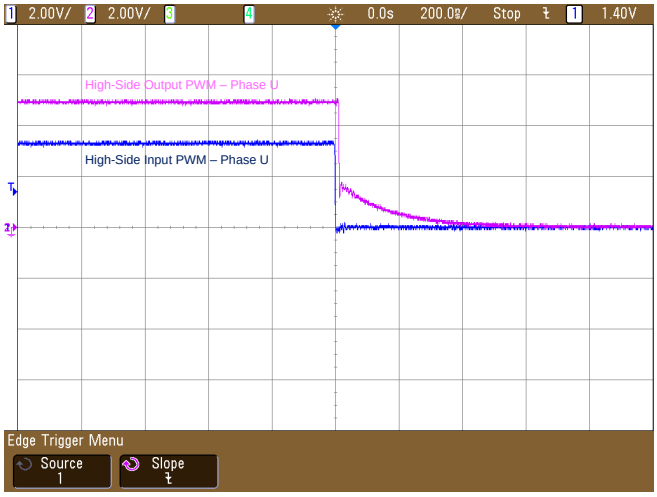


Figure 30. Falling Edge of PWM Signal—Propagation Delay

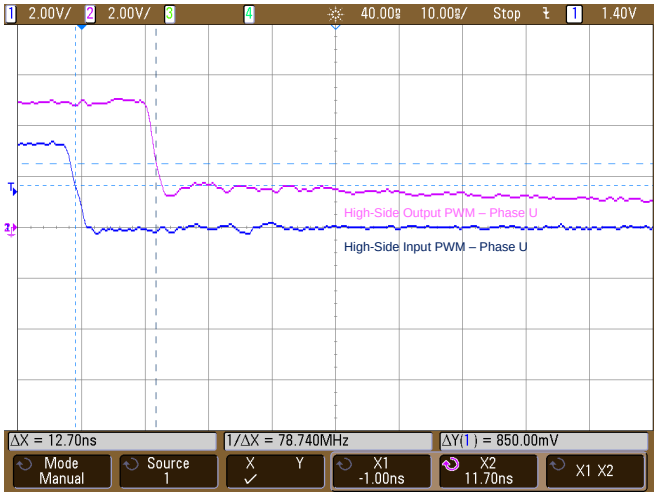


Figure 31. Falling Edge of PWM Signal Zoomed (Measured 12.7 ns)

Figure 32 to Figure 35 show the channel-to-channel propagation delay skew for the ISO7760F on the reference design. This test uses a 8-kHz PWM signal with a 50% duty cycle. The same PWM signal is provided for all the high-side and low-side switches. The DC bus of the inverter is not powered.

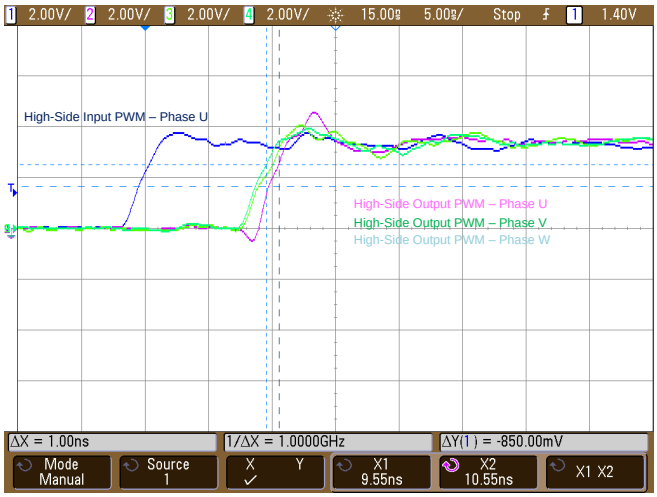


Figure 32. High-Side PWM Propagation Delay Skew—Rising Edge (Measured 1 ns)

Figure 33. High-Side PWM Propagation Delay Skew—Falling Edge (Measured 1.55 ns)

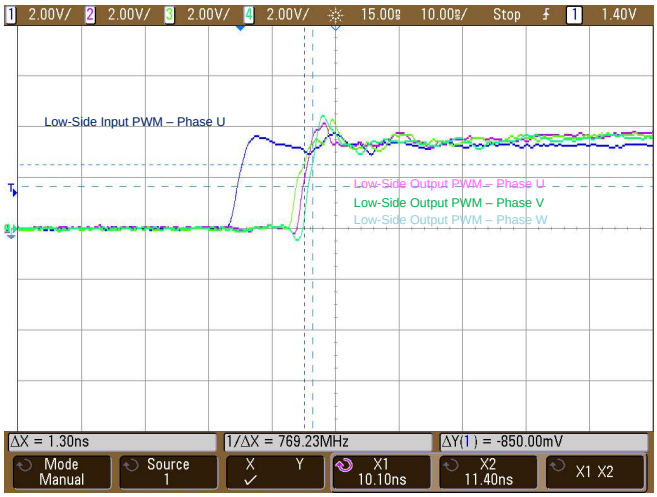


Figure 34. Low-Side PWM Propagation Delay Skew—Rising Edge (Measured 1.3 ns)

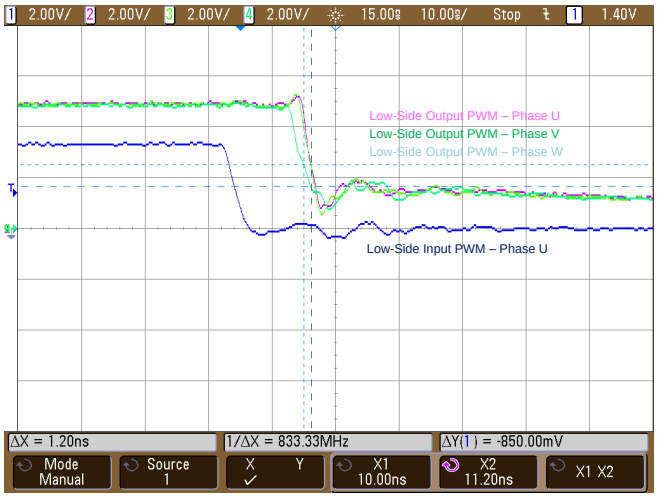


Figure 35. Low-Side PWM Propagation Delay Skew—Falling Edge (Measured 1.2 ns)

3.2.2.2 PWM Isolator Thermal Plot

Figure 36 and Figure 37 show the current waveforms of the isolator power supply on the secondary side at 2-kHz and 20-kHz PWM switching frequencies. For this test, all the high-side and low-side PWM signals are set at a 50% duty cycle.

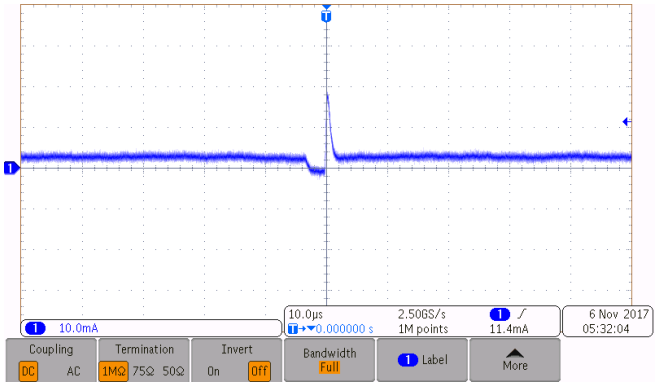


Figure 36. Icc2 at 2-kHz PWM

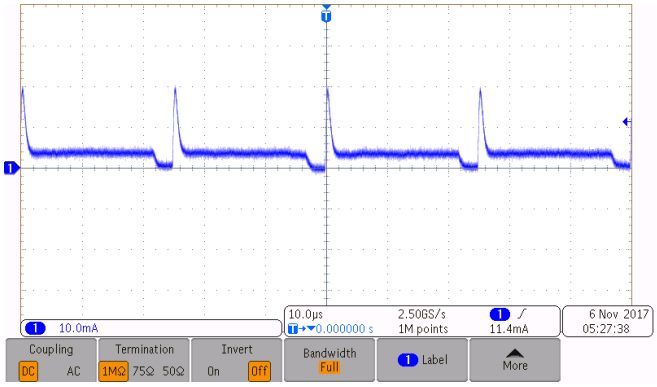


Figure 37. Icc2 at 20-kHz PWM

For the thermal plot capture, the PWM signals are set at a maximum 20-kHz switching frequency as limited by the IPM used in this reference design. This test uses a 50% duty cycle. Figure 38 shows the temperature of the ISO7760F device after 30 minutes. For this test, the DC bus voltage is not powered on to capture only the temperature rise of the ISO7760F due to self heating.

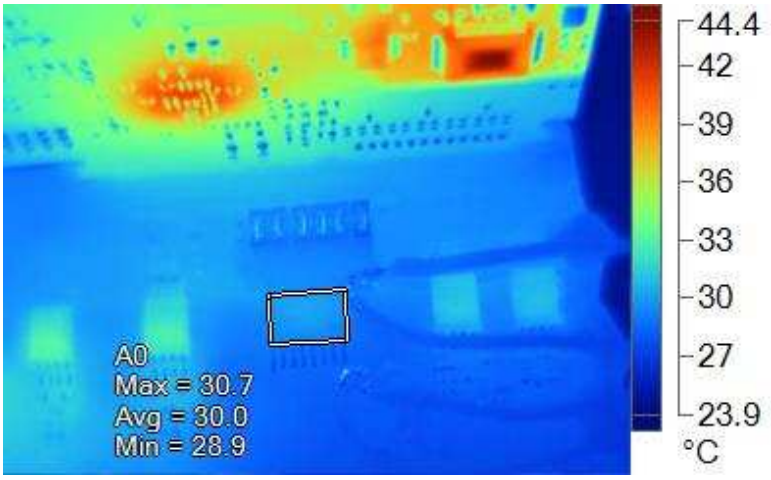


Figure 38. ISO7760F Temperature Rise After 30 Minutes

3.2.2.3 IPM Input PWM and Switch Node Waveforms

This section shows the functionality of the inverter. The DC bus voltage is powered up with 565-V DC, which corresponds to a grid voltage of 400-V AC. The voltage of the inverter switch node for Phase U and the corresponding PWM signals are captured at different switching conditions. The inverter is run at a 8-kHz switching frequency and the dead time is set at 3.2 µs. The motor current is taken as positive if it is leaving the switch node and negative if it is entering the switch node.

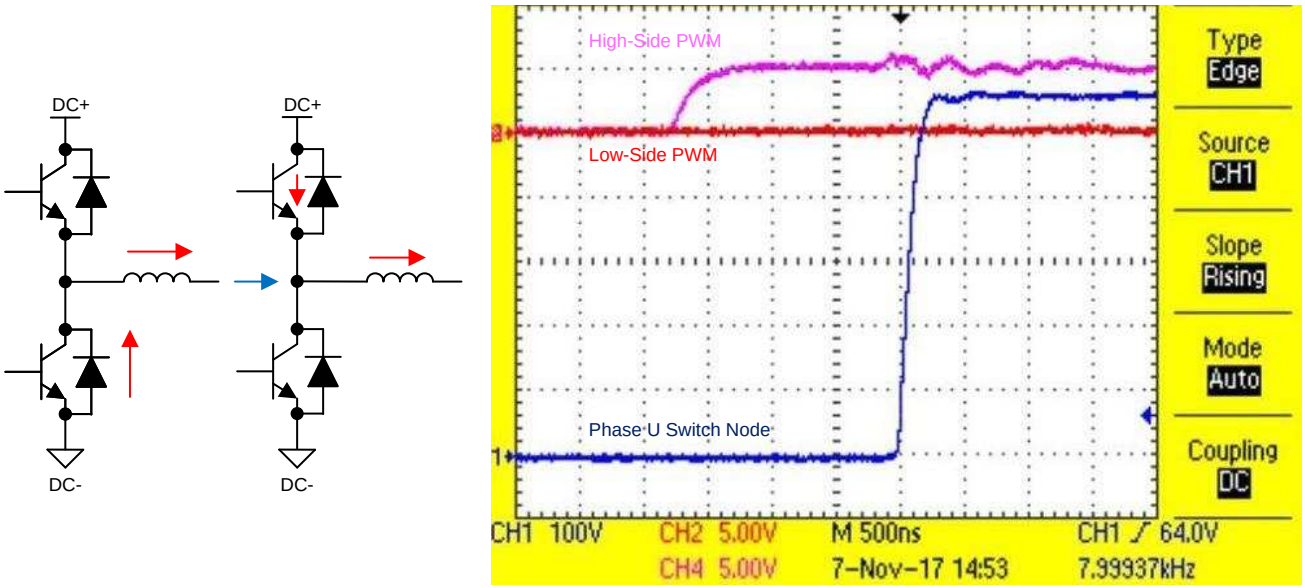


Figure 39. Hard Switch on—High-Side IGBT Captured at 5-A Motor Current

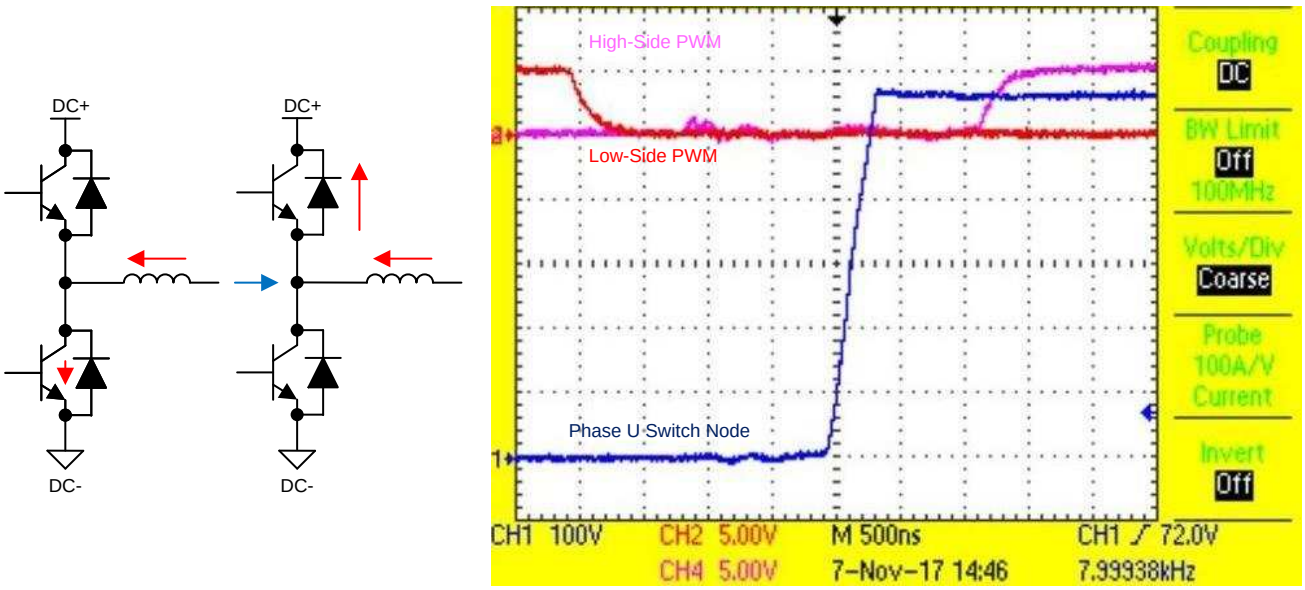


Figure 40. Soft Switch on—High-Side IGBT Captured at –5-A Motor Current

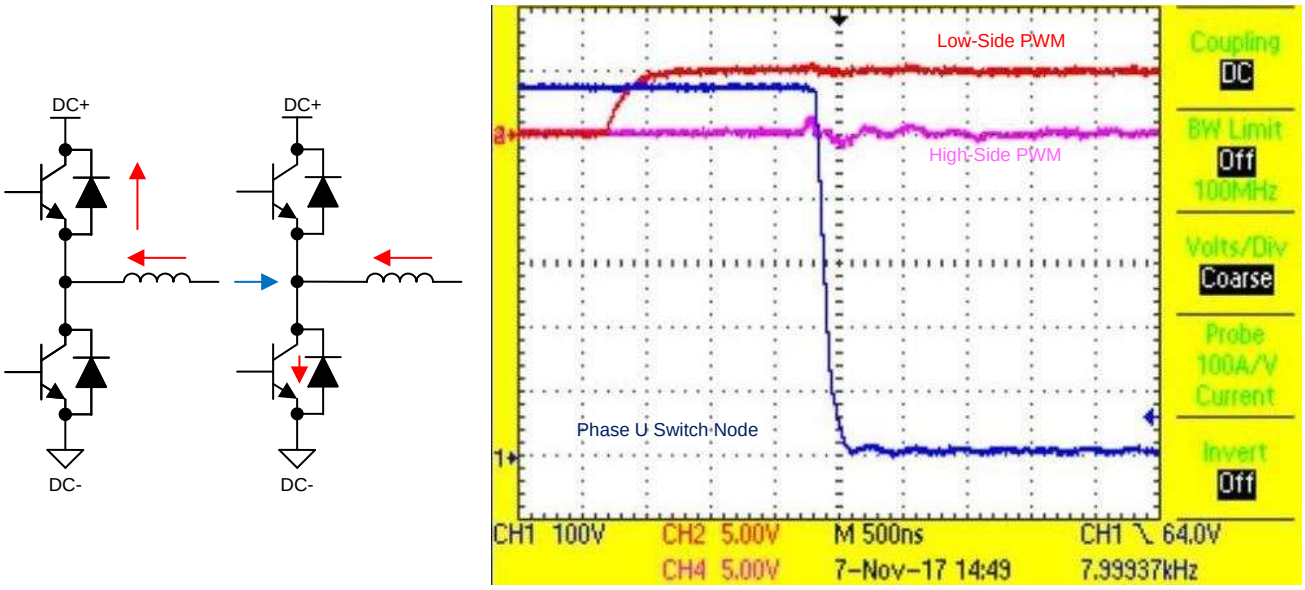


Figure 41. Hard Switch on—Low-Side IGBT Captured at –5-A Motor Current

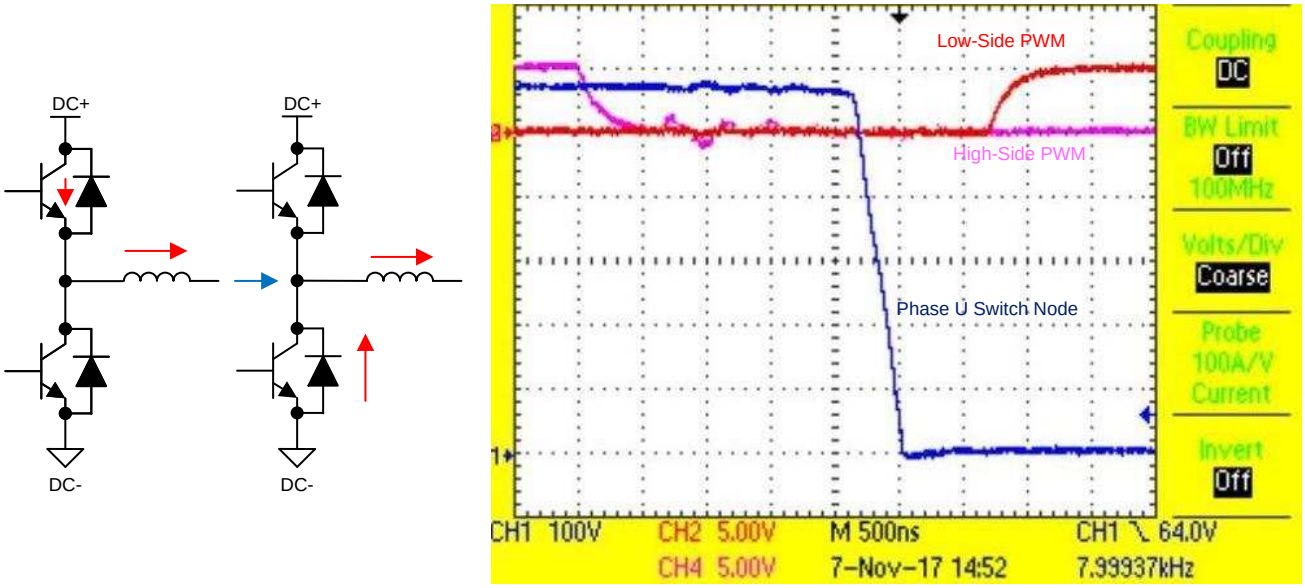


Figure 42. Soft Switch on—Low-Side IGBT Captured at 5-A Motor Current

3.2.2.4 PWM Interlocking Using Optional Add-on Card

This section shows the functionality of the add-on interlocking card. For testing the card, a PWM signal of 8 kHz with a 3.2-µs dead time is used. The dead time is made purposefully negative to overlap the high-side and low-side PWM signals and show the interlocking function.

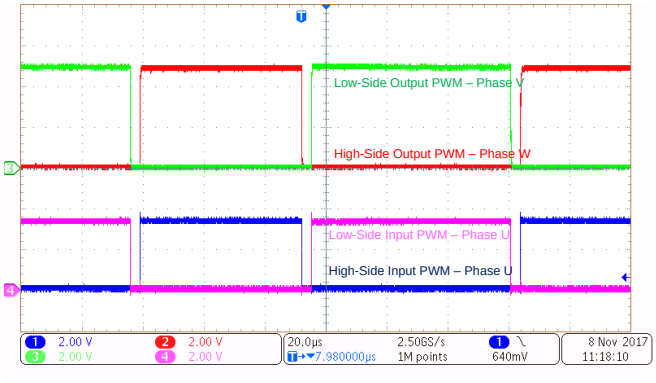


Figure 43. Normal Operation of High-Side and Low-Side PWM Signals (Phase U)

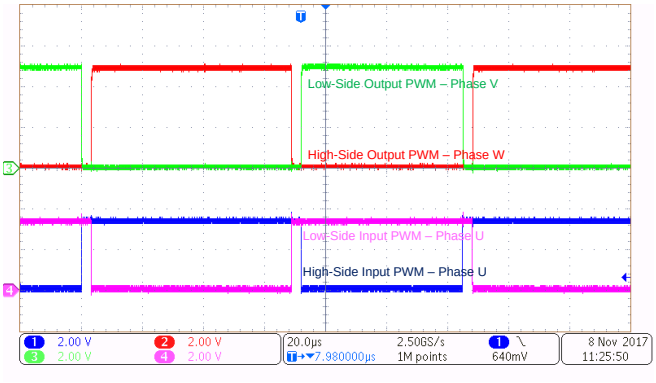


Figure 44. Negative Dead Time Fault Purposefully Introduced to Check Interlocking Function (Phase U)

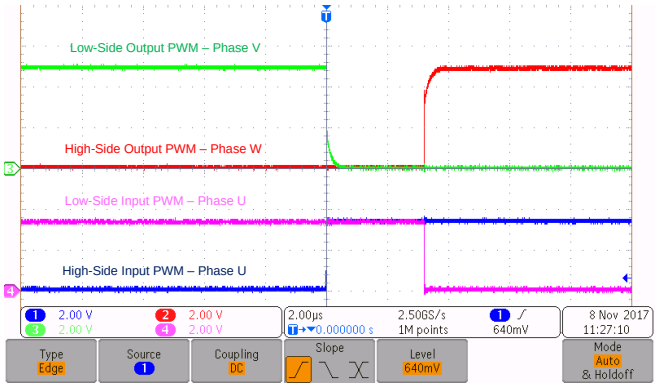


Figure 45. Rising Edge of PWM Signal Interlock (Phase U)

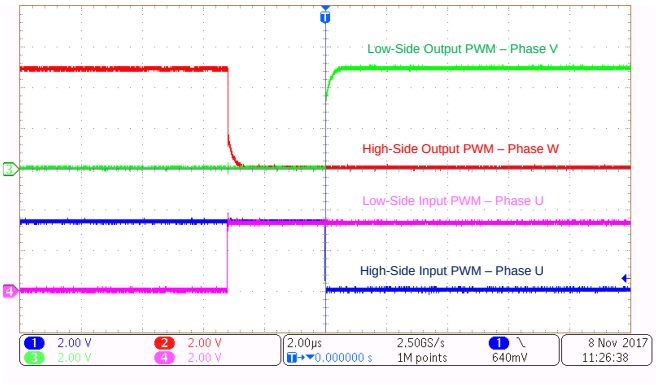


Figure 46. Falling Edge of PWM Signal Interlock (Phase U)

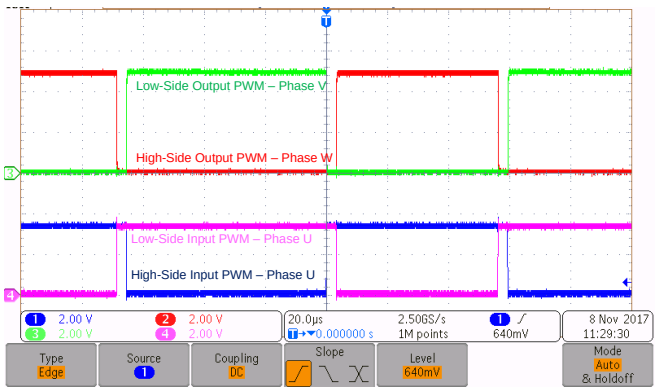


Figure 47. Interlocking (Phase V)

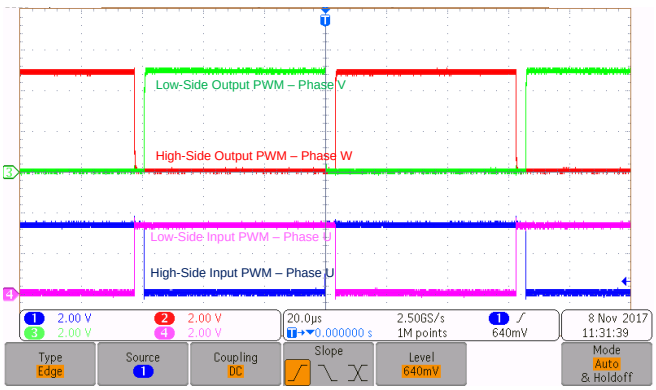


Figure 48. Interlocking (Phase W)

3.2.2.5 EFT on Motor Power Interface

This section shows the robustness of the ISO7760F to external EFT events. EFT pulses of different amplitudes and polarities are applied on the power interface cable between the three-phase inverter and the motor as shown in Figure 49. The tests are conducted according to IEC 61800-3, which refers to IEC 61000-4-4 for EFT tests.

Figure 49 to Figure 52 show the setup for the EFT test. The power cable is passed through a 1-m capacitive coupling clamp, through which EFT is injected into the cable. A 1-m cable length is maintained from the capacitive clamp to the inverter. The inverter and the motor are placed on a wooden platform, which is at a height of 10 cm from the table reference. The cable shield is connected to the table reference using a copper strap. This connection has the same effect as earthing the cable gland or collar in drive systems. The heat sink and the primary-side ground are also connected to the table reference.

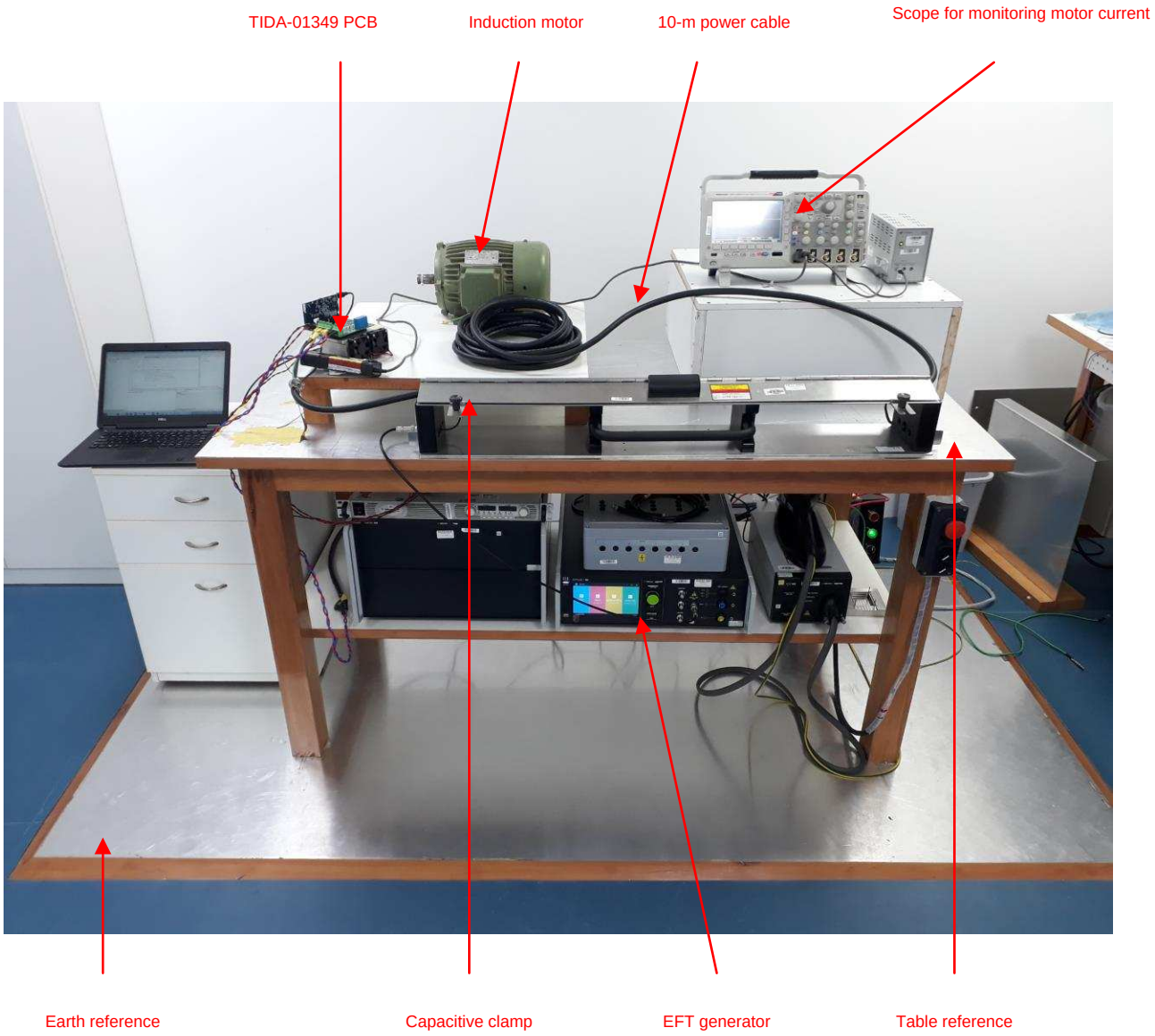


Figure 49. EFT Test Setup

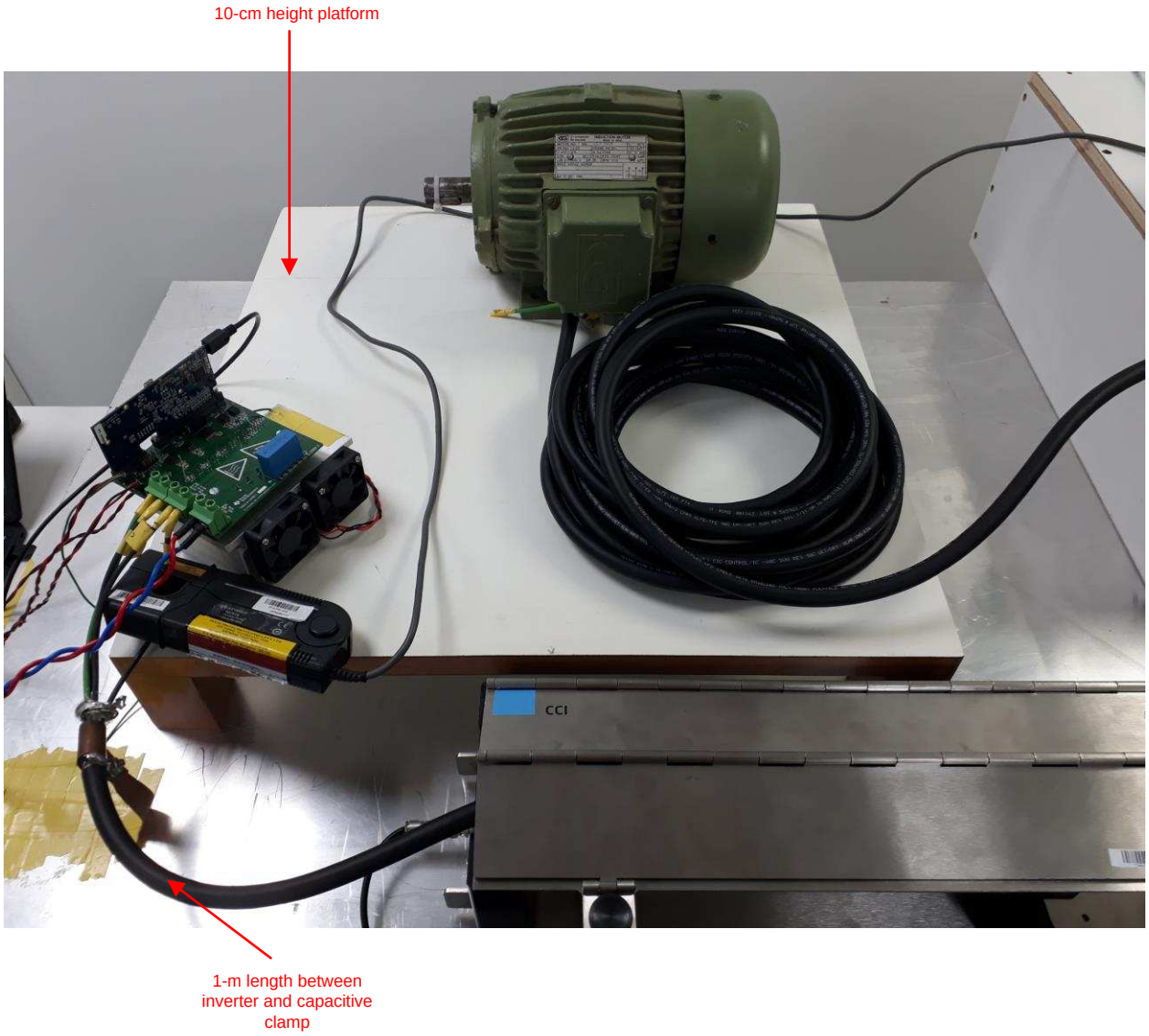


Figure 50. Inverter and Motor Placed on Wooden Board at Height of 10 cm From Table Reference

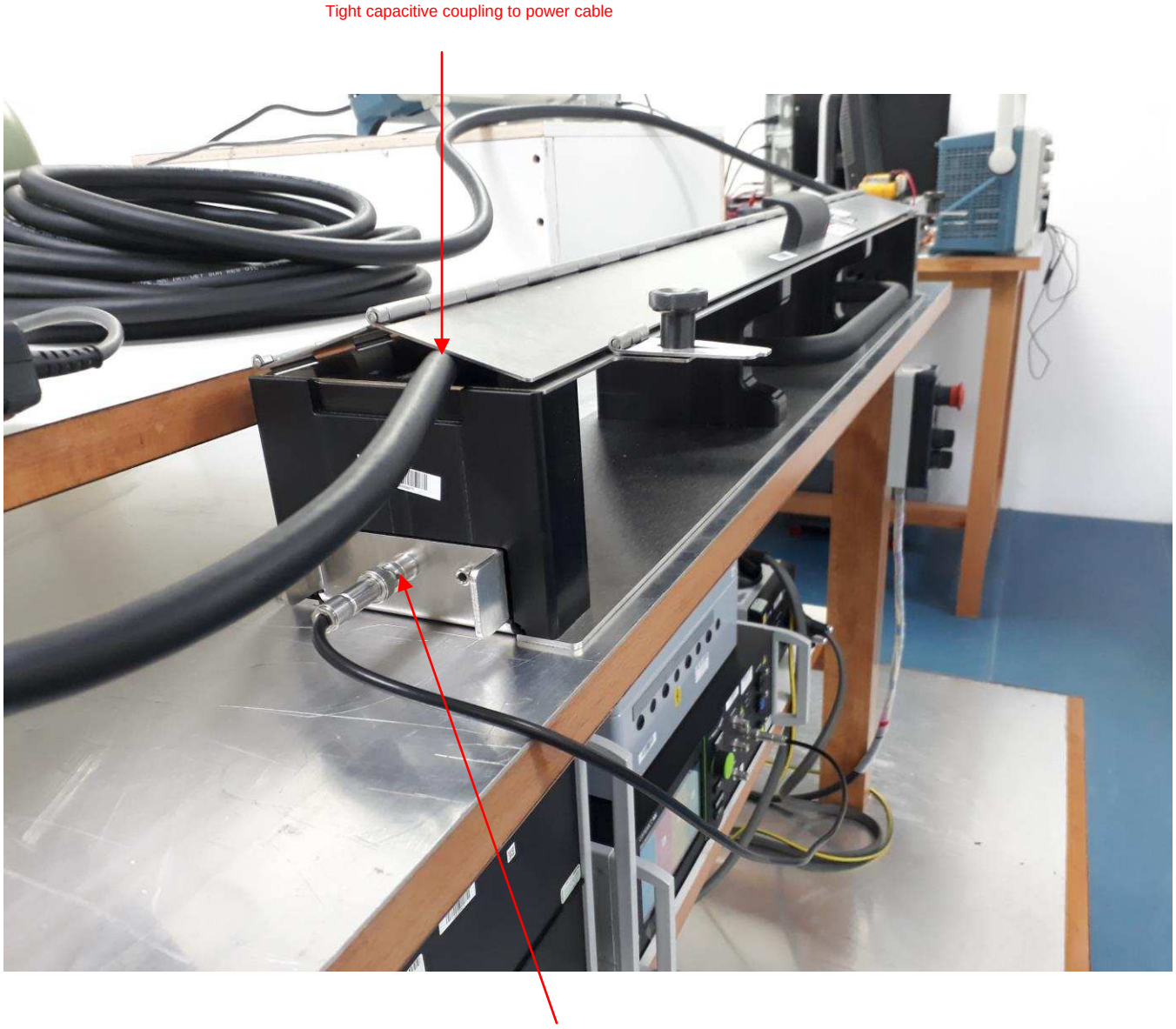


Figure 51. Power Cable Passed Through Capacitive Clamp

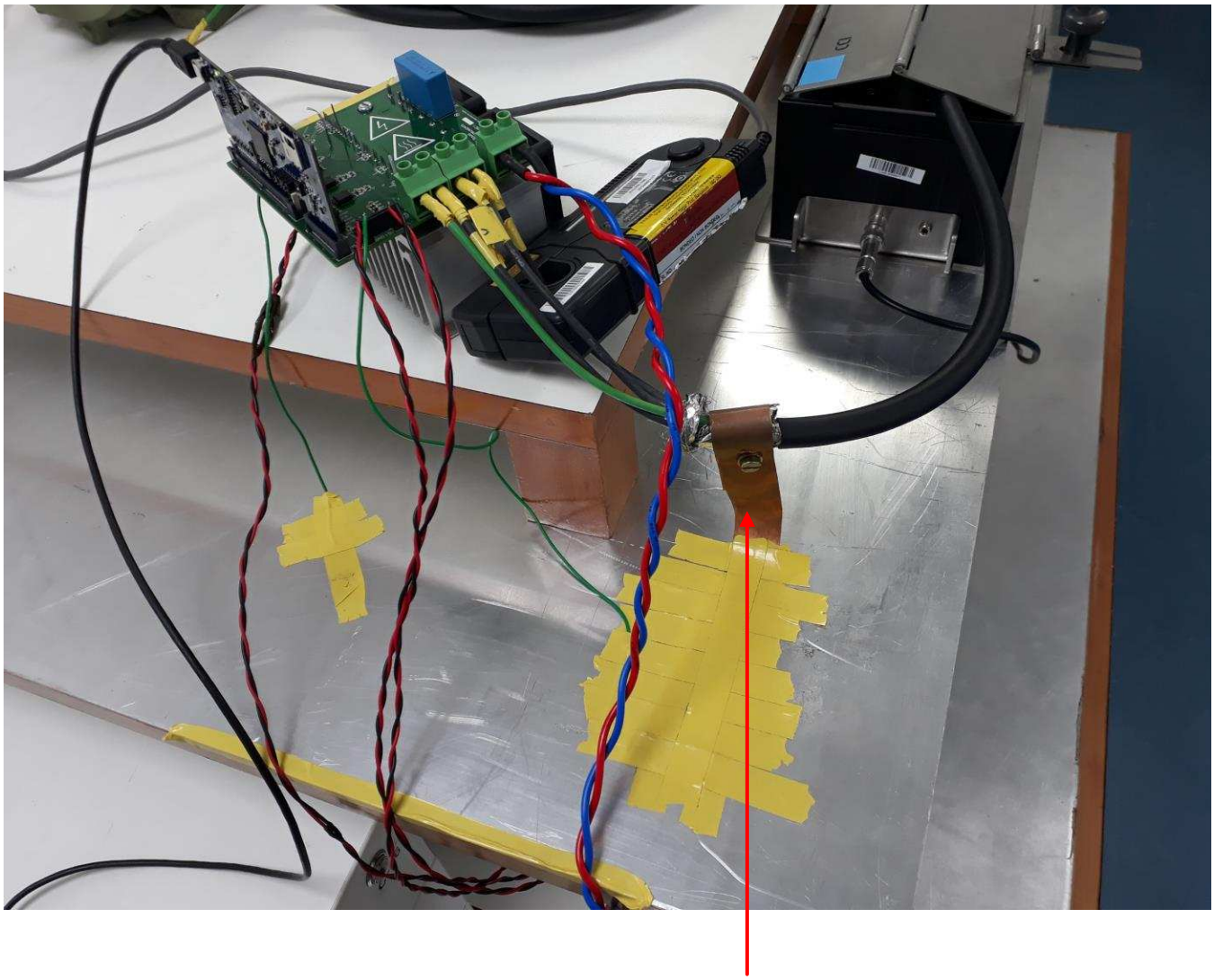


Figure 52. Connection of Shield of Power Cable to Table Reference

3.2.2.5.1 Test Conditions

The 5-kHz EFT pulse bursts for 60 s. The burst duration is 15 ms and burst period is 300 ms. A typical EFT pulse of 5 ns rise time, and a duration of 50 ns is used. For the test, a 10-m shielded 4 conductor cable is used (part number: V16016 BK005, manufacturer: Alpha wire). Three conductors are used for the UVW phases, and the fourth conductor is left floating. 565-V DC is applied to the inverter DC bus. The inverter is switched at a frequency of 8 kHz, the motor frequency is set at 10 Hz, and the RMS voltage applied to the motor is approximately 120 V_{RMS} phase to phase.

3.2.2.5.2 Pass and Fail Conditions

The motor must run continuously without any unusual sounds and without malfunction observed in the power stage. Table 3 defines the performance criteria.

Table 3. EFT Test Performance Criteria

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module must continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance during test is accepted. After the test, the module must continue to operate as intended without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module must continue to operate as intended, after manual restart, power off, or power on. Not self-recoverable.
D	Damage to hardware.

Table 4. EFT Results

EFT PULSES (kV)	PERFORMANCE CRITERIA
0.5	A
–0.5	A
1	A
–1	A
2	A
–2	A
4	A
–4	A

NOTE: The EFT testing is done only for the PWM isolation subsystem while running the inverter in open loop control. The current and voltage sensing are not characterized.

3.2.2.6 Multiplexing Fault Signal With Temperature Measurement

In this reference design, the IPM fault signal is multiplexed with the analog temperature signal to save an isolation channel. The IPM fault can be triggered by either an UVLO event on the IPM control power supply or by a short-circuit detection in one of the low-side IGBT switches of the IPM. For the test, the IPM fault signal is activated by lowering the IPM control power supply from 15 V to 8 V. This new voltage triggers the IPM UVLO diagnostic feature.

Figure 53 to Figure 55 show the fault signal multiplexing with the temperature measurement data. The fault signal is an active low signal. As long as it is high, the delta-sigma modulator outputs the data to the controller. When the fault signal goes low, the input stage of the delta-sigma modulator is overranged. The diagnostic feature of the delta-sigma modulator forces the output to zero with a bit toggle every 128 bits as shown in Figure 56.

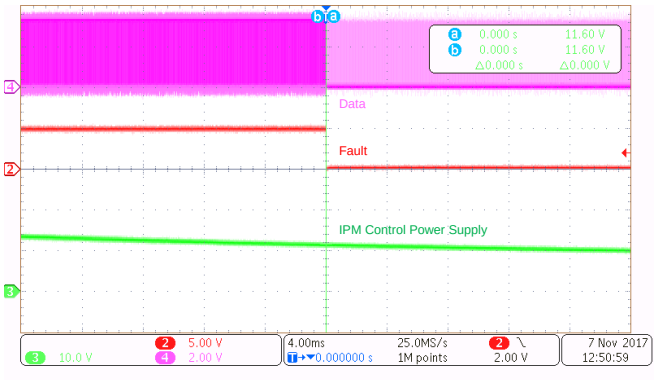


Figure 53. Fault Signal Detection

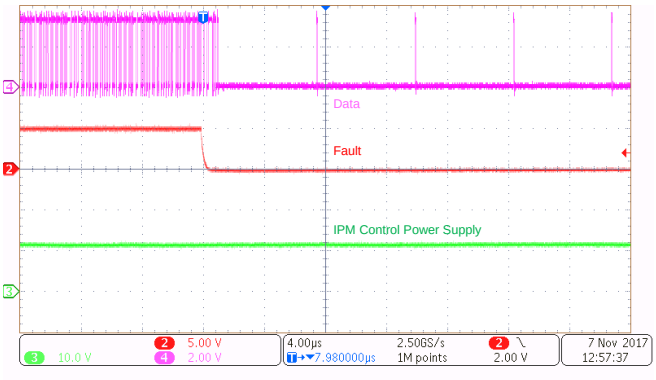


Figure 54. Fault Signal Detection Zoomed

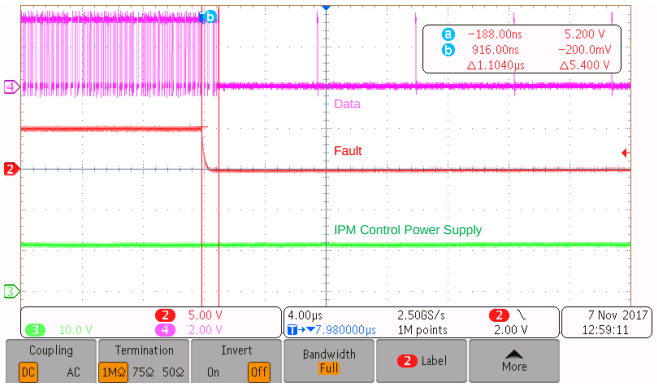


Figure 55. Fault Detection Delay Across Isolator

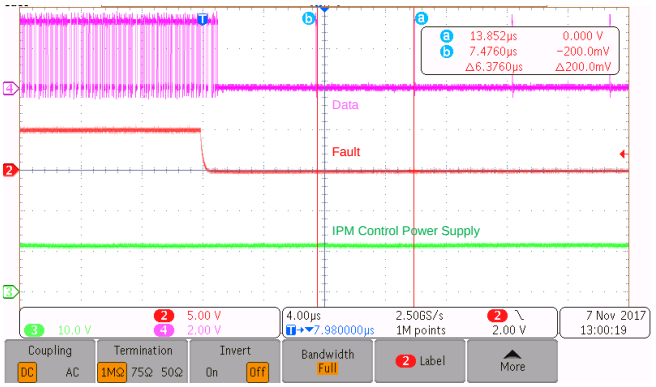


Figure 56. Bit Toggle Every 128 Bits

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01349.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01349.

4.3 PCB Layout Recommendations

4.3.1 Reinforced Isolation Barrier

Figure 57 shows the isolation barrier and the ground split. The copper tracks on the high-voltage inverter side and the low-voltage controller side are separated from each other by a reinforced isolation barrier. The wide body package of the digital isolator and the delta-sigma modulators are placed across the isolation barrier. The creepage spacing of the isolation barrier is maintained to a minimum of 8 mm.

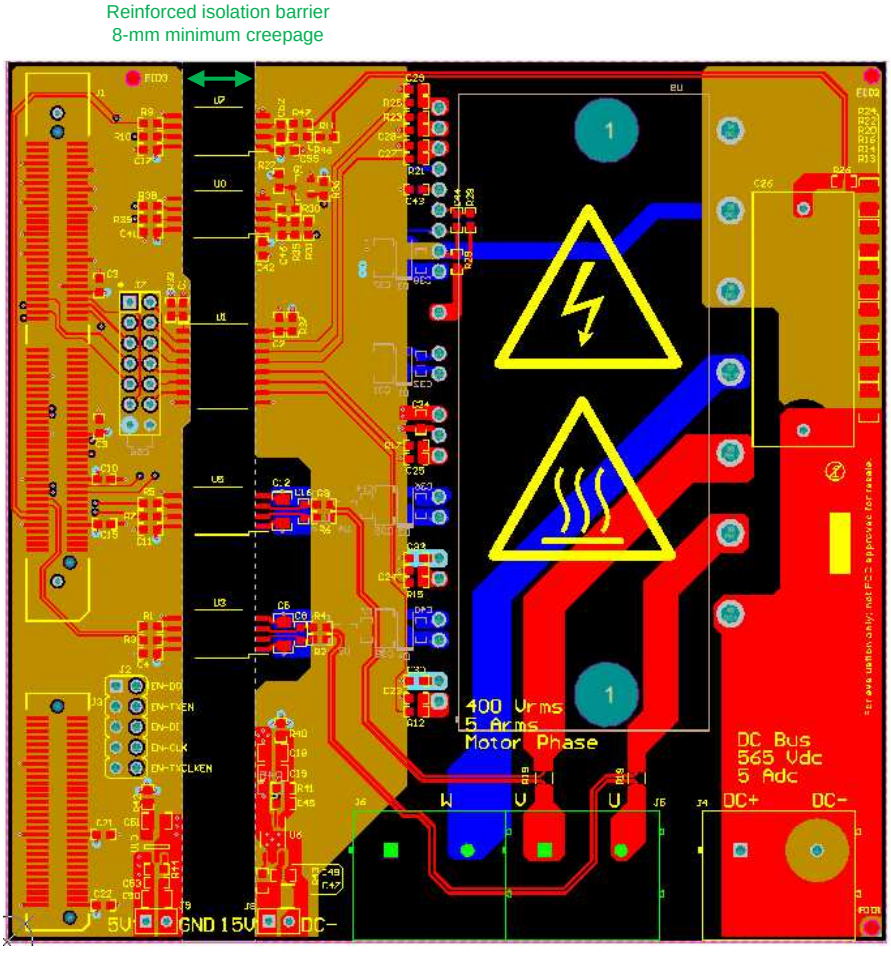


Figure 57. Reinforced Isolation Barrier and Creepage Spacing

4.3.2 Current Sensing

Use Kelvin connections on the shunt resistors for accurate current sensing as shown in Figure 58. The current sense signals are then routed like a differential pair to the delta-sigma modulator input stages. The differential routing ensures that noise if any equally impacts both the current sense lines, and this will get rejected by the common-mode rejection of the delta-sigma modulator.

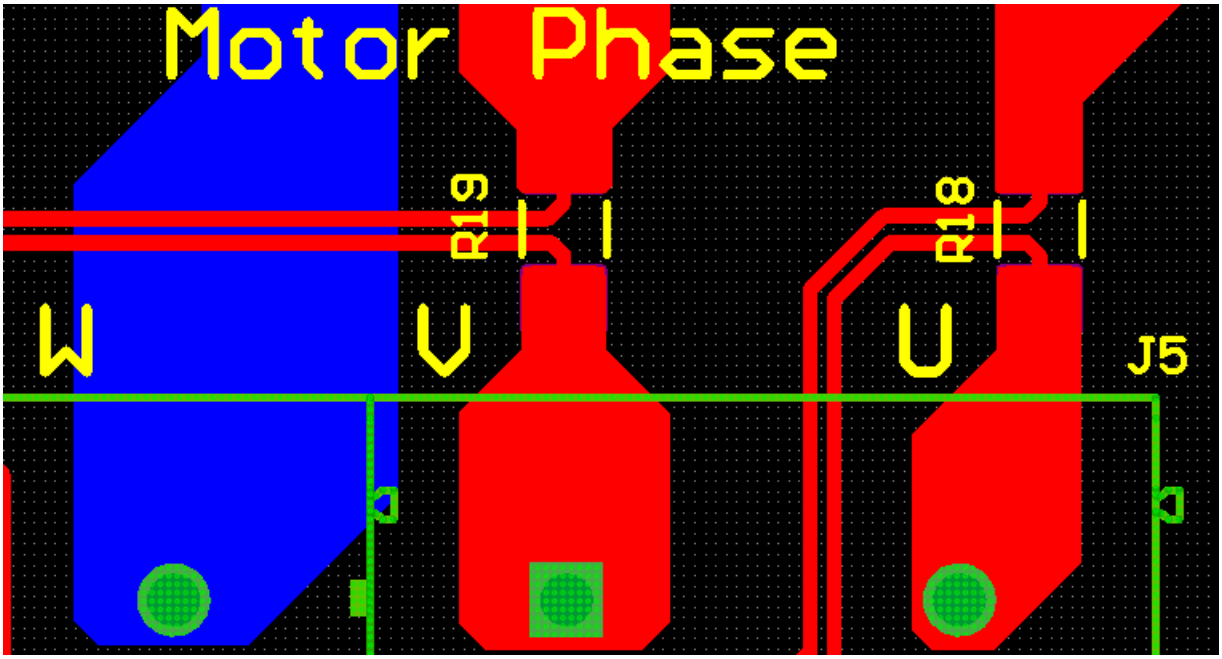


Figure 58. Kelvin Connection to Shunt Resistors

At the delta-sigma modulator, place the differential RC filter comprising of R2, R4, and C8 close to the input stage of the device U3. Place the decoupling capacitor of the power supply (C5) close to the power supply pins of the device and connect it directly without the use of vias. The TLV76050 LDO (U2), placed on the bottom side of the PCB (Figure 60), generates the 5-V supply for the delta-sigma modulator from the 15-V bootstrap supply and is placed close to the modulator. The small SOT-23 package of the LDO enables this while still managing to keep sufficient creepage distances from the neighboring high-voltage nets. Place input and output decoupling capacitors close to LDO.

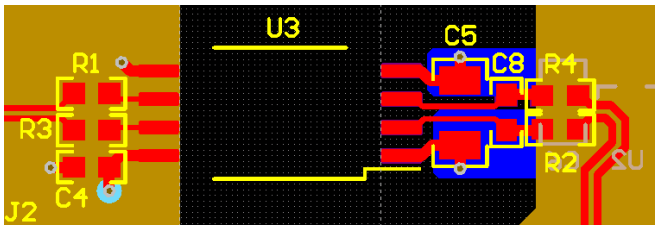


Figure 59. AMC1303M0520 Layout

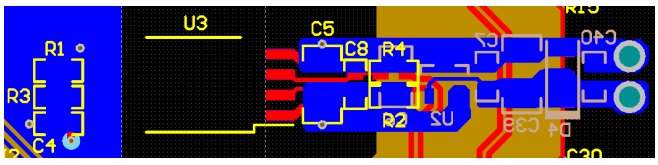


Figure 60. LDO Placement

4.3.3 LDO Layout

Place input decoupling capacitors C50 and C53 close to input of LDO U10 and the output decoupling capacitor C51 close to the output stage to improve PSRR, output noise, and transient response.

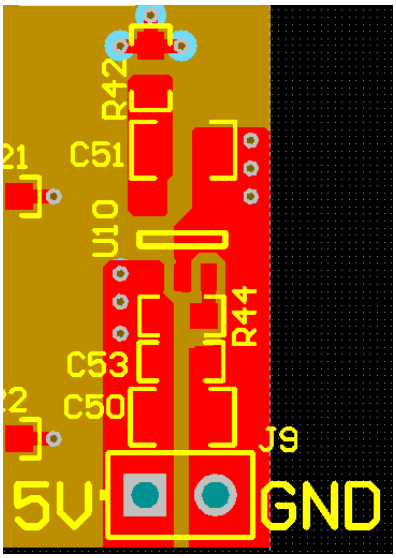


Figure 61. Layout for TPS70633

To improve AC performance like PSRR, output noise, and transient response of LDO U6, place decoupling capacitors C47, C49, C19, and C18 close to the device. Place all the decoupling capacitors on the same side of the PCB as the device. The metal pad beneath the device is connected to the DC-ground plane with multiple vias to further improve thermal performance of the package.

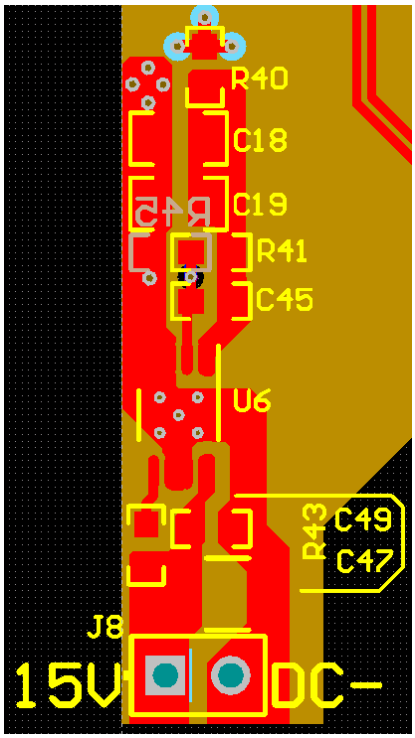


Figure 62. Layout for TPS7A4201

4.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-01349.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01349.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01349.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01349.

5 Related Documentation

1. Texas Instruments, *Sensored Field Oriented Control of 3-Phase Permanent Magnet Synchronous Motors Using TMS320F2837x Application Report*
2. Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity Application Report*
3. Mitsubishi Electric, *1200V LARGE DIPIPM Ver.6 Series APPLICATION NOTE PSS**SA2FT*

5.1 Trademarks

6 Terminology

IGBT— Insulated gate bipolar transistor

IPM— Intelligent power modules

HVIC— High-voltage IC

LVIC— Low-voltage IC

PWM— Pulse width modulation

UVLO— Undervoltage lockout

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265