PMP40274 Test Results

1 General

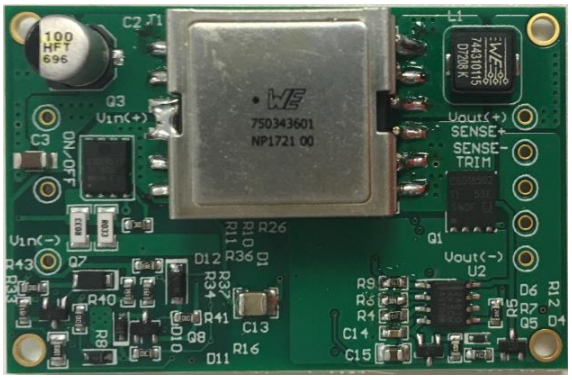
1.1 PURPOSE

The PMP40274 is a power module reference design solution for power train applications. The module enables a high efficiency with flyback-CCM synchronous rectifier. The efficiency is >88% at full load. This design features <0.2W standby power. Integrated input UVLO, OVP and output OVP, OCP keeps the whole power system reliability. The design is achieved in a compact form factor (50.8mm X 40.6mm X 15mm).

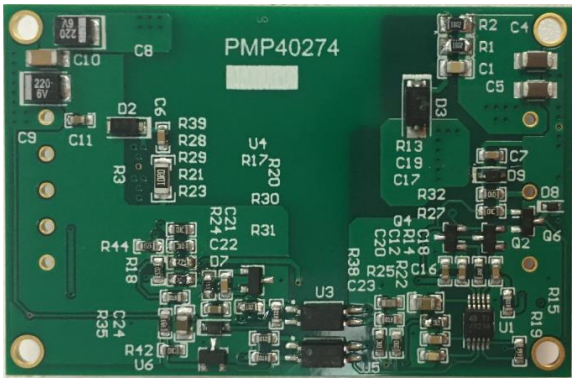
TEST EQUIPMENTS

Multi-meter: Fluke Multimeter 287C, Agilent 34401A, Fluke 8845A
DC Source: TDK-Lambda, DC Load: Chroma 63103A
Ambient Temperature at 25DegC

1.2 TEST Setup Photos



Top View of the Board



Bottom View of the Board

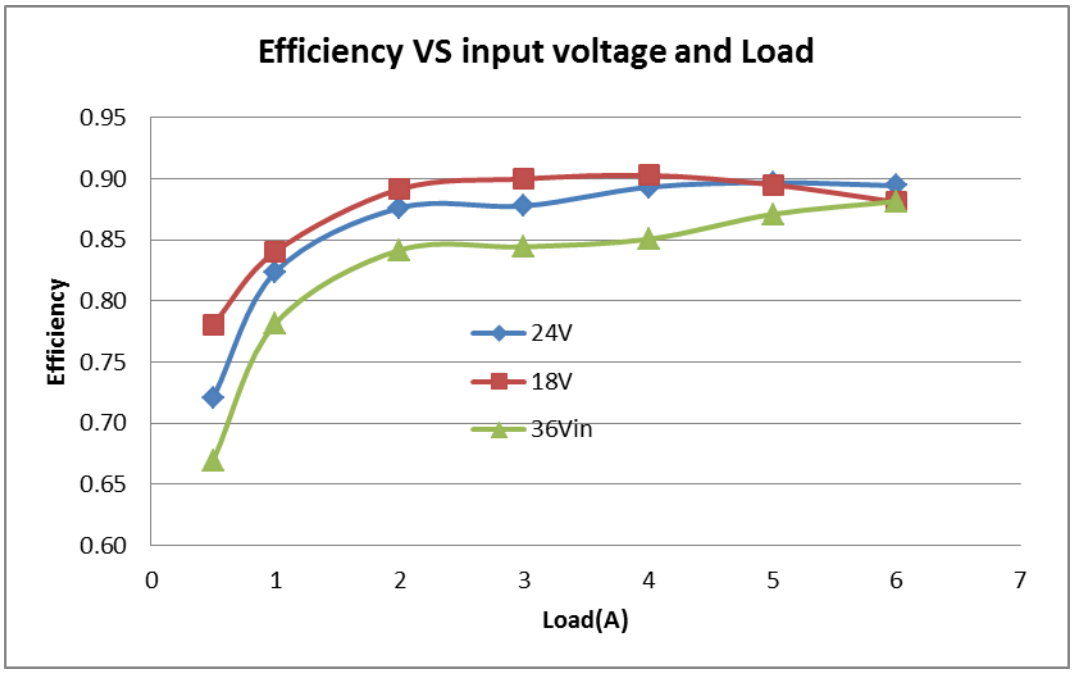
2 INPUT & Output CHARACTERISTICS

2.1 : Efficiency data vs Output

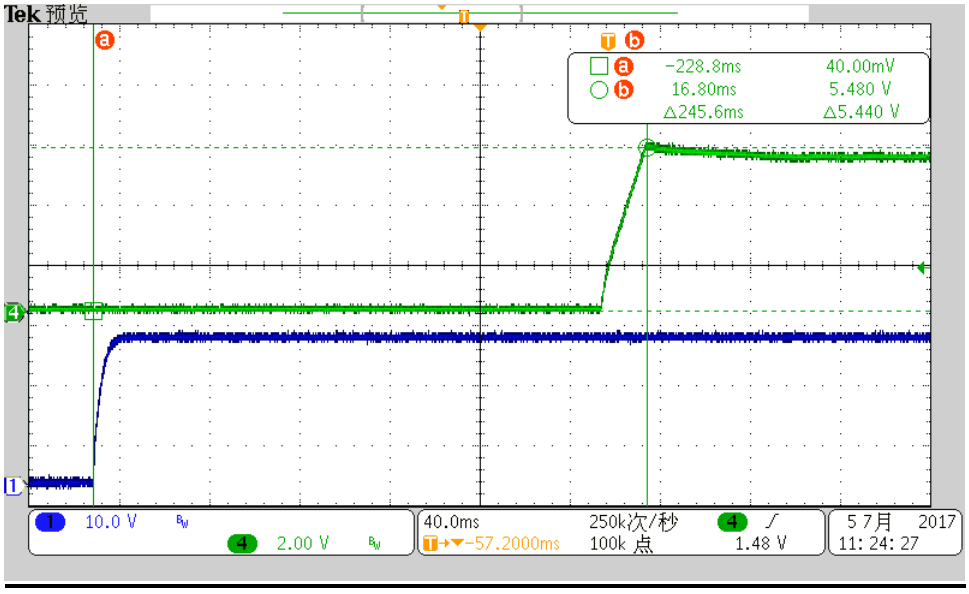
Vin(V)	Iin(A)	Vout(V)	Iout(A)	Efficiency	Pin(W)
18.149	0.01	5.091	0		0.18
18.265	0.176	5.048	0.4972	0.7808	3.21
18.218	0.329	5.047	0.9981	0.8404	5.99
18.125	0.624	5.046	1.9984	0.8916	11.31
18.025	0.933	5.044	3.0008	0.9000	16.82
17.921	1.247	5.041	4.0025	0.9029	22.35
17.820	1.579	5.034	5.0038	0.8952	28.14
17.721	1.932	5.025	6.0024	0.8809	34.24

Vin(V)	Iin(A)	Vout(V)	Iout(A)	Efficiency	Pin(W)
24.367	0.006	5.061	0		0.15
23.991	0.145	5.044	0.4972	0.7209	3.48
23.957	0.255	5.042	0.9981	0.8238	6.11
23.887	0.481	5.038	1.9984	0.8763	11.49
23.810	0.722	5.029	3.0008	0.8779	17.19
23.737	0.949	5.027	4.0025	0.8932	22.53
23.661	1.185	5.026	5.0038	0.8970	28.04
23.579	1.430	5.024	6.0024	0.8944	33.72

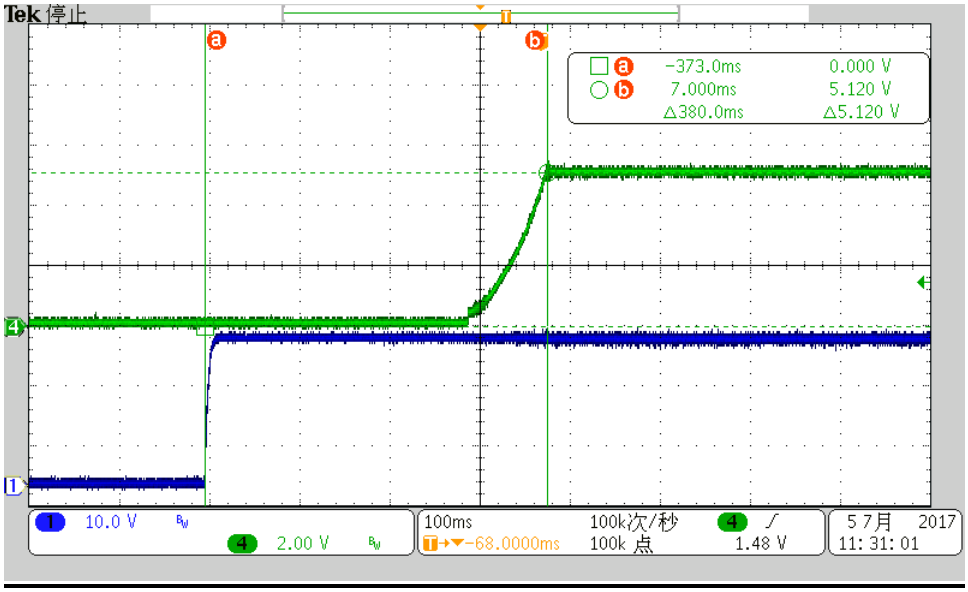
Vin(V)	Iin(A)	Vout(V)	Iout(A)	Efficiency	Pin(W)
36.258	0.004	5.063	0		0.15
36.316	0.103	5.038	0.4972	0.6697	3.74
36.293	0.177	5.030	0.9981	0.7815	6.42
36.248	0.329	5.023	1.9984	0.8417	11.93
36.194	0.493	5.021	3.0008	0.8444	17.84
36.151	0.653	5.017	4.0025	0.8506	23.61
36.107	0.798	5.016	5.0038	0.8711	28.81
36.061	0.947	5.016	6.0024	0.8816	34.15



2.2 : Startup

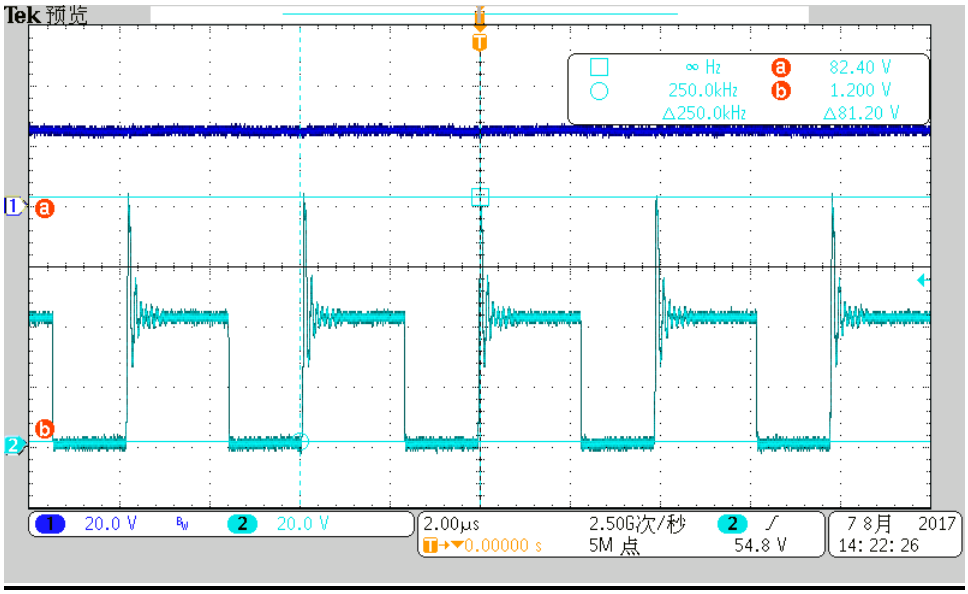


CH1=Vin;CH4=Vout; 24Vin Startup with no load

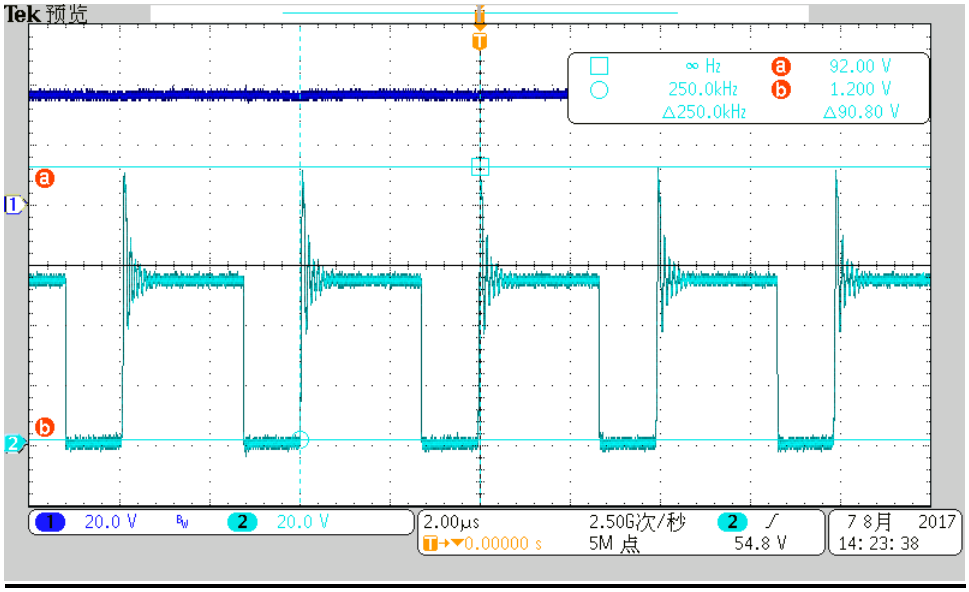


CH1=Vin; CH4=Vout; Startup with Full load

2.3: Primary MOSFET Voltage Stress

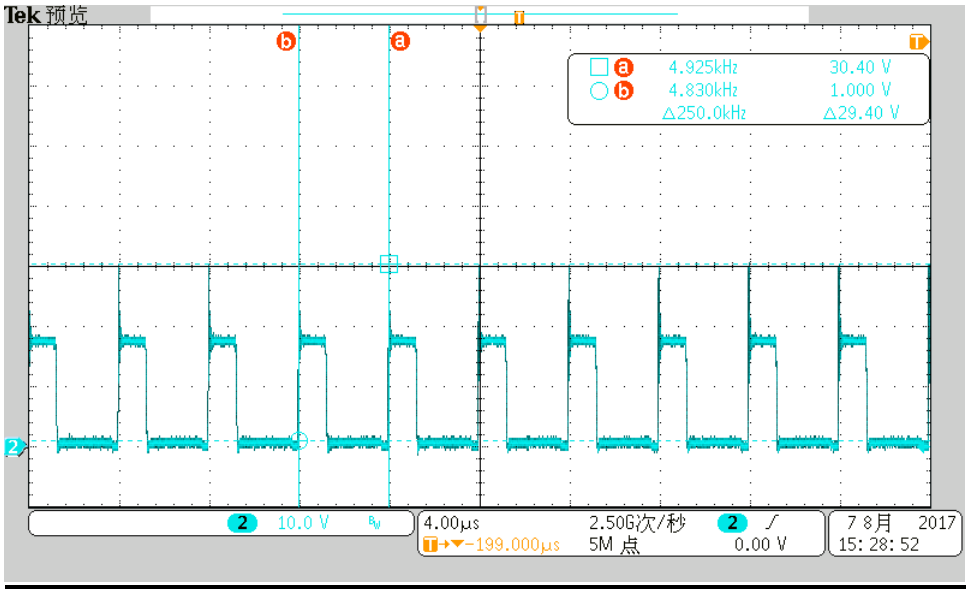


24Vin, CH1=Vin; CH2=Vprids



CH1=Vin; CH2=Vprids; CH4=Vout; 36Vin

2.4: Secondary Synchronous Rectifier MOSFET

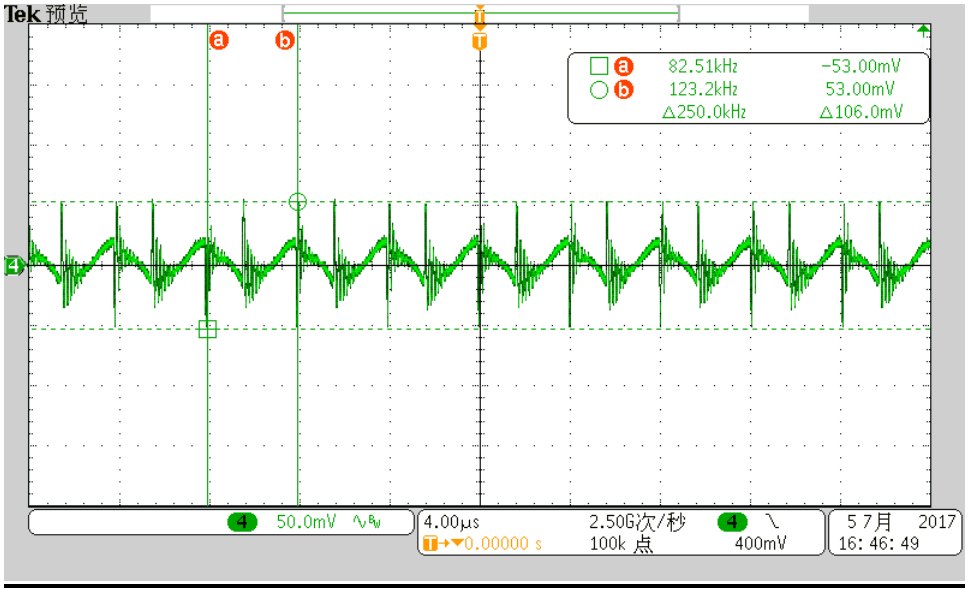


CH2=Vsrdrv; 36Vin

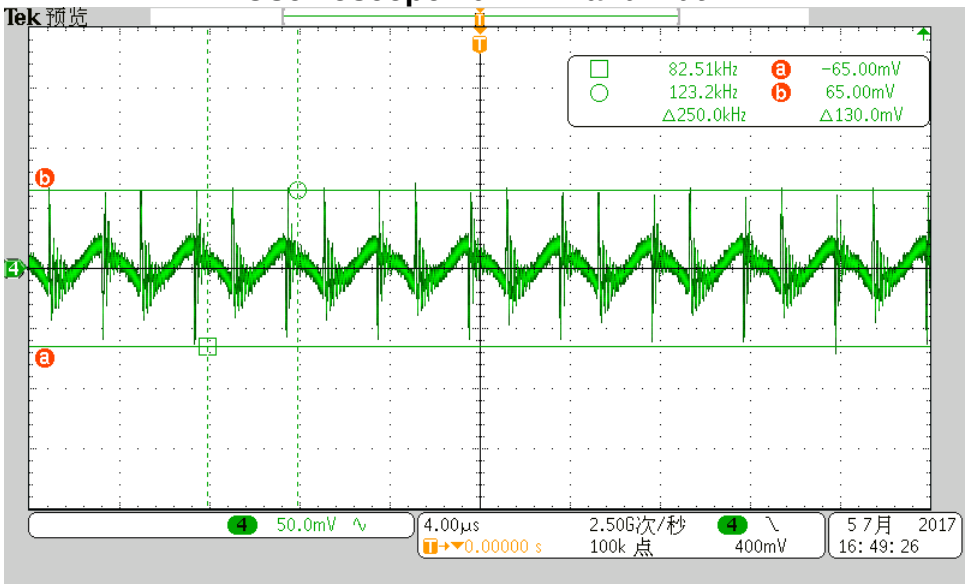
2.5: Output Voltage Ripple

Note: C8 is replaced by 4pcs 0805 X7R/25V ceramic capacitor for the following output voltage ripple

Test condition: 24Vin 5V/6A full load



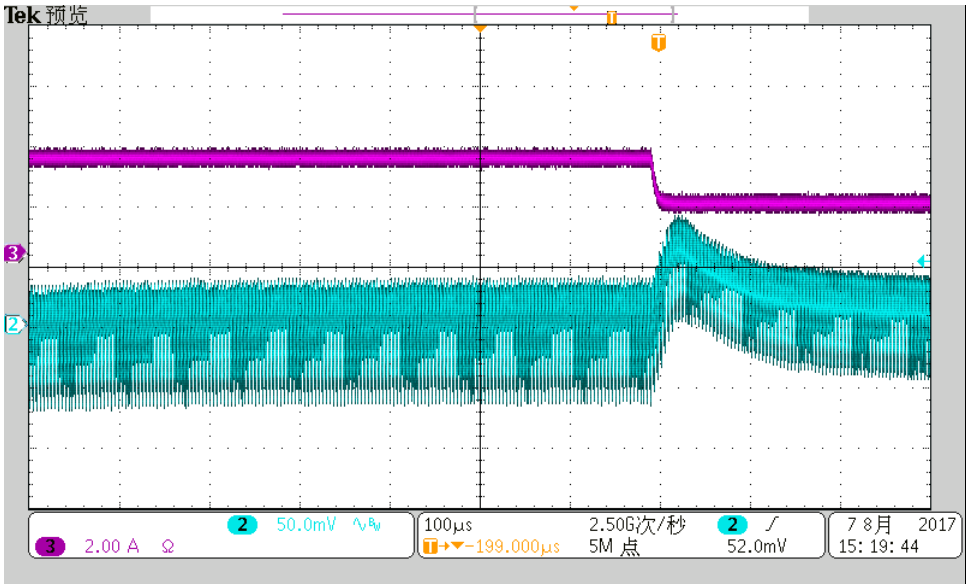
Oscilloscope 20MHz Bandwidth



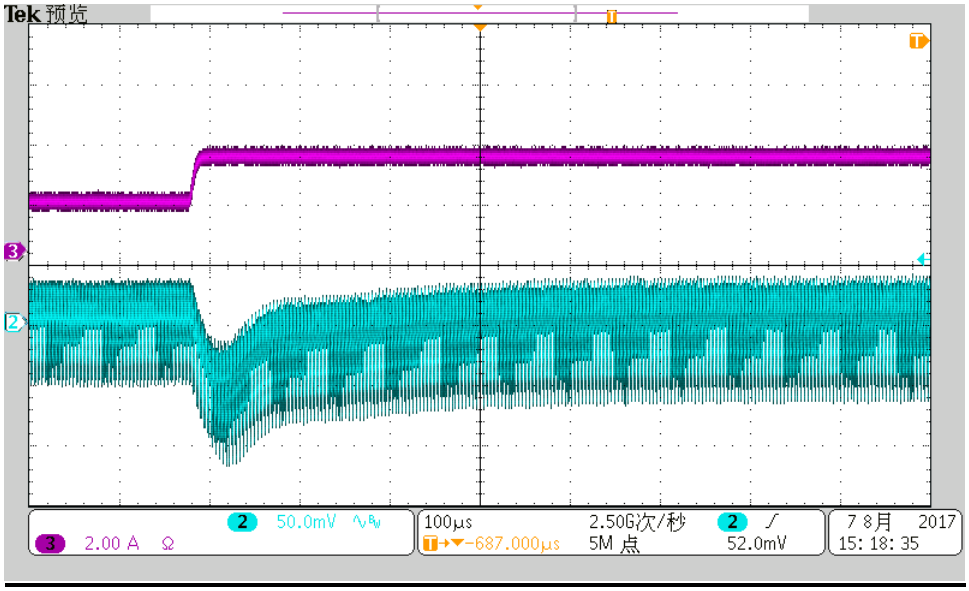
Oscilloscope Full Bandwidth

2.6: Dynamic Response

Test condition: 24Vin, Load step from 1.5A to 3A(25%-50%), 500Hz cycle, 1A/us

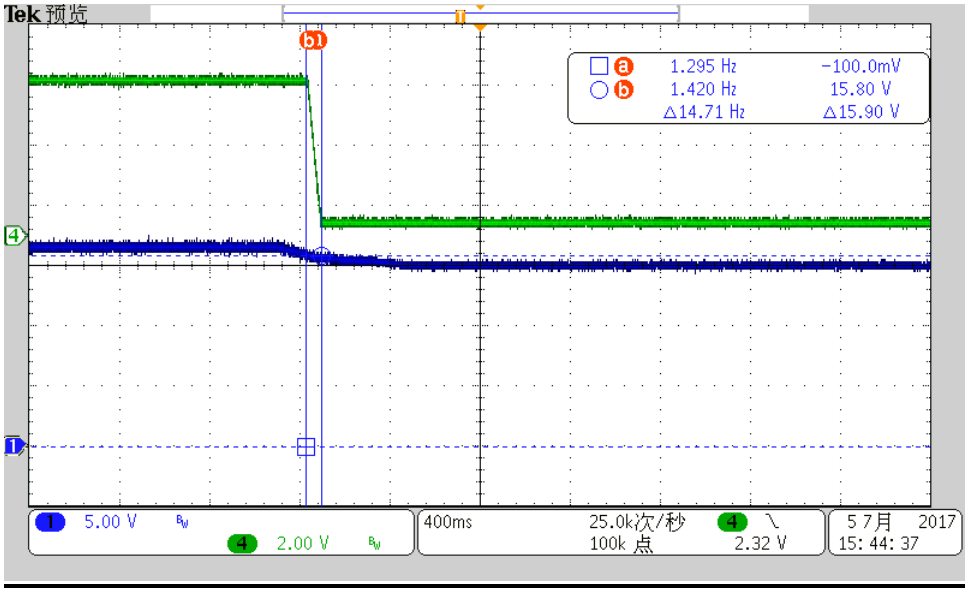


Overshoot



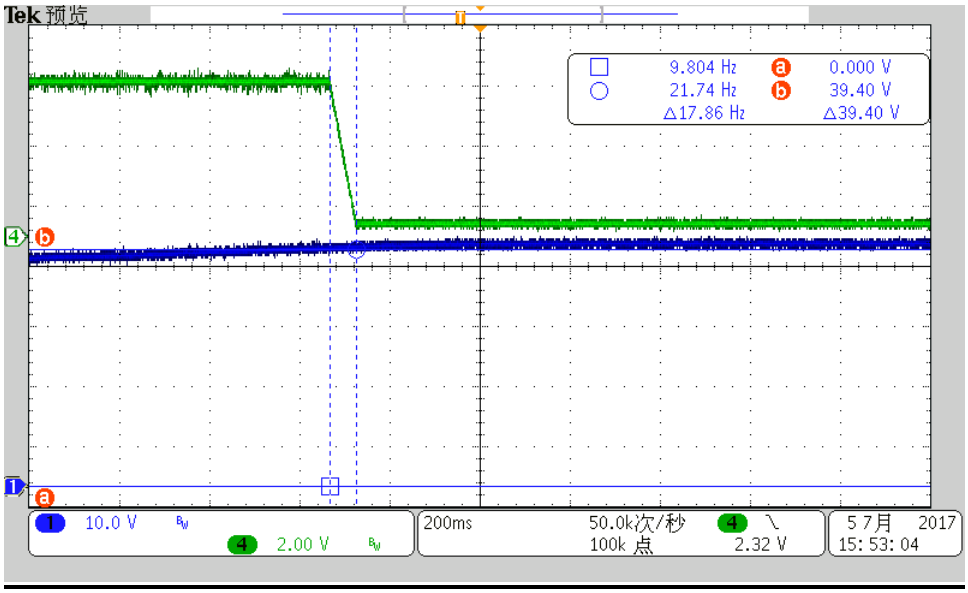
Undershoot

2.7 : Input Under Voltage Protection



CH1=Vin; CH4=Vout; UVLO 16V

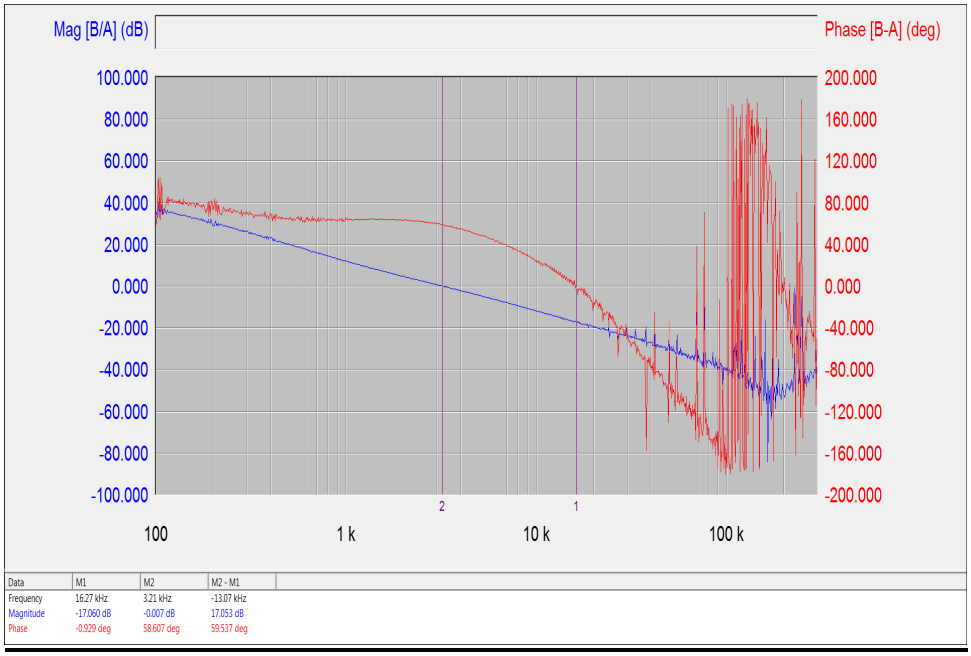
2.8：Input Over Voltage Protection



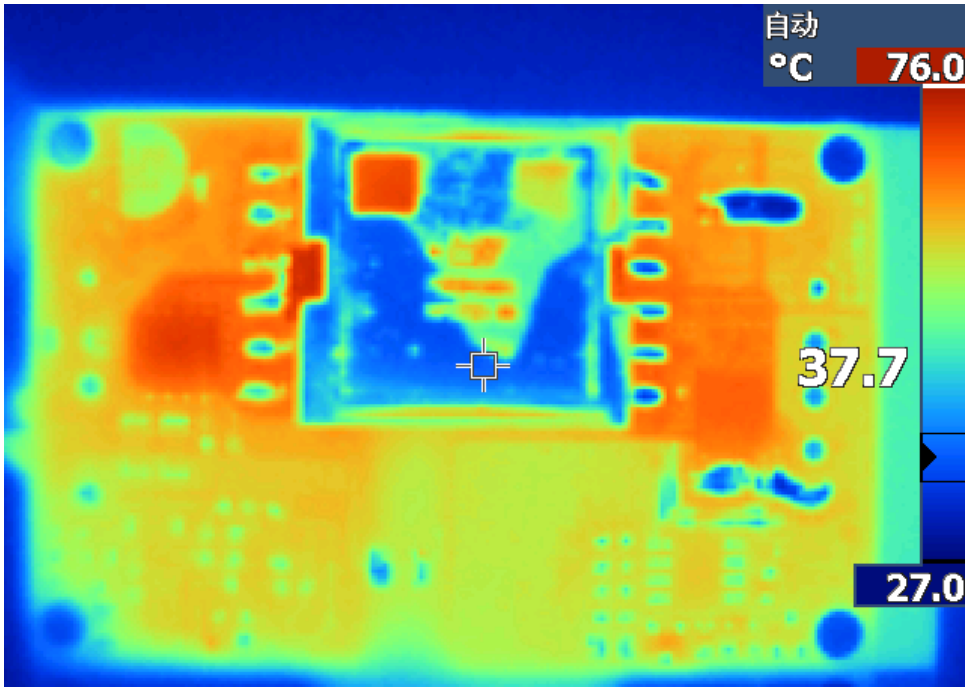
CH1=Vin; CH4=Vout; UVLO 40V

2.9：Frequency Response

Test condition: 24Vin 5V/6A full load



2.10: Thermal image



24V Input, output is 6A load (30 minutes) without fan cooling

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