TI Designs: TIDA-01417
Integrated 30-W Sensorless BLDC Motor Drive Retrofit Reference Design With 90- to 265-V AC Input

Description

The TIDA-01417 design provides a reference solution to drive the low-voltage brushless DC (BLDC) motor with a universal AC power supply input. This TI Design has an onboard, reinforced isolated AC-DC switch power supply to convert the AC main input to an isolated low-voltage DC output. The design also combines a fully integrated and well protected single-chip, sensorless, sinusoidal brushless motor controller to operate with low audible noise. The total solution is optimized with a high efficiency and a very small form factor to easily fit into the motor.

Resources

TIDA-01417	Design Folder
UCC28740	Product Folder
DRV10983	Product Folder
TL431B	Product Folder

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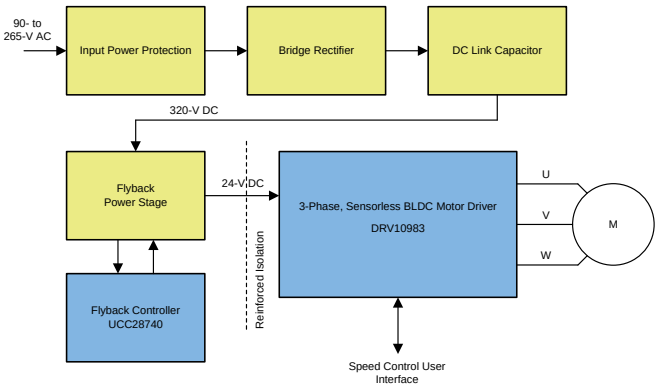
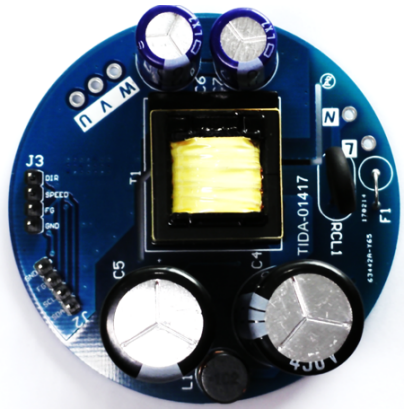
Features

- Universal Main Power Supply Input From 90- to 265-V AC
- Reinforced Isolated Flyback AC/DC Power Supply Providing 24-V, 36-W Output
- Very Low Standby Power Below 50 mW and High Efficiency AC/DC Power Supply Giving a Full Load Efficiency of 86%
- Highly Integrated and Protected Single-Chip, Sinusoidal Brushless Motor Controller Reduces External Parts Count Eliminating Programming Overhead of Motor Control
- Small PCB Form Factor of Ø64 mm
- Startup and Full-Speed Operation Even at 90-V AC Input
- Fully Protected System With Short Circuit, Overcurrent, Blocked Rotor Protection
- Flexible User Interface Options for Speed Control: I^2C, PWM, Analog

Applications

- Washing Machine Drain Pump
- Dishwasher Drain Pump
- Air Conditioner Circulation Fan
- Water Pump





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1 System Description

The use of brushless DC (BLDC) motors is getting more and more popular in home appliances and replacing the universal motor for its high efficiency and low audible noise as compared to universal AC motors. Based on the power level, the brushed DC motors can be drive by either high voltage or low voltage. Each option has its benefits. There are a wide range of low-power motors below 30 W used in the home appliances such as cooling fans, circulation fans, water circulation pumps, water drain pumps, and so on. This reference design focuses on such low-power BLDC motors.

For low-power applications, a power level below 30 W for example, using low-voltage motors offers several advantages:

- *Safety*: The most obvious benefit of low-voltage motors is that they make systems safer for maintenance service personnel and designers. Moving pumps and fans to a low-voltage keeps the major part of the system isolated from the high-voltage input. The insulation required in the motor will be less and reduces the risk of insulation breakdown in the motor and the driver board. Therefore, it safely prevents electrical shock and is especially suitable for applications in high humidity environments, such as drain pumps.
- *Flexibility*: The low-voltage motor drive can be used with either a 110- or 220-V line input using a universal input AC/DC converter. The low-voltage motor drive subsystem is easily adaptable into battery or solar-powered systems. This adaptability gives the benefit of using a single motor and controller platform for a wide number of systems.
- *Integration level*: The latest integrated circuits (ICs) for low-voltage motor controllers are highly integrated, with features like cycle-by-cycle overcurrent protection, over-temperature protection, stall detection, auto dead-time insertion, and slew-rate control. Some driver ICs are equipped with linear or switching voltage regulators, operation amplifiers for shunt current sensing, power stages, and embedded control algorithms. Highly integrated drivers like the TI DRV10983 three-phase sensorless BLDC motor controller integrate the MOSFET's gate driver and control algorithm into a single IC, and implement sinusoidal current control without any current shunt resistors.
- *Size and cost*: Low-voltage motor controller ICs are usually with much smaller packages compared to high-voltage IPMs, given the different technologies used and the low clearance and creepage distance requirements. While designing the printed circuit board (PCB), the high-voltage area on the board usually requires more clearance, creepage distance, and care for isolation than the low-voltage area, which could result in a larger board size. In low-voltage low-power applications, even with higher current, the optimized R_{DSON} and the gate charge of the MOSFET help achieve very low FET losses. With optimized thermal management, the power stage may not require extra heat-dissipation components, thus saving on overall system cost.
- *Shorter design cycle*: With high integration level, using an advanced low-voltage BLDC motor driver IC may significantly reduce the subsystem's design cycle. For example, using the DRV10983 for a fan control subsystem design does not require any software effort on the motor control algorithm. The device only needs to tune the motor parameters through the I^2C communication interface to the controller IC and start evaluating.

The TIDA-01417 proposes the use of low-voltage (24 V) BLDC motor drives instead of high-voltage (above 300 V) motors. The reference design provides an optimized compact AC/DC flyback power supply and highly integrated sinusoidal BLDC motor driver with full protection. The very small form factor of the design enables the designer to integrate the drive board inside the motor and provides a retrofit solution. The AC/DC flyback power supply converts the 90- to 265-V, 50- or 60-Hz AC input to a regulated 24-V DC output with reinforced isolation between the high side and low side. This TI Design uses the UCC28740 as the AC/DC flyback controller. The 24-V DC generated by the power supply is used to power the three-phase, sensorless BLDC motor controller DRV10983, which drives the motor and control the motor speed.

1.1 Key System Specifications

Table 1. Power Supply Electrical Performance Specifications

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
Input voltage	V_{IN}	—	90	230	265	V AC
Line frequency	f_{AC}	—	47	—	63	Hz
Maximum input current	I_{IN_max}	$V_{IN} = V_{INmin}$, $I_{OUT} = I_{OUTmax}$	—	0.85	—	A
Standby power	P_S	$V_{INmin} \le V_{IN} \le V_{INmax}$, $I_{OUT} = 0$ A	—	40	50	mW
Brownout voltage	V_{IN_UVLO}	0 A ≤ I_{OUT} ≤I_{OUTmax}	—	—	80	V AC
OUTPUT CHARACTERISTICS						
Output voltage	V_{OUT}	$V_{INmin} \le V_{IN} \le V_{INmax}$; 0 A ≤ $I_{OUT} \le I_{OUTmax}$	23	24	25	V
Output current	I_{OUT}	$V_{INmin} \le V_{IN} \le V_{INmax}$	0	—	1.5	A
Output power	P_{OUT}	$V_{INmin} \le V_{IN} \le V_{INmax}$	0	—	36	W
Line regulation		$V_{INmin} \le V_{IN} \le V_{INmax}$; 0 A ≤ $I_{OUT} \le I_{OUTmax}$	—	—	0.5	%
Load regulation		0 A ≤ $I_{OUT} \le I_{OUTmax}$	—	—	0.5	%
Output voltage ripple	V_{OUT_RIPPLE}	$V_{INmin} \le V_{IN} \le V_{INmax}$; 0 A ≤ I_{OUT} ≤I_{OUTmax}	—	—	100	mV
Output overcurrent	I_{OCP}	$V_{INmin} \le V_{IN} \le V_{INmax}$	—	—	1.8	A
SYSTEM CHARACTERISTICS						
Switching frequency	f_{SW}	—	—	—	90	kHz
Average efficiency	η	25%, 50%, 75%, 100% load average at nominal input voltages	—	85	—	%
Operating temperature	T_{OT}	Open frame	–40	25	70	°C

Table 2. Motor Driver Electrical Performance Specifications

PARAMETERS	SPECIFICATIONS
DC input voltage	24-V DC (28 V max)
Current	1.25 A continuous
Power level	Thermal design for 30-W continuous operation
Control method	Single chip, sensorless, completely integrated 180° sinusoidal control with power drive
Speed range	2700 RPM max
Protection circuits	Overcurrent, lock detection, voltage surge protection, UVLO protection, thermal shutdown protection
Operating ambient	–40°C to 70°C
Cooling	Thermally-enhanced 24-pin HTSSOP with PCB layout for thermal management

2 System Overview

2.1 Block Diagram

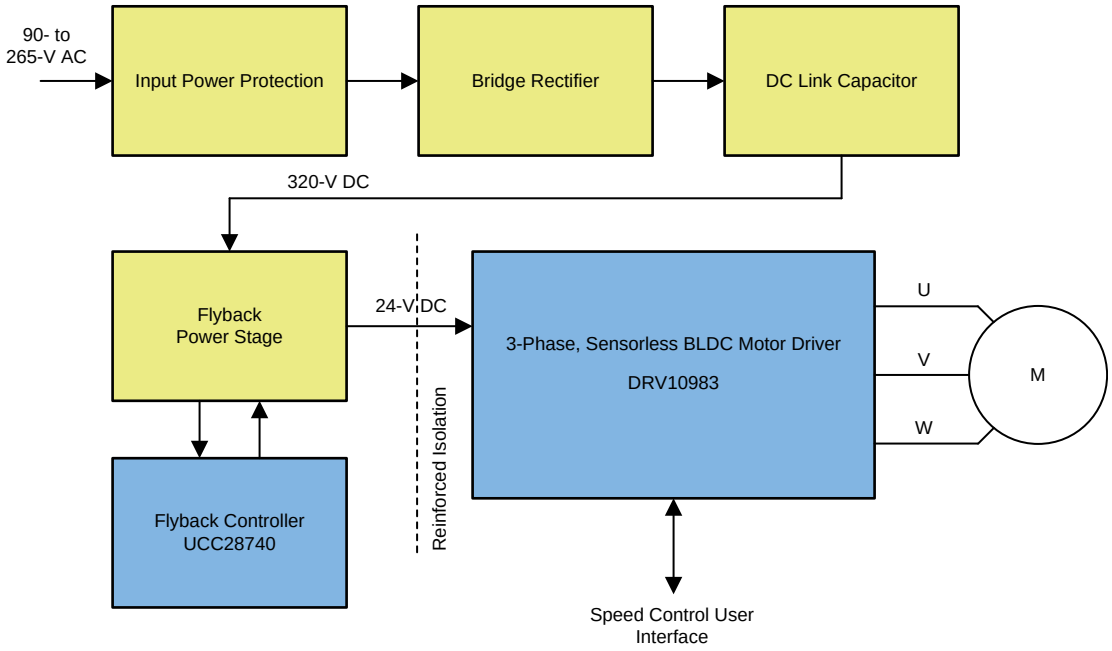

Figure 1. TIDA-01417 System Block Diagram

2.2 Highlighted Products

The following subsections detail the highlighted products used in this reference design, including the key features for their selection. See their respective product datasheets for complete details on any highlighted device.

2.2.1 UCC28740

The UCC28740 is a flyback power-supply controller that provides high-performance voltage regulation using an optically coupled feedback signal from a secondary-side voltage regulator. The device provides accurate constant-current regulation using primary-side feedback. The controller operates in discontinuous conduction mode (DCM) with valley switching to minimize switching losses. The control law scheme combines frequency with primary peak-current amplitude modulation to provide high-conversion efficiency across the load range. The control law provides a wide dynamic operating range of output power, which allows the power supply designer to easily achieve less than a 30-mW standby power dissipation using a standard shunt regulator and optocoupler. A standby power of less than 10 mW requires a careful loss-management design with a low-power regulator and high-CTR optocoupler.

During low-power operating conditions, the power management features of the controller reduce the device operating current at switching frequencies below 32 kHz. At and above this frequency, the UCC28740 includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. A complete low-cost and low component count charger solution is realized using a straight-forward design process.

Key features that make this device unique are:

- Optocoupled feedback regulation for constant voltage (CV) and PSR for constant current (CC)
- Enables ±1% voltage regulation and ±5% current regulation across line and load
- 100-kHz max switching frequency enables high-power density charger designs
- QR valley switching operation for highest overall efficiency
- Frequency jitter scheme to ease EMI compliance
- Wide VDD range (35 V) allows small bias capacitor
- Drive output for MOSFET
- Enables <10-mW system standby and no load power
- Protection functions: Overvoltage, low line, and overcurrent
- SOIC-7 package

2.2.2 DRV10983

The DRV10983 is a three-phase sensorless motor driver with integrated power MOSFETs, which provide drive current capability up to 2 A continuous. It uses a proprietary 180° sensorless control scheme to provide continuous sinusoidal drive, which significantly reduces the pure-tone acoustics that typically occur as a result of commutation by keeping the electrically induced torque ripple small. Therefore, it is specifically designed for low-noise, low external component count, 12- to 24-V motor drive applications.

The device is configurable through a simple I^2C interface to reprogram specific motor parameters in registers and program the EEPROM to accommodate different motor parameters and spin-up profiles for different customer applications. The user can control the motor directly through the PWM input, analog input, or I^2C inputs. The motor speed feedback is available through either the FG pin or I^2C interface.

The DRV10983 features extensive protection and fault detect mechanisms to ensure reliable operation. Voltage surge protection prevents the input VCC capacitor from overcharging, which is typical during motor deceleration. The device provides overcurrent protection without the need for an external current sense resistor. Rotor lock detect is available through several methods. These methods can be configured with register settings to ensure reliable operation. The device provides additional protection for undervoltage lockout (UVLO) and for thermal shutdown.

The DRV10983 driver features an integrated buck and linear regulator to efficiently step down the supply voltage to either 5 V or 3.3 V for powering both internal and external circuits. The device is available in either a sleep mode or a standby mode version to conserve power when the motor is inactive. The standby mode (3-mA) version leaves the regulator running and the sleep mode (180-μA) version shuts it off. Use the standby mode version in applications where the regulator is used to power an external MCU.

2.2.3 TL431

The TL431 is a three-terminal adjustable shunt regulator with specified ranges for thermal stability over temperature. The output voltage can be set to any value between VREF (approximately 2.5 V) and 36 V, with two external resistors. Active output circuitry provides a very sharp turnon characteristic, making these devices excellent replacements for Zener diodes in many applications. The "B-grade" version comes with initial tolerances (at 25°C) of 0.5% and TL431BQ devices are characterized for operation from –40°C to 125°C.

3 System Design Theory

The block diagram in Figure 1 shows that the complete system is composed by two main sections: the first one is flyback AC/DC converter and second one is the BLDC motor driver.

The first one provides 36 W of continuous power over a wide AC input range from 90- to 265-V AC in a small form factor. This TI Design has a flyback power stage implemented using the UCC28740 QR PSR CC-CV flyback controller to deliver 24 V and 1.5 A. The total system efficiency is over 88% with a 230-V AC input and over 86% with a 115-V AC input under full load conditions. The design has precise current limit and limits the power to ≤ 36 W under all fault conditions. In addition, several protections are embedded into this TI Design, which includes input undervoltage protection and output short-circuit protection.

The second one provides a single-chip solution for BLDC motor driver with very few external components based on a 180° sensorless control scheme.

3.1 QR Flyback Converter With PSR

Flyback converters provide a cost-effective solution for AC/DC conversion needs. They are widely used for AC/DC converters up to 150 W. There are three modes of operation namely discontinuous mode (DCM), QR mode (QRM), and continuous conduction mode (CCM). For lower power applications, the DCM or QRM is preferred as they have reduced power losses and optimal peak currents in low-power applications. As the output wattage increases, CCM becomes more efficient due to the reduced peak and RMS currents.

Flyback converters designed with PSR flyback controllers eliminate the use of conventional optocoupler-based feedback. The PSR flyback controllers sense the voltage feedback through auxiliary winding and current feedback through the current sense resistor used in series with switching FET. In addition, TI PSR flyback controllers provide a wide range of protections and accurate limiting of both current and power. The UCC28740 controller has both PSR feedback and opto-feedback, enhancing the reliability of the system.

3.2 Flyback Circuit Component Design

The UCC28740 is a flyback controller that provides both CV mode and CC mode control for precise output regulation. While in CV operating range, the controller uses an optocoupler for tight voltage regulation and improved transient response to large load steps. Accurate regulation while in CC mode is provided by primary side control. The UCC28740 uses frequency modulation, peak primary current modulation, valley switching, and valley hopping in its control algorithm to maximize efficiency over the entire operating range.

The design process and component selection for this TI Design are illustrated in the following subsections. All design calculations are available in the TIDA-01417_Design_Calculator.

3.2.1 Design Goal Parameters

Table 3 elucidates the design goal parameters for this TI Design. These parameters are used in further calculations to select components.

Table 3. Design Goal Parameters

PARAMETER		MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS					
Input voltage	V_{IN}	90	230	265	V AC
Line frequency	f_{AC}	47	—	63	Hz
OUTPUT CHARACTERISTICS					
Output voltage	V_{OUT}	23	24	25	V
Output current	I_{OUT}	0	—	1.5	A
Output power	P_{OUT}	0	—	36	W
Switching frequency	f_{SW}	—	—	90	kHz
Average efficiency	η	—	85	—	%

3.2.2 Input Bulk Capacitance and Minimum Bulk Voltage

The value of the bulk capacitor used determines the minimum input voltage for the flyback converter. This in turn determines the primary-to-secondary turns ratio of the transformer.

Input capacitance value, C_{BULK}, is based on the maximum load power, converter efficiency, minimum operational input voltage, and minimal operational input frequency. Maximum AC input power is determined by the V_{OCV}, I_{OCC}, and full-load efficiency targets.

Primary output: $V_{OUT} = V_{OCV} = 24$ V

The converter is designed for 1.5 A of maximum output current on primary output and is designed to limit the current at 1.5 A for overload conditions. So, $I_{OCC} = 1.5$ A.

Total maximum output power needed is:

$$P_{OUT} = V_{OUT} \times I_{OCC} = 24\ V \times 1.5\ A = 36\ W \quad (1)$$

To calculate component specifications, the minimum targeted efficiency is considered as η =80 %.

$$P_{IN} = \left(\frac{P_{OUT}}{\eta}\right) = \frac{36\ W}{0.8} = 45\ W \quad (2)$$

Equation 3 provides an accurate solution for input capacitance needed to achieve a minimum bulk valley voltage target ($V_{BULK(min)}$). Alternatively, if a given input capacitance value is prescribed, one can calculate the $V_{BULK(min)}$ expected for that capacitance.

$$C_{BULK} = \frac{2 \times P_{IN} \times \left(0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right)}{\left(2\ V_{IN(min)}^2 - V_{BULK(min)}^2\right) \times f_{LINE}} \quad (3)$$

The minimum recommended valley voltage on the input bulk capacitors is taken as 60% of the peak of the minimum AC voltage.

$$V_{BULK(min)} = V_{IN(min)} \times \sqrt{2} \times 0.6 = 90\ V \times \sqrt{2} \times 0.6 = 76.36\ V \quad (4)$$

$$C_{BULK} \geq \frac{2 \times 45\ W \times \left(0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{76.36\ V}{\sqrt{2} \times 90\ V}\right)\right)}{\left(2 \times 90\ V^2 - 76.36\ V^2\right) \times 50\ Hz} = 61.2\ \mu F$$

To meet the needs of hold-up time, bulk capacitance is selected higher than this calculated value. The bulk capacitor selected is 47 µF × 2 = 94 µF.

Using Equation 3 and C_{BULK}= 94 µF, the actual $V_{BULK(min)}$ = 94.5 V.

The maximum AC voltage is 265 V. Then the maximum DC bus voltage is $265 \times \sqrt{2} = 375$ V. Therefore, a 450-V capacitor with proper margin is a good choice.

3.2.3 Bridge Rectifier Selection

The input fuse and bridge rectifier are selected based upon the input current and rated voltage calculations.

For this TI Design, the voltage is designed to vary from 127- to 375-V DC for an input AC voltage range of 90- to 265-V AC operation. When the input AC voltage is 90-V AC, the input current averaged over the AC line period reaches the maximum value. With this conclusion, the maximum input RMS line current, , is calculated as follows:

$$I_{IN\_RMS(max)} = \frac{P_{IN}}{V_{IN(min)} \times PF} = \frac{45\ W}{90\ V \times 0.5} = 1\ A \quad (5)$$

NOTE: The target power factor is assumed as PF = 0.5

Then the maximum input current, , and the maximum average input current, , can be calculated with the following equations (assuming the waveform is sinusoidal):

$$I_{IN(max)} = \sqrt{2} \times I_{IN\_RMS(max)} = \sqrt{2} \times 1\ A = 1.414\ A \quad (6)$$

$$I_{IN\_AVG(max)} = \frac{2}{\pi} \times I_{IN(max)} = \frac{2}{\pi} \times 1.414\ A = 0.9\ A \quad (7)$$

The input bridge rectifier must have an average current capability that exceeds the input average current ($I_{IN\_AVG(max}$). To optimize the power loss due to the diode forward voltage drop, a bridge rectifier with a higher current rating is recommended. DF1506S-T from Diodes is selected with an average forward rectified current of 1.5 A and a peak repetitive reverse voltage of 600 V.

Forward voltage drop of bridge rectifier diode, V_{FD} = 1.1 V

The estimated power dissipated in bridge rectifier diode (P_{DA}) is:

$$P_{BRI} = 2 \times I_{IN\_AVG(max)} \times V_{FD} = 2 \times 0.9\ A \times 1.1\ V = 1.98\ W \quad (8)$$

3.2.4 Transformer Parameter Calculations: Turns Ratio, Primary Inductance, and Peak Primary Current

The target maximum switching frequency at full-load, the minimum input-capacitor bulk voltage, and the estimated DCM QR time determine the maximum primary-to-secondary turns-ratio of the transformer.

First determine the maximum-available total duty-cycle of the on-time and secondary conduction time based on the target switching frequency, f_{MAX}, and DCM resonant time. For DCM resonant frequency, assume 500 kHz if an estimate from previous designs is not available. At the transition mode operation limit of DCM, the interval required from the end of secondary current conduction to the first valley of the V_{DS} voltage is half of the DCM resonant period (t_R), or 1 µs assuming a 500-kHz resonant frequency. The maximum allowable MOSFET on-time D_{MAX} is determined using Equation 9.

$$D_{MAX} = 1 - D_{MAGCC} - f_{MAX} \times \frac{t_R}{2} \quad (9)$$

Where:

- t_R is the estimated period of the LC resonant frequency at the switch node
- D_{MAGCC} is defined as the secondary-diode conduction duty-cycle during CC operation and is fixed internally by the UCC28740 at 0.425
- t_R = 2 µs

$$D_{MAX} = 1 - 0.425 - 90\ kHz \times \frac{2\ \mu s}{2} = 0.485$$

When D_{MAX} is known, the maximum primary-to-secondary turns-ratio is determined with . Calculate the total voltage on the secondary winding by adding V_{OCV}, V_F, and V_{OCBC}.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F + V_{OCBC})} \quad (10)$$

V_{OCBC} is the additional voltage drop of post filter inductor and any other target cable compensation voltage added to V_{OCV} (provided by an external adjustment circuit applied to the shunt regulator). Set V_{OCBC} equal to 0 V if not used.

$$N_{PS(max)} = \frac{0.485 \times 94.5\ V}{0.425 \times (24\ V + 0.86\ V + 0\ V)} = 4.34$$

A higher turns-ratio generally improves efficiency, but may limit operation at low input voltage. The transformer turns ratio selected affects the MOSFET V_{DS} and secondary rectifier reverse voltage, so these should be reviewed. The UCC28740 requires a minimum on time of the MOSFET ($t_{ON(min)}$) and minimum secondary rectifier conduction time ($t_{DM(min)}$) in the high line and minimum load condition. The selection of f_{MAX}, L_P, and R_{CS} affects the minimum $t_{ON(min)}$ and $t_{DM(min)}$.

The secondary rectifier and MOSFET voltage stress can be determined by Equation 11 and Equation 12, respectively.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} + V_{OCBC} \quad (11)$$

For the MOSFET V_{DS} voltage stress, include an estimated leakage inductance voltage spike (V_{LK}).

$$V_{DSPK} = V_{IN(max)} \times \sqrt{2} + (V_{OCV} + V_{OCBC} + V_F) \times N_{PS} + V_{LK} \quad (12)$$

Equation 13 determines if $t_{ON(min)}$ exceeds the minimum target of 280 ns (maximum t_{CSLEB}). Equation 14 verifies that $t_{DM(min)}$ exceeds the minimum target of 1.2 µs.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)}}{K_{AM}} \quad (13)$$

Where:

- K_{AM} denotes the AM control ratio

$$t_{DM(min)} = \frac{t_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times (V_{OCV} + V_F)} \quad (14)$$

To determine the optimum turns ratio N_{PS}, design iterations are generally necessary to optimize and evaluate system-level performance trade-offs and parameters mentioned in Equation 11 through Equation 14. The design spreadsheet provides an easy way to iterate and arrive at the optimum value for N_{PS} .

When the optimum turns ratio N_{PS} is determined from a detailed transformer design, use this ratio for the following parameters. For this TI Design, N_{PS} = 4.2 is selected on optimization.

The UCC28740 CC regulation is achieved by maintaining D_{MAGCC} at the maximum primary peak current setting. The product of D_{MAGCC} and $V_{CST(max)}$ defines a CC-regulating voltage factor V_{CCR}, which is used with N_{PS} to determine the current sense resistor value necessary to achieve the regulated CC target, I_{OCC} (see Equation 15).

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (15)$$

Because a small portion of the energy stored in the transformer does not transfer to the output, a transformer efficiency term is included in Equation 15. This efficiency number includes the core and winding losses, the leakage-inductance ratio, and a bias-power to maximum-output-power ratio. For example, an overall transformer efficiency of 0.9 is a good estimate based on 3.5% leakage inductance, 5% core and winding loss, and 0.5% bias power. Adjust these estimates as needed based on each specific application.

$$R_{CS} = \frac{0.318 \times 4.2}{2 \times 1.5} \times \sqrt{0.9} = 0.4224\ \Omega$$

$V_{CCR(min)}$ is the minimum CC regulation factor and device parameter = 0.318 V.

The standard value of the current sense resistor selected is R_{CS} = 0.43 Ω; a parallel resistor to R_{CS} is added in the schematic to easily adjust values.

For primary inductance calculation, determine the transformer primary peak current using Equation 16. Peak primary current is the maximum current-sense threshold divided by the current sense resistance

$$I_{pp(max)} = \frac{V_{CST(max)}}{R_{CS}} \tag{16}$$

$$I_{pp(max)} = \frac{0.81}{0.43} = 1.88 \text{ A}$$

$$I_{pp(norn)} = \frac{0.773}{0.43} = 1.8 \text{ A}$$

The primary transformer inductance is calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency, output voltage and current targets, and transformer power losses are included in Equation 16. First, determine the transformer primary peak current using Equation 17. Peak primary current is the maximum current-sense threshold divided by the current-sense resistance.

$$L_P = \frac{2 \times (V_{OCV} + V_F + V_{OCBC}) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \tag{17}$$

$$L_P = \frac{2 \times (24 \text{ V} + 0.86 \text{ V}) \times 1.5 \text{ A}}{0.9 \times 1.88 \text{ A}^2 \times 90 \text{ kHz}} = 260 \ \mu\text{H}$$

The actual primary inductance selected is L_P = 280 µH.

N_{AS} is determined by the lowest target operating output voltage while in CC regulation and by the VDD UVLO turnoff threshold of the UCC28740. Additional energy is supplied to VDD from the transformer leakage inductance, which allows a lower turns-ratio to be used in many designs.

$$N_{AS} = \frac{V_{VDD(off)} + V_{FA}}{V_{OCC} + V_F} = \frac{8.15 \text{ V} + 0.9 \text{ V}}{12 \text{ V} + 0.86 \text{ V}} = 0.7 \tag{18}$$

3.2.5 Transformer Parameter Calculations: Primary and Secondary RMS Currents

With a primary inductance of 280 µH, the absolute maximum switching frequency is calculated from Equation 19:

$$f_{MAX} = \frac{2 \times (24 \text{ V} + 0.86 \text{ V}) \times 1.5 \text{ A}}{0.9 \times 1.8 \text{ A}^2 \times 280 \ \mu\text{H}} = 91 \text{ kHz} \tag{19}$$

The maximum switching period is:

$$t_{SW} = \frac{1}{f_{MAX}} = \frac{1}{91 \text{ kHz}} = 11 \ \mu\text{s} \tag{20}$$

The actual maximum ON-time is given by:

$$t_{ON(max)} = \frac{I_{PP(nom)} \times L_p}{V_{BULK(min)}} \tag{21}$$

$$t_{ON(max)} = \frac{1.8 \text{ A} \times 280 \ \mu\text{H}}{94.5 \text{ V}} = 5.33 \ \mu\text{s}$$

The maximum duty cycle of operation D_{MAX} is:

$$D_{MAX} = \frac{t_{ON(max)}}{t_{SW}} = \frac{5.33 \ \mu\text{s}}{11 \ \mu\text{s}} = 0.485 \tag{22}$$

The transformer primary RMS current (I_{PRI_RMS}) is:

$$I_{PRI\_RMS} = I_{PP(nom)} \times \sqrt{\frac{D_{MAX}}{3}}$$
$$I_{PRI\_RMS} = 1.8 \times \sqrt{\frac{0.485}{3}} = 0.72 \text{ A} \quad (23)$$

The transformer secondary peak current RMS current ($I_{SEC(max)}$) is:

$$I_{SEC(max)} = I_{pp(nom)} \times N_{PS} = 1.8 \text{ A} \times 4.2 = 7.56 \text{ A} \quad (24)$$

The transformer secondary RMS current (I_{SRMS}) is:

$$I_{SEC\_RMS} = I_{SEC(max)} \times \sqrt{\frac{D_{MAX}}{3}}$$
$$I_{SEC\_RMS} = 7.56 \times \sqrt{\frac{0.485}{3}} = 3.04 \text{ A} \quad (25)$$

Based on these calculations, a Wurth Electronik transformer was designed for this application (part number 750343466), which has the following specifications:

- N_{PS} = 4.2
- N_{PA} = 6
- L_P = 280 µH
- L_{LK} = 5 µH
- L_{LK} denotes the primary leakage inductance

3.2.6 Main Switching Power MOSFET Selection

The drain-to-source RMS current, I_{DS_RMS}, through switching FET is calculated as:

$$I_{DS\_RMS} = \frac{I_{PP(max)}}{\sqrt{3}} \times \sqrt{D_{MAX}} = \frac{1.88 \text{ A}}{\sqrt{3}} \times \sqrt{0.485} = 0.756 \text{ A} \quad (26)$$

It is recommended to select a MOSFET with five times the I_{DS_RMS}calculated. The maximum voltage across the FET can be estimated using Equation 12. Considering a de-rating of 25%, the voltage rating of the MOSFET should be 650-V DC. The TK7P65W,RQ MOSFET of 650 V and 6.8 A at 25°C is selected for this TI Design.

The recommended clamping voltage on drain is:

$$V_{DRAIN\_Clamp} = 0.95 \times V_{DS} - \left(\sqrt{2} \times V_{IN(max)} + N_{PS} \times \left(V_{OCV} + V_F + V_{OCBC}\right)\right)$$
$$V_{DRAIN\_Clamp} = 0.95 \times 650 \text{ V} - \left(\sqrt{2} \times 265 \text{ V} + 4.2 \times \left(24 \text{ V} + 0.86 \text{ V}\right)\right) = 138 \text{ V} \quad (27)$$

3.2.7 Rectifying Diode Selection

Calculate the secondary output diode reverse voltage or blocking voltage needed ($V_{DIODE\_BLOCKING}$) with Equation 28:

$$V_{DIODE\_BLOCKING} = \frac{\sqrt{2} \times V_{IN(max)} + V_{DRAIN\_Clamp}}{N_{PS}} + V_{OUT\_OVP} + V_{OCBC}$$
$$V_{DIODE\_BLOCKING} = \frac{\sqrt{2} \times 265 \text{ V} + 138 \text{ V}}{4.2} + 28 \text{ V} + 0 \text{ V} = 150 \text{ V} \quad (28)$$

The required minimum rectified output current is I_{DOUT} = I_{SEC_RMS} = 3.1 A.

The MBRS4201T3 200 V 4 A from ON Semiconductor is selected.

3.2.8 Select Output Capacitors

For this TI Design, the output capacitor (C_{OUT}) was selected to prevent V_{OUT} (24 V) from dropping below the minimum output voltage (V_{OTRM}) during transients up to 0.30 ms.

$$V_{OTRM} = 23.7\ V \tag{29}$$

$$C_{OUT} \geq \frac{\frac{I_{OUT}}{2} \times (t)}{V_{OUT} - V_{OTRM}} \tag{30}$$

$$C_{OUT} \geq \frac{\frac{1.5\ A}{2} \times (0.3\ ms)}{24\ V - 23.7\ V} = 750\ \mu F$$

Considering the allowable output ripple voltage of 120 mV (5%), the ESR of the capacitor should be:

$$ESR = \frac{V_{OUT\_RIPPLE}}{I_{SEC(max)}} = \frac{120\ mV}{7.56\ A} = 15.9\ m\Omega \tag{31}$$

$$I_{COUT\_RMS} = \sqrt{\left(I^2_{SEC\_RMS} - I^2_{OUT}\right)} = \sqrt{3.04^2 - 1.5^2} = 2.64\ A \tag{32}$$

A 470-µF×2, 35-V capacitor was selected on the output.

3.2.9 Capacitance on VDD Pin

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in CC regulation.

The capacitance on VDD must supply the primary-side operating current used during startup and between low-frequency switching pulses. The largest result of two independent calculations denoted in Equation 33 and determines the value of C_{VDD}.

At startup, when $V_{VDD(on)}$ is reached, C_{VDD} alone supplies the device operating current and MOSFET gate current until the output of the converter reaches the target minimum operating voltage in CC regulation, V_{OCC}. Now the auxiliary winding sustains VDD for the UCC28740 above UVLO. The total output current available to the load and to charge the output capacitors is the CC regulation target, I_{OCC}. Equation 33 assumes that all of the output current of the converter is available to charge the output capacitance until V_{OCC} is achieved. For typical applications, Equation 33 includes an estimated $q_G f_{SW(max)}$ of average gate-drive current and a 1-V margin added to V_{VDD}.

$$C_{VDD} \geq \frac{\left(I_{RUN} + q_G f_{SW(max)}\right) \times \frac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{V_{VDD(on)} - \left(V_{VDD(off)} + 1\ V\right)} \tag{33}$$

$$C_{VDD} \geq \frac{\left(2.65\ mA + 26\ nC \times 98\ kHz\right) \times \frac{940\ \mu F \times 12\ V}{1.5\ A}}{23 - \left(8.15 + 1\ V\right)} = 2.8\ \mu F$$

Where:

- I_{RUN} is the supply current of UCC28740 in run state (see Electrical Characteristics of the UCC28740 datasheet)

During a worst-case unload transient event from full load to no load, C_{OUT} overcharges above the normal regulation level for duration of t_{OV} until the output shunt regulator loading is able to drain V_{OUT} back to regulation. During t_{OV}, the voltage feedback loop and optocoupler are saturated, driving maximum I_{FB} and temporarily switching at $f_{SW(min)}$. The auxiliary bias current expended during this situation exceeds that normally required during the steady-state no-load condition. Equation 34 calculates the value of C_{VDD} (with a safety factor of 2) required to ride through the t_{OV} duration until steady-state no-load operation is achieved.

$$C_{VDD} \geq \frac{2 \times I_{AUXNL(max)} \times t_{OV}}{V_{VDDFL} - \left(V_{VDD(off)} + 1\right)}$$

$$C_{VDD} \geq \frac{2 \times 1.2\ \text{mA} \times 20\ \text{ms}}{18.2\ \text{V} - \left(8.15\ \text{V} + 1\ \text{V}\right)} = 5.33\ \mu\text{F} \quad (34)$$

To address the start-up of the converter for heavy capacitive loads (which is around 8000 to 10,000 μF), a higher value of C_{VDD} is needed. This TI Design uses a 10-μF capacitor.

3.2.10 Open-Loop Voltage Regulation VS Pin Resistor Divider, Line Compensation Resistor

The resistor divider at the VS pin determines the output voltage regulation point of the flyback converter. The high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on the transformer auxiliary-to-primary turns ratio and desired input voltage operating threshold as per Equation 35:

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (35)$$

Where:

- N_{PA} is the transformer primary to auxiliary turns ratio
- $V_{IN(min)}$ is the voltage to enable turn-on of the controller (run); for the DC input, leave out the $\sqrt{2}$term in the equation
- $I_{VSL(run)}$ is the run threshold for the current pulled out of the VS pin during the switch on-time (see Electrical Characteristics of the UCC28740 datasheet)

$$R_{S1} = \frac{90\ \text{V} \times \sqrt{2}}{6 \times 275\ \mu\text{A}} = 77\ \text{k}\Omega$$

A standard resistor of 75 kΩ is selected for this TI Design.

The low-side VS pin resistor is selected based on the desired V_{OUT} regulation voltage in open-loop conditions and sets the maximum allowable voltage during open-loop conditions. Use Equation 36 to determine its value:

$$R_{S2} = \frac{R_{S1} \times V_{OVPTH}}{N_{AS} \times \left(\left(V_{OV} + V_F\right) - V_{OVPTH}\right)} \quad (36)$$

Where:

- V_{OV} is the maximum allowable peak voltage at the converter output
- V_F is the output-rectifier forward drop at near-zero current
- N_{AS} is the transformer auxiliary-to-secondary turns ratio
- R_{S1} is the VS divider high-side resistance
- V_{OVPTH} is the overvoltage detection threshold at the VS input (see Electrical Characteristics of the UCC28740 datasheet)

$$R_{S2} = \frac{75\ \text{k}\Omega \times 4.6\ \text{V}}{0.7 \times \left(28\ \text{V} - 0.86\ \text{V}\right) - 4.6\ \text{V}} = 24\ \text{k}\Omega$$

A standard resistor of 24 kΩ is selected.

The UCC28740 maintains a tight CC regulation over varying input lines by using the line-compensation feature. The line-compensation resistor (R_{LC}) value is determined by current flowing in R_{S1} and the total internal gate drive and external MOSFET turnoff delay. Assuming an internal delay of 50 ns in the UCC28740, the value of R_{LC} is calculated with Equation 37:

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \quad (37)$$

Where:

- R_{CS} is the value of the current sense resistor
- t_D is the current sense delay including MOSFET turnoff delay; add ≈ 50 ns to MOSFET delay
- N_{PA} is the transformer primary-to-auxiliary turns ratio
- L_P is the transformer primary inductance
- K_{LC} is a current-scaling constant (see Electrical Characteristics of UCC28740 datasheet)

$$R_{LC} = \frac{28.6 \times 75\ k\Omega \times 0.43\ \Omega \times (75\ ns + 50\ ns) \times 6}{280\ \mu H} = 2.47\ k\Omega$$

A standard 2.7-kΩ resistor is selected for this TI Design.

3.2.11 Feedback Elements

The output voltage is set through the sense network resistors R_{FB1} and R_{FB2}. The design spreadsheet "TIDA-01417_Design_Calculator.xlsx" has all relevant equations for characterization of the optocoupler and its adjustments of the initial values to accommodate variations of the UCC28740 (see Section 6.7). Also using the design sheet, the shunt regulator parameters can be optimized for overall system performance.

The compensation network of the shunt regulator, Z_{FB}, is determined using well-established design techniques for control-loop stability. Typically, a type-II compensation network is used.

3.2.12 Flyback Power Supply Schematic

Figure 2 shows the schematic of flyback power supply based on the UCC28740 controller.

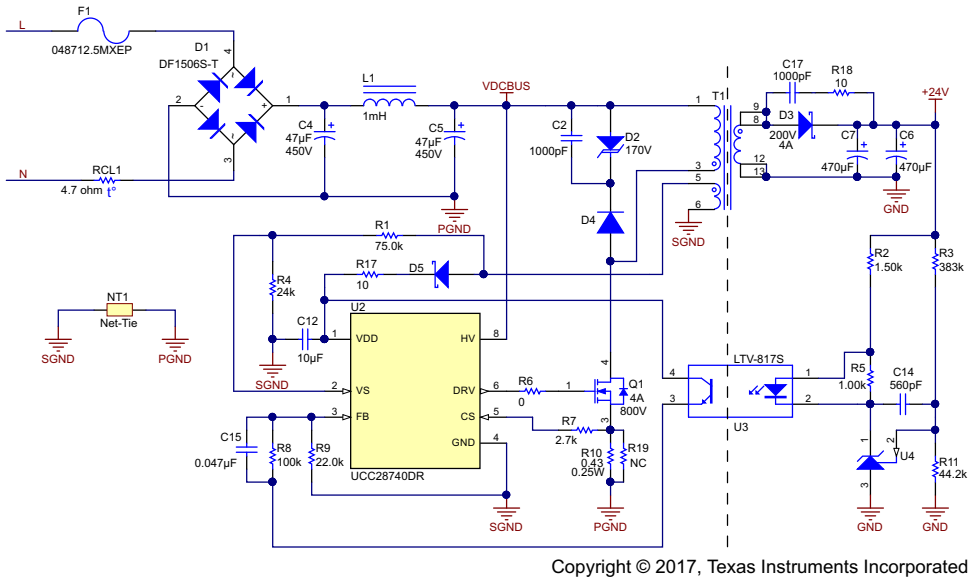

Figure 2. Flyback Power Supply Schematic

3.3 DRV10983—Integrated BLDC Motor Driver

The DRV10983 is the integrated motor driver which has a built-in 180° sensorless control scheme. Figure 3 shows the schematic of motor drive section based on the DRV10983.

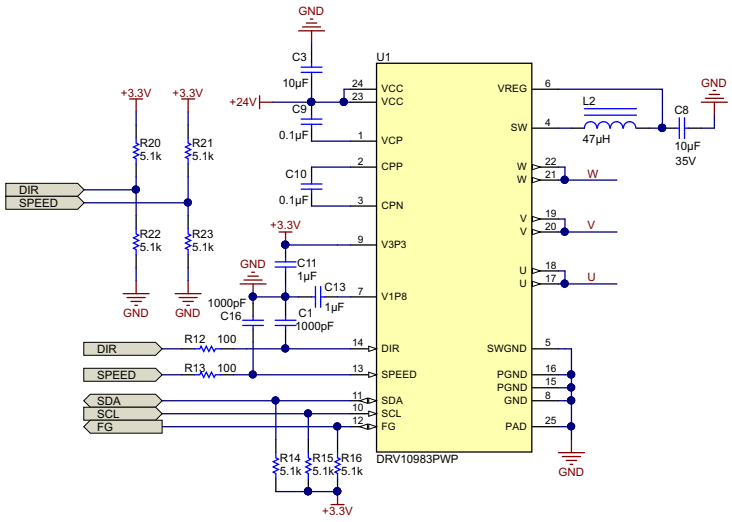

Figure 3. DRV10983 Motor Drive Schematic

3.3.1 Step-Down Voltage Regulator of DRV10983

The DRV10983 includes a step-down voltage regulator that can be operated as either a switching buck style regulator or as a linear regulator (see Figure 3). The regulator output voltage can be configured by register bit, VregSel. When VregSel = 0, the regulator output voltage is 5 V, and when VregSel = 1, the regulator output voltage is 3.3 V with a 100-mA capacity.

3.3.2 Motor Speed Control

The DRV10983 accepts three kinds of input speed control signal: analog, PWM, and I^2C. The user can choose J2 or J3 for the speed control input. The definitions for these two interfaces are shown in Table 4. In this reference design, the default configuration is analog input and is derived from two resistors: R21 and R23. The default value is 5.1 kΩ.

3.3.3 Thermal Design

Proper thermal design is crucial for the safe and reliable operation of semiconductors. The operation of the semiconductor at higher operating temperatures leads to a reduction in the safe operating area and can result in failure or reduced life of the device.

The goal of the thermal design is to limit the junction temperature of the switches inside the DRV10983 device within the safe values. The datasheet specifies that the insulated-gate bipolar transistor (IGBT) has a maximum junction temperature rating of 150ºC. This specification indicates that the user must design a heat dissipation area to account for this limit when operating at the full load capacity.

4 Getting Started Hardware and Firmware

4.1 Getting Started Hardware

4.1.1 PCB Overview

Figure 4 shows the top view and bottom view of the PCB for the TIDA-01417 design with brief description of all the connectors.

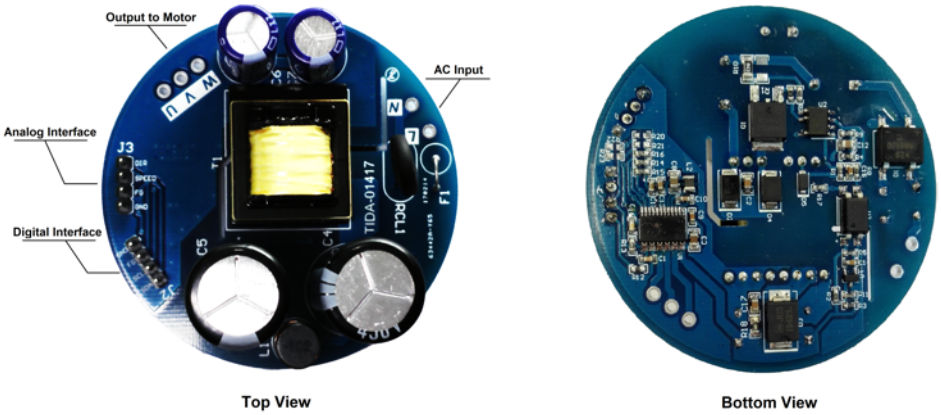

Figure 4. TIDA-01417 PCB Top and Bottom View

4.1.2 Interface Definition

Table 4. Interface Definition

PIN NUMBER	J2 DEFINITION	J3 DEFINITION
1	GND	GND
2	FG	FG
3	SCL	SPEED
4	SDA	DIR

4.1.3 Test Conditions

An adjustable AC source with capability of varying between 85- to 265-V AC is proposed for the test setup of the AC/DC flyback power supply in the TIDA-01417 design. Set the input current limit to 2.5 A. With respect to the output of flyback power, an electronic load capable of 40 V and a load variable in range from 0 to 3 A is preferred for the test. A rheostat or resistive decade box can be used in place of an electronic load. Figure 5 shows the setup and the test equipment used for flyback power supply.

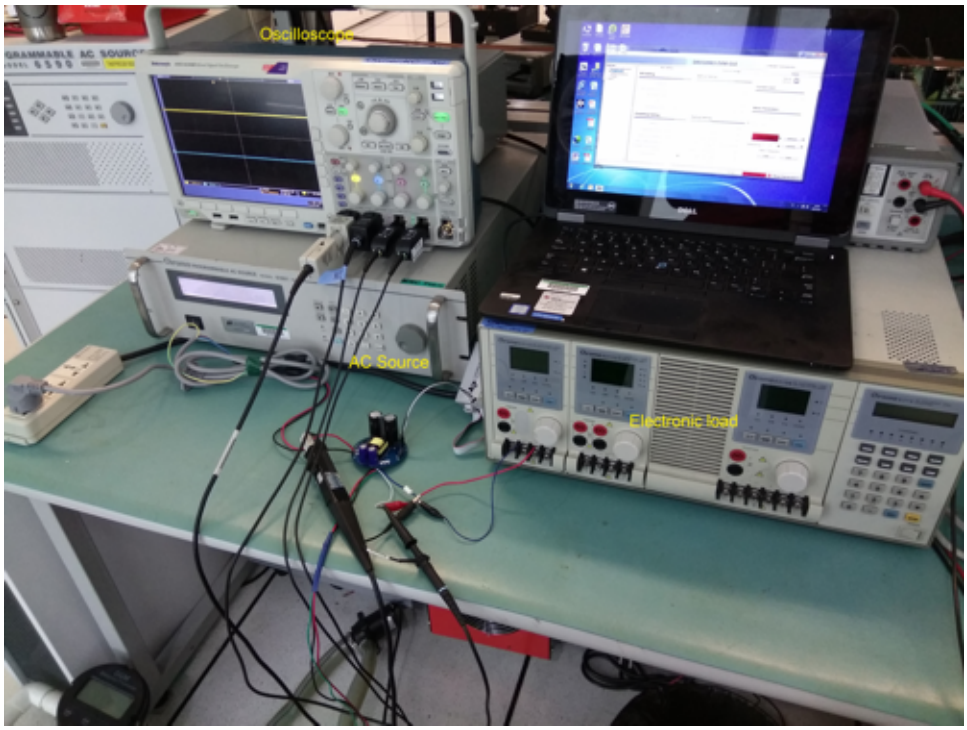

Figure 5. Picture of Test Setup for Flyback Power

Simple-pump test equipment is used to perform the motor driver load test of the system. Figure 6 shows the test equipment built for the design. The system consists of a BLDC motor pump, water tank, flow meter, pressure meter, and two mechanical valves.

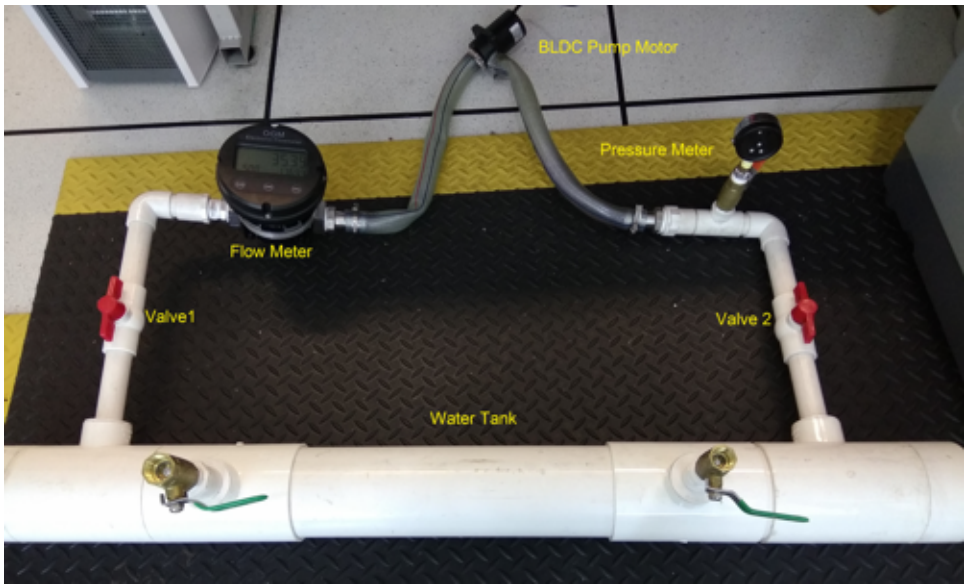

Figure 6. Picture of Test Setup for Motor Driver

The motor under test is connected to the test equipment. A 2400-RPM/86.4-W (rated) motor is used for testing. The loading on the brushless motor is done by circulating the water in the test system. Adjust the water pressure of the system by closing or opening valve 1 and valve 2. The load testing was done by driving the motor by DRV10983 at a constant speed, which is a closed loop speed control. During testing, the speed of the BLDC motor varied from 0 to 2400 RPM using the GUI.

4.1.4 Test Equipment

Table 5 lists the recommended test equipment used to test the TIDA-01417 design.

Table 5. Test Equipment

TEST EQUIPMENT	PART NUMBER
Oscilloscope	Tektronix MSO 4104B
Voltage probe	Tektronix P6139A
Current probe	Tektronix TCP202
Multimeter	Fluke 287C
AC source	Chroma 61601
Electronic load	Chroma 63103
Thermal camera	Fluke TI110

4.1.5 Power Supply Test Procedure

1. Connect the AC input terminals (L and N) of the board to adjustable AC source.
2. Solder two wires from output capacitor C6, red for "+" and black for "–", then connect them to electronic load or rheostat, maintaining correct polarity.
3. Set and maintain a minimum load of about 10 mA.
4. Gradually increase the input voltage from 0 V to turn on the voltage of 90-V AC.
5. Turn on the load to draw current from the output terminals of the flyback power supply.
6. Observe the startup conditions for smooth switching waveforms.
7. Observe the voltage and waveform of flyback power output to verify it works normally. The user can check the performance of power supply by electronic load or rheostat, specified as < 36 W.

4.2 Getting Started Firmware

The BLDC motor driver DRV10983 has an I^2C communication interface. The user can configure the motor parameters into the DRV10983 by external MCU or GUI in PC with calibration tool (for example, USB2ANY). Once all the parameters are optimized and fixed, the user can program the motor parameters to the EEPROM of the DRV10983. The firmware is usually a one-time configuration unless the user wants to modify parameters runtime of the configuration.

For GUI usage and tuning, see the *DRV10983 and DRV10975 Tuning Guide* (SLOU395).
For programming, see the *Programming Guide for the DRV10983* (SLVUAA5) for more information.

4.2.1 Hardware Connection

1. Connect the L and N input of TIDA-01417 board to the AC source.
2. Connect the U, V, and W output of the TIDA-01417 board to target the BLDC motor.
3. Connect the USB2ANY tool to computer through the USB cable.
4. Connect the TIDA-01417 board and USB2ANY tool by the I^2C interface. The pin assignment for USB2ANY is as follows:

Table 6. USB2ANY Connector Definition

PIN	DESCRIPTION
6	GND
9	SDA
10	SCL

Figure 7 shows a physical image of these connections.

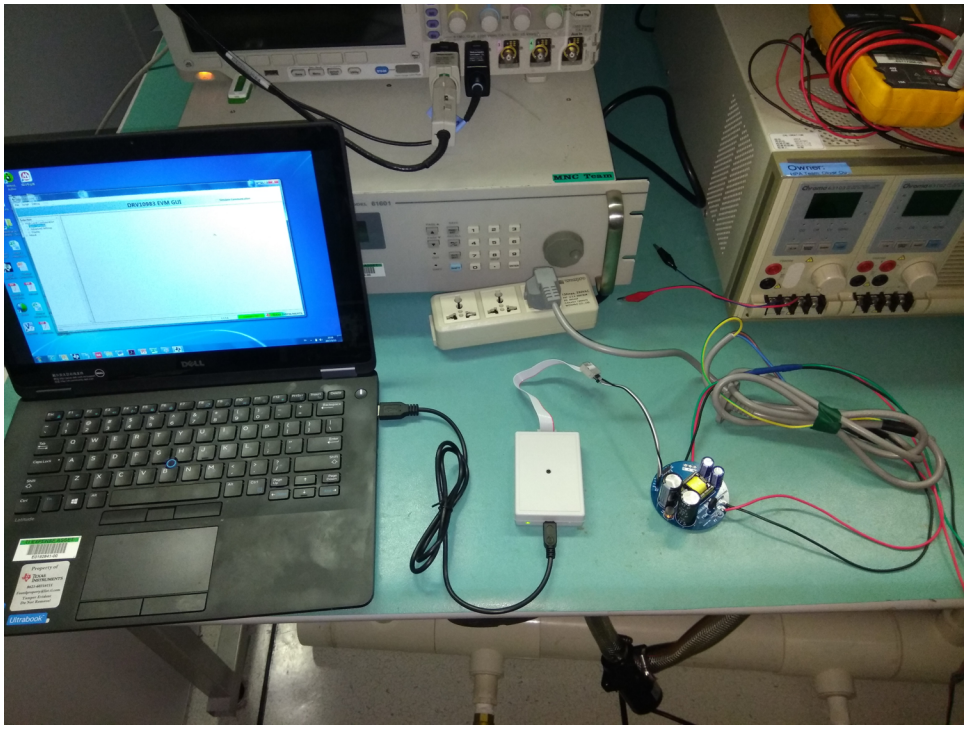

Figure 7. Picture of GUI Hardware Connection

4.2.2 Configuring DRV10983 Registers

1. Download the GUI from the DRV10983EVM product page.
   - Download and install DRV10983EVM Software (SLOC312).
   - Install the LabVIEW™ Runtime Engine (required) after the GUI is installed (see the "README.rtf" in the GUI download folder).
2. Start the GUI.
   - Select the DRV10983 from the device pop up menu.
   - Click *Enable Configuration*, which turns green, verifying the device is connected.
3. Set the parameters.

For a user specified motor, the tuning procedure is demonstrated in Figure 8. Contact a local support team for more information about documentation and support.

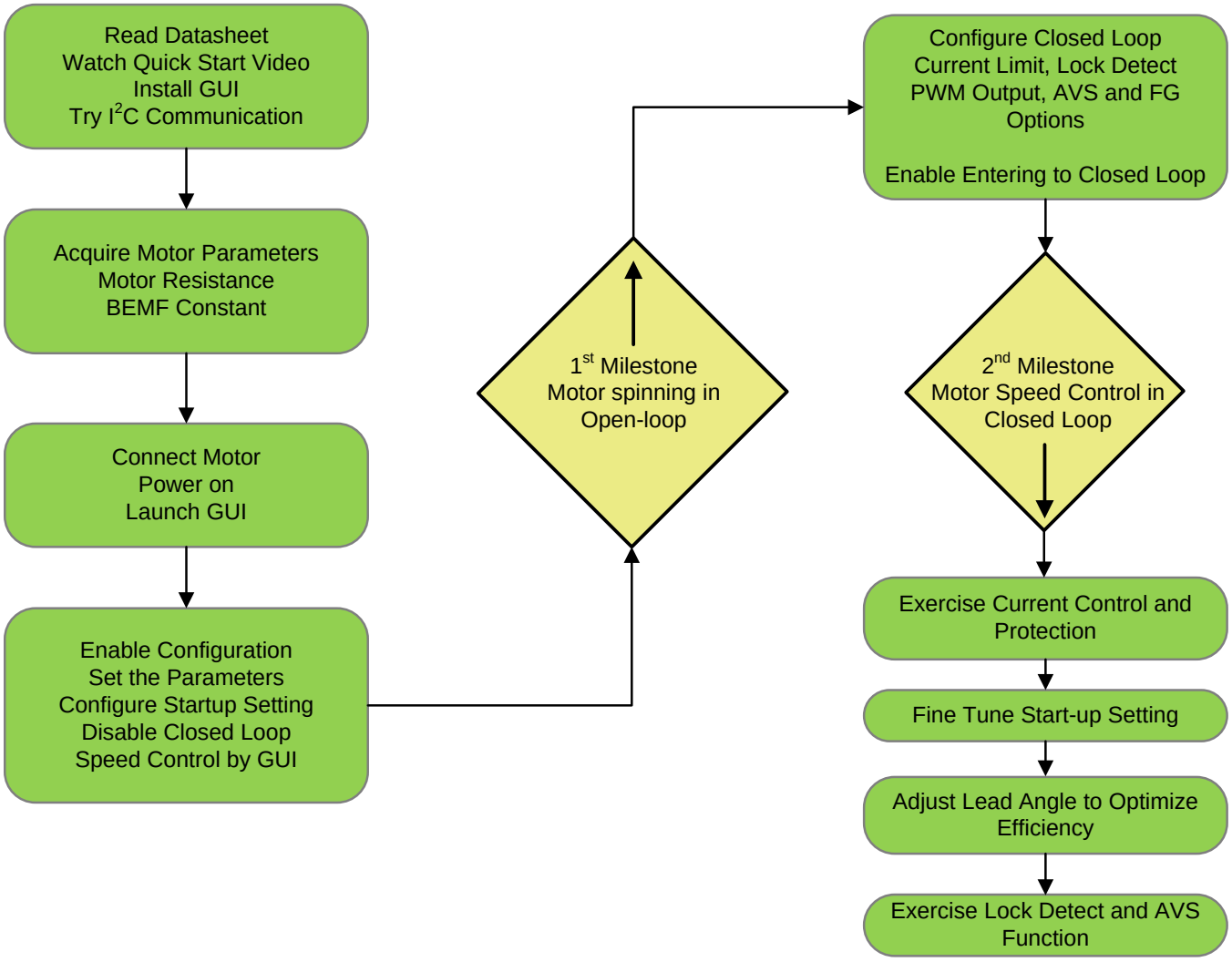

Figure 8. Events for Tuning Motor Parameters for DRV10983

5 Testing and Results

The test results for the flyback power supply are divided into multiple sections that cover the steady state performance measurements, functional performance waveforms and test data, transient performance waveforms, and thermal measurements.

The motor driver test includes the startup profile, runtime waveform, acceleration, deceleration, and rotor lock.

5.1 Performance Data for Flyback Power

5.1.1 Efficiency and Regulation With Load Variation

Table 7 shows the efficiency and regulation performance data at a 115-V AC input for the flyback power supply part.

Table 7. Efficiency and Regulation Performance at 115-V AC Input

V_{INAC} (V)	I_{INAC} (A)	PF	P_{INAC} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFF (%)
115	0.058	0.420	2.82	24	0.1	2.4	85.11
115	0.148	0.487	8.35	24	0.3	7.2	86.23
115	0.238	0.506	13.87	24	0.5	12.0	86.52
115	0.325	0.518	19.40	24	0.7	16.8	86.60
115	0.412	0.528	25.00	24	0.9	21.6	86.40
115	0.494	0.537	30.40	24	1.1	26.4	86.84
115	0.578	0.538	35.80	24	1.3	31.2	87.15
115	0.665	0.542	41.60	24	1.5	36.0	86.54

Table 8 shows the efficiency and regulation performance data at a 230-V AC input for the flyback power supply part.

Table 8. Efficiency and Regulation Performance at 230-V AC Input

V_{INAC} (V)	I_{INAC} (A)	PF	P_{INAC} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFF (%)
230	0.039	0.331	2.9	24	0.1	2.4	82.76
230	0.093	0.388	8.3	24	0.3	7.2	86.75
230	0.141	0.420	13.7	24	0.5	12.0	87.59
230	0.189	0.440	19.1	24	0.7	16.8	87.96
230	0.236	0.452	24.6	24	0.9	21.6	87.80
230	0.285	0.457	30.0	24	1.1	26.4	88.00
230	0.332	0.460	35.1	24	1.3	31.2	88.89
230	0.384	0.461	40.8	24	1.5	36.0	88.24

5.1.2 Standby Power Consumption

The standby power consumption was noted at multiple AC input voltages with a constant no load on the output DC bus while the motor controller DRV10983 stay at standby mode. Table 9 lists the results:

Table 9. Standby Power Consumption for Flyback Power

INPUT VOLTAGE (VAC)	INPUT CURRENT (mA)	PF	STANDBY POWER (mW)	OUTPUT (V)
90	1.63	0.248	36	24
120	1.36	0.236	38	24
150	1.16	0.219	38	24
180	1.07	0.211	40	24
230	0.97	0.199	40	24
265	1.03	0.192	50	24

5.2 Performance Curves for Flyback Power

5.2.1 Efficiency With Load Variation

Figure 9 shows the measured efficiency for the flyback power supply with AC input voltage variation.

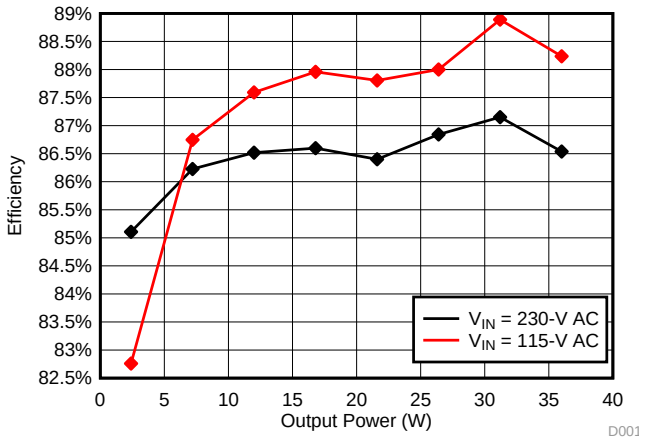

Figure 9. Efficiency versus Output Power

5.2.2 Load Regulation

Figure 10 shows the measured load regulation of the flyback power supply with load variation.

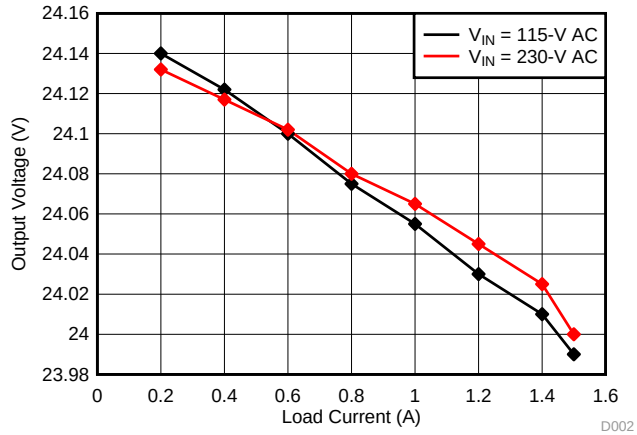

Figure 10. Output Voltage Variation With Load Current

5.2.3 AC Line Regulation With AC Input Voltage Variation

Figure 11 shows the output voltage regulation with AC line voltage variation.

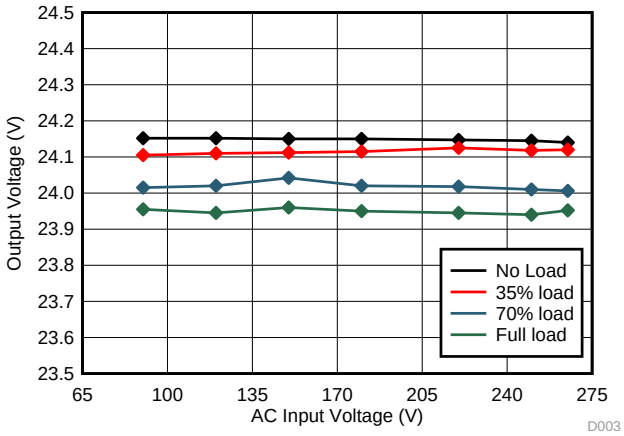

Figure 11. Load Regulation With Load Current

5.2.4 Standby Power Variation

Figure 12 shows the standby power variation under a different AC input voltage.

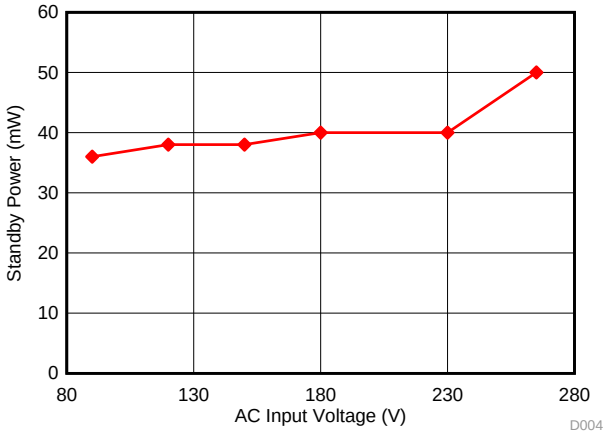

Figure 12. Standby Power With AC Input Variation

5.3 Functional Waveforms for Flyback Power

5.3.1 Inrush Current Waveform

Inrush current drawn by the system is observed and recorded at a maximum input voltage of 230-V AC, which is shown in Figure 13.

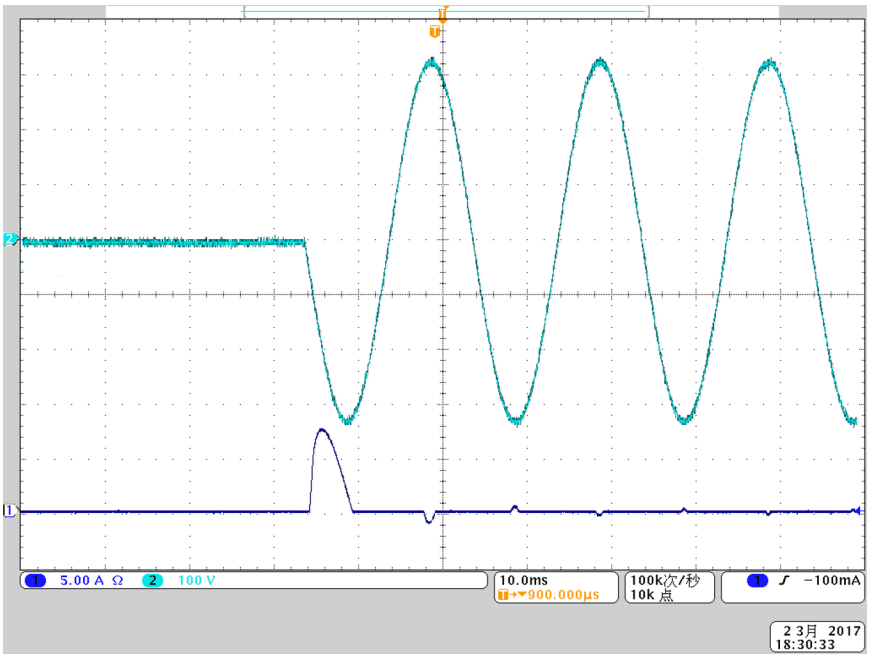

Figure 13. Input Inrush Current at 230-V AC

NOTE: Channel 1: Inrush current, 5 A/div; Channel 2: Input Voltage, 100 V/div

5.3.2 Flyback MOSFET Switching Node Waveforms

Waveforms at the flyback switching node (SW) were observed along with the MOSFET current for 115- and 230-V AC under full load (1.5 A) conditions, which is shown in Figure 14.

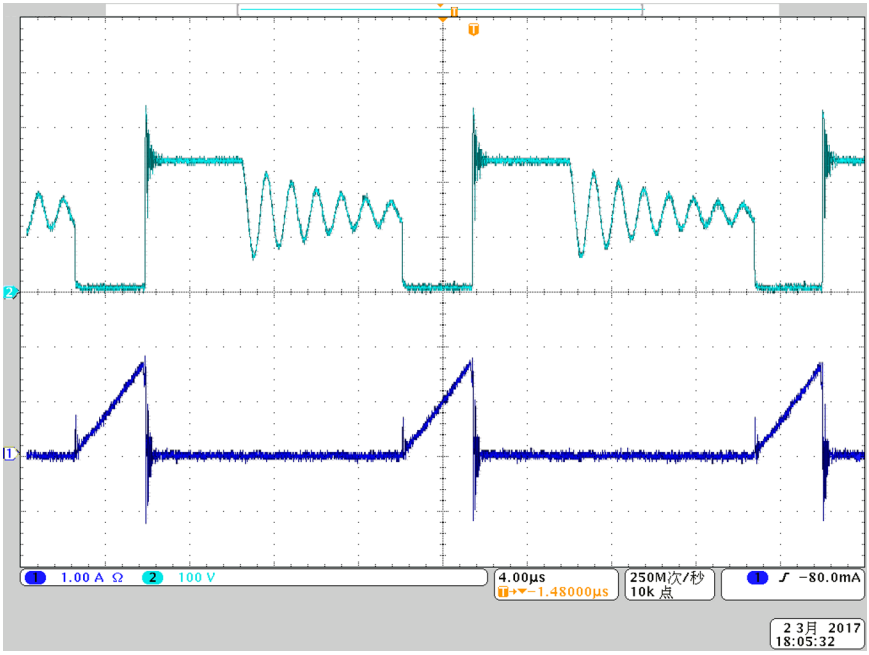

Figure 14. SW Node Waveform and MOSFET Current at V_{INAC} = 115-V AC, Full Load

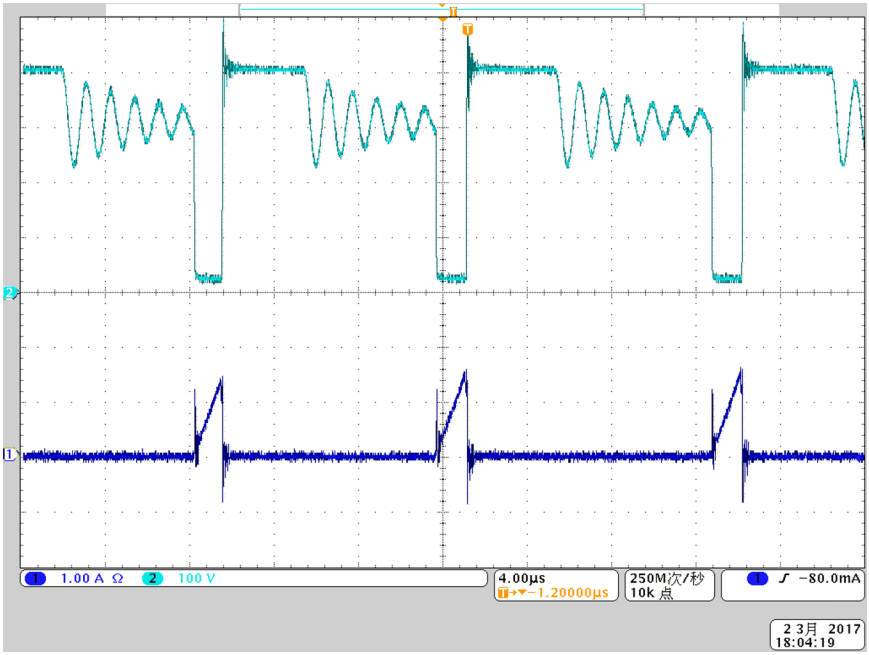

Figure 15. SW Node Waveform and MOSFET Current at V_{INAC} = 230-V AC, Full Load

NOTE: Channel 1: Drain current, 1 A/div; Channel 2: Drain Voltage, 100 V/div

5.3.3 Output Voltage Ripple

The output ripple is observed at a 24-V DC output and full load 1.5 A at both 115- and 230-V AC inputs, which are shown in Figure 16 and Figure 17.

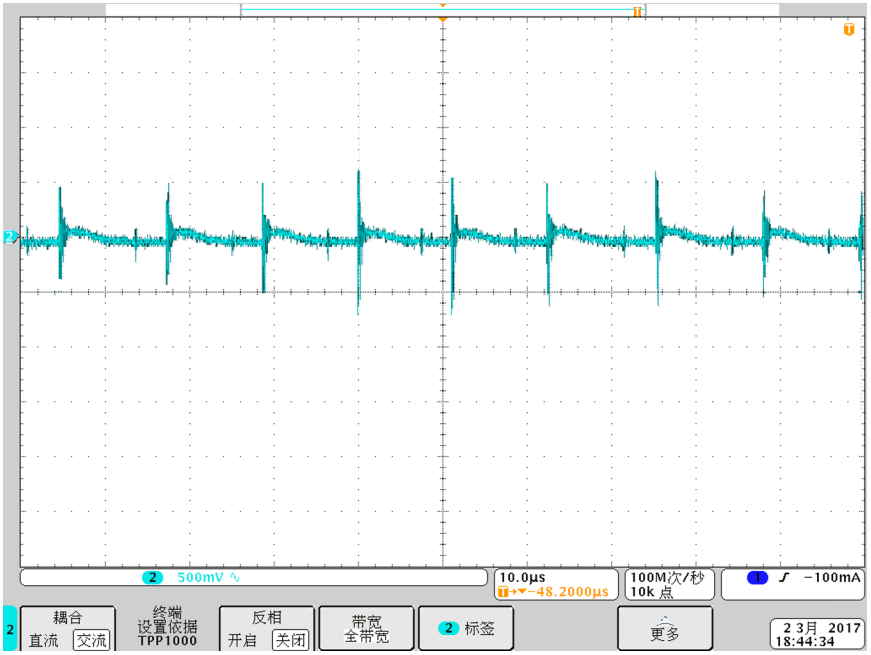

Figure 16. Output Voltage Ripple at V_{INAC} = 115-V AC, Full Load

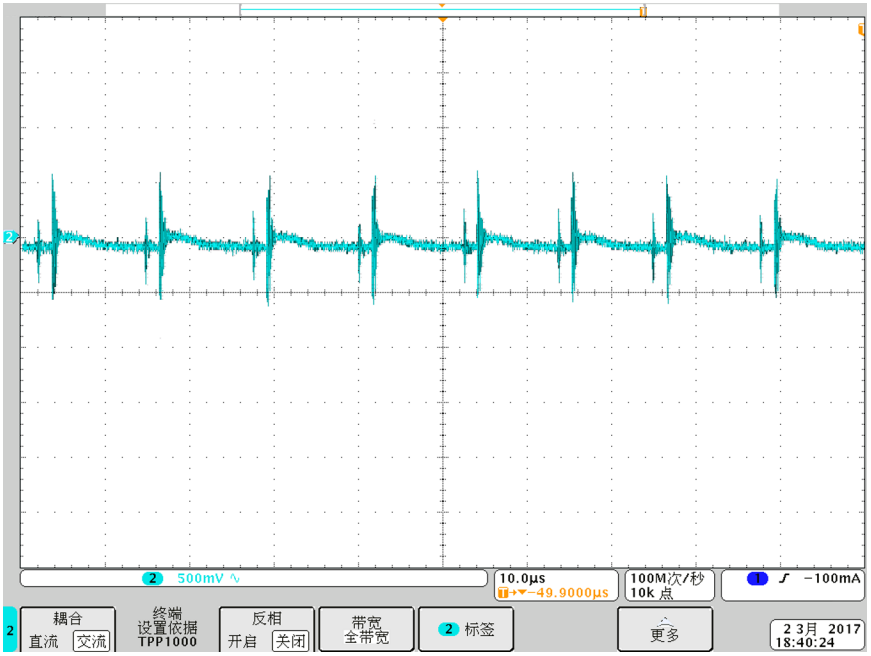

Figure 17. Output Voltage Ripple at V_{INAC} = 230-V AC, Full Load

5.4 Transient Waveforms for Flyback Power

5.4.1 Turnon Characteristics

Figure 18 shows the 24-V output turnon with a resistive load (21.5 Ω) and Figure 19 shows a CC load of 1 A at the output.

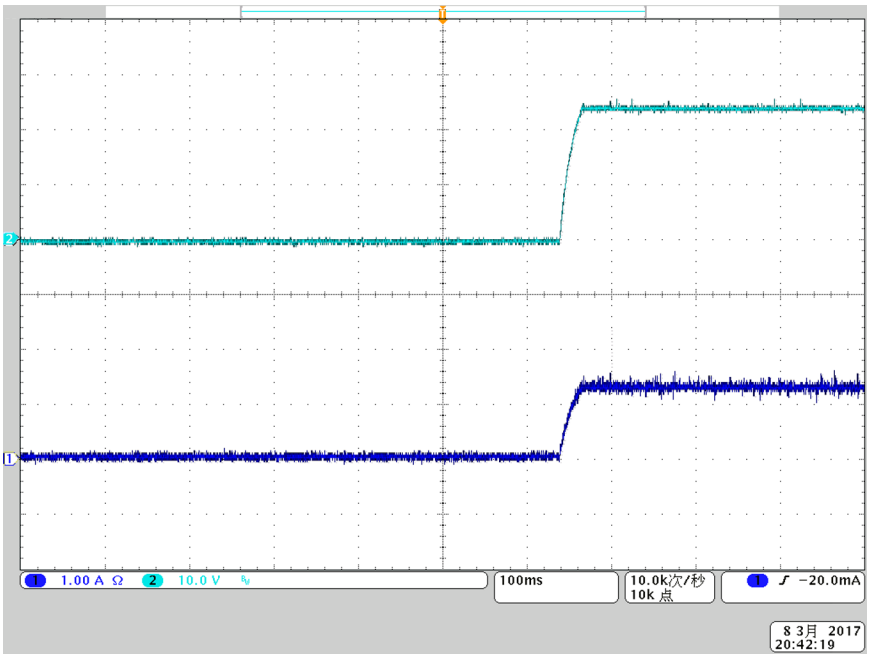

Figure 18. Output Turnon Waveform With Resistive Load of 21.5 Ω

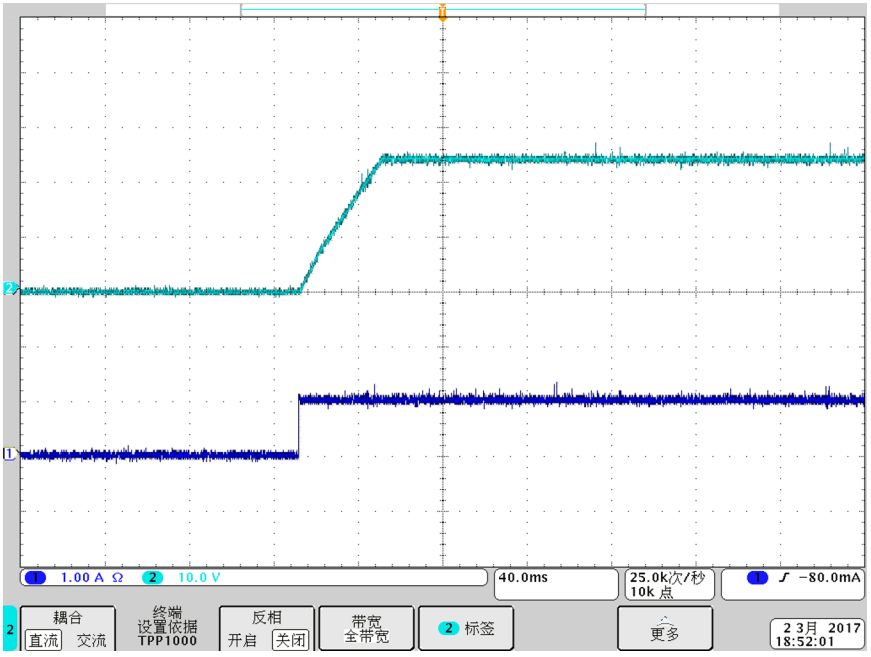

Figure 19. Output Turnon Waveform With CC Load of 1 A

NOTE: Channel 1: Output current, 1 A/div; Channel 2: Output voltage, 10 V/div

5.4.2 Transient Load Response

Load transient performance is observed with the load switched at a 0.2-m wire length. The output load is switched using electronic load.

V_{IN} = 230-V AC, load transient from 0 to 1.5 A, and vice-versa performance at a 24-V output.

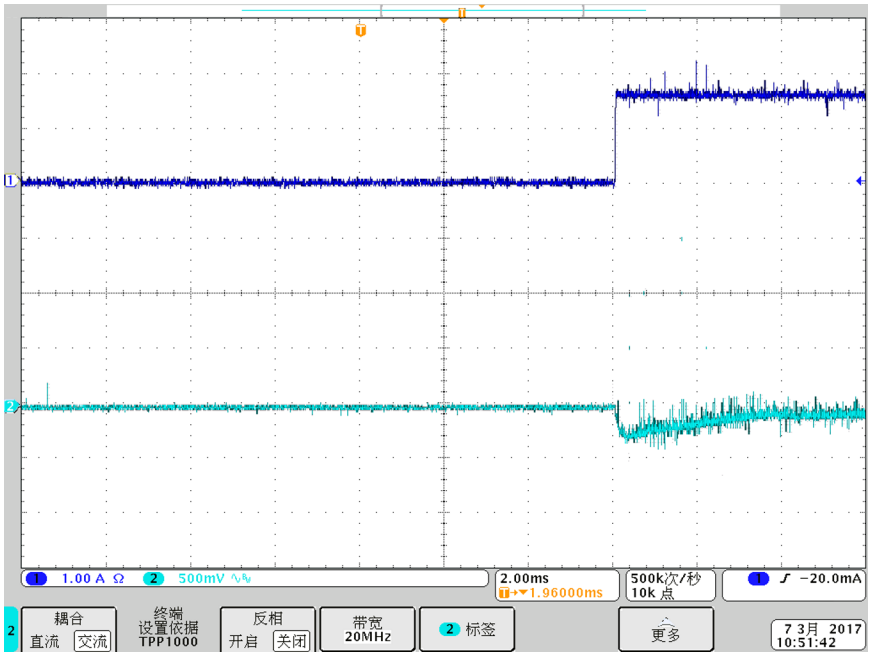

Figure 20. Output Voltage and Current Waveform, Load Transient From 0 to 1.5 A

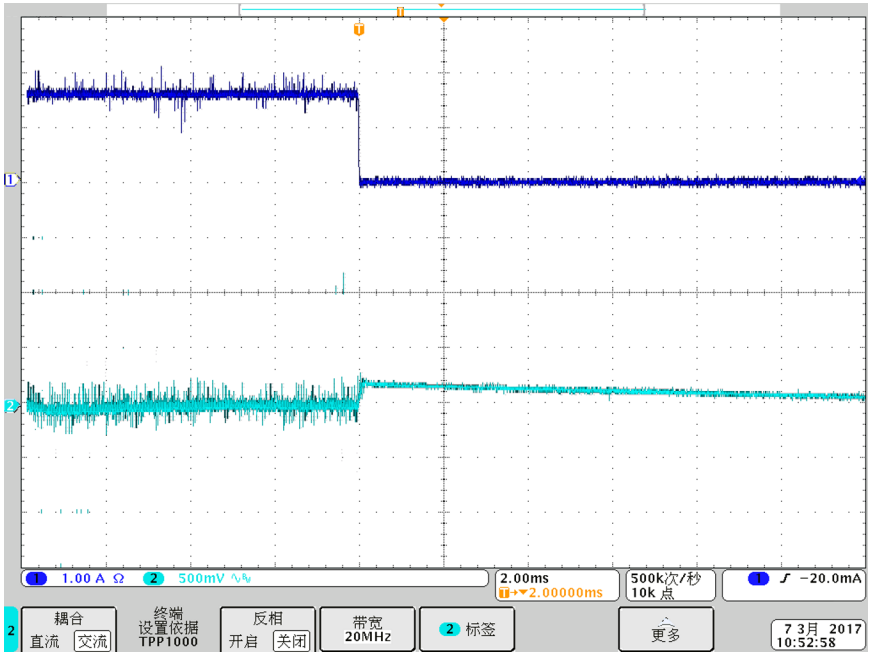

Figure 21. Output Voltage and Current Waveform, Load Transient From 1.5 to 0 A

NOTE: Channel 1: Output Current, 1 A/div; Channel 2: Output Voltage, 500m V/div

5.4.3 Overload and Overcurrent Response

The converter is driven to an overcurrent condition by applying a step change in load from 1 to 3 A. The performance of the converter output was observed and shown in Figure 22.

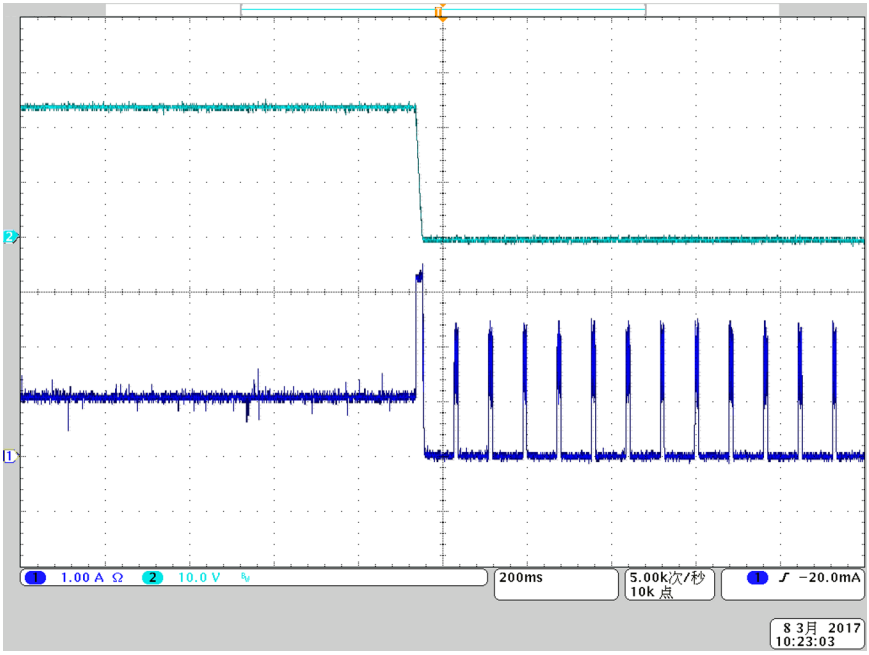

Figure 22. Output Voltage and Current Waveform, Step-Load Transient From 1 to 3 A

NOTE: Channel 1: Output current, 1 A/div; Channel 2: Output voltage, 10 V/div

5.4.4 Short-Circuit Response

A short circuit was applied and removed to observe the output turnoff and auto-recovery cycle. When the short is applied, the converter shuts down and goes into hiccup mode. When the short is removed, the converter recovers back to normal operation.

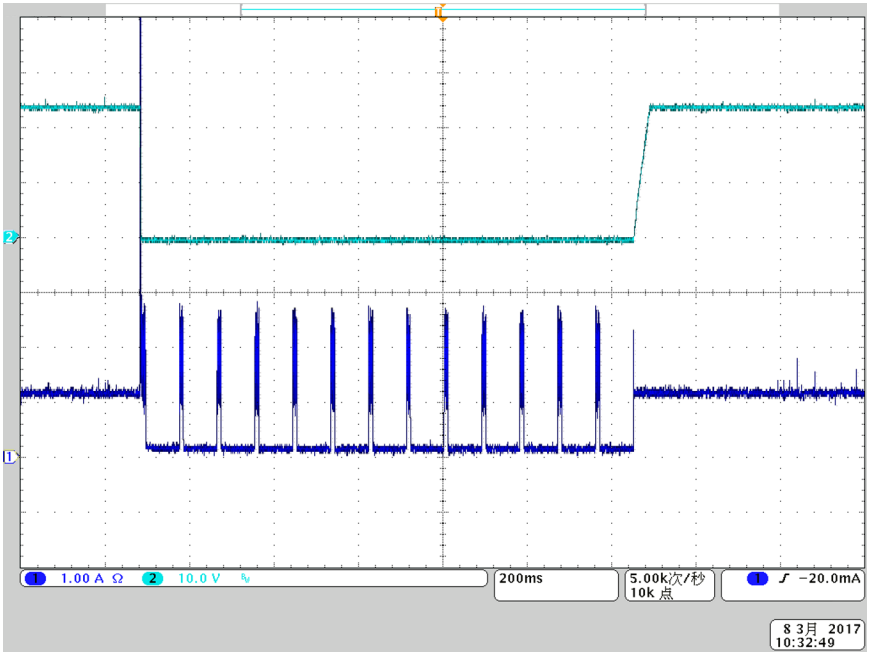

Figure 23. Response During Short-Circuit and Auto-Recovery When Short is Removed

NOTE: Channel 1: Output current, 1 A/div; Channel 2: Output voltage, 10 V/div

5.5 BLDC Motor Driver Test

A GUI was used during functional testing of the board to configure the parameters for the DRV10983 devices to spin the specific motor. The following images specify the configuration of parameters for the tested motor.

5.5.1 Acceleration

Figure 24 shows the winding current waveform as well as the three phase output voltage with respect to the negative DC bus during the acceleration period.

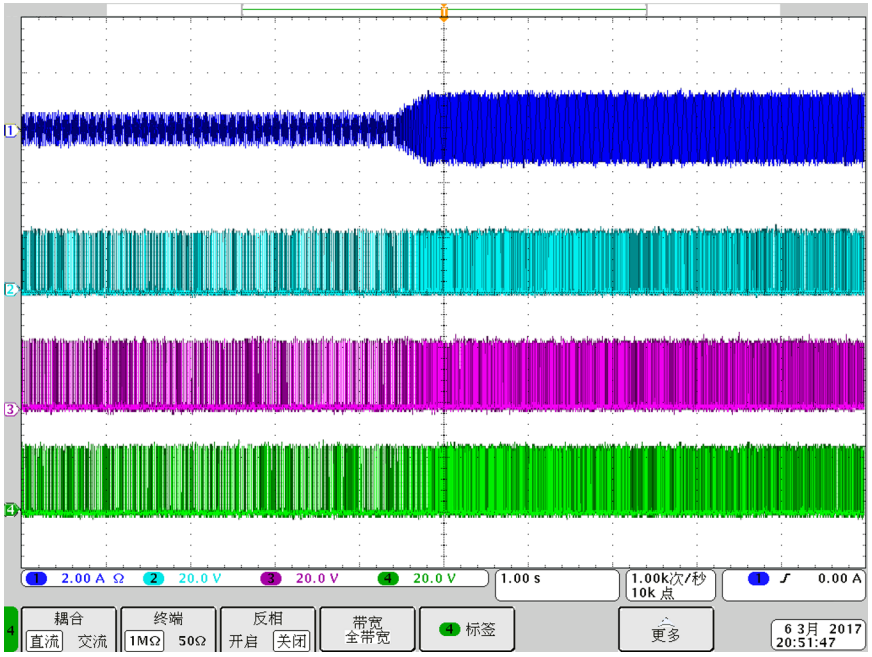

Figure 24. Acceleration

NOTE: Channel 1: Winding current, 2 A/div; Channel 2, 3, 4: U, V, W output voltage, 20 V/div

5.5.2 Deceleration

Figure 25 shows the winding current waveform of motor as well as the three phase output voltage with respect to the negative DC bus during the deceleration period.

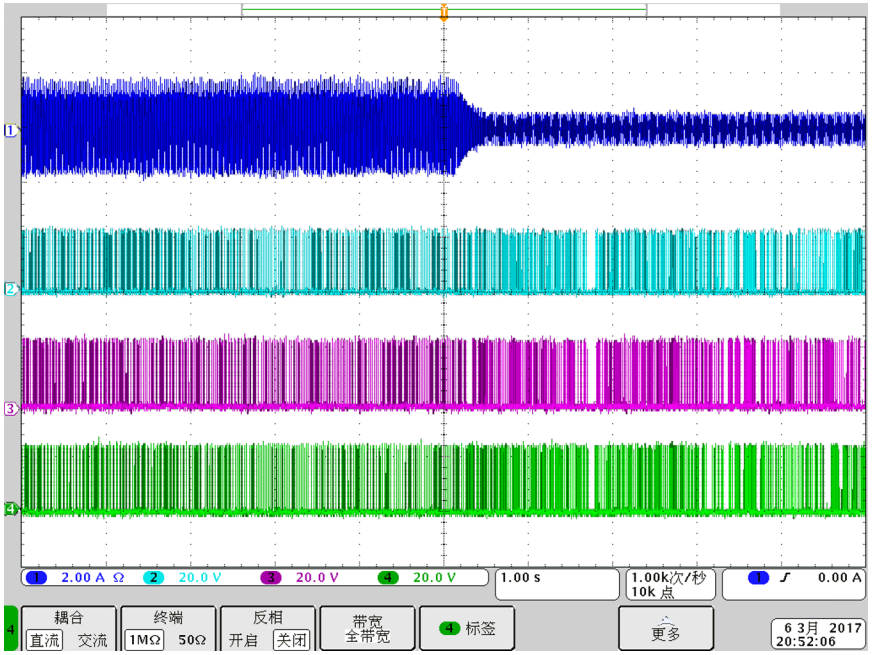

Figure 25. Deceleration

NOTE: Channel 1: Winding current, 2 A/div; Channel 2, 3, 4: U, V, W output voltage, 20 V/div

5.5.3 Runtime Waveform

Figure 26 shows the winding current of the motor driven by the DRV10983 and the winding voltage measured with respect to the negative DC bus.

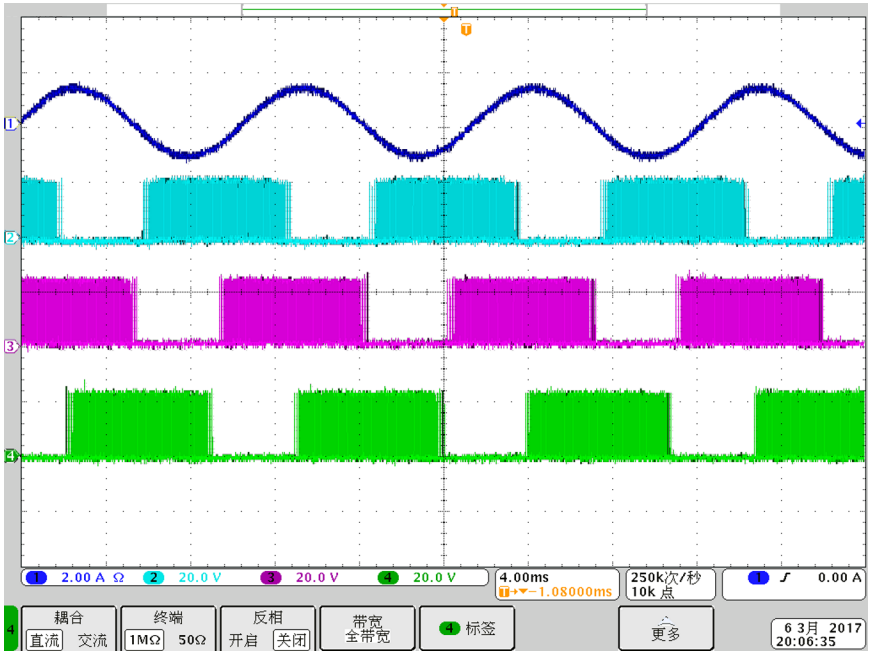

Figure 26. Runtime Waveform

NOTE: Channel 1: Winding current, 2 A/div; Channel 2, 3, 4: U, V, W output voltage, 20 V/div

5.5.4 FG Signal

Figure 27 shows the FG signal together with the winding current waveform.

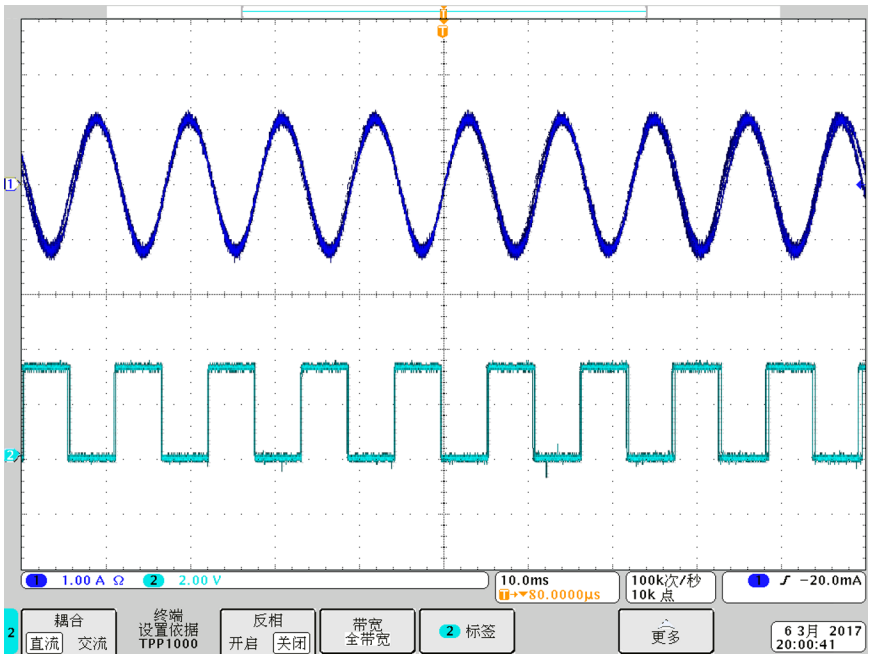

Figure 27. DRV10983 Speed Signal versus FG

NOTE: Channel 1: Winding current, 1 A/div; Channel 2: FG Signal, 2 V/div

5.5.5 Buck Converter Output

Figure 28 shows the 3.3 V generated from the DRV10983 step-down regulator. The ripple in the 3.3-V rail is shown Figure 29.

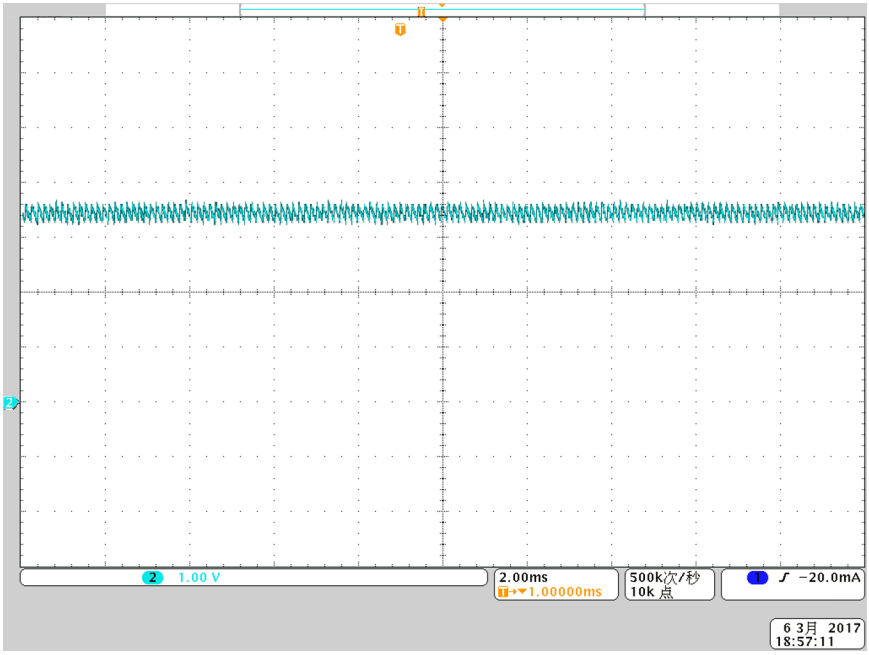

Figure 28. Output Voltage of 3.3 V From Step-Down Regulator of DRV10983

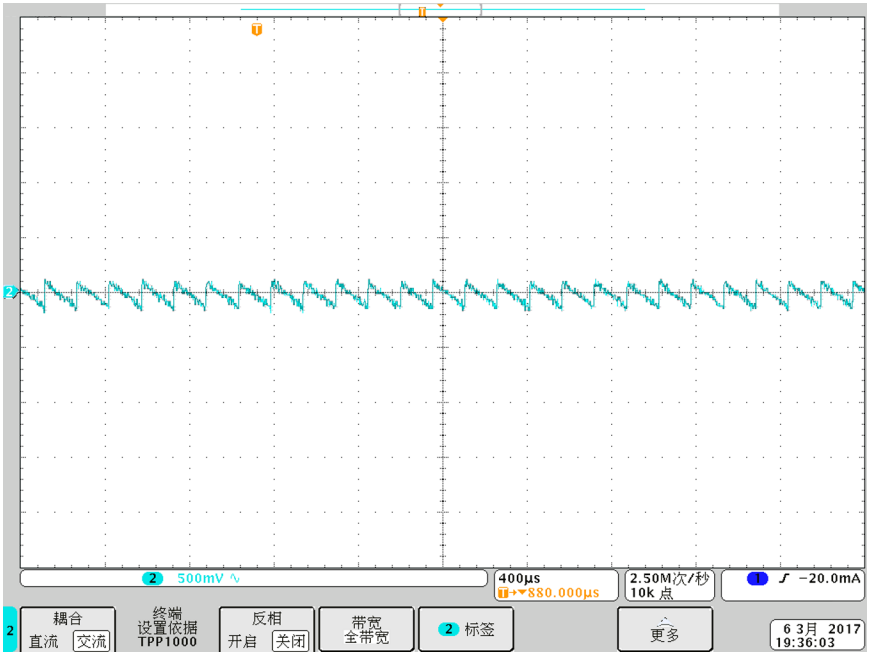

Figure 29. Ripple in 3.3-V Output From Step-Down Regulator of DRV10983

5.5.6 Startup Profile

As Figure 30 shows, during the align time, the supply draws a very small current. After the motor align time, the open loop acceleration occurs. When the motor reaches the threshold, the speed threshold enters a closed loop where it accelerates further.

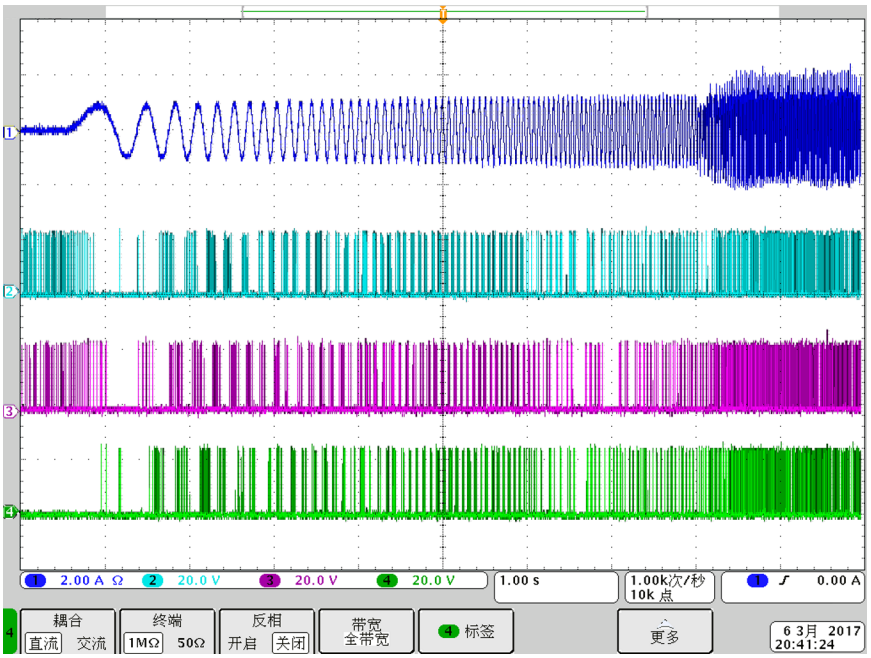

Figure 30. Start-up Profile

NOTE: Channel 1: Winding current, 2 A/div; Channel 2, 3, 4: U, V, W output voltage, 20 V/div

5.5.7 Rotor Lock

Figure 31 shows that when the lock detection current limit feature is triggered, the device stops driving the motor and waits for 5 seconds to retry.

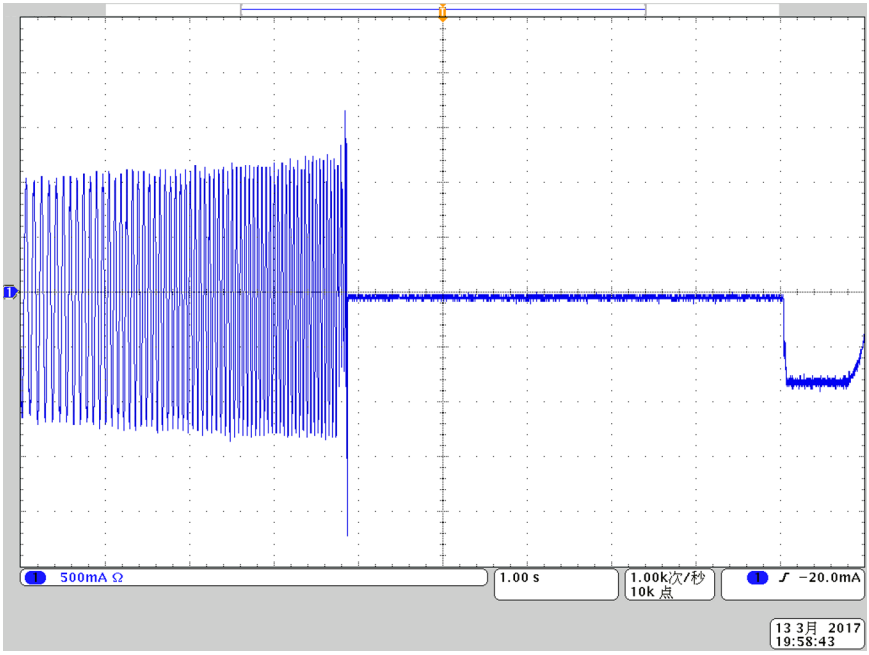

Figure 31. Winding Current Waveform During Rotor Lock

5.6 Thermal Measurements

To better understand the temperature of power components and maximum possible operating temperature, the thermal images were plotted at room temperature (25°C) with a closed enclosure, no airflow, and at different load conditions with different input voltages. The board was allowed to run for 30 minutes before capturing a thermal image.

5.6.1 Thermal Image for Lo-Line (115-V AC) Operation

Figure 32 shows the thermal image for both top side and bottom side of the board. The input voltage is 115-V AC, and the load on 24-V DC bus is 1.5 A with a 36-W power output.

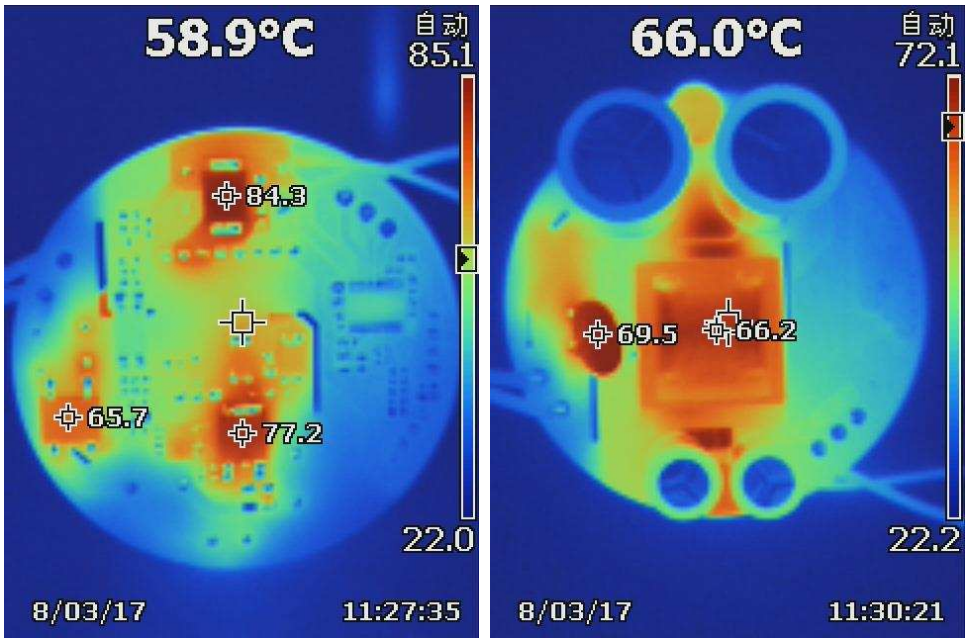

Figure 32. Temperatures at 115-V AC Input and 36-W Output

Table 10. Highlighted Image Markers

PARAMETER	VALUE
Input voltage	115-V AC
Output power	36 W
Ambient temperature	25°C
Transformer	66.2°C
Main switching FET (Q1)	77.2°C
Output rectifying diode	84.3°C
Bridge diode	65.7°C

5.6.2 Thermal Image for Hi-Line (230-V AC) Operation

Figure 33 shows the thermal image for both the top and bottom side of the board. The input voltage is 230-V AC, and the load on 24-V DC bus is 1.5 A with a 36-W power output.

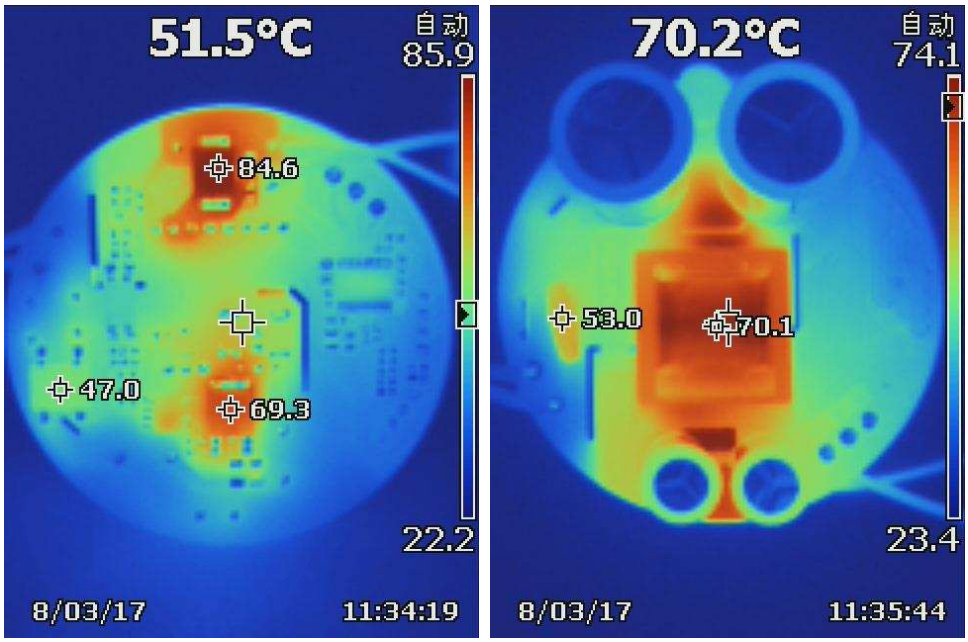

Figure 33. Temperatures at 230-V AC Input and 36-W Output

Table 11. Highlighted Image Markers

PARAMETER	VALUE
Input voltage	230-V AC
Output power	36 W
Ambient temperature	25°C
Transformer	70.1°C
Main switching FET (Q1)	69.3°C
Output rectifying diode	84.6°C
Bridge diode	47°C

5.6.3 Thermal Image for DRV10983

Figure 34 shows a thermal image of the PCB assembly when the pump is running at its rated output power of 30 W (1.77 A_{PEAK}) when V_{DC} = 24 V.

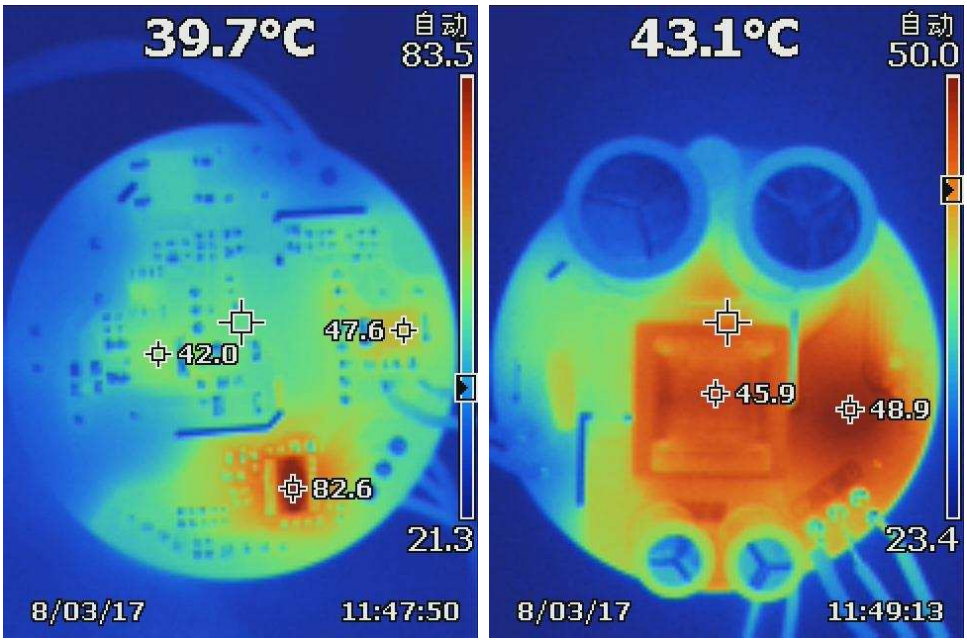

Figure 34. Temperatures for Motor Driver DRV10983

Table 12. Highlighted Image Markers

PARAMETER	VALUE
Input voltage	230-V AC
Ambient temperature	25°C
Transformer	45.9°C
DRV10983	82.6°C

6 Design Files

6.1 Schematics

To download the schematics, see the design files at TIDA-01417.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01417.

6.3 PCB Layout Recommendations

The following are key guidelines for routing power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high-frequency switching currents. This will help in reducing EMI and improve converter overall performance.
- Keep the switch node as short as possible. A short and optimal trace width helps to reduce induced ringing caused by parasitic inductance.
- Keep traces with high dV/dt potential and high di/dt capability away from or shielded from sensitive signal traces, with adequate clearance and ground shielding.
- For each power supply stage, keep power ground and control ground separately. Tie them together (if they are electrically connected) in one point near DC input return or output return of the given stage correspondingly.
- For controller specific guidelines, see the placement and routing guidelines and layout example presented in the UCC28740 datasheet.
- For motor driver specific guidelines, see the layout guideline and layout example presented in the DRV10983 datasheet.

6.3.1 Layout Prints

To download the layout prints, see the design files at TIDA-01417.

6.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-01417.

6.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-01417.

6.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at TIDA-01417.

6.7 Design Calculator Spreadsheet

To download the design calculator spreadsheet, see the design files at TIDA-01417.

7 Related Documentation

1. Texas Instruments, *UCC28740 Constant-Voltage Constant-Current Flyback Controller Using Opto-Coupled Feedback*, UCC28740 Datasheet (SLUSBF3)
2. Texas Instruments, *DRV10983 12- to 24-V, Three-Phase, Sensorless BLDC Motor Driver*, DRV10983 Datasheet (SLVSCP6)
3. Texas Instruments, *24-V DC, 100-W/30-W Dual Sensorless Brushless DC Motor Drive Reference Design*, TIDA-00447 Design Guide (TIDUA50)
4. Texas Instruments, *90- to 265-V AC, 91% Efficiency, >0.94 PF Buck-PFC Plus 24-V, 30-W Brushless DC Motor Drive Reference Design*, TIDA-00652 Design Guide (TIDUAS3)
5. Texas Instruments, *60-W, 24-V, High-Efficiency Industrial Power Supply With Precision Voltage, Current, and Power Limit*, TIDA-00702 Design Guide (TIDUB51)
6. Texas Instruments, *DRV10983 and DRV10975 Tuning Guide*, DRV10983 and DRV10975 User's Guide (SLOU395)
7. Texas Instruments, *Programming Guide for the DRV10983*, DRV10983 Application Report (SLVUAA5)
8. Texas Instruments, *DRV10983 and DRV10975 Evaluation Module*, DRV10983 and DRV10975 User's Guide (SLOU393)

7.1 Trademarks

8 Terminology

SPI— Serial peripheral interface

PWM— Pulse width modulation

BLDC— Brushless DC motor

MCU— Microcontroller unit

FETs, MOSFETs—Metal-oxide-semiconductor field-effect transistor

RPM— Rotation per minute

RMS— Root mean square

9 About the Author

YICHANG (RICHARD) WANG is a systems architect at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Richard brings to this role his extensive experience in home appliances, including power electronics, high-frequency DC-DC, AC-DC converters, analog circuit design, and so on. Richard got his master’s degree in electrical engineering and automation from Nanjing University of Aeronautics and Astronautics, China.

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