TI Designs: PMP15027
High-Current SEPIC Reference Design for Automotive Lighting and ADAS Systems

Description

This reference design showcases a TPS92691-Q1 LED SEPIC (buck-boost) driver solution that can be used in a variety of automotive and vehicle aftermarket lighting applications. This design is ideal for high-current pulse operation of IR LEDs in applications for Advanced Driver Awareness Systems (ADAS). The SEPIC topology is intended for LED driver designs that are single stage, which results in a simpler and more cost-effective lighting solution. Additional design flexibility includes analog and PWM dimming support as well as built-in monitoring for fault detection and protection of the continuous LED current. EMI filtering is included and designed to meet CISPR-25, Class 3 conduction requirements.

Resources

PMP15027	Design Folder
TPS92691-Q1	Product Folder
TPS92691 SEPIC EVM	Tool Folder
TPS92691 Boost and Boost-to-Battery EVM	Tool Folder
TPS92961 Boost and SEPIC P-Spice Model	Tool Folder

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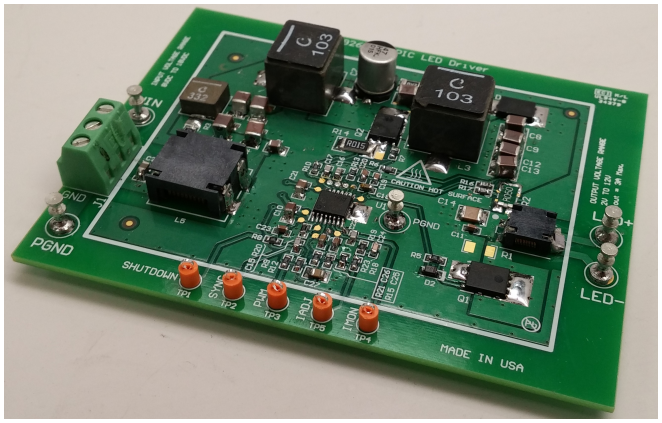
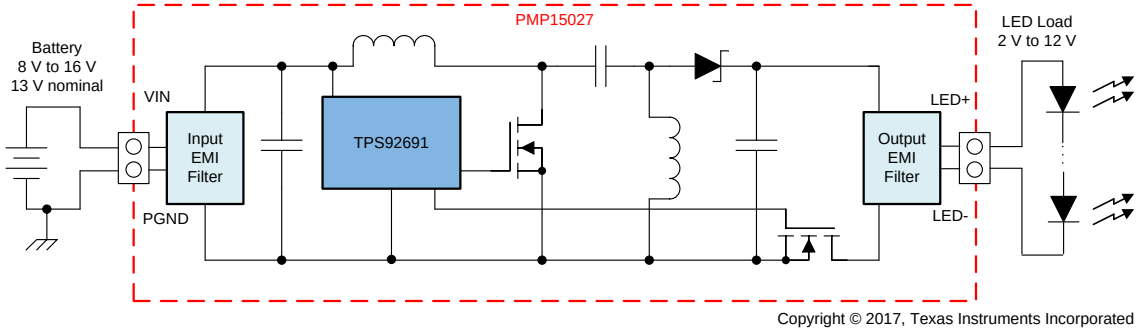
Features

- Optimized for Infrared LEDs and Other High-Current LED Lighting Applications
- CISPR-25 Tested EMI
- Switching Frequency Outside of AM Band
- Analog and PWM Dimming
- Operation Through Warm Crank and Load Dump
- Continuous LED Current Monitoring Output
- Overvoltage Protection and Input Undervoltage Lockout

Applications

- Automotive Lighting:
  - IR LEDs for ADAS Systems
  - Headlights
- Industrial Cameras





1 System Description

Energy efficiency, safety, and precise dimming control are all factors that are causing widespread adoption of infrared light-emitting diodes (IR LEDs) in automotive ADAS applications. IR LEDs offer clear performance and reliability advantages over traditional light sources while enhancing longevity and dimming performance. However, short development cycles and intense competition put pressure on product vendors to reduce their time to market while still offering high-quality lighting solutions in terms of low electromagnetic interference (EMI), thermal efficiency, and light quality.

The PMP15027 reference design gives a simple, easy to adopt implementation for a high-output accuracy SEPIC LED driver with integrated current monitoring. This reference design uses the TPS92691 multi-topology controller and has an input voltage range of 8 V to 16 V. This design meets CISPR-25 Class 3 EMI standards, and the switching frequency for the controller is set outside the AM frequency band. External frequency synchronization capability as well as analog and PWM dimming make this reference design attractive for a variety of other automotive lighting applications.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
V_{IN} input voltage (nominal)	—	8	13	16	V
V_{IN} input voltage (min or max)	Warm crank or load dump	7	—	42	V
V_{IN} undervoltage lockout	—	—	4.4	—	V
OUTPUT CHARACTERISTICS					
LED forward voltage	—	—	2	—	V
Number of LED in series	—	1	—	6	—
V_{LED} output voltage	LED+ to LED–	—	—	12	V
I_{LED} output current	V_{IADJ} = 0.1 to 2.1 V, six LEDs	0.33	1.5	3	A
Output power	—	—	18	36	W
PWM dimming range	60 Hz, six LEDs	—	900:1	—	—
SYSTEM CHARACTERISTICS					
Output overvoltage protection level	—	—	51	—	V
Overvoltage hysteresis	—	—	3	—	V
f_{SW} switching frequency		—	350	—	kHz
Efficiency	V_{IN} = 13 V, six LEDs at 1.5 A	—	87	—	%
	V_{IN} = 13 V, six LEDs at 3 A	—	84	—	
EMI (conducted)	—	CISPR-25 Class 3			
BASE BOARD CHARACTERISTICS					
Form factor	—	3.3"L × 2.5"W			
Number of layers	—	4			
Height	—	0.4"			

2 System Overview

2.1 Block Diagram

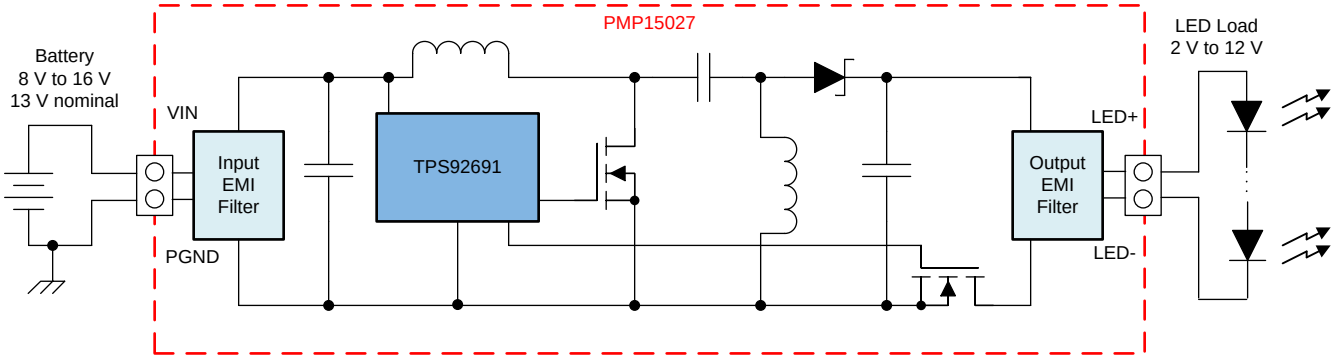


Figure 1. PMP15027 Block Diagram

2.2 Highlighted Products

2.2.1 TPS92691-Q1

The TPS92691 device is a versatile LED controller that can support a range of topologies. The device is intended for high-brightness LED lighting applications where efficiency, high accuracy, high power, and PWM or analog dimming (or both) are important. The device includes a gate driver for an external LED string disconnect FET to enable faster turnon and turnoff of the LED string for high contrast ratios.

Steady-state accuracy is aided by the inclusion of a low-offset rail-to-rail current sense amplifier that can directly measure LED current using either a high-side or a low-side series current sense resistor. LED current can be modulated using either analog dimming, PWM dimming, or both simultaneously. Other features include undervoltage lockout (UVLO), wide input voltage operation, open and overvoltage protection (OVP) operation, and wide-operating temperature range with thermal shutdown.

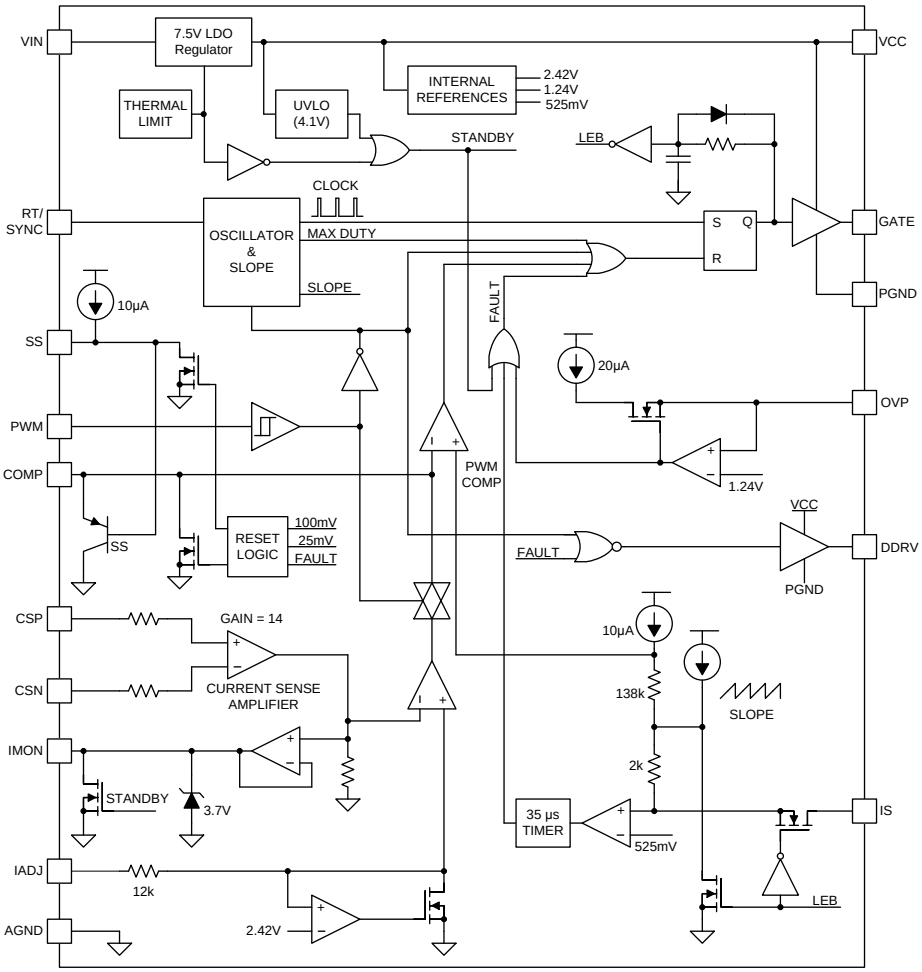


Figure 2. TPS92691 Block Diagram

The TPS92691 device has an operational input range up to 65 V. The device is available in a thermally enhanced 16-pin HTSSOP package.

Key features of this device include:

- Wide input voltage range: 4.5 V to 65 V
- Wide output voltage range: 2 V to 65 V
- Low input offset rail-to-rail current sense amplifier:
  - Better than ±3% LED current accuracy over 25°C to 140°C junction temperature range
  - Compatible with high-side and low-side current sense implementations
- High-impedance analog LED current adjust input (IADJ) with over 15:1 contrast ratio
- Over 1000:1 series FET PWM dimming ratio with integrated series N-Channel dim driver interface
- Continuous LED current monitor output for system fault detection and diagnoses
- Programmable switching frequency with external clock synchronization capability
- Programmable soft-start and slope compensation
- Comprehensive fault protection circuitry including VCC UVLO, output OVP, cycle-by-cycle switch current limit, and thermal protection
- TPS92691-Q1: Automotive Q100 Grade 1 qualified

2.3 System Design Theory

This reference design consists of a high-performance LED controller configured in a SEPIC (buck-boost with input to output isolation) topology with EMI filtering and a load disconnect FET for high slew rate PWM dimming (see Figure 3). The input voltage range is 8-V to 16-V nominal operation with the capability to run as low as 7 V for warm crank operation and as high as 42 V for load dump operation. This design supports up to 3 A of output current and an output power rating of up to 36 W maximum. The design is optimized to drive up to a 12-V IR or white LED string at 3 A from a typical voltage supply of 13 V. However, multiple combinations of input supplies and LED loads can easily be created using this reference design as a starting point. Standard recommended component values (such as the VCC capacitor) are not covered in this section.

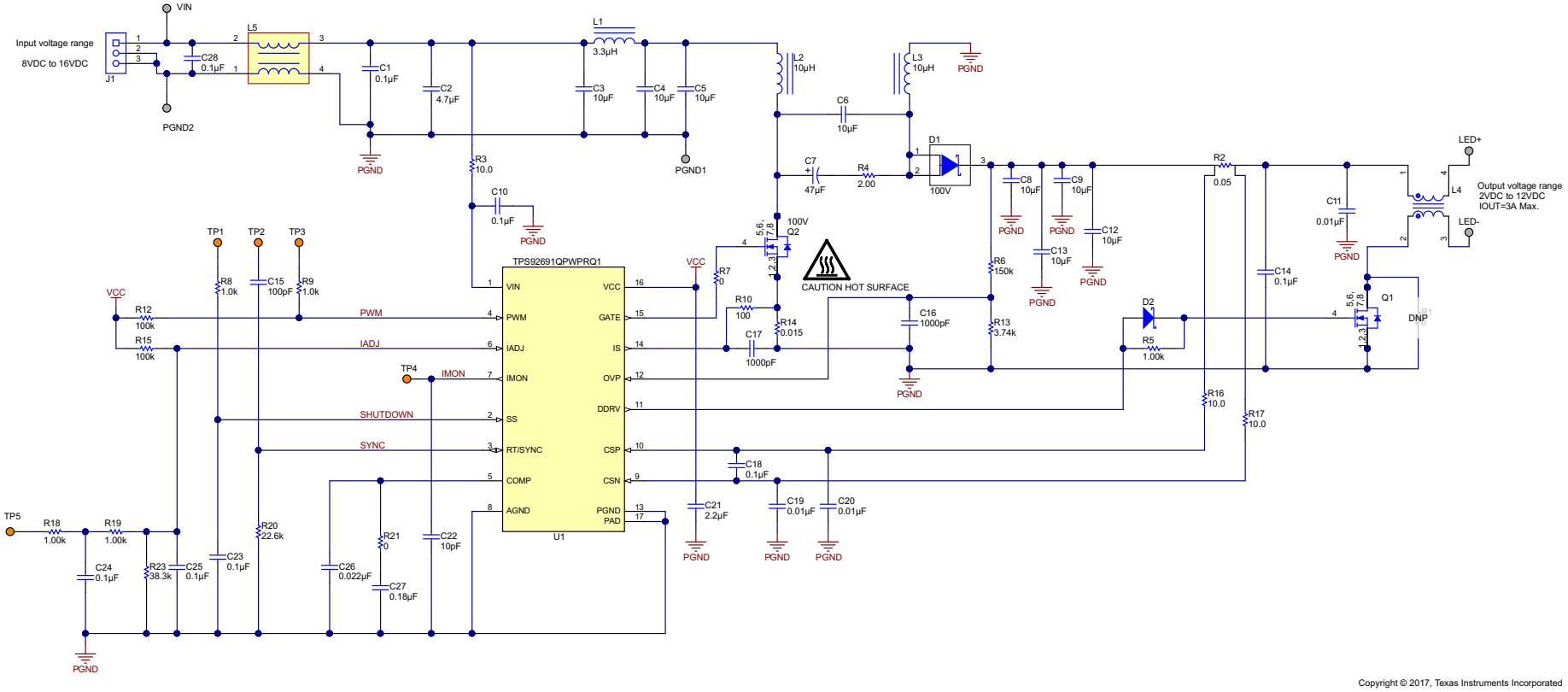


Figure 3. PMP15027 Schematic (R1 Not Populated for PWM Dimming)

Table 2. PMP15027 Bill of Materials

DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
C1, C10	2	0.1uF	C2012X7R2A104K	TDK	0.1 µF, 100 V, +/- 10%, X7R	0805
C2	1	4.7uF	C3225X7S2A475K200AE	TDK	4.7 µF, 100 V, +/- 10%, X7S	1210
C3, C4, C5, C6, C8, C9, C12, C13	8	10uF	CGA6P3X7S1H106K250AB	TDK	10 µF, 50 V, +/- 10%, X7S, AEC-Q200 Grade 1	1210
C7	1	47uF	EEE-FK1H470XP	Panasonic	47 µF, 50 V, +/- 20%, 0.68 ohm	SMT Radial D8
C11, C19, C20	3	0.01uF	C1608X8R2A103K	TDK	0.01 µF, 100 V, +/- 10%, X8R	0603
C14	1	0.1uF	C1210C104K5RACTU	Kemet	0.1 µF, 50 V, +/- 10%, X7R	1210
C15	1	100pF	C1608C0G1H101J	TDK	100 pF, 50 V, +/- 5%, C0G/NP0	0603
C16, C17	2	1000pF	C1608C0G2A102J	TDK	1000 pF, 100 V, +/- 5%, C0G/NP0	0603
C18	1	0.1uF	GRM188R72A104KA35D	MuRata	0.1 µF, 100 V, +/- 10%, X7R	0603
C21	1	2.2uF	C2012X7R1C225K	TDK	2.2 µF, 16 V, +/- 10%, X7R	0805
C22	1	10pF	C1608C0G1H100D	TDK	10 pF, 50 V, +/- 5%, C0G/NP0	0603
C23, C24, C25	3	0.1uF	C1608X8R1E104K	TDK	0.1 µF, 25 V, +/- 10%, X8R	0603
C26	1	0.022uF	GRM188R71C223KA01D	MuRata	0.022 µF, 16 V, +/- 10%, X7R	0603
C27	1	0.18uF	GRM21BR71C184KA01L	MuRata	0.18 µF, 16 V, +/- 10%, X7R	0805
C28	1	0.1uF	08055C104JAT2A	AVX	0.1 µF, 50 V, +/- 5%, X7R	0805
D1	1	100V	FSV8100V	Fairchild Semiconductor	Schottky, 100 V, 8 A, AEC-Q101	TO-277A
D2	1	30V	BAT54HT1G	ON Semiconductor	Schottky, 30 V, 0.2 A	SOD-323
L1	1	3.3uH	XAL6030-332MEB	Coilcraft	Inductor, 3.3 µH, 9.8 A, 0.02 ohm	IND_6.4x3.1x6.6
L2, L3	2	10uH	XAL1010-103MEB	Coilcraft	Inductor, 10 µH, 15.5 A, 0.01 ohm	Inductor, 11.3x10x10mm
L4	1		ACM7060-701-2PL-TL01	TDK Corporation	CMC 4A 2LN 700 OHM	Horizontal, 4 PC Pad
L5	1		ACM1211-102-2PL-TL01	TDK Corporation	Coupled inductor, 6 A, 0.014 ohm	SMD, 12x11mm
Q1, Q2	2	100V	STL8N10LF3	STMicroelectronics	MOSFET, N-CH, 100 V, 20 A, AEC-Q101	8-PowerVDFN
R2	1	0.05	LVK20R050DER	Ohmite	0.05, 0.5%, 0.75 W	2010 sense
R3	1	10.0	CRCW120610R0FKEA	Vishay-Dale	10.0, 1%, 0.25 W	1206
R4	1	2.00	ERJ-14BQF2R0U	Panasonic	2.00, 1%, 0.5 W, AEC-Q200 Grade 0	1210
R5, R18, R19	3	1.00k	CRCW06031K00FKEA	Vishay-Dale	1.00 k, 1%, 0.1 W	0603
R6	1	150k	CRCW0603150KFKEA	Vishay-Dale	150 k, 1%, 0.1 W	0603
R7, R21	2	0	CRCW06030000Z0EA	Vishay-Dale	0, 5%, 0.1 W	0603
R8, R9	2	1.0k	CRCW06031K00JNEA	Vishay-Dale	1.0 k, 5%, 0.1 W	0603
R10	1	100	CRCW0603100RFKEA	Vishay-Dale	100, 1%, 0.1 W	0603
R12, R15	2	100k	CRCW0603100KFKEA	Vishay-Dale	100 k, 1%, 0.1 W	0603

Table 2. PMP15027 Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
R13	1	3.74k	CRCW06033K74FKEA	Vishay-Dale	3.74 k, 1%, 0.1 W	0603
R14	1	0.015	CSRN2010FK15L0	Stackpole Electronics Inc	0.015, 1%, 1 W	2010
R16, R17	2	10.0	CRCW060310R0FKEA	Vishay-Dale	10.0, 1%, 0.1 W	0603
R20	1	22.6k	CRCW060322K6FKEA	Vishay-Dale	22.6 k, 1%, 0.1 W	0603
R23	1	38.3k	CRCW060338K3FKEA	Vishay-Dale	38.3 k, 1%, 0.1 W	0603
U1	1		TPS92691QPWPRQ1	Texas Instruments	Multi-Topology LED Driver with Rail-to-Rail Current Sense Amplifier	PWP0016J
R1	0	0	CRCW12060000Z0EA	Vishay-Dale	0, 5%, 0.25 W	1206

2.3.1 Design Procedure

The following subsections describe the design procedure used to calculate component values and ratings. These equations are based on the key specifications given in Table 1.

2.3.1.1 Operating Parameters—Duty Cycle

The typical operating duty cycle (D), the maximum operating duty cycle (D_{MAX}), and the minimum operating duty cycle (D_{MIN}) are required to calculate the inductor values. These values can be calculated using the following equations:

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}} = \frac{12\ V}{12\ V + 13\ V} = 0.48 \quad (1)$$

$$D_{MAX} = \frac{V_{OUT}}{V_{OUT} + V_{IN(MIN)}} = \frac{12\ V}{12\ V + 8\ V} = 0.6 \quad (2)$$

$$D_{MIN} = \frac{V_{OUT}}{V_{OUT} + V_{IN(MIN)}} = \frac{12\ V}{12\ V + 16\ V} = 0.43 \quad (3)$$

2.3.1.2 Setting the Switching Frequency

For this design, a switching frequency of 350 kHz is selected to keep the fundamental switching noise out of the AM band. The RT resistor (R20) can be calculated for 350 kHz using Equation 4:

$$R_T = \frac{1.432 \times 10^{10}}{(f_{SW})^{1.047}} = \frac{1.432 \times 10^{10}}{(350\ kHz)^{1.047}} = 22.45\ k\Omega \quad (4)$$

A value of 22.6 kΩ is selected for R20. Alternatively, a signal can be applied to TP2 to synchronize to an external clock frequency.

2.3.1.3 Inductor Value Calculation

The inductor value is calculated to ensure the circuit operates in continuous conduction mode (CCM) for a certain range of output currents at the typical operating points. In this design, the CCM to DCM boundary is set to 1/3 of the maximum output power, or a 1-A LED current with a 12-V LED load. As a result, this power boundary ($P_{O(BDRY)}$) is set for 12 W and the inductor values can be calculated using Equation 5 for two inductor SEPIC regulators:

$$L = \frac{1}{P_{O(BDRY)} \times f_{SW} \times \left(\frac{1}{V_{OUT}} + \frac{1}{V_{IN}}\right)^2} = \frac{1}{12\ W \times 350\ kHz \times \left(\frac{1}{12\ V} + \frac{1}{13\ V}\right)^2} = 9.27\ \mu H \quad (5)$$

Where f_{SW} is the switching frequency of the circuit. A value of 10 µH is selected for L2 and L3.

2.3.1.4 Peak Inductor Current

To determine the minimum saturation rating of the inductor current, the peak inductor current at the minimum input voltage must be known and the inductor sized accordingly. This peak inductor current can be calculated using the following equations for average current (I_L) and peak current ($I_{L(PK)}$):

$$I_L = \frac{P_{OUT(MAX)}}{V_{IN(MIN)} \times \eta} = \frac{36\ W}{8\ V \times 0.8} = 5.625\ A \quad (6)$$

$$I_{L(PK)} = I_L + \frac{V_{IN(MIN)} \times D_{MAX}}{2 \times L \times f_{SW}} = 5.625\ A + \frac{8\ V \times 0.6}{2 \times 10\ \mu H \times 350\ kHz} = 6.31\ A \quad (7)$$

Set the current limit and inductor saturation current rating above 6.31 A.

2.3.1.5 Peak Switch Current

In a SEPIC regulator, the peak switch current is the sum of the peak currents in each inductor. The peak inductor current for the second inductor can be found by calculating the peak-to-peak current ripple and adding half of that to the average current. The average current in the inductor is equal to the output current, which is 3 A maximum.

$$\Delta I_{L2\,(PP)} = \frac{V_{IN\,(MIN)} \times D_{MAX}}{L \times f_{SW}} = \frac{8\ V \times 0.6}{10\ \mu H \times 350\ kHz}\ 1.37\ A \tag{8}$$

Therefore, the peak switch current can be found using Equation 9:

$$I_{Q\,(PK)} = I_{L\,(PK)} + I_{LED} + \frac{I_{L2(PP)}}{2} = 6.31\ A + 3\ A + \frac{1.37\ A}{2}\ 10\ A \tag{9}$$

The current limit set using the IS pin must be set above 10 A to avoid faults.

2.3.1.6 Calculating R_{IS} (R14)

There are two equations for calculating R_{IS} depending on dominant factors. Due to the relatively high peak switch currents in this design, the equation based on current limit results in a much lower value. The value can be found using Equation 10:

$$R_{IS} = \frac{V_{IS(LIMIT)} - V_{SL} \times D_{MAX}}{I_{Q(PK)}} = \frac{525\ mV - 200\ mV \times 0.6}{10\ A} = 0.0195\ \Omega \tag{10}$$

For this design, a value of 0.015 Ω is selected for R14.

2.3.1.7 Calculate the Minimum SEPIC Capacitor Value

The SEPIC capacitor (C_S) value is based on a maximum voltage ripple that is based on the minimum input voltage. A maximum voltage ripple (ΔV_C) of 10% is recommended. This voltage ripple and the minimum SEPIC capacitor value can be found using the following equations:

$$\Delta V_C = 10\% \times V_{IN(MIN)} = 0.1 \times 8V = 0.8\ V \tag{11}$$

$$C_S = \frac{I_{LED(MAX)} \times D_{MAX}}{f_{SW} \times \Delta V_C} = \frac{3\ A \times 0.6}{350\ kHz \times 800\ mV} = 6.43\ \mu F \tag{12}$$

The calculated value is 6.43 µF minimum. A 10-µF capacitor is chosen for C6 in this design.

2.3.1.8 Minimum Output Capacitance

For this reference design, a maximum peak-to-peak LED ripple current ($\Delta I_{LED(PP)}$) of 50 mA or less is desired. Using the inductor current ripple and the LED string dynamic resistance, the minimum output capacitance can be calculated. For this example, the LED string designed for has a total dynamic resistance (R_D) of 3 Ω at 3 A of current.

$$C_{OUT} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times r_D \times \Delta i_{LED(PP)}} = \frac{3\ A \times 0.6}{350\ kHz \times 3\ \Omega \times 50\ mA} = 34.3\ \mu F \tag{13}$$

A total output capacitance (C8, C9, C12, C13) of 40 µF is used.

2.3.1.9 Minimum Input Capacitance

The worst case input voltage and current ripple occurs at the maximum input voltage. For this design, prepare a worst case input voltage ripple ($\Delta V_{IN(PP)}$) of 50 mV. The maximum input inductor current ripple and the minimum input capacitance required to achieve this can be found using the following equations:

$$\Delta I_{L\,(PP\,MAX)} = \frac{V_{IN\,(MIN)} \times D_{MIN}}{L \times f_{SW}} = \frac{16\ V \times 0.43}{10\ \mu H \times 350\ kHz} = 0.96\ A \tag{14}$$

$$C_{IN} = \frac{I_{L(PPMAX)}}{f_{SW} \times \Delta v_{IN(PP)} \times 8} = \frac{1.96\ A}{350\ kHz \times 50\ mV \times 8} = 14\ \mu F \tag{15}$$

This value is the minimum to achieve 50 mV of ripple. C4 and C5 are chosen to be 10-µF capacitors directly at the regulator input. To pass EMI requirements, additional filtering is required and the total input capacitance is greater.

2.3.1.10 Setting the LED Current

To lower the current sense resistor power dissipation and still keep a wide potential analog dimming range, a current sense voltage of 150 mV is used. To achieve this, 2.1 V (14 × 150 mV) is applied to the IADJ pin using a resistor divider (R15 and R33) from VCC. For a maximum of 3 A at a 150-mV current sense voltage, the current sense resistor value (R2) can be calculated using Equation 16:

$$R_{CS} = \frac{150\ mV}{I_{LED}} = \frac{150 mV}{3\ A} = 0.05\ \Omega \tag{16}$$

A 0.05-Ω, ¾-W resistor is chosen.

2.3.1.11 Soft-Start Capacitor

A soft-start time of approximately 8 ms is used for this design to reduce stress on the input supply and prevent startup overshoots. The soft-start capacitor can be calculated using Equation 17:

$$C_{SS} = 12.5 \times 10^{-6} \left(t_{SS} - \frac{C_{OUT} \times V_{OUT}}{I_{LED}} \right) = 12.5 \times 10^{-6} \left(8\ ms - \frac{40\ \mu F \times 12\ V}{3\ A} \right) = 98\ nF \tag{17}$$

A value of 100 nF is used in this design.

2.3.1.12 Overvoltage Protection (OVP)

To protect the switching FET, diode, and output capacitors during an output open-circuit event, OVP is used. The overvoltage trip point is set to 51 V with 3 V of hysteresis. First, R_{OV2} (R6) is calculated to determine the hysteresis, and then R_{OV1} (R13) is calculated for the correct trip point using the following equations:

$$R_{OV2} = \frac{V_{OV(HYS)}}{20\ \mu A} = \frac{3\ V}{20\ \mu A} = 150\ k\Omega \tag{18}$$

$$R_{OV1} = \left(\frac{1.24\ V}{V_{O(OV)} - 1.24\ V} \right) R_{OV2} = \left(\frac{1.24\ V}{51\ V - 1.24\ V} \right) 150\ k\Omega = 3.74\ k\Omega \tag{19}$$

The standard values of R6 = 150 kΩ and R13 = 3.74 kΩ are used.

2.3.1.13 Main N-Channel MOSFET Selection

The main switching FET (Q2) needs to be able to stand off the input voltage plus the output voltage, even during output OVP events. This FET must also have a sufficient current rating for this application. The minimum transistor voltage and current rating can be calculated using the following equations:

$$V_{DS} = 1.2 \times \left(V_{O(OV)} + V_{IN(MAX)} \right) = 1.2 \times (51\ V + 16\ V) = 80.4\ V \tag{20}$$

$$I_Q = I_{LED} + I_L = 3A + 5.625\ A = 8.625\ A \tag{21}$$

$$I_{Q(RMS)} = \sqrt{\int_0^{D_{MAX}} I_Q^2 dt} = 6.68\ A \tag{22}$$

A 100-V, 20-A Q-grade FET is chosen for the switching FET (Q2) and is also used for the PWM dimming FET (Q1).

2.3.1.14 Rectifier Diode Selection

The rectifier diode (D1) must also stand off the input voltage plus the output voltage and be rated for the maximum output current. These ratings can be calculated using the following equations:

$$V_{D(BR)} = 1.2 \times \left(V_{O(OV)} + V_{IN(MAX)}\right) = 1.2 \times (51\ V + 16\ V) = 80.4\ V \quad (23)$$

$$I_D = I_{LED(MAX)} = 3\ A \quad (24)$$

A 100-V, 8-A Q-grade schottky diode is chosen for D1.

2.3.2 Thermal Protection

Internal thermal protection circuitry protects the controller in the event of exceeding the maximum junction temperature. At 175°C, the converter typically shuts down, thus protecting all the circuitry in the reference design. The maximum junction temperature is a function of the system operating points (that is, efficiency, ambient temperature, and thermal management), component choices, and switching frequency.

2.3.3 Designing for Low EMI

2.3.3.1 EMI Performance

Figure 4 shows the passing conducted EMI scan for this design at a nominal 13-V input voltage and driving a 12-V LED load (that is, six IR LEDs in series) at 3 A of LED current. The blue trace is the peak scan, and the line labeled "C25Px" denotes the peak limits for CISPR-25 Class 3. The black trace is the average scan with the line labeled "C25Ax" denoting average limits for CISPR-25 Class 3. The scan covers the entire conducted frequency range of 150 kHz to 108 MHz. This is a pre-compliance test scan used for engineering development and evaluation and not a certified EMI test result. If an official EMI test result is required, it is the responsibility of the end-user to submit any design based on this reference design to a certified EMI lab.

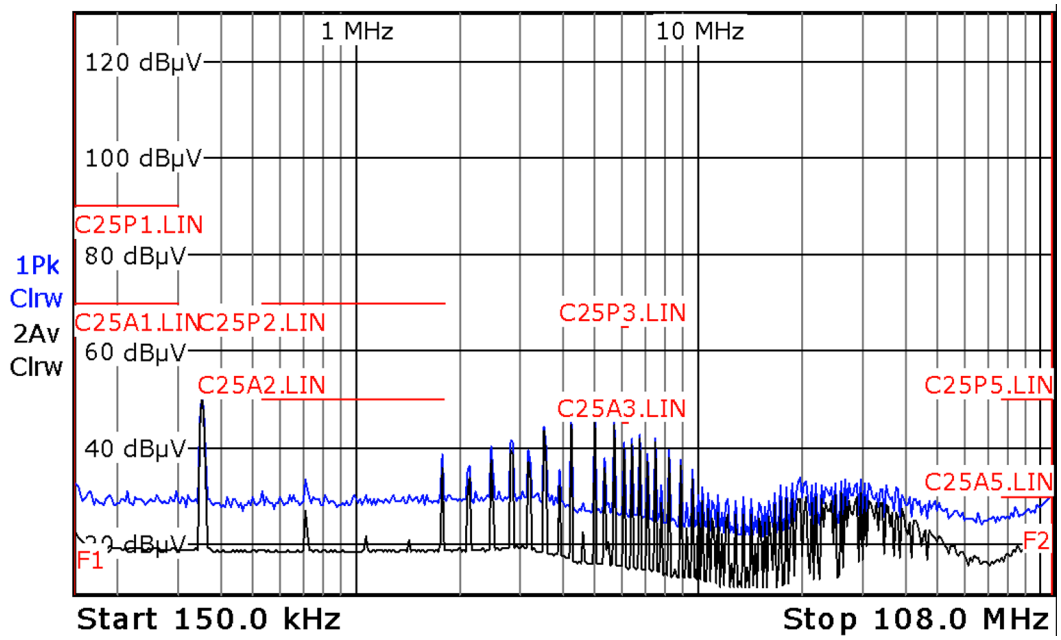


Figure 4. CISPR-25 Class 3 Conducted EMI Scan (C25Px: Peak Limits, C25Ax: Average Limits) V_{IN} = 13 V, V_F = 12 V, I_{LED} = 3 A (Pre-Compliance Data)

2.3.3.2 EMI Filter Design

The input EMI filter consists of a differential mode PI filter formed by the input capacitors (C1 through C3, C4, and C5) and the input inductor (L1). The primary purpose of the filter is to minimize EMI conducted from the circuit to prevent it from interfering with the electrical network supplying power to the LED driver. Frequencies in and around the switching frequency of the LED driver (that is, fundamental and harmonics) are primarily addressed with this filter, and the filter cutoff frequency is determined by the inductor and capacitor resonance. An input common-mode filter (L5) is also included to reduce high-frequency common-mode noise at 30 MHz and above.

Sufficient differential mode noise filtering on the output is generally provided by the output capacitor assuming low equivalent-series-resistance (ESR) ceramics are used as in this reference design for CISPR-25 class 3 conducted limits. A common-mode filter has also been added to the output (L4) to account for high frequencies with unknown loads. This may not be required in an end application depending on the load. This LED driver has been designed with the assumption that a connection to chassis ground is not available.

For more information on EMI filter design, see the application notes *AN-2162 Simple Success With Conducted EMI From DC-DC Converters* and *Input Filter Design for Switching Power Supplies*.

2.3.3.2.1 Additional EMI Considerations

Higher power levels may likely require increased EMI filtering to pass CISPR-25 class 3 limits. Options include increasing input capacitance or output capacitance (or both), adding ferrite bead resistance to mitigate high-frequency EMI, or increasing input and output choke inductance for common-mode noise reduction.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

This reference design does not feature any required hardware or software.

3.2 Testing and Results

3.2.1 Test Setup

Figure 5 shows the test setup. The input voltage was supplied by a DC power supply connected to the connector J1. The LED load is connected to the board using test points LED+ and LED–. Four digital multimeters (DMMs) measure input voltage, input current, output voltage, and output current. To enable PWM dimming, an external signal generator is connected to the PWM using test point TP3. For analog adjustment and dimming measurements, an external voltage supply is connected to the IADJ pin at TP5. TP5 also includes RC filtering so that PWM to analog dimming is possible if desired.

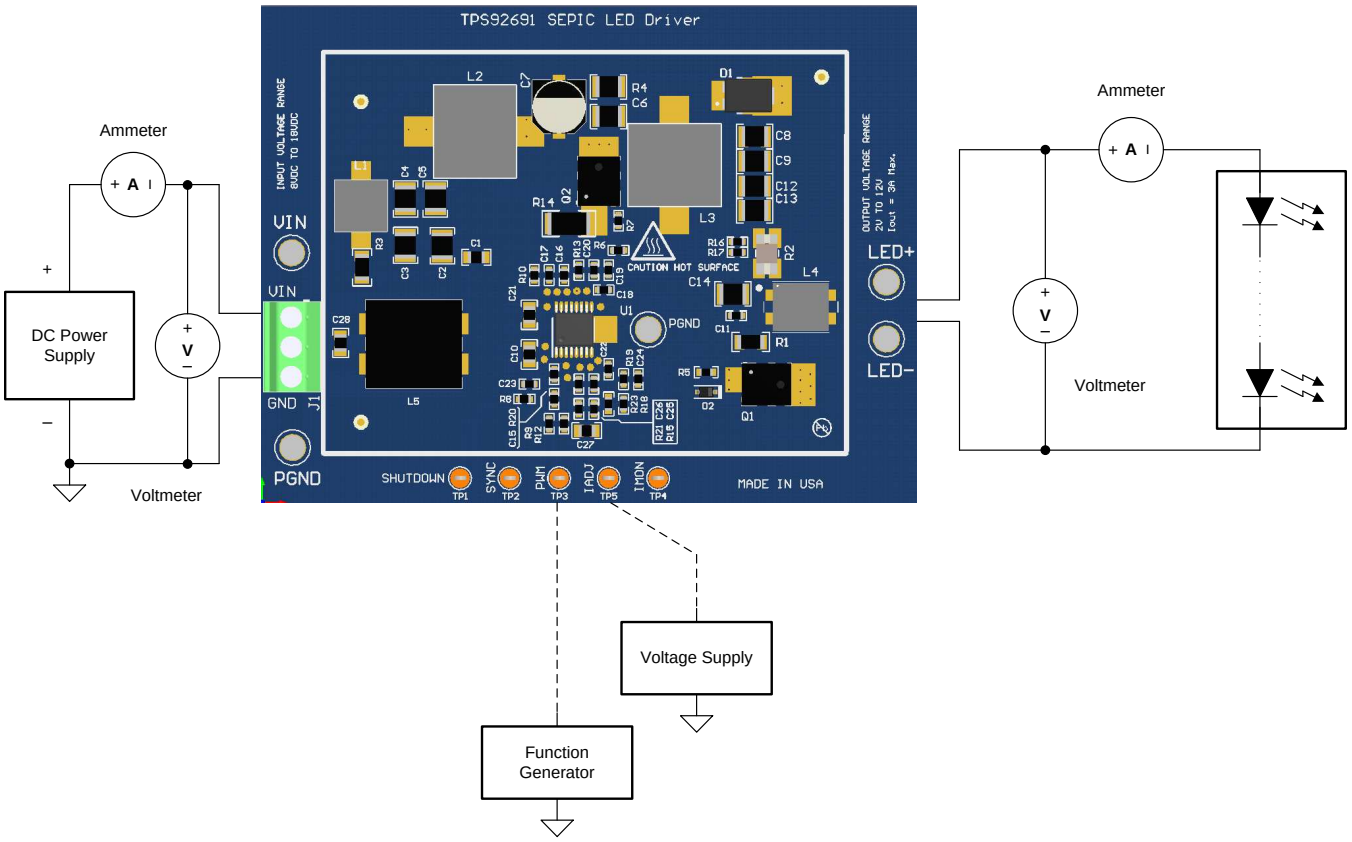


Figure 5. Test Setup Connections

3.2.2 Test Results

The test setup described in Figure 5 generates the following data for efficiency, analog dimming, and PWM dimming measurements. All graphs and oscilloscope shots are with an input of 13 V, six IR LEDs in series, and a nominal LED current of 3 A unless otherwise noted.

3.2.2.1 Nominal Operation Waveforms

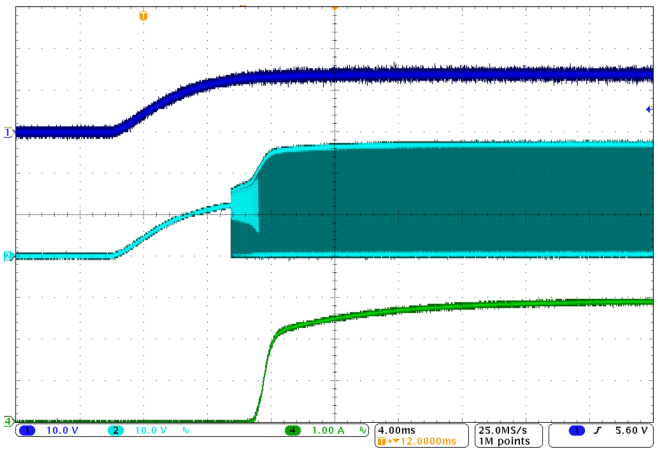


Figure 6. Startup—CH1: VIN, CH2: Switch Node (Q2 Drain) Voltage, and CH4: LED Current

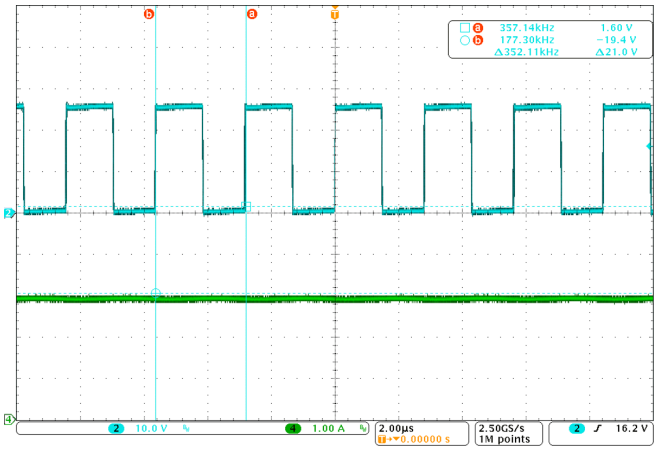


Figure 7. Steady State Switching—CH2: Switch Node (Q2 Drain) Voltage and CH4: LED Current

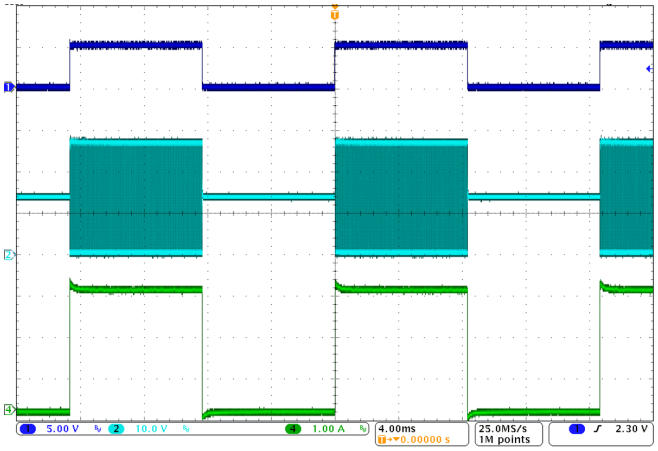


Figure 8. 60 Hz, 50% Duty Cycle PWM Dimming—CH1: PWM, CH2: Switch Node (Q2 Drain) Voltage, and CH4: LED Current

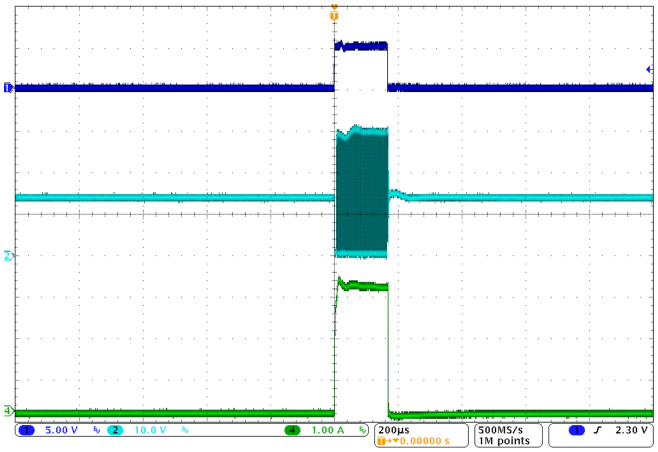


Figure 9. 60 Hz, 1% Duty Cycle PWM Dimming—CH1: PWM, CH2: Switch Node (Q2 Drain) Voltage, and CH4: LED Current

3.2.2.2 Efficiency and Line Regulation

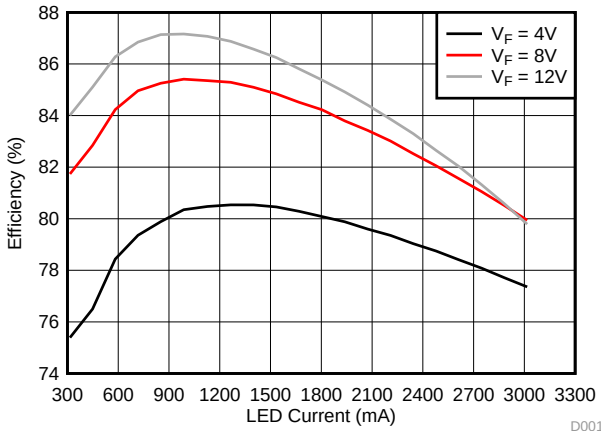


Figure 10. 9-V Input Efficiency versus LED Current

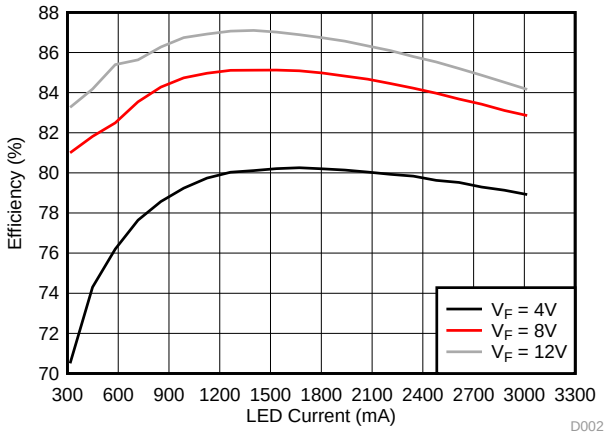


Figure 11. 13-V Input Efficiency versus LED Current

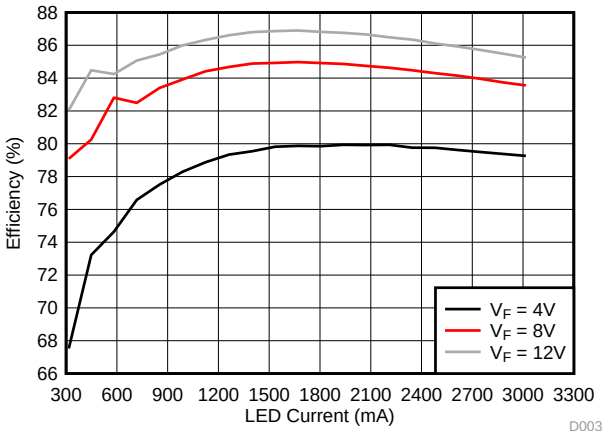


Figure 12. 16-V Input Efficiency versus LED Current

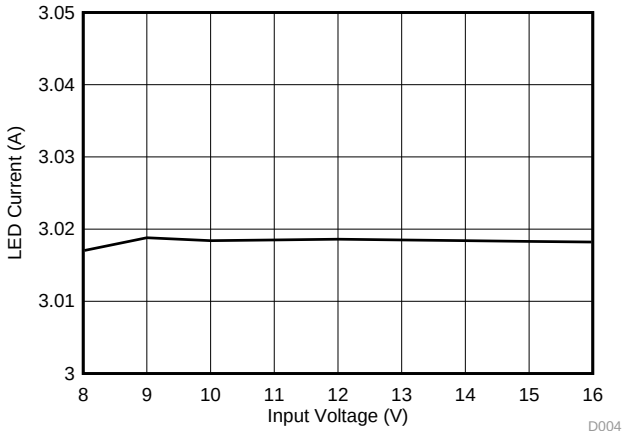


Figure 13. Line Regulation

3.2.2.3 Analog Dimming

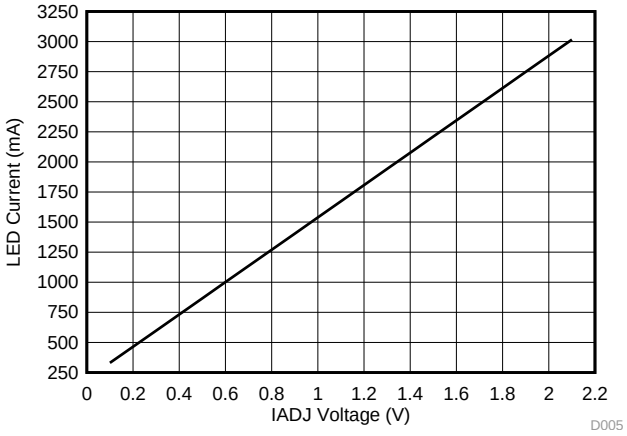


Figure 14. LED Current versus IADJ Voltage (IADJ Varied From 0.1 V to 2.1 V)

3.2.2.4 PWM Pin Dimming

For this reference design, a PWM frequency of 60 Hz is used, which, along with 30 Hz, is typical for ADAS systems. Dimming below 1% is possible at 60 Hz and even greater contrast ratios can be realized at 30 Hz.

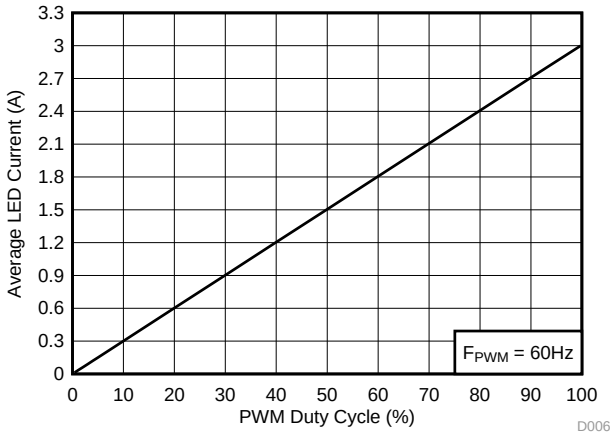


Figure 15. LED Current versus PWM Duty Cycle (0% to 100%)

3.2.2.5 Thermal Scan

Figure 16 shows a thermal scan of the board running at a room temperature (≈ 25°C) with no air flow. Table 3 lists measured temperatures of key components.

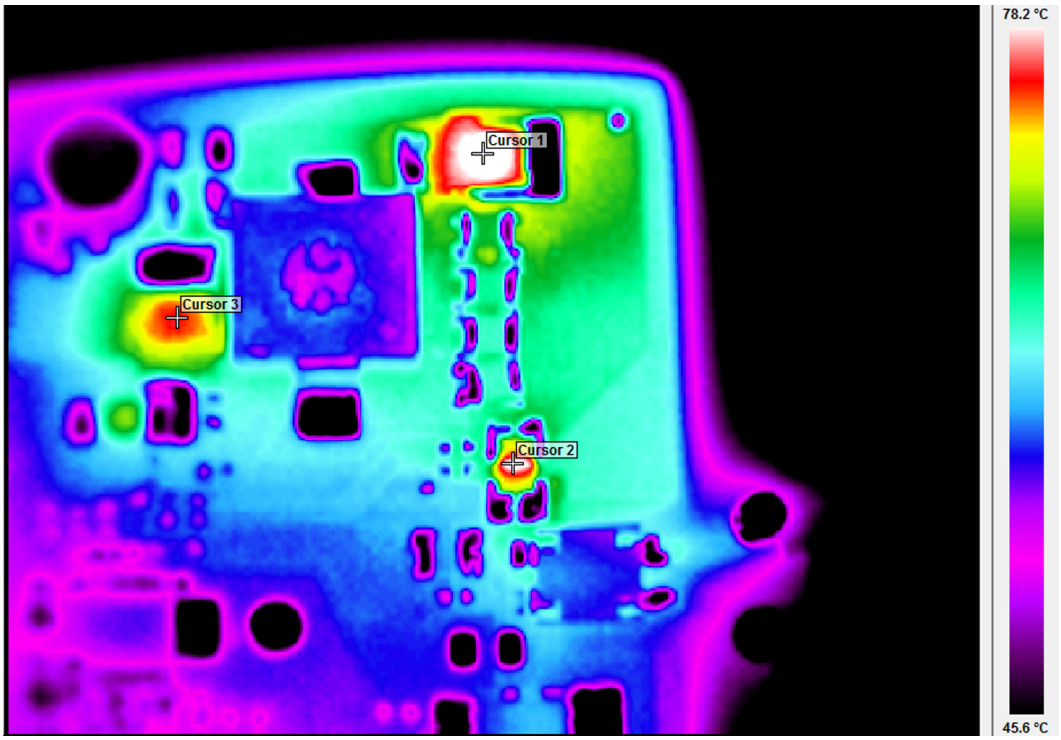


Figure 16. Thermal Scan—Top-View (Power Components): V_{IN} = 13 V, Six LEDs, I_{LED} = 3 A

Table 3. Component Temperatures

CURSOR	COMPONENT	TEMPERATURE (°C)
1	D1	81.2
2	R2	78.3
3	Q2	75.3

4 Design Files

4.1 Schematics

To download the schematics, see the design files at PMP15027.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at PMP15027.

4.3 Layout Prints

To download the layer plots, see the design files at PMP15027.

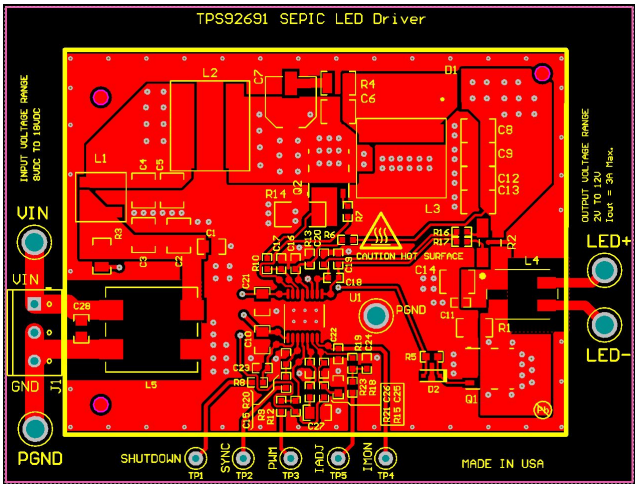


Figure 17. Top Layer

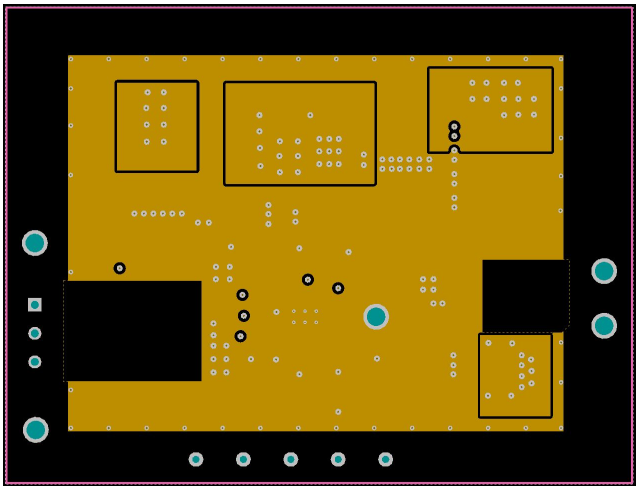


Figure 18. Middle Layer—Top

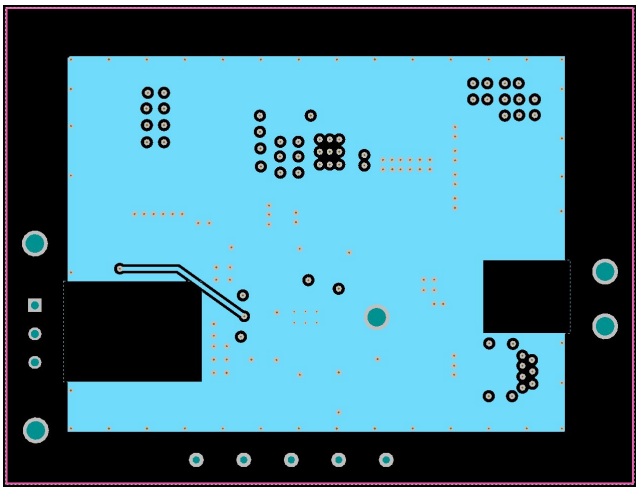


Figure 19. Middle Layer—Bottom

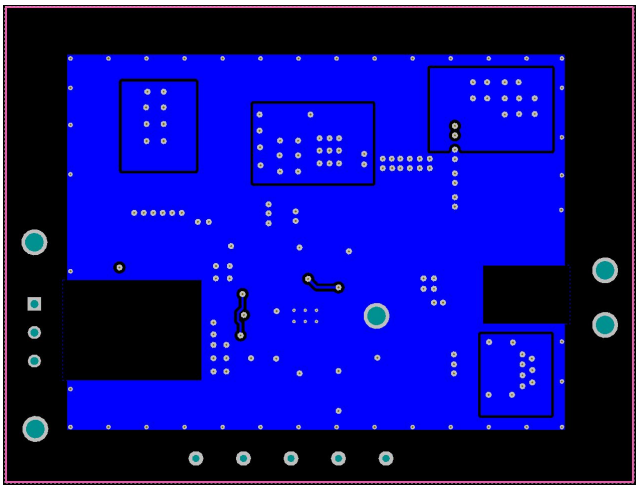


Figure 20. Bottom Layer

4.4 Altium Project

To download the Altium project files, see the design files at PMP15027.

4.5 Gerber Files

To download the Gerber files, see the design files at PMP15027.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at PMP15027.

5 Related Documentation

1. Texas Instruments, *TPS92691/TPS92691-Q1 Multi-Topology LED Driver With Rail-to-Rail Current Sense Amplifier Data Sheet*

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