TI Designs

Compact, Half-Bridge, Reinforced Isolated Gate Drive Reference Design

Description

The TIDA-01159 design provides a reference solution for half-bridge isolated gated drivers used in driving power stages of UPS, inverters, server and telecom applications.

This TI Design is based on the UCC21520 reinforced insulated gate driver from TI, and is capable of driving MOSFETs and SiC-FETs. The reference design contains a built-in isolated push-pull auxiliary power supply for powering the output of the isolated gate driver.

By bringing together the isolated gate driver and isolated power supply in a compact board with a form factor (30 mm × 35 mm), this reference design provides a fully tested robust half-bridge driver solution, capable of withstanding >100 kV/µs common-mode transient immunity (CMTI).

Resources

TIDA-01159	Design Folder
UCC21520	Product Folder
SN6505B	Product Folder

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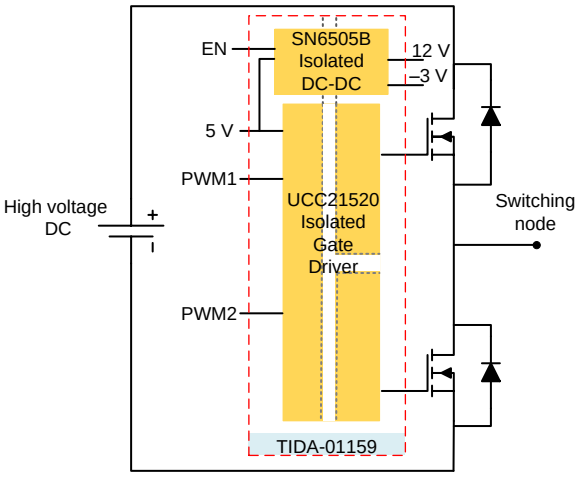
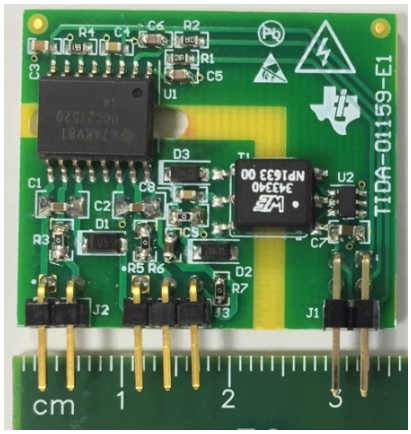
Features

- Compact Gate Drive Solution for Driving Power Stages Used in Mid- and High-Voltage Power Converters, Single-Phase and Three-Phase Inverters Operating From AC Input Voltage Range (100- to 690-V AC)
- High Driving Current (4-A Source and 6-A Sink) Suits Driving MOSFET / IGBT / SiC-FET With Currents up to 100 A and Operating Frequencies up to 2 MHz, Reducing Switching Losses Significantly
- Supports 3250-V_{PK} and 3000-V_{RMS} Basic Isolation
- Provides Very High CMTI of > 100 kV/µs for Robust Operation in Noisy Environments
- Flexible and Configurable Solution as a Dual Low-Side, Dual High-Side, High-Side/Low-Side, or Half-Bridge Driver
- Built-in Compact, High Efficient Isolated Supply to Power Output Side of Gate Driver
- Integrated Dead-Time in Gate Driver Improves Reliability

Applications

- Server PSUs and Telecom Rectifiers
- Uninterruptible Power Supplies (UPS)
- Industrial Power Supplies
- Battery Chargers
- Energy Storage Systems





1 System Overview

1.1 System Description

Any UPS or server power supply system makes use of many gate drivers supporting the main power conversion circuits. Many of the circuits used above 1 kW use bridge type power conversion stages. Examples are high-voltage DC/DC converters (phase shifted full bridge, LLC) used in telecom/server power supplies, bidirectional DC/DC converters (active bridges) in UPS systems, and so on. Depending upon the location of the controlling MCU, many of the power stages may also require isolation. The need for isolation can be due to a combination of safety requirements, avoidance of ground loops, and voltage level translation.

Considering the system requirements indicated above, a half-bridge isolated gate driver solution is a key element in systems performing kW level power conversion. This reference design is an attempt at optimizing gate drive performance in half/full bridge power stages. The benefits of this reference design in these applications include:

- Compact form factor gate drive solution
- Built-in isolated power supply allows flexibility in routing
- Excellent common-mode transient immunity (CMTI) performance ensuring reliable switching
- Hardware shoot-through/overlap protection ensures safe operation
- Reliability further enhanced by independent UVLO on low-side and high-side gate drive supplies
- Low propagation delay makes control easier especially at higher switching frequencies
- Efficient gate drive power supply ensures lower operating temperature

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Input supply voltage (V_{CCI})		4.5	5.0	5.5	V
PWM threshold (L to H)		1.6	1.8	2.0	V
PWM threshold (H to L)		0.8	1.0	1.2	V
OUTPUT CONDITIONS					
Gate drive voltage	V_{CCI}= 5 V	11.5	12.5	13.5	VDC
Source current	C_{VDD}= 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz	3.0	4.0	—	A
Sink current		5.0	6.0	—	A
Ensured dead-time	PWM inputs overlapping	80.0	100.0	120.0	ns
Propagation delay		—	38.0	50.0	ns
Driver PSU efficiency	V_{CCI} = 5 V, Load = 50 mA	80.0	85.0	—	%
SYSTEM CHARACTERISTICS					
CMTI		100	—	—	kV/µs
Operating ambient		–10	25	55	°C
Board size	Length × Width × Height	30×35×8			mm

1.3 Block Diagram

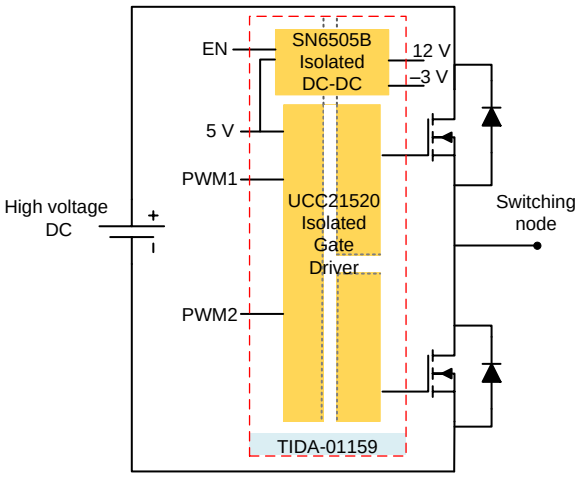


Figure 1. Block Diagram for Half-Bridge, Reinforced Isolated Gate Driver

Figure 1 shows the high-level block diagram of circuit. The main parts of this design are push-pull transformer driver (SN6505B) and isolated dual-channel gate driver (UCC21520).

1.4 Highlighted Products

This TIDA-01159 reference design features the following devices, which were selected based on their specifications. The key features of the highlighted products are mentioned as follows. For more information on each of these devices, see their respective product folders at http://www.TI.com or click on the links for the product folders on the first page of this reference design.

1.4.1 SN6505B

The SN6505 is a low-noise, low-EMI push-pull transformer driver, specifically designed for small form factor, isolated power supplies. It drives low-profile, center-tapped transformers from a 2.25- to 5-V DC power supply. Ultra-low noise and EMI are achieved by slew rate control of the output switch voltage and through spread spectrum clocking (SSC). The SN6505 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive ground referenced N-channel power switches. The device includes two 1-A power-MOSFET switches to ensure start-up under heavy loads. The switching clock can also be provided externally for accurate placement of switcher harmonics, or when operating with multiple transformer drivers. The internal protection features include a 1.7-A current limiting, undervoltage lockout (UVLO), thermal shutdown, and break-before-make circuitry.SN6505 includes a soft-start feature that prevents high inrush current during power up with large load capacitors.

1.4.2 UCC21520

The UCC21520 is an isolated dual-channel gate driver with a 4-A source and a 6-A sink peak current. It is designed to drive power MOSFETs, IGBTs, and SiC MOSFETs up to 5 MHz with best-in-class propagation delay and pulse-width distortion. The input side is isolated from the two output drivers by a 5.7-kV_{RMS} reinforced isolation barrier, with a minimum of 100 V/ns CMTI. Internal functional isolation between the two secondary-side drivers allows a working voltage of up to 1500-V DC. This driver can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver with programmable dead time (DT). A disable pin shuts down both outputs simultaneously when it is set high, and allows normal operation when left open or grounded. As a fail-safe measure, primary-side logic failures force both outputs low. The device accepts VDD supply voltages up to 25 V. A wide input VCCI range from 3 to 18 V makes the driver suitable for interfacing with both analog and digital controllers. All the supply voltage pins have UVLO protection. With all these advanced features, the UCC21520 enables high efficiency, high power density, and robustness in a wide variety of power applications.

2 System Design Theory

The design of the push-pull auxiliary supply and the gate driver are described in the following subsections.

2.1 Isolated Gate Driver Design

Isolated Gate Driver is required to drive two power switches in a half-bridge configuration. With high-voltage operation, it is necessary to have enough isolation between primary and secondary side of the gate driver. The UCC21520 is an isolated dual-channel gate driver with a 4-A source and a 6-A sink peak current. It is designed to drive power MOSFETs, IGBTs, and SiC MOSFETs up to 5 MHz with best-in-class propagation delay and pulse width distortion. The internal structure of the UCC21520 is shown in Figure 2.

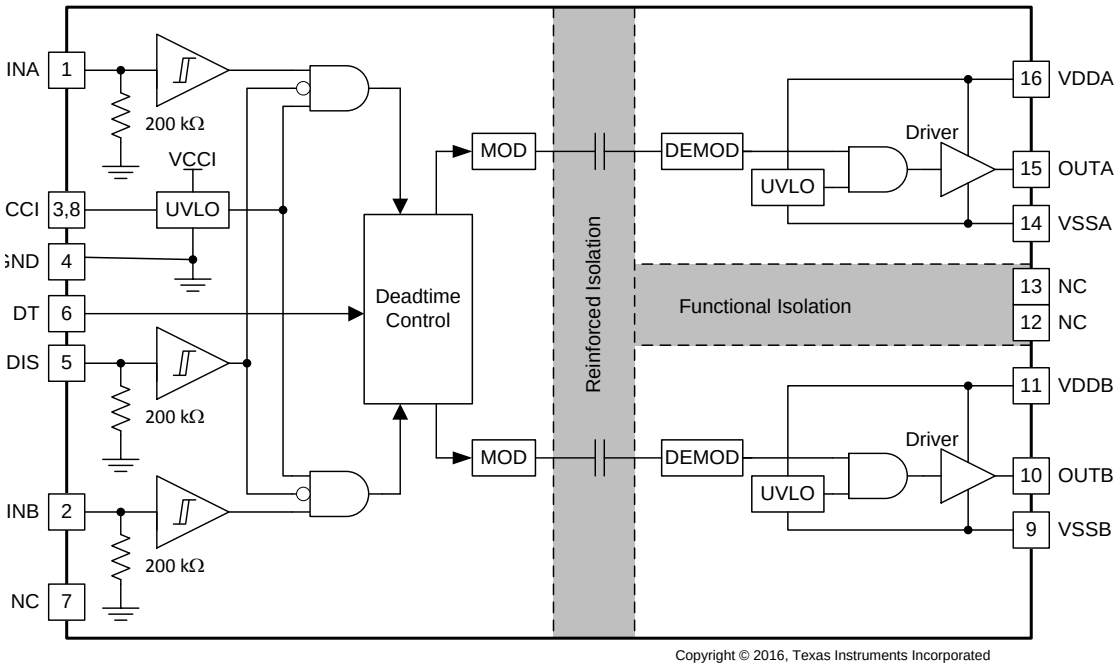


Figure 2. Internal Structure of UCC21520

Figure 3 shows the circuit for the UCC21520 and associated components implemented for half-bridge configuration.

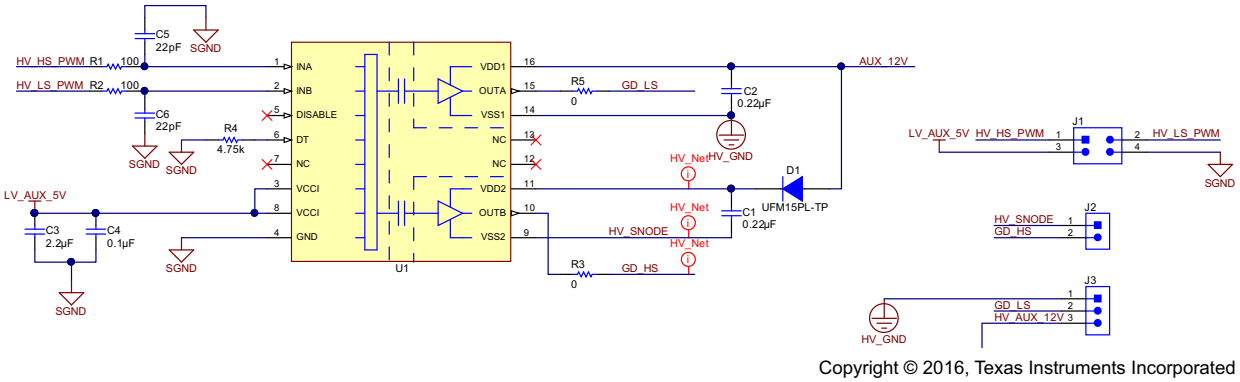


Figure 3. Isolated Gate Driver Design

This section goes into the details of the gate driver components dimensioning and power requirements. To calculate the required gate drive power and boost strap capacitor, the IPP60R190P6 is taken as an example.

2.1.1 Gate Driver Power Requirement

From the datasheet of the IPP60R190P6 MOSFET, Q_{GTOT} = 37 nC. In the TIDA-01159 design, the gate source voltage (V_{GS}) is 12.5 V.

Substituting in Equation 1:

$$P_{DRV} = Q_{GTOT} \times V_{GS} \times f_{SW} \quad (1)$$

$$P_{DRV} = 37\ nC \times 12.5\ V \times 200\ kHz = 92.5\ mW$$

The power consumed by the gate driver in driving the half-bridge stage is twice the P_{DRV}. Ideally, the power consumed by the gate driver for switching the bottom (synchronous) FET will be lower as it is soft-switched. But this not needed to estimate the power requirements of the gate driver.

The total power required by the gate driver is the sum of the power required to drive the half-bridge stage and the quiescent power consumption of the gate driver itself. This can be calculated using Equation 2:

$$P_{GDTOT} = 2 \times P_{DRV} + V_{VCCI} \times I_{VCCI} + V_{VDDA} \times I_{VDDA} + V_{VDDB} \times I_{VDDB} \quad (2)$$

Substituting the values from the datasheet into Equation 2:

$$P_{GDTOT} = 185\ mW + (5 \times 2.5)\ mW + (2 \times (12.5) \times 1.5)\ mW = 235\ mW$$

2.1.2 Bootstrap Power Supply for High-Side Gate Drivers

The high-side driver output –OUTB (Pin 10) is designed to drive a floating MOSFET (high-side). The gate voltage for the high-side driver is referenced to the floating node (HV_SNODE). Therefore, the gate voltage for the high-side driver is developed by a bootstrap circuit, which consists of a bootstrap diode (D1) and a bootstrap capacitor (C1) connected between VDD2 (Pin 11) and VSS2 (Pin 9) as shown in the Figure 3. When OUTA goes high, the low-side MOSFET turns on, the switch node (HV_SNODE) is pulled to ground and the bootstrap capacitor charges to VDD2 through the diode. When OUTB goes high, the high-side driver will begin to turn on the high-side MOSFET using the stored charge of the bootstrap capacitor. The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

The bootstrap capacitor must be sized to have more than enough energy to drive the gate of the high-side MOSFET without depleting the bootstrap capacitor more than 10%. A good guideline is to size C1(C_{BOOT}) to be at least 10 times as large as the equivalent MOSFET gate capacitance (C_G). C_G must be calculated based on the voltage driving the high-side gate of the MOSFET (V_{GS}) and the gate charge of the MOSFET (Q_G). $V_{GS}$is approximately the bias voltage supplied to V_{DD} after subtracting the forward voltage drop of the bootstrap diode D1 (V_{DBOOT}. In this design example, the estimated V_{GS} is approximately 10.8 V, as Equation 3 shows:

$$V_{GS} = V_{DD} - V_{DBOOT} \quad (3)$$

$$V_{GS} = 12.5\ V - 1.7\ V = 10.8\ V$$

The MOSFET used in this reference design has a specified Q_G of 37 nC. The equivalent gate capacitance of the MOSFET can be calculated as shown in Equation 4.

$$C_G = \frac{Q_G}{V_{GS}} \quad (4)$$

$$C_G = \frac{37\ nC}{10.8} = 3.43\ nF$$

After estimating the value for C_G, C_{BOOT} must be sized to at least ten times larger than C_G, as Equation 5 shows.

$$C_{BOOT} \geq 10 \times C_G \quad (5)$$

$$C_{BOOT} = 10 \times 3.43\ nF = 0.0343\ \mu F$$

For this reference design, a 0.22-µF capacitor has been chosen for the bootstrap capacitor.

2.1.3 Selection of Bootstrap Diode

The voltage that the bootstrap diode encounters is the same as the full DC bus voltage (in this case a maximum of 400-V DC). The bootstrap diode voltage rating must be greater than the DC bus rail voltage. The bootstrap diode must be a fast recovery diode to minimize the recovery charge and thereby the charge that feeds from the bootstrap capacitor to the 12-V supply. This TIDA-01159 reference design uses a 600-V, 1-A UFM15PL-TP diode.

The bootstrap diode power dissipation (P_{DBOOT}) can be estimated based on the switching frequency, diode forward voltage drop, and the switching frequency of the PWM signal (f_{SW}). In this reference design, the switching frequency has been set to 200 kHz. Equation 6 calculates the estimated power loss for the bootstrap diode.

$$P = \frac{1}{2} \times Q_G \times V_{DBOOT} \times f_{SW} \tag{6}$$

$$P = \frac{1}{2} \times 37\ nC \times 1.7\ V \times 200\ kHz = 6.29\ mW$$

2.1.4 PWM Inputs

PWM signals "HV_HS_PWM" and "HV_LS_PWM" are given to INA (Pin 1) and INB (Pin 2), respectively.

2.1.5 Dead Time Control

The UCC21520 has a programmable dead time function using the DT pin. Tying DT to VCCI allows the outputs to overlap. Leaving DT floating sets the dead time to < 15 ns.Placing a 500-Ω to 500-kΩ resistor between DT and GND adjusts dead time according to Equation 7.

$$DT(ns) = 10 \times R_{DT}(\text{in k}\Omega) \tag{7}$$

A 12-kΩ resistor connected between DT pin and GND pin sets the dead time to 120 ns as per Equation 7. This resistor must be selected for 1% tolerance to prevent any drift in the dead time.

An input signal's falling edge activates the programmed dead time for the other signal. The output signals' dead time is always set to the longer of either the driver's programmed dead time or the input signal's own dead time. If both inputs are high simultaneously, both outputs will immediately be set low. This feature is used to prevent shoot-through, and it does not affect the programmed dead time setting for normal operation.

2.2 Isolated Auxiliary Push-Pull Power Supply

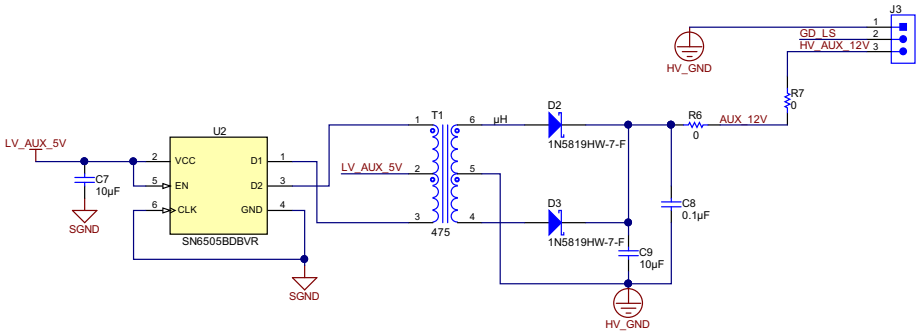


Figure 4. Isolated Power Supply Based on Push-Pull Topology

The auxiliary power supply input and output parameters are mentioned inTable 2.

Table 2. Transformer Requirements

PARAMETER	SPECIFICATION
V_{IN}	5 V
V_{OUT}	12.5 V
Output power	1 W
Output ripple	200 mV pk-pk
Switching frequency	420 kHz

2.2.1 Push-Pull Transformer Design

The important parameters that need to calculated for the push-pull transformer are

1. Turns Ratio (Ns/Np)
2. Volt Sec product
3. Primary current carrying capability

To calculate the turns ratio, the nominal input voltage is taken to be V_{NOM} = 5 V.

Assuming a 85% efficiency for the push-pull stage, the primary current I_{PRI} can be calculated using the Equation 8.

$$I_{PRI} = \frac{P_{OUT}}{(\eta \times V_{NOM})} \tag{8}$$

$$I_{PRI} = \frac{1}{(0.85 \times 5)} = 235 \text{ mA}$$

The voltage appearing across the primary of the transformer when one of the push-pull FET is switched on is calculated using Equation 9.

$$V_{PRI} = V_{NOM} - I_{PRI} \times R_{DSon} - I_{PRI} \times DCR \tag{9}$$

$$V_{PRI} = 5 - 0.235 \times (0.16 + 0.15) = 4.927 \text{ V}$$

The required reflected voltage across the secondary winding of the transformer is given by Equation 10.

$$V_{SEC} = V_{OUT} + V_{FDROP} \tag{10}$$

From Equation 9 and Equation 10, the turns ration Ns/Np can be calculated from Equation 11.

$$\frac{N_S}{N_P} = \frac{V_{SEC}}{V_{PRI}} \tag{11}$$

$$\frac{N_S}{N_P} = \frac{12.8}{4.927} = 2.597$$

The minimum required volt second product of the transformer can be calculated using Equation 12.

$$V_{Tmin} \geq V_{PRImax} \times T_{max} \times D_{max} \geq V_{PRImax} \times \frac{D_{max}}{F_{min}} \tag{12}$$

The V_{PRImax} is assumed to be 1.05 times the V_{NOM}. V_{PRImax} = 1.05 × 5 = 5.25 V.

Because the SN6505B operates with a fixed duty cycle of 50%, the D_{max} is taken as 0.5.

The minimum switching frequency of the SN6505B when using the internal oscillator can be obtained from the datasheet. F_{min} = 363 kHz.

Substituting the values in Equation 12:

$$V_{Tmin} \geq 5.25 \times \frac{0.5}{363000} = 7.23\ V\mu s$$

A transformer from Wurth (750343341) with 1:2.6 turns ratio is chosen for this TI Design.

2.2.2 Rectifier Diode Selection

To increase the efficiency of the push-pull forward converter, the forward voltage drop of the secondary side rectifier diodes should be as small as possible. Also, as the SN6505B is a high frequency switching converter, the diode must possess a short recovery time. Schottky diodes are selected as they meet the requirements of low forward voltage drop and fast recovery time. The diode must also withstand a reverse voltage of twice the output voltage.

This TI Design uses a 40-V, 1-A Schottky diode (D2, D3).

3 Getting Started Hardware

This section explains the top and bottom views of the PCB for the TIDA-01159 showing all the different sections. It also explains the power supply requirement and connectors used to connect the external world. The test setup needed to validate the board is also discussed.

3.1 TIDA-01159 PCB Overview

Figure 5 shows the top view of the TIDA-01159 PCB.

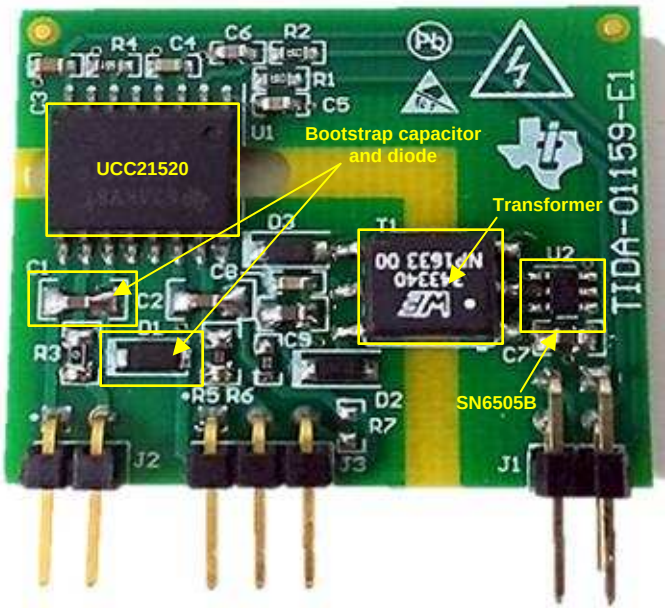


Figure 5. Top View of TIDA-01159

Figure 6 shows the bottom view of the TIDA-01159 PCB.

Figure 6. Bottom View of TIDA-01159

Figure 7 shows how the C2000™ Piccolo™ LaunchPad™ is connected to the connector J1. This is used to generate PWM inputs (high side and low side) for testing the gate driver.

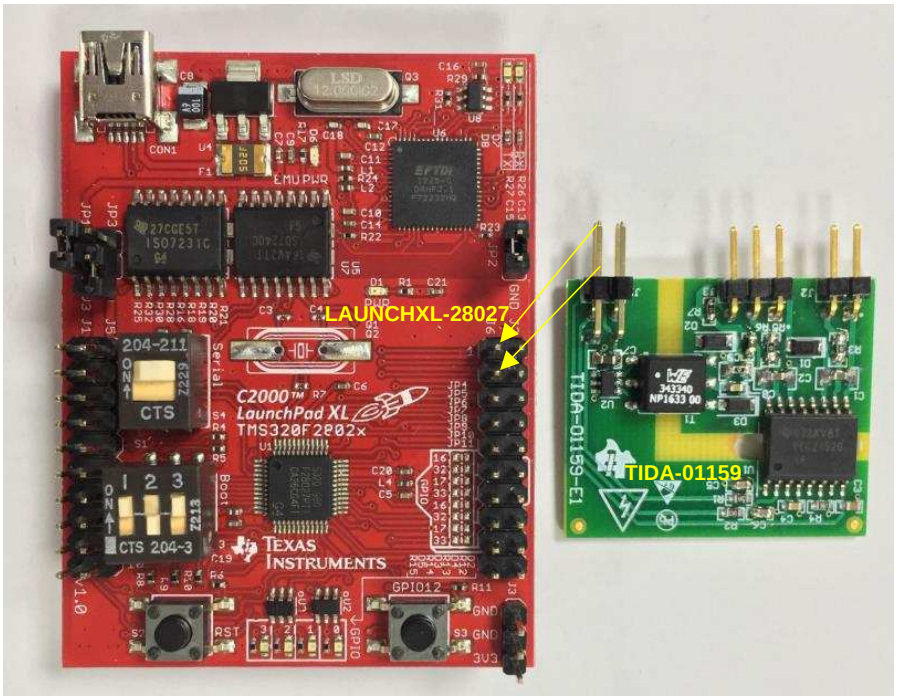


Figure 7. Connecting C2000 Piccolo LaunchPad Board to TIDA-01159

3.2 Connectors

Table 3 shows the connectors used on the TIDA-01159 PCB and their purposes.

Table 3. Connectors

CONNECTOR	PURPOSE
J1	High-voltage high-side PWM, high-voltage low-side PWM, low-voltage auxiliary 5 V, ground
J2	High-voltage switch node, gate driver high-side
J3	High-voltage ground, gate driver low side, high-voltage auxiliary 12 V

3.3 Test Setup

In order to test the TIDA-01159 board a half-bridge power stage is used. A top-level representation of the test setup is shown in Figure 8.

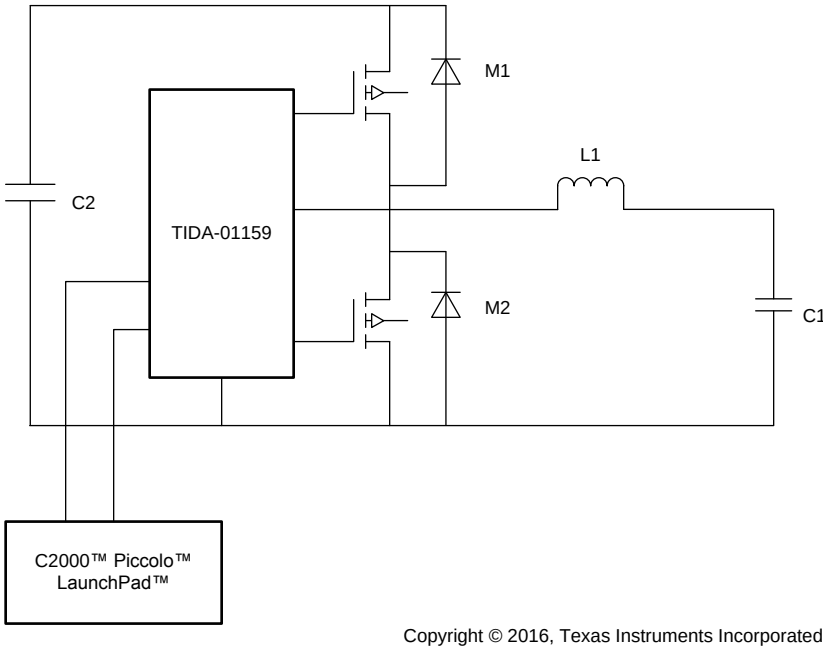


Figure 8. Test Setup for TIDA-01159

The TIDA-01159 is connected to the half-bridge power stage comprising of MOSFET M1 and M2, the inductor L1, and capacitors C1 and C2. The high-side gate drive output of the TIDA-01159 is connected to the MOSFET M1, and the low-side output of the TIDA-01159 is connected to MOSFET M2. The C2000 Piccolo LaunchPad is used to generate two PWM signals for driving the half-bridge power stage. The PWM input signals are fed to the input pins of the TIDA-01159.

3.4 Test Equipment Needed to Validate the Board

- DC source: 0- to 400-V DC, 2 A rated
- DC source : 0 10 V, 200 mA
- Four-channel digital oscilloscope
- Current probe: 0 to 30 A, 50 MHz
- Electronic or resistive load capable of working up to 400 V, 2 A
- C2000 LaunchPad or other source for generating complementary PWM

3.5 Test Conditions

3.5.1 Input

The half-bridge power stage needs to be powered from the 0- to 450-V DC power stage. The 0- to 10-V power source used as the auxiliary power supply to power the TIDA-01159 board.

3.5.2 Output

The output of the half-bridge power stage is connected to the electronic load or resistive load. The load must be capable of varying from 0 to 2 A.

3.5.3 Signal

A complementary PWM signal with configurable dead time, duty cycle, and frequency needs to be connected to the input of the TIDA-01159 board.

3.6 Test Procedure

1. Set the 0- to 10-V auxiliary supply to 5 V with a current limit of 200 mA and connect it to J1 pin 3 (5 V)and pin 4 (GND) of the TIDA-01159 board.
2. Connect the complementary PWM generated from a C2000 LaunchPad or any other source to pin 1 and pin 2 of the TIDA-01159 board.
3. Connect the 0- to 400-V DC power supply to the half-bridge input.
4. Connect the electronic or resistive load to the half-bridge output.
5. Power up the 0- to 400-V DC power supply to 100 V.
6. Slowly increase the electronic or resistive load to about 100 mA.
7. Increase the 0- to 400-V DC power supply to 400 V.
8. Increase the electronic or resistive load to about 1 A.
9. Capture the switching waveforms in the oscilloscope.

4 Testing and Results

This section shows the test results for TIDA-01159. To see the test conditions, see Section 3.3.

4.1 CMTI Waveforms

This section shows the CMTI test results. The CMTI test is important to characterize the immunity of the gate drive when it experiences high dv/dt transients. In a half-bridge gate driver, the switching node experiences high dv/dt, which can then couple to the gate driver's input pins and distort the PWM signal. Therefore, it is important to have high dv/dt immunity.

For this test, both the inputs (pin 1 and pin 2 of UCC21520) were tied to VCC and a transient pulse was applied across the isolated grounds with the test port. During the test, the slew rate of the transient was increased and change in the output state was observed.

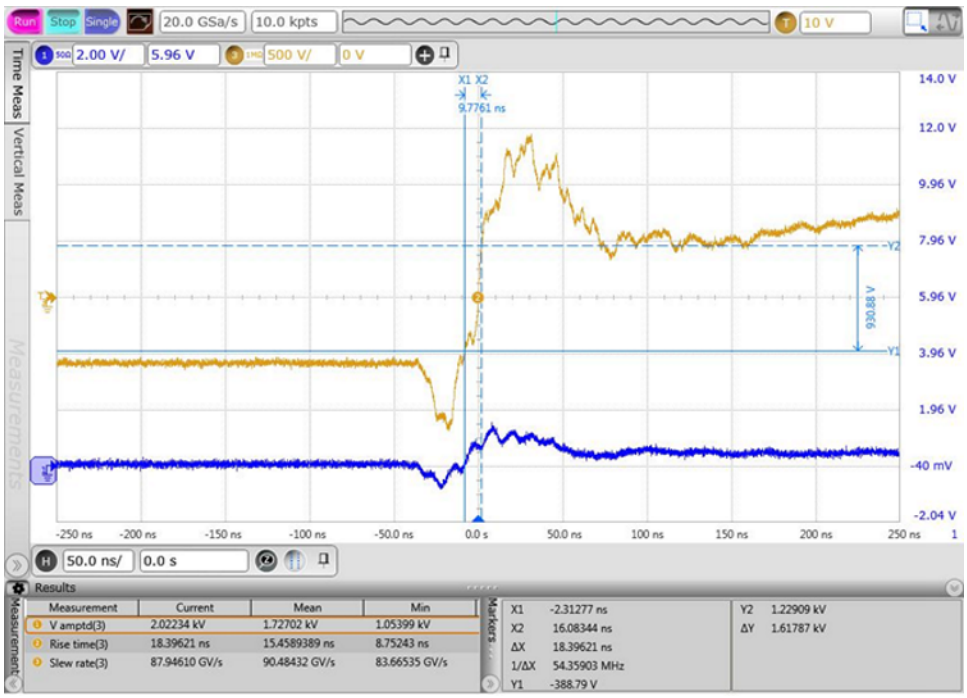


Figure 9. CMTI 87 kV/µs

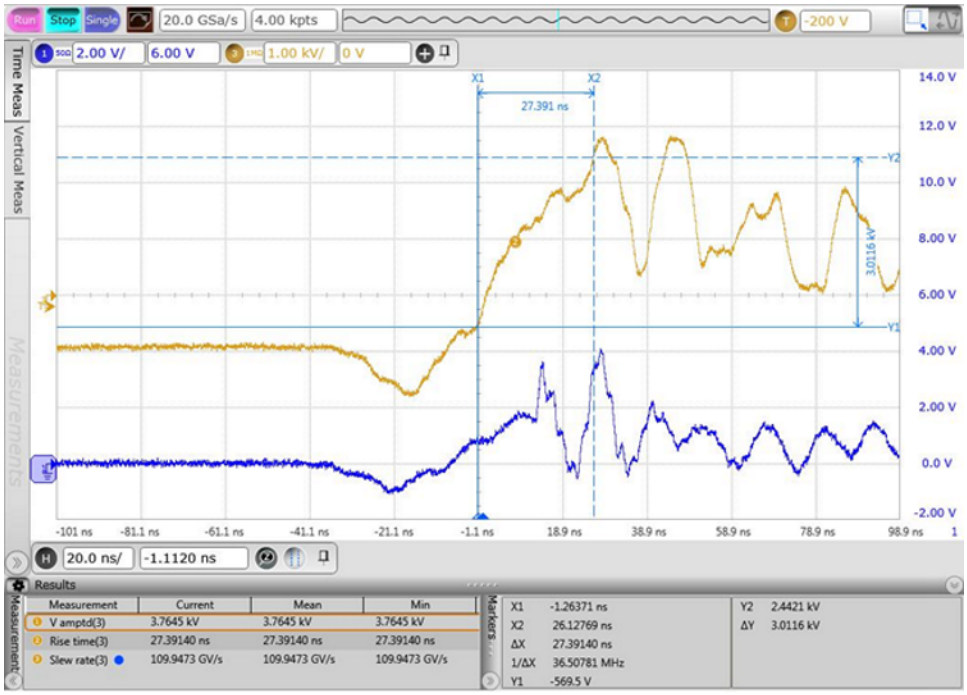


Figure 10. CMTI 109 kV/µs

In the waveforms shown in Figure 9 and Figure 10, the blue trace is the CMTI pulse applied and the yellow trace is the low-side gate drive output. The output does not go high even when a CMTI pulse of > 100 kV/µs is applied.

4.2 Propagation Delay Waveforms

Figure 11 and Figure 12 show the turnon and turnoff propagation delays measured for the low-side gate driver. A propagation delay of 38 ns is seen. This propagation delay also takes into account the RC filter connected at the input PWM pins.

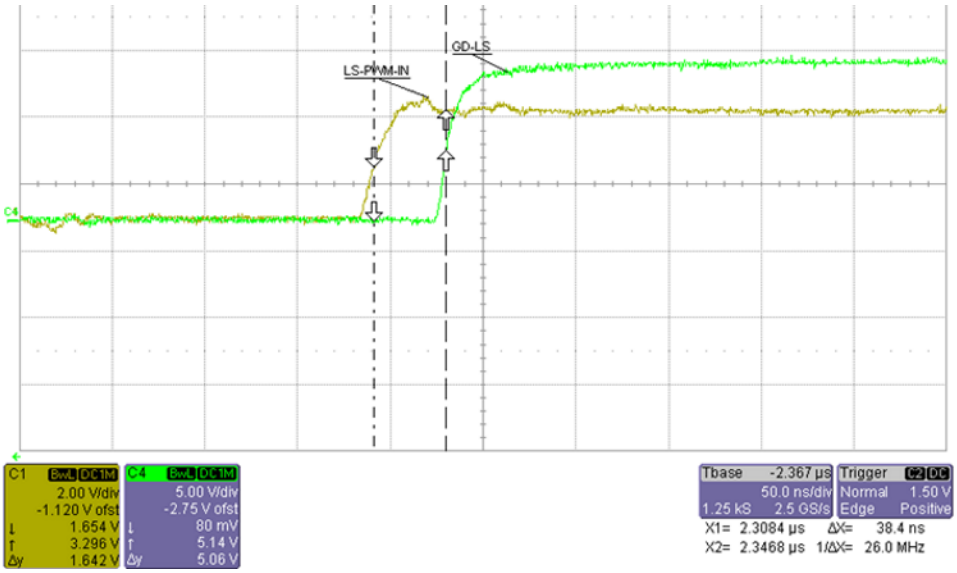


Figure 11. Turnon Propagation Delay

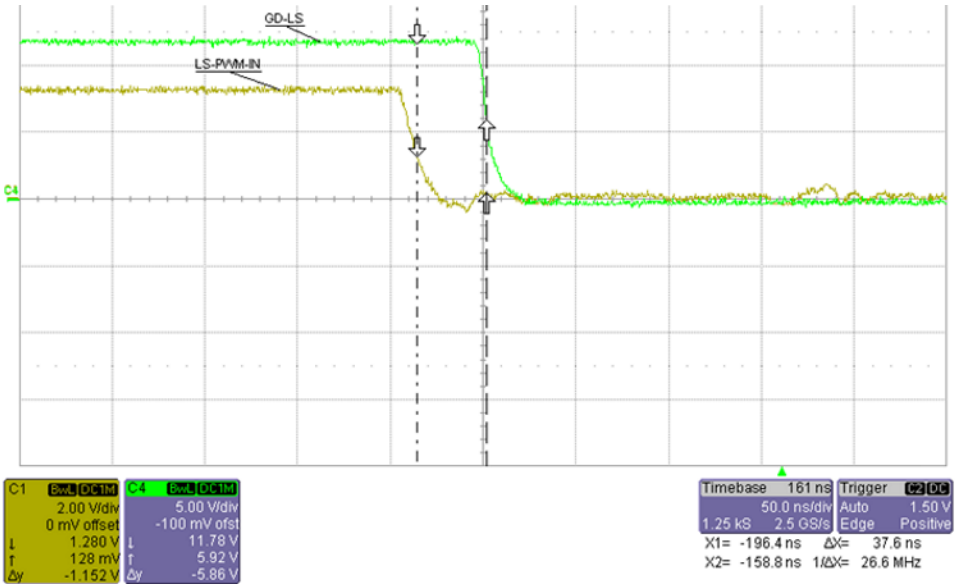


Figure 12. Turnoff Propagation Delay

4.3 Hardware Overlap Protection and Dead Time Insertion

Figure 13 shows the hardware overlap avoidance of UCC21520. This is critical to ensure that there is no overlap of the outputs and is an important feature to avoid short circuit in half-bride stages. The yellow and red waveform show the PWM inputs. The blue and green waveform show the PWM outputs. When the PWM inputs are overlapping, both the outputs go low.

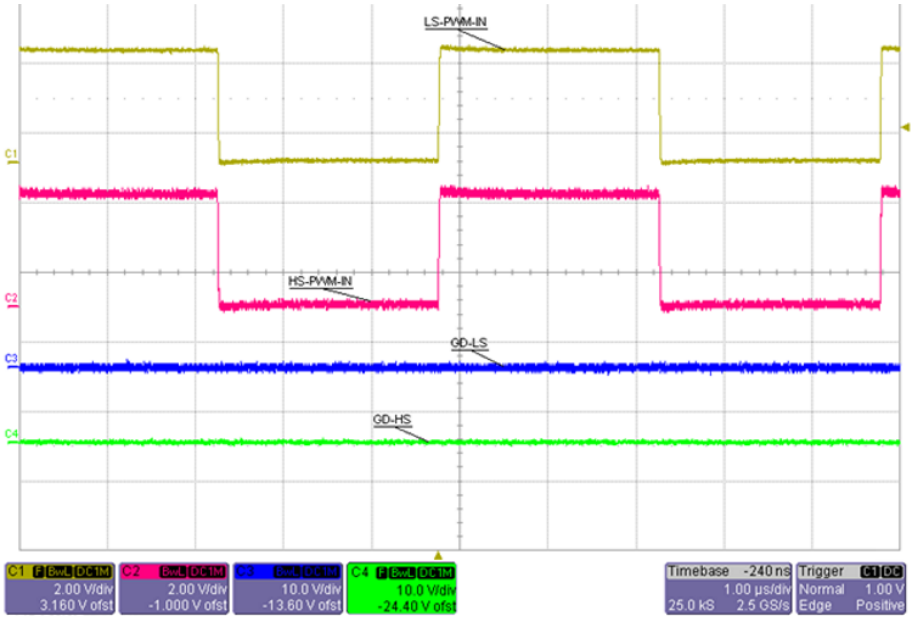


Figure 13. Hardware Overlap Avoidance

Figure 14 shows the programmable hardware dead time insertion feature of the UCC21520. This feature adds a level of protection to the half-bridge stage as it helps in avoiding shoot-through. For this test, a hardware dead time of 114 ns has been set. The input PWM signals do not have a dead time. This is shown by the red and yellow trace. The UCC21520 inserts the dead time in the gate drive outputs as shown in Figure 14. The green and blue traces show the hardware dead time insertion. This dead time can be programmed as explained in Section 2.1.5.

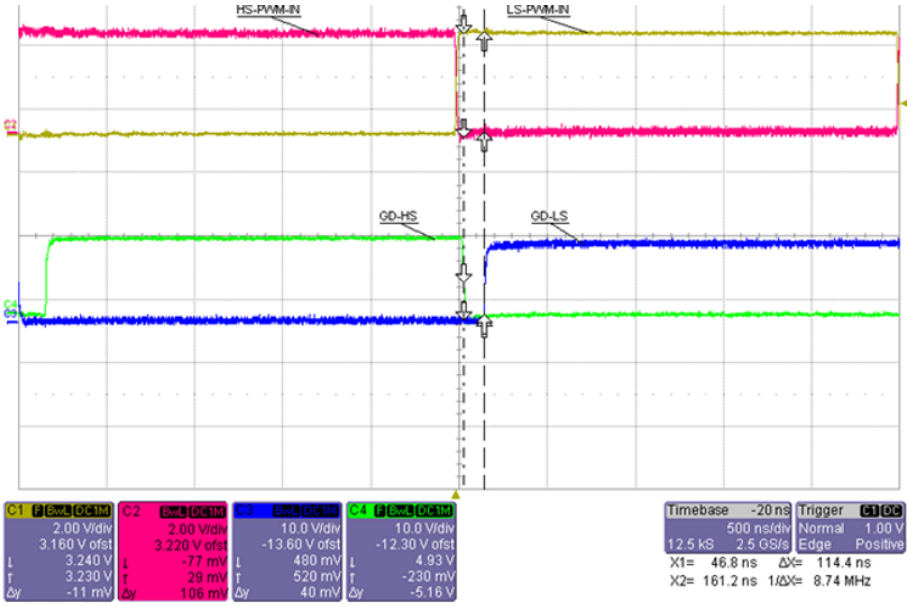


Figure 14. Hardware Dead Time Insertion

4.4 Gate Drive Current Test

Figure 15 shows the gate drive current test for a 47-nF load at a 200-kHz switching frequency. The yellow waveform is the low-side gate driver input and the pink waveform is the gate driver current. The gate drive source current reaches > 3 A and sink current is > 5 A. The gate drive current in the actual system will be higher than the observed waveform.

Figure 15. Gate Drive Current Test

4.5 Switching Node Waveform (Low Side)

Figure 16 and Figure 17 show the switching node waveforms of low-side gate driver. The pink waveform is the low-side gate driver input, the blue waveform is the drain-to-source voltage for the low-side driven MOSFET, and the green waveform is the half-bridge inductor current.

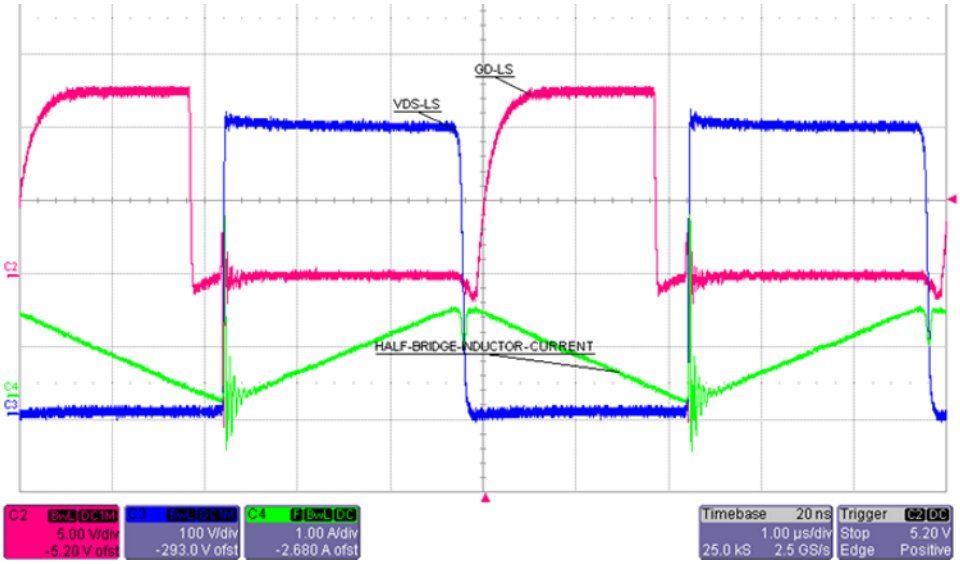


Figure 16. Low-Side Switching Waveform

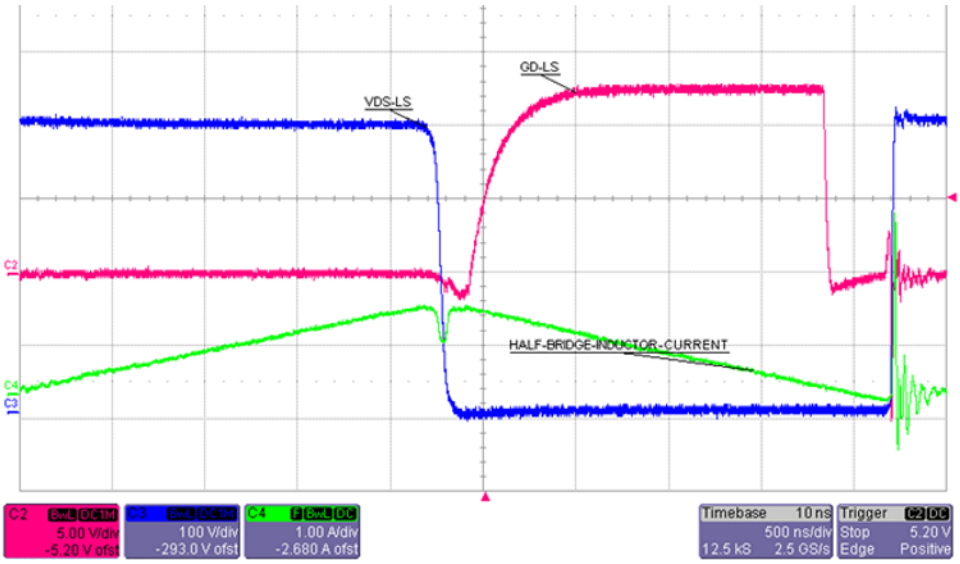


Figure 17. Low-Side Switching Waveform (Zoomed)

4.6 Switching Node Waveform (High Side)

Figure 18 ,Figure 19, and Figure 20 show the switching node waveforms of high-side gate driver. For these figures, the yellow waveform is the high-side gate driver input, the green waveform is the drain-to-source voltage for the high-side driven MOSFET, and the pink waveform is the half-bridge inductor current.

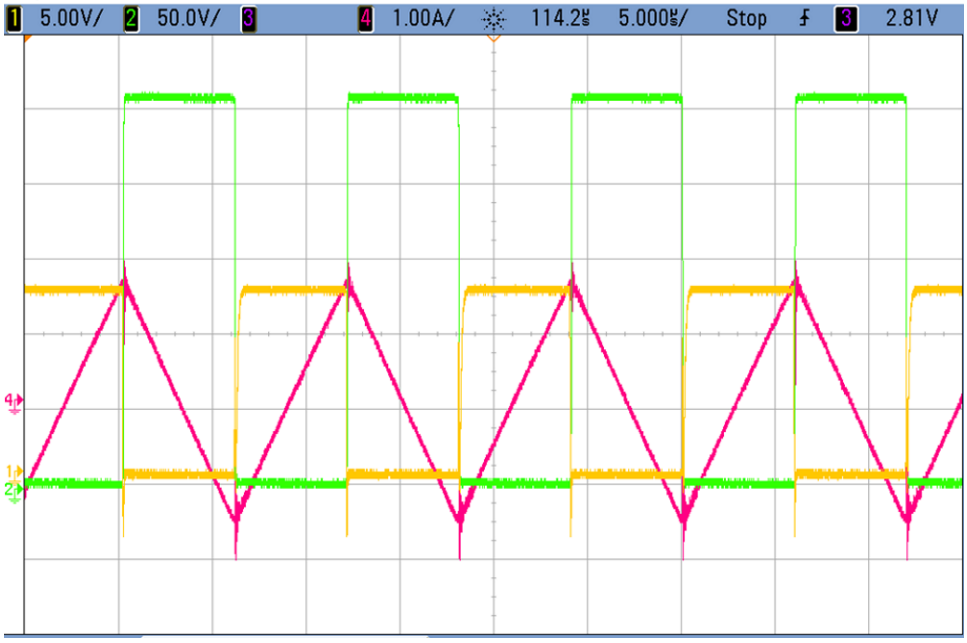


Figure 18. High-Side Switching Waveform

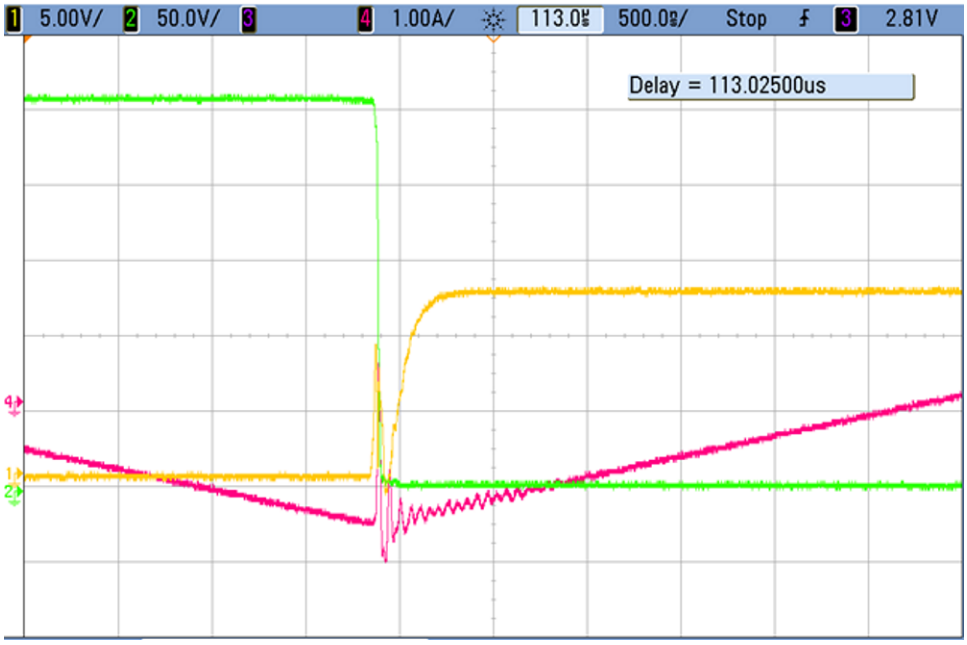


Figure 19. High-Side Switching Waveform (Zoomed, Turnon)

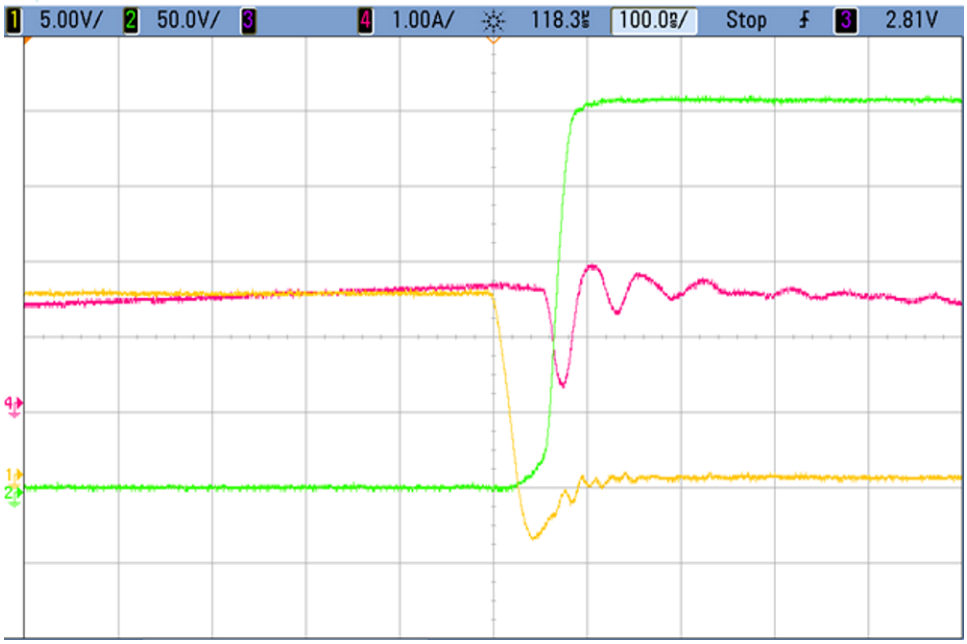


Figure 20. High-Side Switching Waveform (Zoomed, Turnoff)

4.7 UVLO Protection Startup

Figure 21 and Figure 22 show the UVLO for the MOSFET gate drivers. The output PWM starts only when the power supply of the gate driver reaches a threshold as defined in the UCC21520 datasheet. There is no spurious behavior at startup.

In Figure 21, the yellow waveform is the low-side PWM input and the red waveform is the low-side gate drive output.

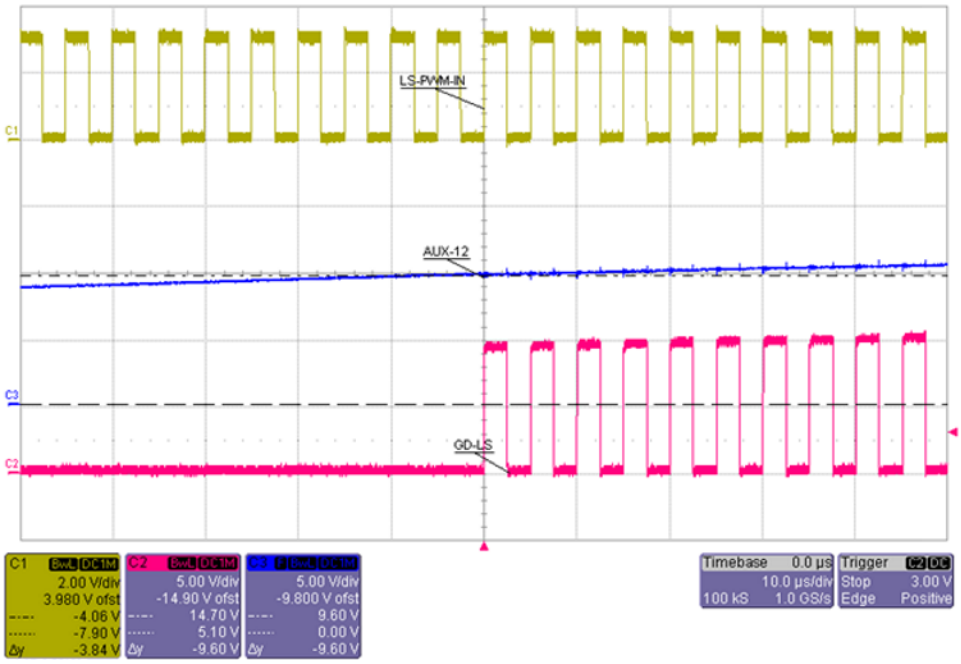


Figure 21. UVLO Start-up for Low-Side

In Figure 22, the yellow waveform is the high-side PWM input, the red waveform is the low-side gate drive output, and the green waveform is the high-side gate drive output.

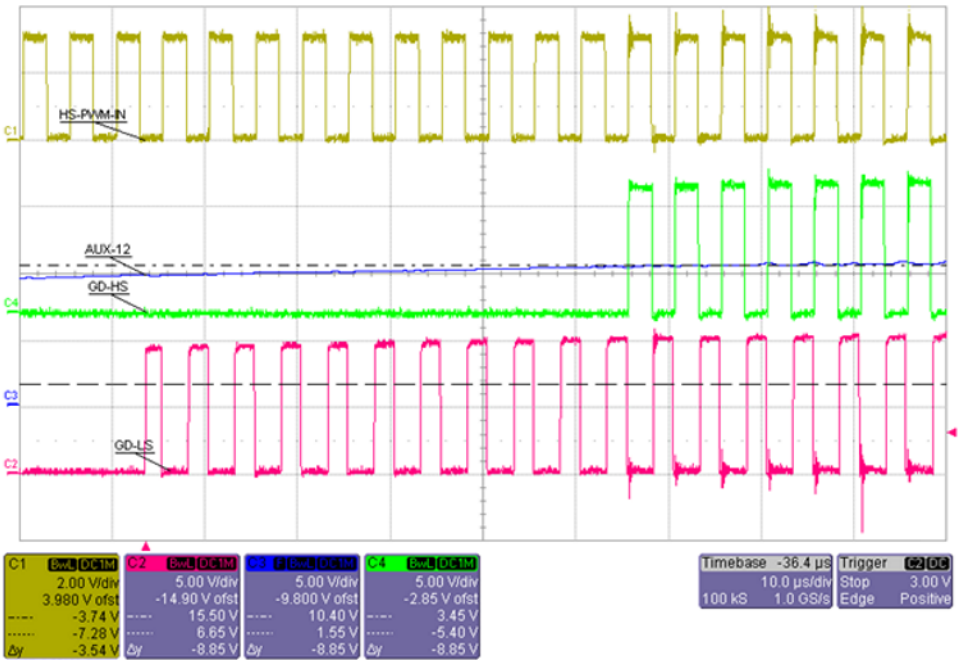


Figure 22. UVLO Startup for High-Side

4.8 Auxiliary Supply (Ripple)

Figure 23 shows the ripple voltage for the auxiliary 12-V supply. A ripple voltage of 200 mV pk-pk is seen. This is shown by the blue waveform.

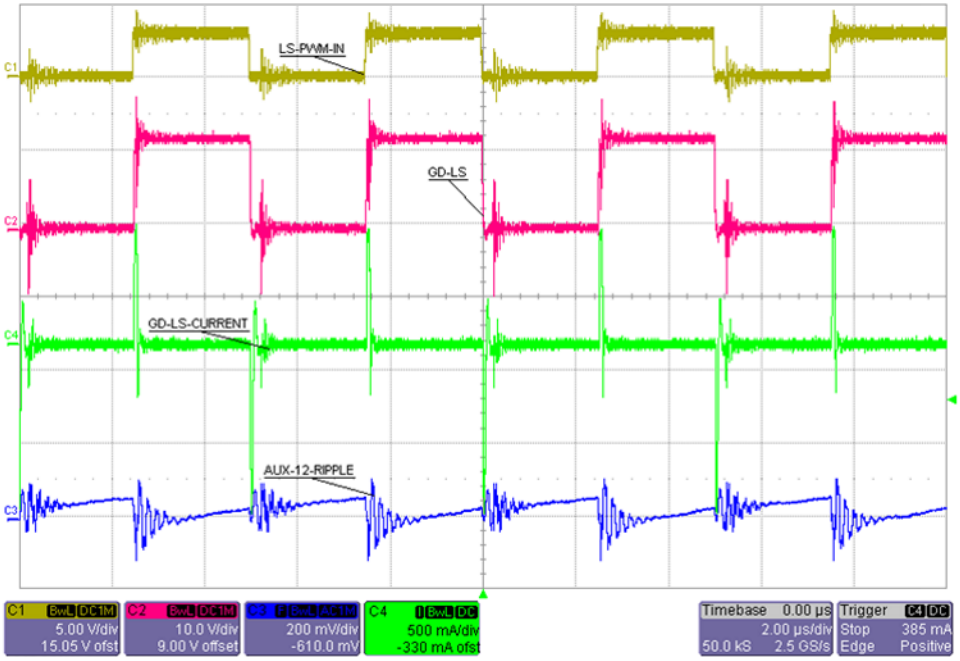


Figure 23. Auxiliary Supply (Ripple)

4.9 Auxiliary Supply (Efficiency and Regulation)

4.9.1 Efficiency With Load Variation

Figure 24 shows the efficiency of the system with load current variation.

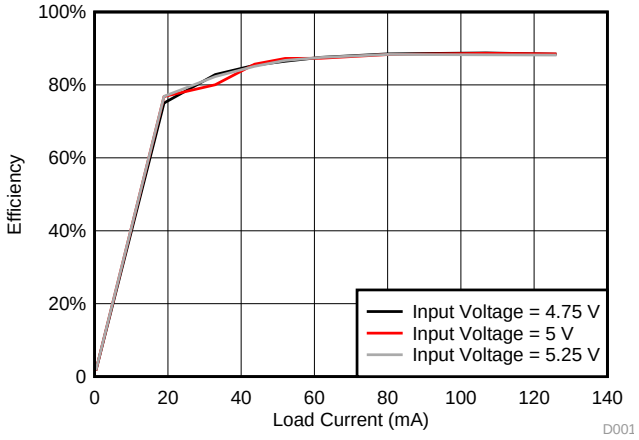


Figure 24. Efficiency versus Output Load

4.9.2 Regulation With Load Variation

Figure 25 shows the regulation of auxiliary supply of 12.5 V with load current.

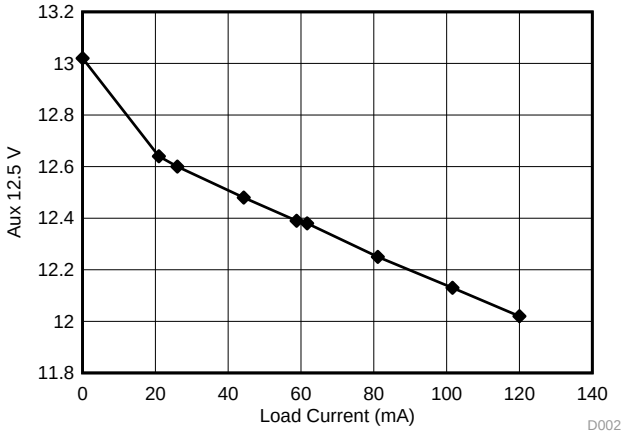


Figure 25. Regulation versus Output Load

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01159.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01159.

5.3 PCB Layout Recommendations

Note that the design contains high voltages. The layout must be done with extreme care.

- Connect low-ESR and low-ESL capacitors close to UCC21520 between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- Consider the high current path that comprises the bootstrap diode, bootstrap capacitor, the VSS2 referenced bypass capacitor, and the low-side transistor body and anti-parallel diode. The bootstrap capacitor is replenished when the bootstrap diode is turned on and this happens in a short time interval, which involves high peak current. Therefore, it is essential that the loop length and the area on the circuit are minimized.
- A PCB cutout is recommended to ensure good isolation performance between the primary and secondary side of UCC21520. To do this, avoid placing any PCB traces or copper below the device.
- The connection of the VCC pin of SN6505B and the transformer center-tap must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1 to 10 μF. The capacitor must have a voltage rating of 16 V minimum and a X5R or X7R dielectric.
- The connections between the device (SN6505B) D1 and D2 pins and the transformer primary endings, and the connection of the device VCC pin and the transformer center-tap must be as close as possible for minimum trace inductance.
- The output of the isolated PSU must be buffered to ISO-Ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1 to 10 μF. The capacitor must have a voltage rating of 16 V minimum and an X5R or X7R dielectric.
- Confine the high peak currents that charge and discharge the transistor gates to a minimal physical area as this will decrease the loop inductance and minimize noise on the gate terminals of the transistors. To ensure this, the TIDA-01159 board should be connected with very short leads to the transistors.
- Maintain appropriate creepage distances between the high and low-side PCB traces.
- Proper PCB layout can help dissipate heat from the devices to the PCB and minimize junction to board thermal impedance

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01159.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01159.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01159.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01159.

6 References

1. Texas Instruments, *High-Voltage Reinforced Isolation: Definitions and Test Methodologies*, Marketing White Paper (SLYY063)
2. Texas Instruments, *LAUNCHXL-F28027 C2000 Piccolo LaunchPad Experimenter Kit User's Guide* (SPRUHH2)
3. Balogh, Laszlo, *Design And Application Guide For High Speed MOSFET Gate Drive Circuits* (www.radio-sensors.se/download/gate-driver2.pdf)

6.1 Trademarks

7 About the Authors

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