TI Designs

Small, Efficient, Easy-to-Use Power Supply for Altera™ MAX® 10 FPGA for up to 125°C

Description

The TIDA-01366 (also known as PMP9799) demonstrates a complete power solution for Altera's MAX® 10 FPGA. This simple solution uses just three DC/DC converters to power the MAX 10 cost-effectively. This TI Design supports numerous industrial applications and any application that requires a small, high efficiency, high temperature power supply.

Resources

TIDA-01366	Design Folder
TPS62097	Product Folder
TPS62480	Product Folder
TPS22925	Product Folder

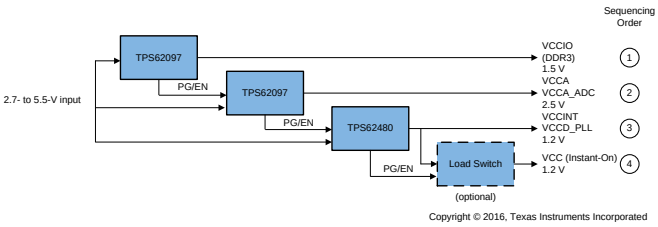
TI E2E™ Community — ASK Our E2E Experts

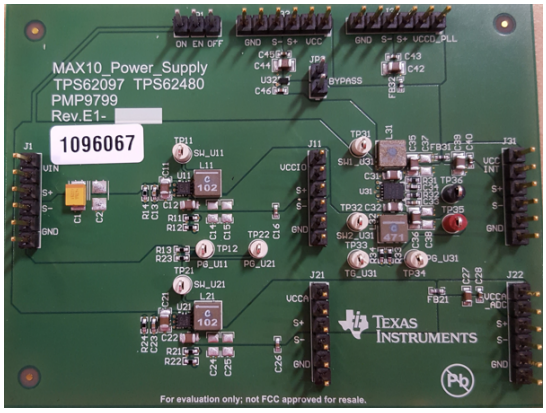
Features

- Supports Dual-Supply Power Option of MAX 10 to Enable Full FPGA Functionality
- Requires Just Three DC/DCs for a Cost-Effective and Simple Power Solution
- Total Solution Size < 300 mm^2 for Space-Constrained Applications
- 92% Efficiency at Half of Rated Load and 89% Efficiency at Full Rated Load for Low Temperature Rise and High Reliability
- Supports Instant-On Feature for Fastest Startup of MAX 10
- 125°C Rated Devices and Passives for High Temperature Applications with a Temperature Warning Flag at 120°C

Applications

- Motor Drives
- Test and Measurement
- Factory Automation and Control
- Electronic Point of Sale
- Medical





An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Overview

1.1 System Description

Altera's MAX® 10 Field-Programmable Gate Array (FPGA) is used in a variety of industrial applications that require a lower power, smaller, and configurable processing device. The TIDA-01366 provides a tested and documented power solution when using the MAX 10 as a dual-supply device. The power architecture follows what is shown in Reference 2 when using the built-in analog-to-digital converter (ADC) feature. A 1.2-V rail is required for the core, a 2.5-V rail for the ADC, and possibly a third rail is required for the input/output (I/O) rails. 1.5 V is chosen for the I/O rail to support DDR3 memory. A load switch is included as an optional feature to support Instant-On.

The TIDA-01366 achieves high efficiency by using efficient, integrated DC/DC converters and no low dropout (LDO) linear regulators. High efficiency results in a low self-temperature rise and higher reliability. All components are rated to 125ºC to support high ambient temperature industrial environments. Furthermore, a temperature warning flag (Thermal Good feature in the TPS62480) is implemented to alert the system host of high temperatures. The three DC/DC converters and their passive components occupy less than 300 mm^2 of printed circuit board (PCB) space. At less than 100 mm^2 per rail, this enables space-constrained systems with little PCB space.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER		SPECIFICATIONS	DETAILS
Input voltage range		2.7 to 5.5 V	—
OUTPUTS PROVIDED			
VCC (JP2 shorted)	Voltage setpoint	1.2 V	Section 4.1
	Ripple	< 20 mV	
	Transient response	< 5% (50% load step)	
	Load regulation	< 1.2%	
	Line regulation	< 0.4%	
VCCIO	Voltage setpoint	1.5 V	Section 4.2
	Ripple	< 25 mV	
	Transient response	< 5% (100% load step)	
	Load regulation	< 1.2%	
	Line regulation	< 0.4%	
VCCA	Voltage setpoint	2.5 V	Section 4.3
	Ripple	< 20 mV	
	Transient response	< 5% (50% load step)	
	Load regulation	< 1.2%	
	Line regulation	< 0.4%, V_{IN} > 2.8V	
VCCD_PLL	Voltage setpoint	1.2 V	Section 4.4
	Transient response	< 3% (50% load step)	
VCCA_ADC	Voltage setpoint	2.5 V	Section 4.5
	Transient response	< 2% (50% load step)	
VCCINT	Voltage setpoint	1.2 V	Section 4.6
	Transient response	< 3% (50% load step)	
Efficiency (each regulator at half of its rated load, JP2 shorted)		92%	Section 4.1, Section 4.2, Section 4.3
Efficiency (each regulator at its full rated load, JP2 shorted)		89%	Section 4.1, Section 4.2, Section 4.3
Sequencing order (JP2 open)		VCCIO, VCCA, 1.2 V (for VCC_INT and VCCD_PLL), VCC	Section 4.7
Sequencing order (JP2 shorted)		VCCIO, VCCA, VCC	—

1.3 Block Diagram

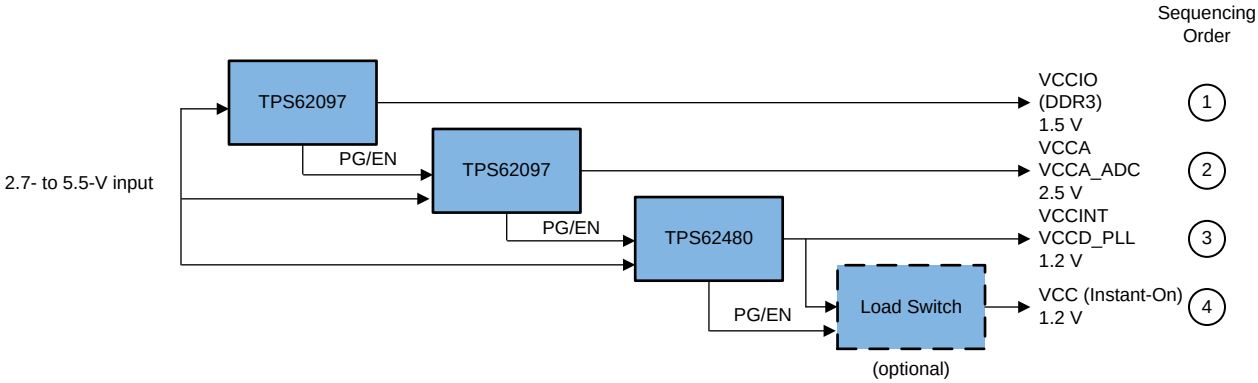


Figure 1. Block Diagram

1.4 Highlighted Products

1.4.1 TPS62097

The TPS62097 is a 2-A, high efficiency step-down converter optimized for a very accurate output voltage and small solution size. Its forced pulse width modulation (PWM) mode and 1% output voltage accuracy provide an accurate DC output voltage. Its iDCS-Control topology enables a very fast transient response to regulate the output voltage during heavy load changes, while its high switching frequency enables the use of a small inductor and output capacitor.

1.4.2 TPS62480

The TPS62480 is a 6-A, dual-phase, high efficiency step-down converter optimized for a very accurate output voltage and small solution size. Its forced pulse width modulation (PWM) mode and 1% output voltage accuracy provide an accurate DC output voltage. A dual-phase architecture is used to reduce the inductor size and the I^2R losses by halving the total output current for each phase. Its high switching frequency enables the use of small inductors and output capacitors.

1.4.3 TPS22925

The TPS22925 is a 3-A load switch that is used for the VCC rail when the MAX 10's Instant-On feature is required. This load switch has a very low on-resistance (R_{ON}) which results in both high efficiency and improved load regulation. If Instant-On is not required, the load switch is omitted and VCC connected directly to the TPS62480's 1.2-V output voltage.

2 System Design Theory

An FPGA's power requirements are a function of the specific FPGA functionality used in a given application. In most cases, the current drawn by each rail is not known precisely during the design phase. Only gross estimates are available when the power supply is designed. For this reason, the TIDA-01366 uses DC/DC converters that are high enough power to support the majority of MAX 10 applications, while still supplying a small solution size and high efficiency. A 2-A converter is used for the I/O rail, as well as the VCCA (2.5-V analog) rail. A 6-A converter is used for the 1.2-V core rail. A 3-A load switch supports a high current core rail when Instant-On is required. The I/O rail converter's output voltage is adjustable for other memory solutions besides DDR3.

Simple sequencing is integrated into the DC/DC converters. Though no specific sequencing is required for the MAX 10 (except for Instant-On support), sequencing is a good design practice to reduce inrush current drawn from the input source, as well as to provide a controlled system startup. The TIDA-01366 starts VCCIO first, then VCCA, and then the 1.2-V converter (VCC rail). If Instant-On is required, JP2 should be left open and a load switch powers the VCC rail after all other rails are in regulation. When Instant-On is used, the entire startup time is about 8 ms. This time is fully adjustable, faster or slower, on each DC/DC converter.

3 Getting Started Hardware

To test this TI Design, simply apply an input voltage (typically 5 V) to the J1 input connector. Then, connect a jumper between ON and EN on JP1. Install or omit a jumper on JP2, as required for Instant-On support. Sequencing is automatically handled by the onboard DC/DC converters.

4 Testing and Results

This section includes the relevant test results to power the MAX 10 FPGA. Unless otherwise noted, all testing was conducted with 5 V_{IN} and at room temperature.

4.1 VCC

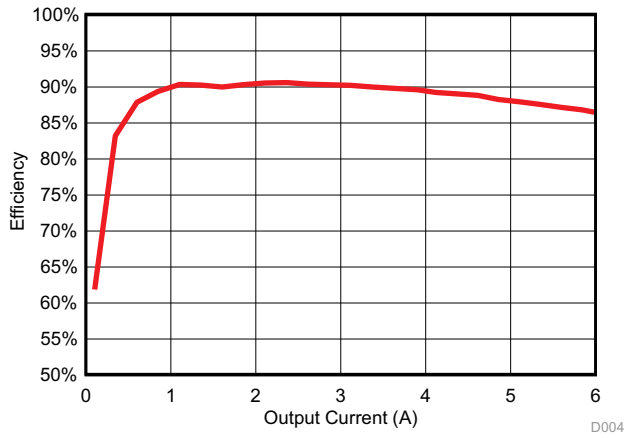


Figure 2. VCC Efficiency (5 V_{IN}, JP2 Shorted, Measured at J33)

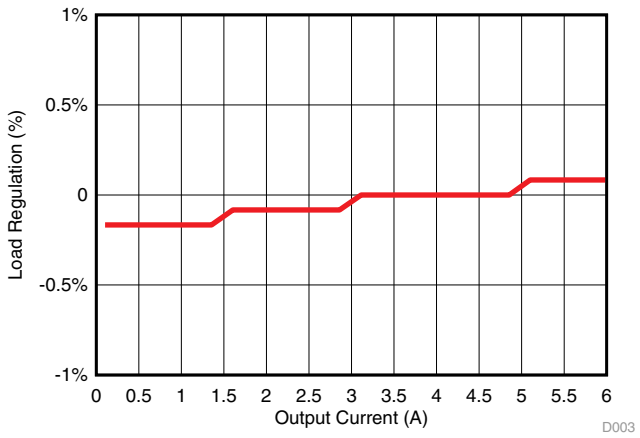


Figure 3. VCC Load Regulation (5 V_{IN}, JP2 Shorted, Measured at TP35/TP36)

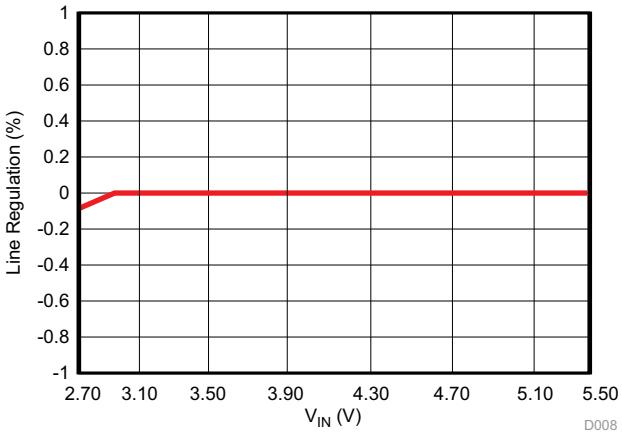


Figure 4. VCC Line Regulation (6-A Load, JP2 Shorted, Measured at J33)

Figure 5. VCC Transient Response (5 V_{IN}, 3- to 6-A Load Step, JP2 Shorted, Measured at J33)

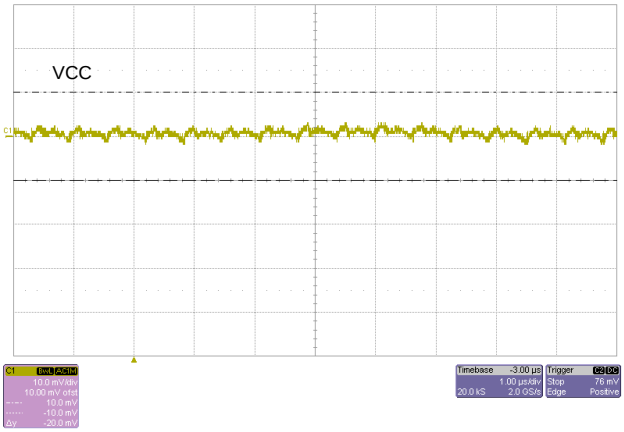


Figure 6. VCC Ripple (5 V_{IN}, 6-A Load, JP2 Shorted, Measured at C45)

4.2 VCCIO

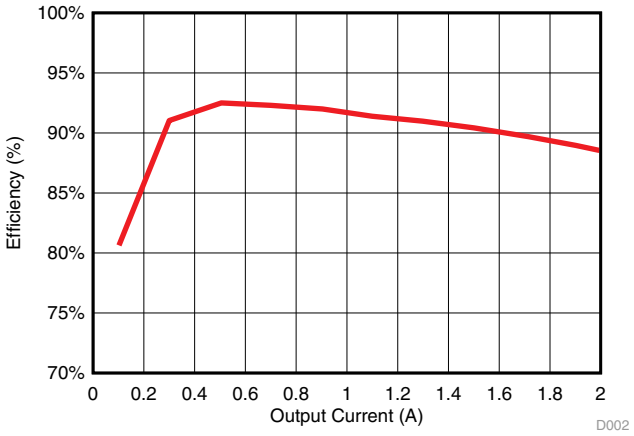


Figure 7. VCCIO Efficiency (5 V_{IN})

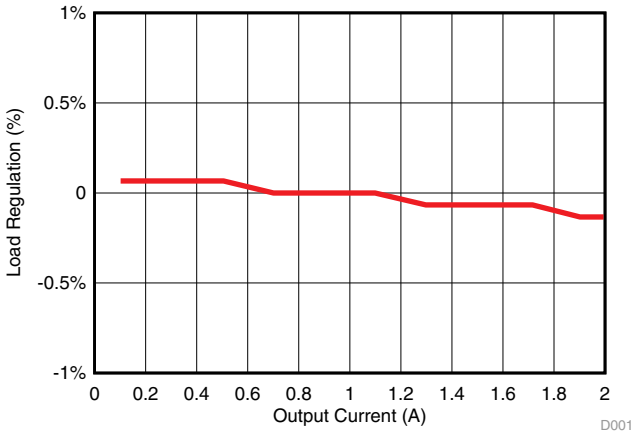


Figure 8. VCCIO Load Regulation (5 V_{IN})

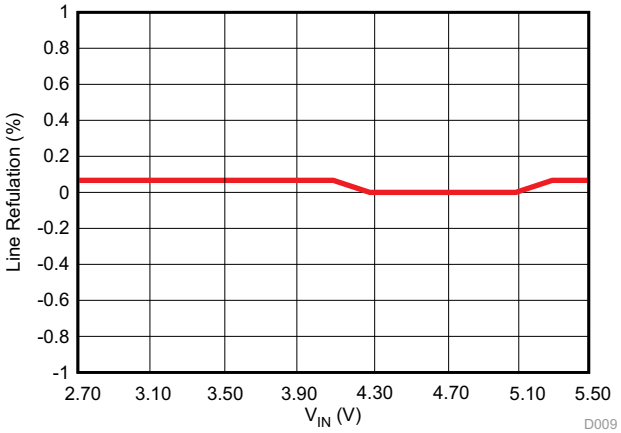


Figure 9. VCCIO Line Regulation (2-A Load)

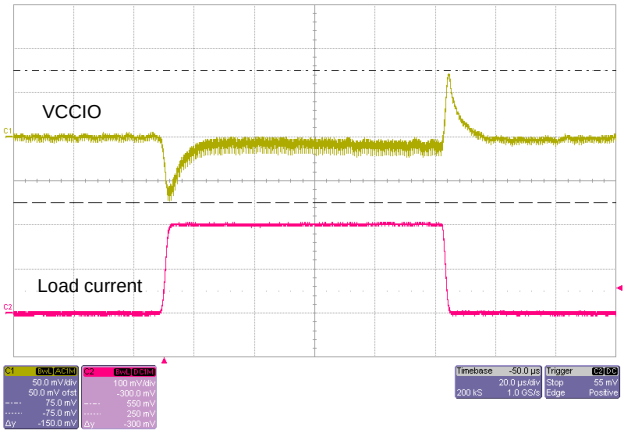


Figure 10. VCCIO Transient Response (5 V_{IN}, 0- to 2-A Load Step)

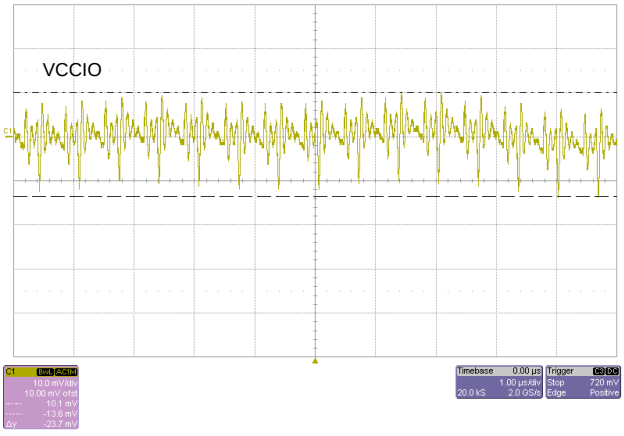


Figure 11. VCCIO Ripple (5 V_{IN}, 2-A Load)

4.3 VCCA

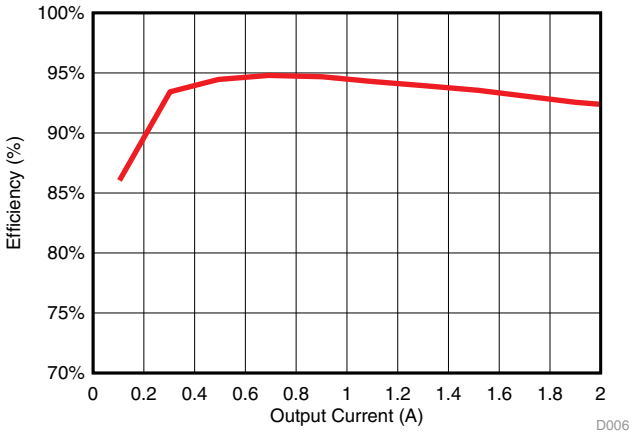


Figure 12. VCCA Efficiency (5 V_{IN})

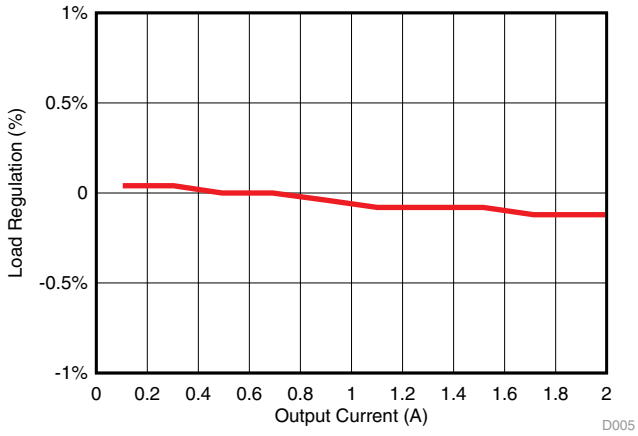


Figure 13. VCCA Load Regulation (5 V_{IN})

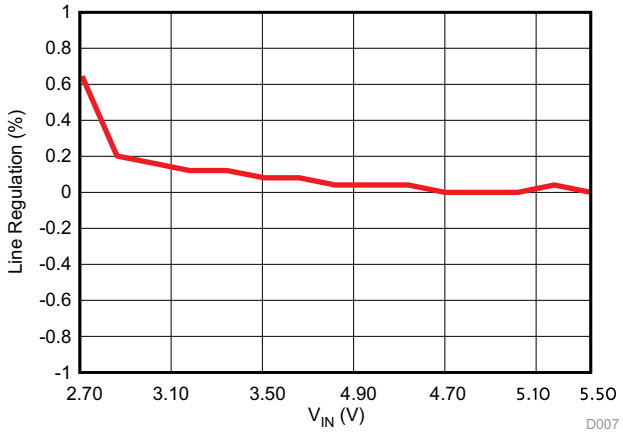


Figure 14. VCCA Line Regulation (2-A Load)

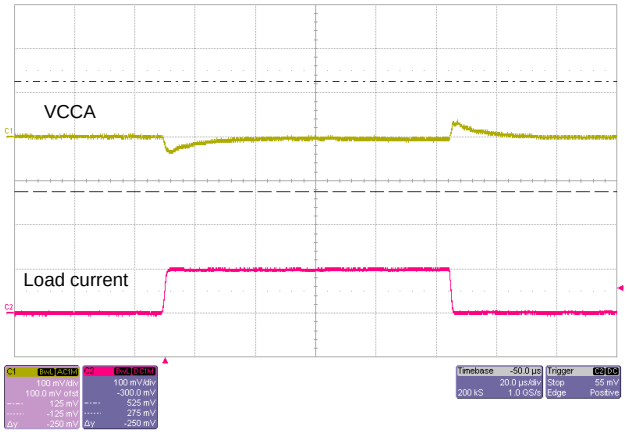


Figure 15. VCCA Transient Response (5 V_{IN}, 0- to 1-A Load Step)

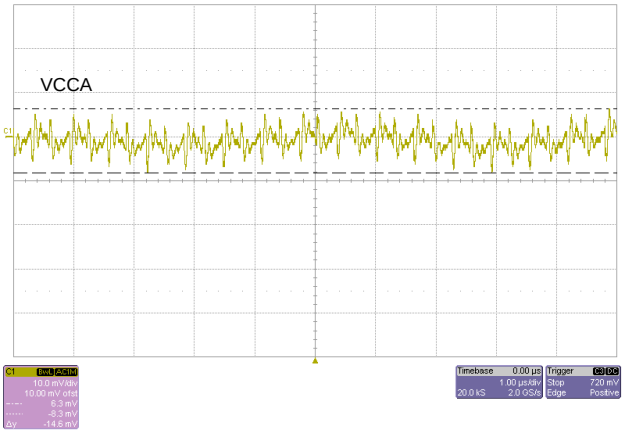


Figure 16. VCCA Ripple (5 V_{IN}, 2-A Load)

4.4 VCCD_PLL

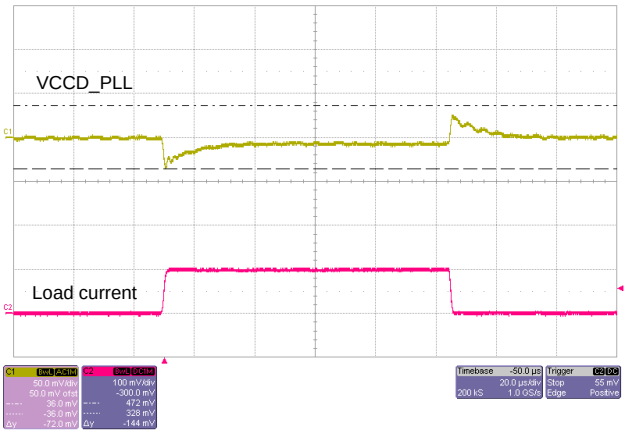


Figure 17. VCCD_PLL Transient Response (5 V_{IN}, 0- to 1-A Load Step)

4.5 VCCA_ADC

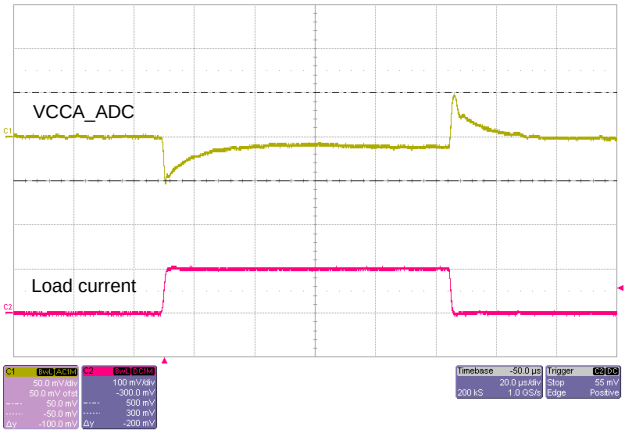


Figure 18. VCCA_ADC Transient Response (5 V_{IN}, 0- to 1-A Load Step)

4.6 VCCINT

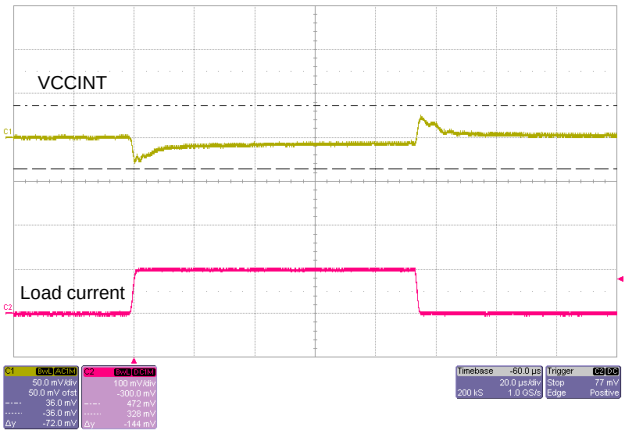


Figure 19. VCCINT Transient Response (5 V_{IN}, 0- to 1-A Load Step)

4.7 System Startup

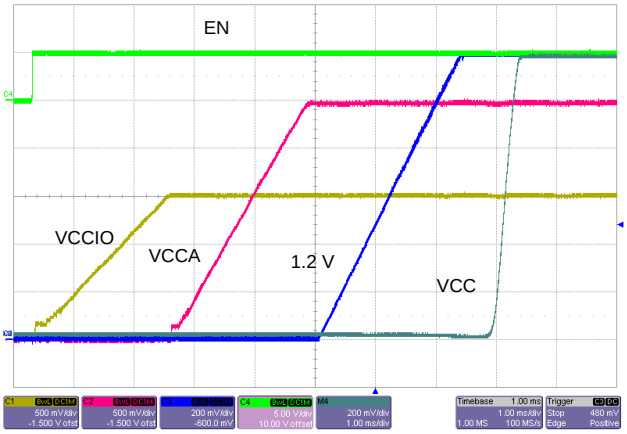


Figure 20. Startup on EN (5 V_{IN}, No Load, JP2 Open)

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01366.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01366.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01366.

5.4 Gerber Files

To download the Gerber files, see the design files at TIDA-01366.

5.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01366.

6 Related Documentation

1. Altera, *MAX 10 Power Management User Guide*
2. Altera, *MAX® 10 FPGA Device Family Pin Connection Guidelines PCG-01018-1.6*
3. Texas Instruments, *2-A High Efficiency Step-Down Converter with iDCS-Control, Forced PWM Mode and Selective Switching Frequency*, TPS62097 Datasheet (SLVSCD6)
4. Texas Instruments, *2.4-V to 5.5-V, 6-A, 2-Phase Step-Down Converter*, TPS62480 Datasheet (SLVSCL9)
5. Texas Instruments, *3.6-V, 3-A, 9-mΩ On-Resistance Load Switch*, TPS22925 Datasheet (SLVS840)
6. Texas Instruments, *High-efficiency, low-ripple DCS-Control™ offers seamless PWM/power-save transitions*, Technical Brief (SLYT531)

6.1 Trademarks

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ('TI") reference designs are solely intended to assist designers ("Designer(s)") who are developing systems that incorporate TI products. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.

TI's provision of reference designs and any other technical, applications or design advice, quality characterization, reliability data or other information or services does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such reference designs or other items.

TI reserves the right to make corrections, enhancements, improvements and other changes to its reference designs and other items.

Designer understands and agrees that Designer remains responsible for using its independent analysis, evaluation and judgment in designing Designer's systems and products, and has full and exclusive responsibility to assure the safety of its products and compliance of its products (and of all TI products used in or for such Designer's products) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to its applications, it has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any systems that include TI products, Designer will thoroughly test such systems and the functionality of such TI products as used in such systems. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

Designers are authorized to use, copy and modify any individual TI reference design only in connection with the development of end products that include the TI product(s) identified in that reference design. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of the reference design or other items described above may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS AND OTHER ITEMS DESCRIBED ABOVE ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNERS AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS AS DESCRIBED IN A TI REFERENCE DESIGN OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

TI's standard terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products. Additional terms may apply to the use or sale of other types of TI products and services.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265