TI Designs: *TIDA-01238*
Controller Area Network (CAN) with Selectable Termination Reference Design

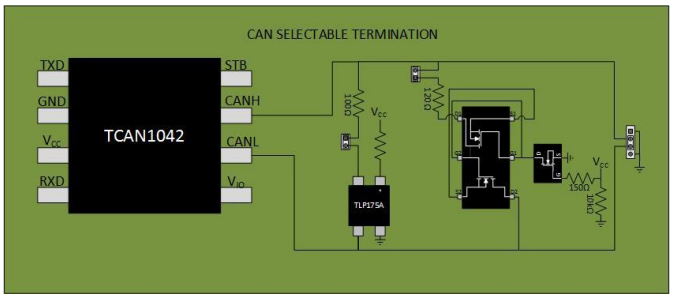
Design Overview

Typically in bus communication technologies such as Controller Area Network (CAN) and RS-485, the two farthest nodes in the network are terminated with 120-Ω termination resistors and the other nodes are left unterminated. This requires that the system designer know the layout of the end application, though, which is not always the case.

TIDA-01238 documents and tests two individual circuits that make termination selectable at individual CAN nodes, making termination at any node possible without modifying hardware. This allows for greater flexibility in CAN bus installations, since the location of the bus termination can be changed on the fly in order to optimize the performance of the bus.

Design Resources

TIDA-01238	Design Folder
TCAN1042	Product Folder
TCAN1051	Product Folder
TCAN1042DEVM	Tools Folder
TCAN1042 IBIS Model	Tools Folder
IEC 61000 CAN Reference Design	Tools Folder



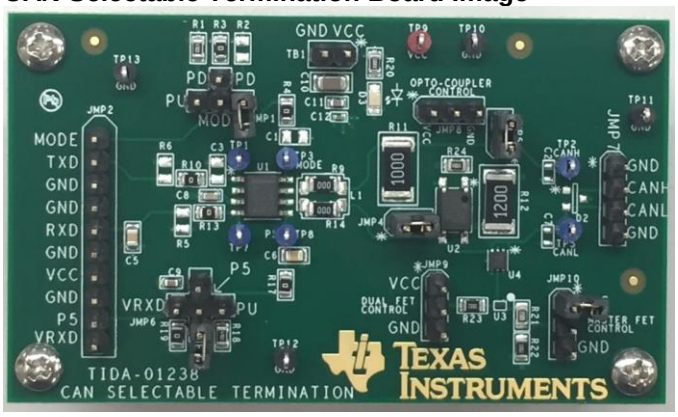
Design Features

- Selectable termination supporting wide input common mode range using opto-coupler technology
- Selectable termination supporting standard input common mode range using MOSFETs

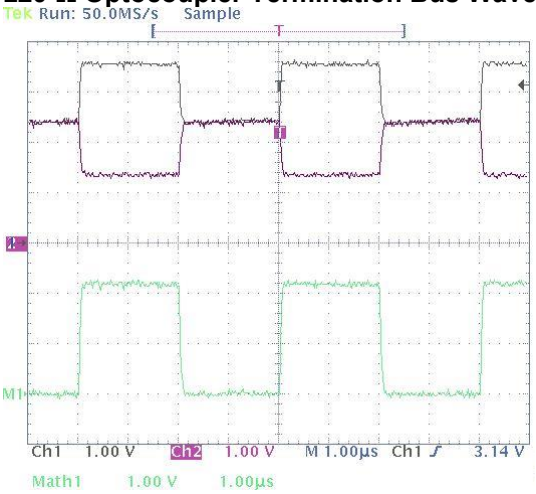
Featured Applications

- Industrial Automation, Control, Sensors, and Drive Systems
- Building Security and Climate Control Automation
- Telecom Base Station Status and Control
- Heavily Loaded CAN Buses

CAN Selectable Termination Board Image



120-Ω Optocoupler Termination Bus Waveform



1 Design Overview

Industrial interfaces such as CAN and RS-485 require termination resistances to be present on a bus in order to provide proper loading for the driver circuits and to provide an endpoint to the network with an impedance that is matched to the characteristic impedance of the transmission lines used. These terminations and their placements are critical in maintaining signal integrity on the bus.

In ideal applications that involve a linear network, the best performance is typically achieved by placing termination at the two distal ends of the network. However, many applications require the use of non-ideal network topologies in which stub nodes or clusters of stub nodes need to branch off from a main bus. In these cases, some experimentation may be needed in order to determine the optimal placement. In other cases, the number of nodes used in a network and its overall topology may not be fixed; instead, it may need to change over time based on the needs of the application. An example of this would be a backplane system in which network cards (each with a CAN interface) can be inserted or removed as needed.

In systems like this, the ability to designate terminating nodes and easily reconfigure them is important. TI Design *TIDA-01238* shows two practical examples of how to implement selectable termination on a multipoint CAN bus. This document walks through the ISO 11898-2 physical layer standard, the selectable termination circuit implementation, the components selected for the design, the performance of the circuit, and the printed circuit board layout.

2 ISO11898-2 Controller Area Network (CAN) Physical Layer Standard

Controller area network (CAN) is an International Standardization Organization (ISO) defined serial communication bus originally developed for the automotive industry to replace the complex wiring harness with a two-wire bus. The specification calls for high immunity to electrical interference and the ability to self-diagnose and repair data errors. These features have led to expanded popularity for CAN in industrial applications such as building automation, process control automation, elevators, construction equipment, and robotics, amongst many others.

The CAN communications standard, ISO-11898, follows the open systems interconnection (OSI) model and defines functions in terms of layers. The specification of the physical layer, which is where the Texas Instruments CAN transceiver resides, is summarized in section two of the ISO11898 standard (ISO11898-2). ISO11898-2 describes the physical layer for high speed CAN as a differential bus technology that supports a signaling rate of up to 5 Mbps. The ISO 11898-2 document also describes the DC requirements that a CAN transceiver must meet in order to be considered complaint. It states that a transceiver must support a minimum output differential voltage of 1.5V across a 54Ω load. The 54Ω requirement comes from the two 120Ω termination resistors at the distal ends plus the parallel combination of the additional unterminated CAN nodes. If 50 TCAN1042 CAN transceivers are in parallel on the bus the effective intendance of those transceivers is 555Ω. The transceiver load of 60Ω in parallel with the 555Ω gives an effective impedance of approximately 54Ω. The TCAN1042 was design to support more nodes than 50 CAN nodes though and is capable of driving the required 1.5V across a 50Ω load. Using the same logic as above it can be calculated that 100 CAN nodes with 30kΩ differential input impedance in parallel gives an effective impedance of 180Ω. This is parallel with 60Ω transceiver load gives a 50Ω load.

Texas Instruments CAN transceivers meet or exceed the requirements set by the ISO 11898 standard and support other features like V_{IO} voltage support, shutdown mode, slope control, and integrated IEC ESD protection. This TI Design focuses on the TCAN1042, a 5-V CAN transceiver with integrated IEC ESD and DC fault protection designed for operation at high data rates.

3 System Description

In this TI Design, two different circuits demonstrate how selectable termination can be implemented. The first solution shows how a photorelay consisting of a photo MOSFET optically coupled to an infrared light emitting diode can be biased from a microprocessor or DC voltage to insert the required 120-Ω termination at the desired node. The second solution consists of three N-Channel MOSFET devices that when biased will provide a channel between CANH and CANL for the 120-Ω termination.

3.1 Components Used

This section provides a short description of each component used in this design.

3.1.1 TCAN1042

The TCAN1042 transceiver meets the ISO 11898-2 (2016) High Speed CAN (Controller Area Network) physical layer standard. They are half duplex transceiver designed for classical CAN data rates and data rates in excess of 1 Mbps for CAN FD. They possess enhanced timing margin for higher data rates in long and highly-loaded CAN networks. It is powered through a 5-V supply, supports CAN FD data rates up to 5 Mbps, and is fully compliant to the ISO11898-2 (2016) standard. The TCAN1042 is feature-rich with under voltage protection (UVLO) on the supply pins, ±58V bus fault protection or ±70V bus fault protection in the high

voltage TCAN1042H, receiver dominant state timeout (RXD DTO), driver dominant state timeout (TXD DTO), and thermal shutdown protection. The bus pins, CANH and CANL, have integrated ESD protection making them robust to ESD events with high levels of protection against HBM, CDM, IEC 61000-4-2, and ISO7637. The TCAN1042 supports ±8 kV of IEC61000-4-2 ESD protection, ±10 kV HBM protection, and ± 4 kV IEC EFT protection without requiring external protection components.

3.1.2 TLP175A Photorelay

The TLP175A photorelay uses a photo MOSFET which is optically coupled to an infrared LED. It is housed in a 4-pin SO6 package. This photorelay requires 1 mA of LED current to turn it on.

3.1.3 CSD17483F4 30-V N-Channel FemtoFET™ MOSFET

The CSD17483F4 is a 200-mΩ, 30-V N-Channel FemtoFET™ MOSFET technology that is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing small single MOSFETs while providing at least 60% reduction in footprint in a 0402 package size.

3.1.4 CSD87502Q2 30-V Dual N-Channel NexFET™ Power MOSFETs

The CSD87502Q2 is a 30-V, 27-mΩ N-Channel device with dual independent MOSFETs in a SON 2 x 2 mm plastic package. The two FETs were designed to be used in a half-bridge configuration for synchronous buck and other power supply applications. Additionally, the NexFET™ power MOSFETs can be used for adaptors, USB input protection, and battery charging applications. The dual FETs feature low drain-to-source on-resistance that minimizes losses and offers low component count for space-constrained applications.

4 System Design Theory

This TI Design features two solutions for implementing termination on a CAN bus node that is selectable. Two different options are proposed for this TI Design: an isolated design which covers a wide common-mode voltage range using a photorelay and an alternative solution using a dual N-Channel MOSFETs and a single N-Channel MOSFET.

The photorelay-based solution uses the TLP175A device from Toshiba. This device consists of a photo MOSFET and an infrared LED in a small 4-pin SO6 package. The anode of the LED is located at pin 1 of the device, and it should be connected to a control voltage from either a microprocessor or from a static DC source. Pin 3 of the TLP175A is the cathode, which is tied to the ground of the CAN node. The LED has a forward current that ranges from 2 to 15 mA, so a current limiting resistor should be placed in between the control voltage source and ground to limit the amount of current draw to this range. If the control voltage is coming from a microprocessor, care should be taken to ensure the series resistance is sized properly.

The MOSFET-based solution uses a combination of the CSD17483F4 single N-Channel FemtoFET™ MOSFET and the dual-channel CSD87502Q2 N-Channel NexFET™ from Texas Instruments. The gate of the CSD17483F4 can be driven by either a control voltage from either a microprocessor or other DC source. There is a voltage divider in between the microprocessor input and the gate of the CSD17483F4 to help limit the amount of current the microprocessor needs to provide to drive the MOSFET gate. The drain of the CSD17483F4 is connected to both gates of the CSD87502Q2 with a pull up resistor option to V_{CC} of the TIDA-01238 board or to an externally-supplied voltage. Since the gate voltage of an N-channel FET needs to be greater than the drain voltage for operation in the active region, pulling both gates of the CSD87502Q2 to V_{CC} is sufficient for applications requiring a 0-V to 5-V common-mode range. For operation over a greater common mode range, a larger voltage can be applied to the gates using a separate DC source.

5 Getting Started Hardware

The TIDA-01238 reference design includes a PCB that is fully assembled with the TCAN1042 CAN transceiver, a CSD17483F4 30 V N-Channel FemtoFET™ MOSFET from Texas Instruments, a CSD87502Q2 30 V dual N-Channel NexFET™ Power MOSFET from Texas Instruments, and a TLP175A photorelay from TOSHIBA. V_{CC} and GND are applied to the board through the berg header TB1 in the center top portion of the board. JMP2 on the left-hand side of the board provides access to the TXD and RXD logical input and output as well as voltage control pin V_{IO} (pin 5 on the TCAN1042). JMP6 also provides access to the V_{IO} pin with pull-up and pull-down resistor options. JMP1 gives control of the STB pin, pin 8, on the TCAN1042 by providing pull-up and pull-down options for enabling or disabling the device. V_{IO} and STB can be driven from the voltages present on the board provided through $V_{CC,}$ or another voltage source can be used for system level testing. JMP7 on the far right side of the board provides access to the CANH and CANL pins, pins 6 and 7 on the TCAN1042 respectively. Throughout the board test points are placed, providing another convenient measurement option for evaluating the CAN signals.

JMP4 and JMP8 are the berg headers needed to implement the photorelay-based solution. JMP4 is used to connect a 120-Ω termination resistor between CANH and CANL, and JMP8 is used to activate and deactivate the photorelay. JMP8 is a 3-pin berg header where pin 1 is tied to the V_{CC} net, pin 2 is tied to the anode of the photorelay, and pin 3 is tied to the GND net. For board-level evaluation of the photorelay solution, the anode can be tied to V_{CC} to engage the termination or to ground to disengage the termination. For system-level evaluation, pin 2 of JMP8 can be tied to a control pin from a microprocessor or to another DC source. The resistor used in parallel between CANH and CANL is 100 Ω due to the approximate 20-Ω impedance introduced by the photorelay placed in series. JMP5, JMP9, and JMP10 should be unpopulated while evaluating the photorelay-based solution.

JMP5, JMP9, and JMP10 are the berg headers needed to implement the MOSFET-based solution. JMP5 connects the 120-Ω termination resistor between CANH and CANL while JMP9 and JMP10 are used to switch on and off the FETs. Pin 1 connects to the V_{CC} net, pin 2 connects to the gates of the FETs, and pin 3 connects to the GND net on the evaluation board for both JMP9 and JMP10. For board-level evaluation of the FET solution, the gates of the FETs can be tied directly to the V_{CC} net to engage the termination resistor or the gates of the FETs can be tied directly to the GND net on the evaluation board to disengage the termination resistor. The resistor in parallel with CANH and CANL is 120 Ω since the on-state resistance of the FETs is extremely low. JMP4 and JMP8 should be unpopulated while evaluating the FET solution.

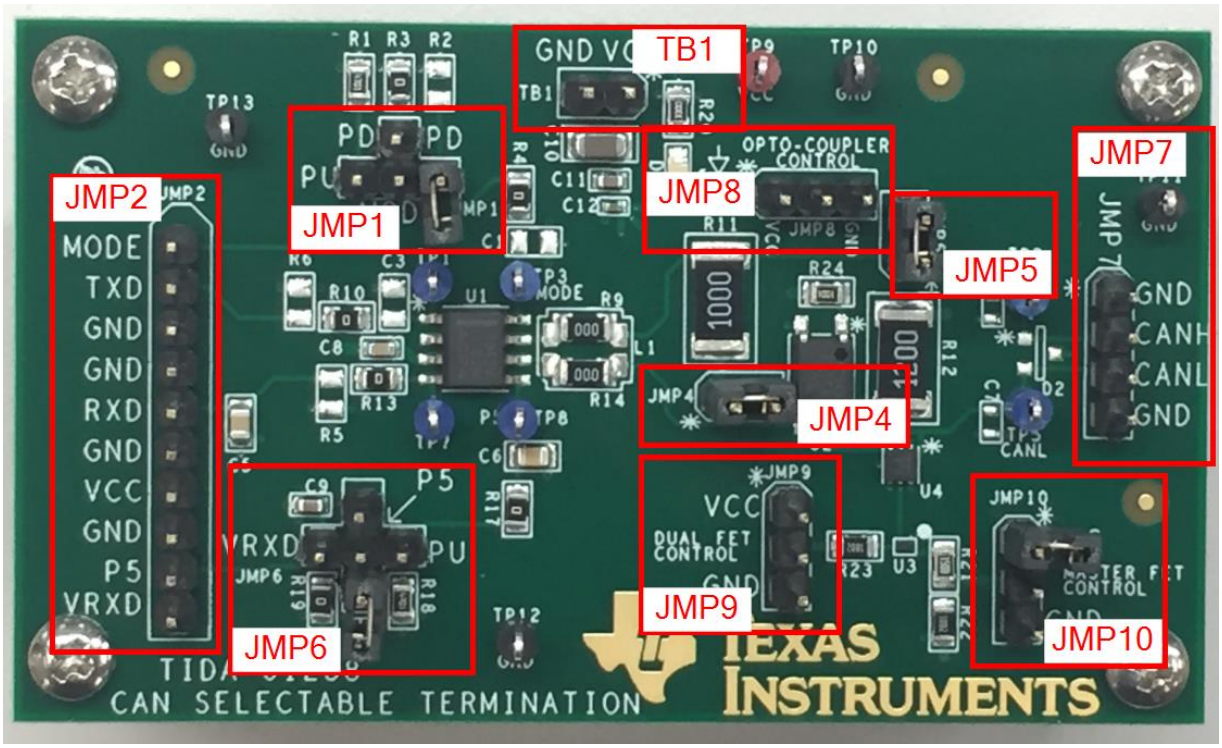


Figure 1: CAN Selectable Termination Evaluation Board

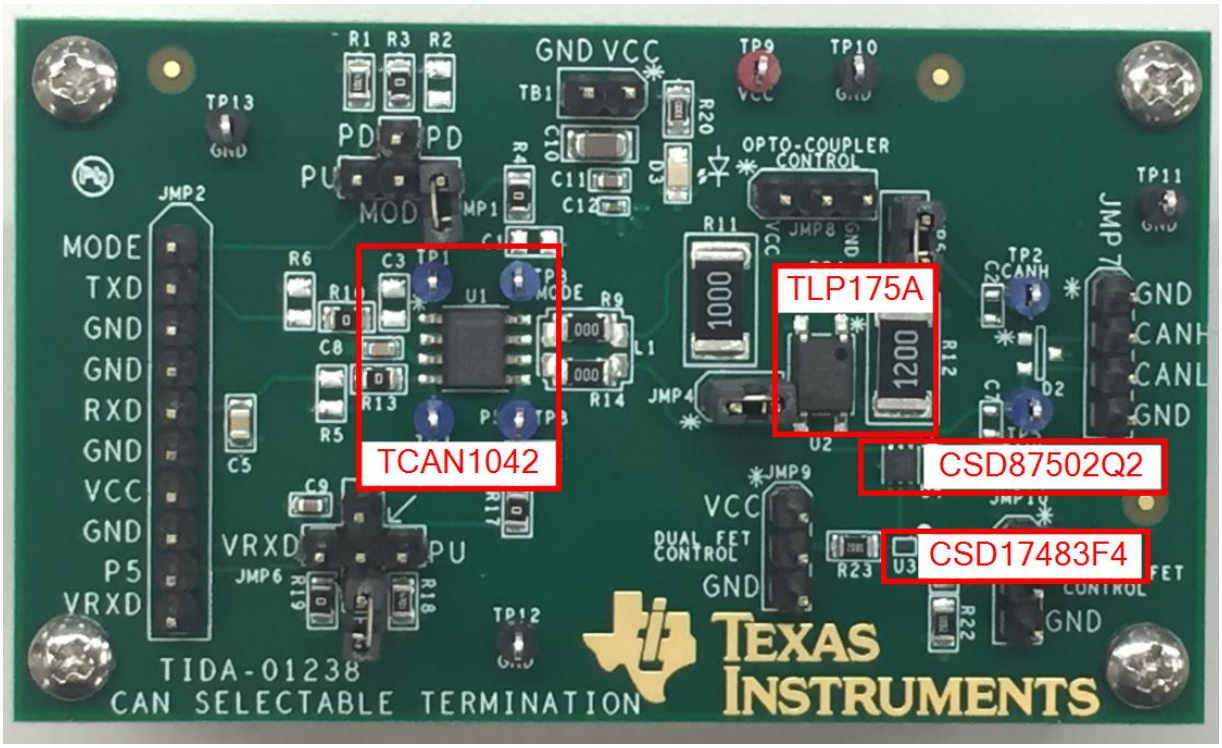


Figure 2: CAN Selectable Termination Evaluation Board Part Placement

6 Test Setup

The configuration of the boards during the evaluation of the photorelay and FET solutions can be seen in Figure 3 and Figure 4 respectively. V_{CC} and GND are supplied via the red and black alligator clips, the TXD signal is provided on the right via the TXD pin on JMP2, V_{IO} is supplied to pin 5 of JMP6 via the V_{CC} pin on JMP2 for both boards, the CAN bus signals are transmitted from board to board through the yellow jumper cables via JMP7, and the oscilloscope captures for CANH and CANL were taken on TP2 and TP5, respectively, in both setups. The only difference between the two setups is how the termination was implemented.

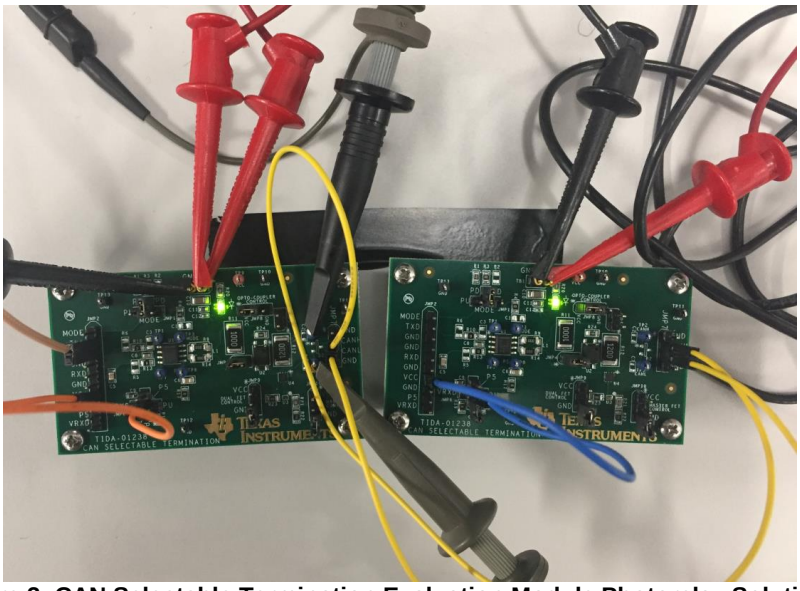


Figure 3: CAN Selectable Termination Evaluation Module Photorelay Solution Setup

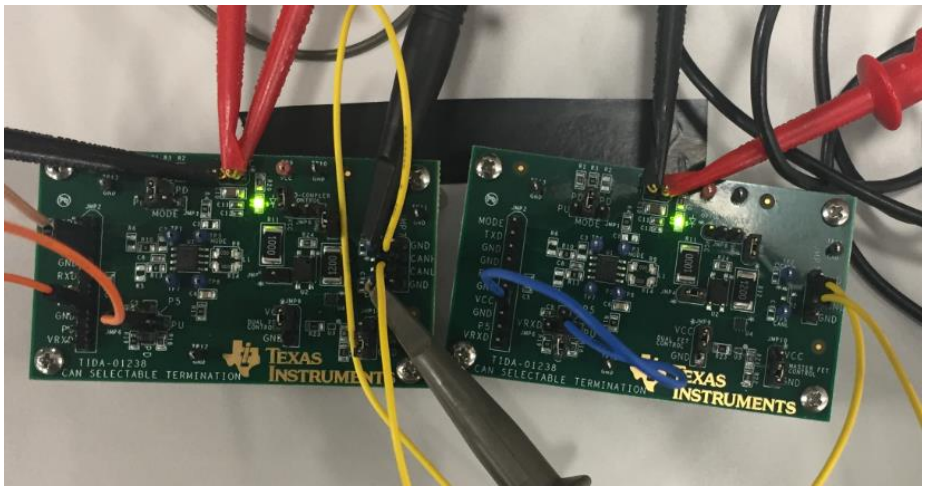


Figure 4: CAN Selectable Termination Evaluation Module FET Solution Setup

7 Test Data

The images below show the performance of both the photorelay termination solution and the FET termination solution at 500kbps, 1Mbps, 2Mbps, and 5Mbps with the latter two being CAN FD data rates.

7.1 TLP175A Termination Scheme

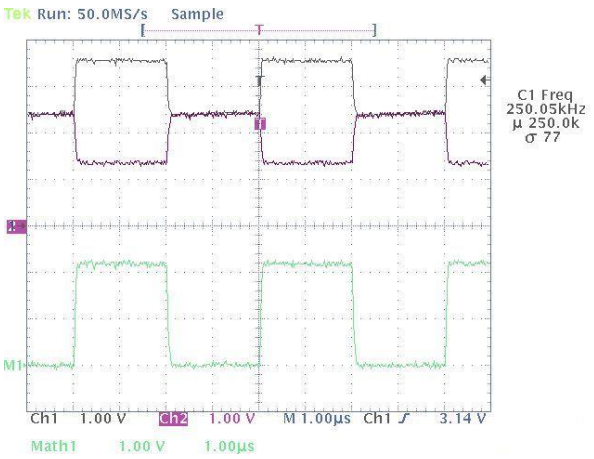


Figure 5: 500kbps Photorelay Termination Scheme

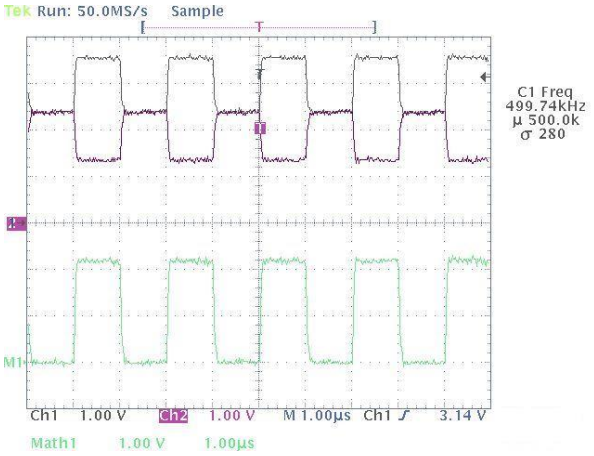


Figure 6: 1Mbps Photorelay Termination Scheme

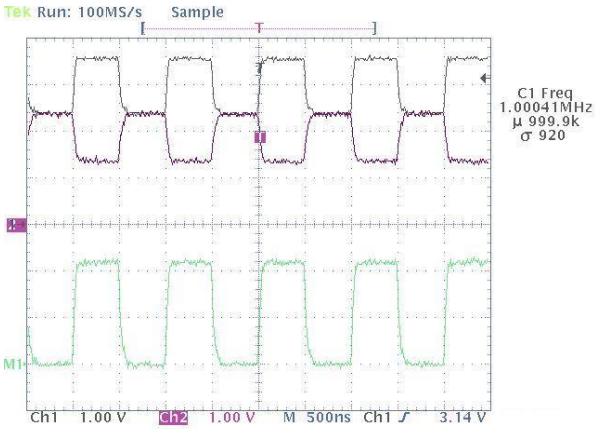


Figure 7: 2 Mbps Photorelay Termination Scheme

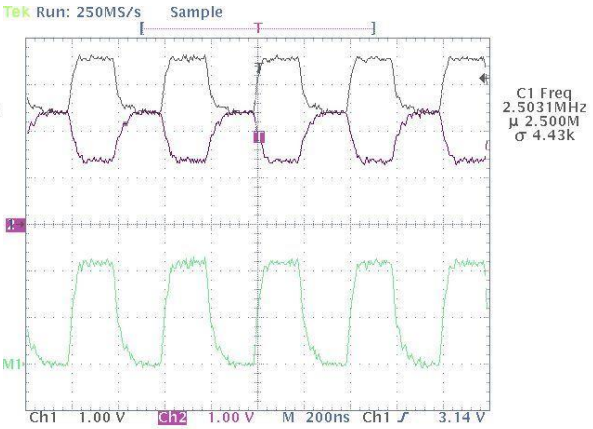


Figure 8: 5 Mbps Photorelay Termination Scheme

7.2 CSD87502Q2 and CSD17483F4 FET Termination Scheme

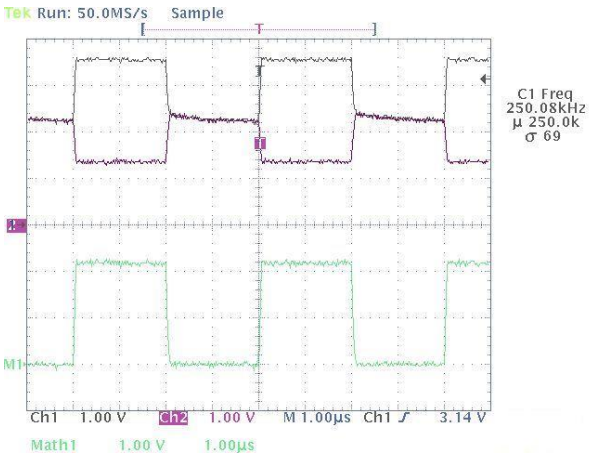


Figure 9: 500 kbps FET Termination Scheme

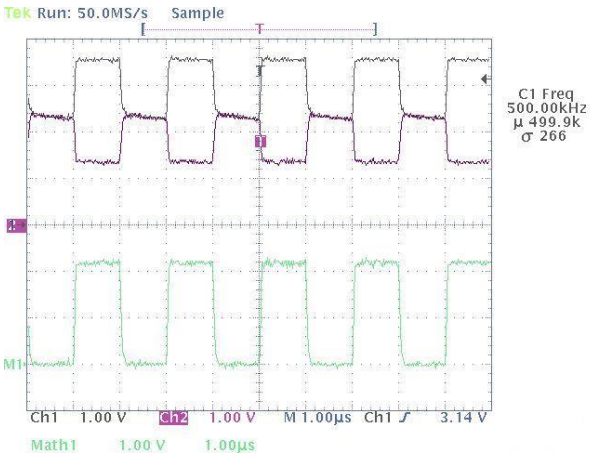


Figure 10: 1 Mbps FET Termination Scheme

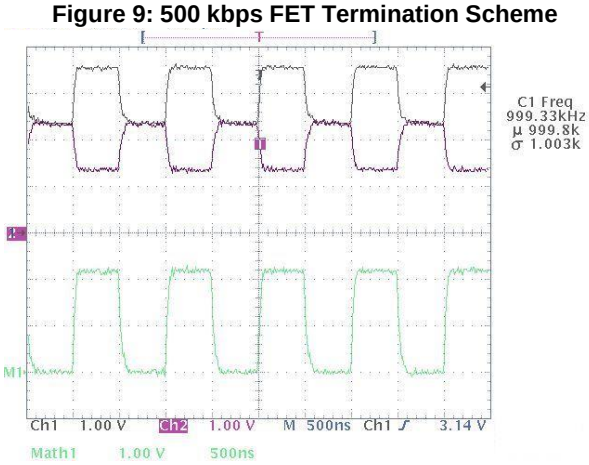


Figure 11: 2 Mbps FET Termination Scheme

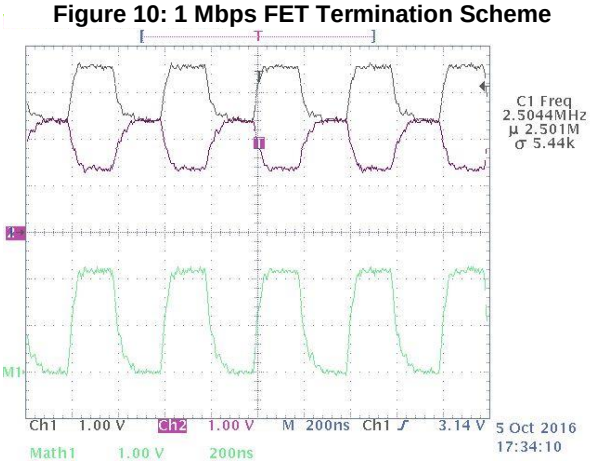


Figure 12: 5 Mbps FET Termination Scheme

8 Design Files

8.1 Schematics

To download the Schematics for each board, see the design files at http://www.ti.com/tool/TIDA-01238

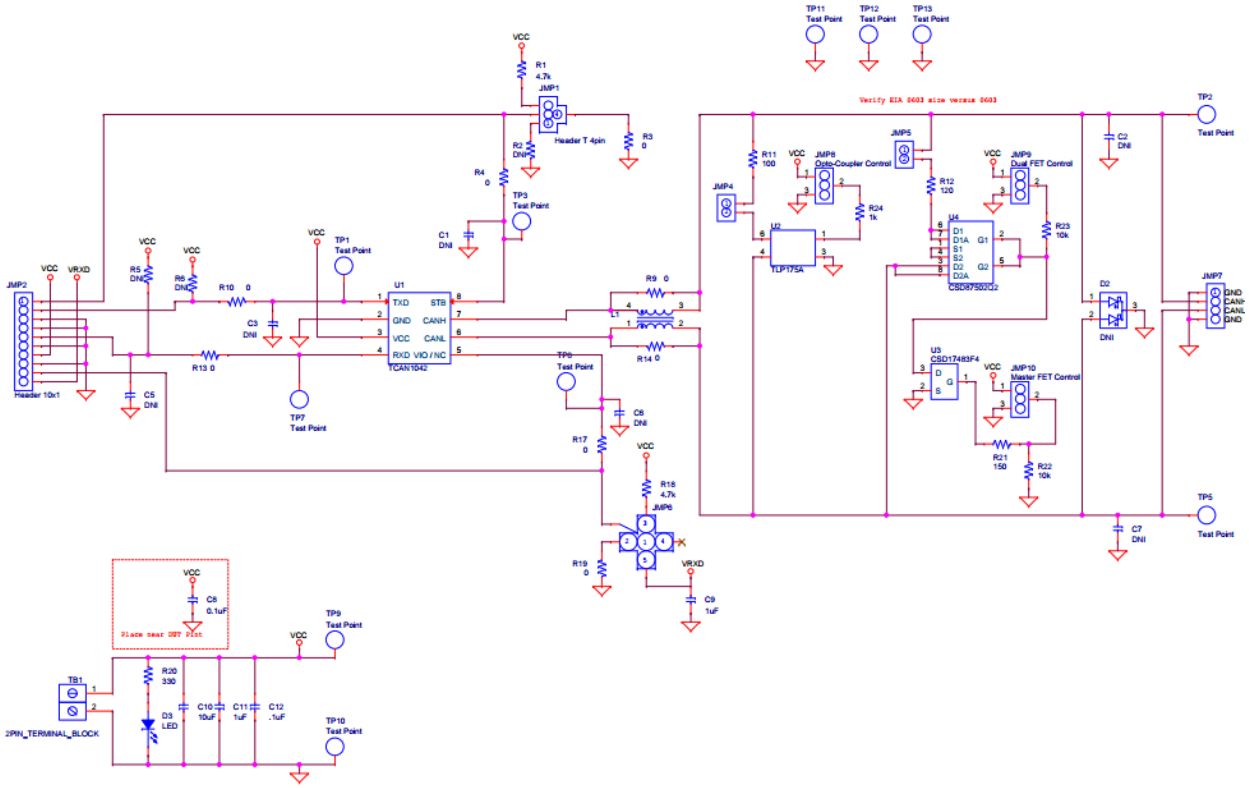


Figure 13: CAN Selectable Termination Evaluation Board Schematic

8.2 Bill of Materials

To download the Bill of Materials for each board, see the design files at http://www.ti.com/tool/TIDA-01238

Table 1: CAN Selectable Termination Bill of Materials

Ref Des	Value	Package_Case	Manufacturer	Manufacturer Part No
C1,C3	DNI	DNI	-	DNI
C5, C6	0.1µF	0805	Kemet	C0805C104J5RACTU
C2,C7	DNI	DNI	-	DNI
C8	0.1µF	0603	Murata Electronics North America	GRM188R71H104KA93D
C9,C11	1.0µF	0603	TDK Corporation	C1608X7R1C105K080AC
C10	10µF	1206	Taiyo Yuden	TMK316B7106KL-TD
C12	0.1µF	0402	Murata Electronics North America	GRM155R71C104KA88D
D2	DNI	DNI	-	DNI
D3	LED - Green Diffused	0805	Lumex Opto Components Inc	SML-LXT0805GW-TR
L1	DNI	DNI	-	DNI
R1,R18	4.70K	0805	Panasonic Electronic Components	ERJ-6ENF4701V
R2,R5,R6	DNI	DNI	-	DNI
R3,R4,R10,R13,R17,R19	0.0 (Zero Ohm)	0805	Yageo	RC0805JR-070RL
R9,R14	0.0 (Zero Ohm)	1206	Vishay Dale	CRCW12060000Z0EA-
R11	100	2512	Vishay/Dale	CRCW2512100RFKEG
R12	120	2512	Vishay Dale	CRCW2512120RFKEG
R20	330	0805	Panasonic Electronic Components	ERJ-6ENF3300V
R21	150	0805	Stackpole	RMCF0805FT150R
R22,R23	10.0K	0805	Vishay Dale	CRCW080510K0FKEA-
R24	1.00K	0805	Vishay Dale	CRCW08051K00FKEA-
U1	TCAN1042HGVDQ1	8-SOIC	Texas Instruments	TCAN1042HGVDQ1
U2	TLP175A(TPL,E	4-SMD	Toshiba Semiconductor and Storage	TLP175A(TPL,E
U3	MOSFET N-Channel, 42pF	0402 (3-XDFN)	Texas Instrument	CSD17483F4T
U4	CSD87502Q2	8-WSON	Texas Instruments	CSD87502Q2

8.3 PCB Layout Recommendations

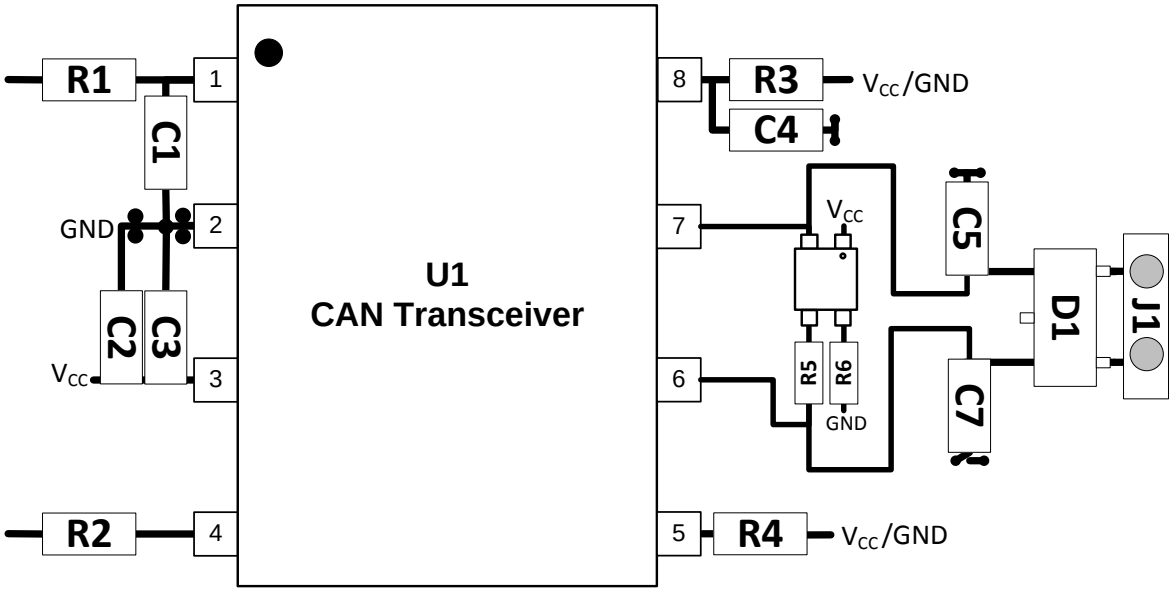


Figure 14: CAN Selectable Termination TLP175A Layout Example

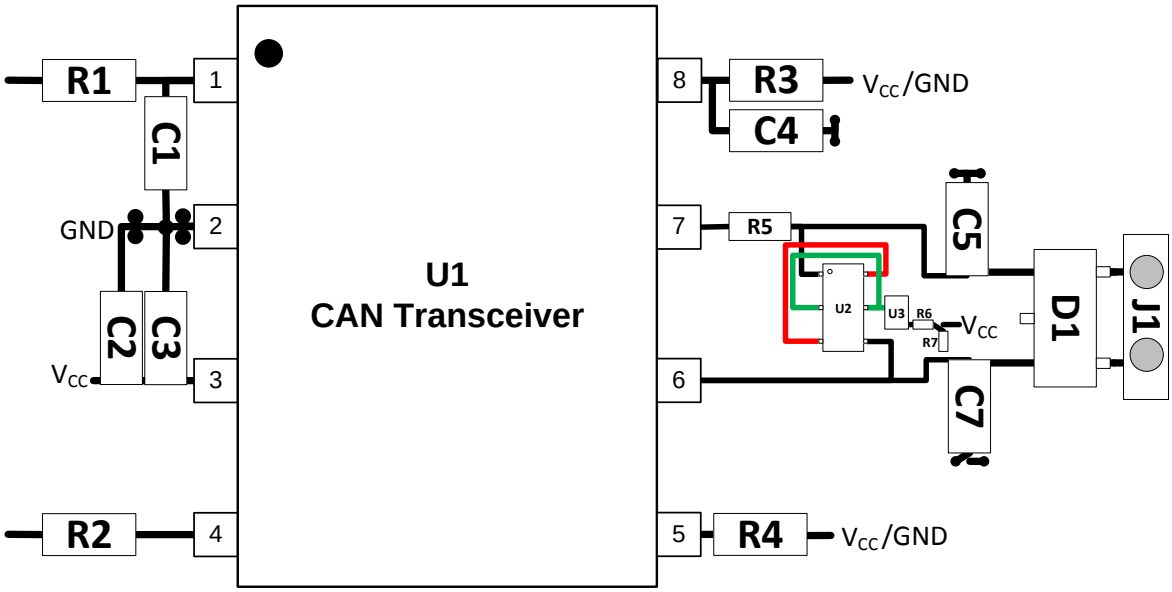


Figure 15: CAN Selectable Termination CSD87502Q2 and CSD17483F4 Layout Example

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. An example placement of the Transient Voltage Suppression (TVS) device is indicated as D1 (either bidirectional diode or varistor solution) and bus filter capacitors C5 and C7 are shown in Figure 15.

The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD, and noise from penetrating onto the board and disturbing other devices.

Bus termination: Figure 14 shows the termination scheme using the TLP175A photorelay. R5 is set to 100Ω with the photorelay providing approximately 20Ω of impedance. The

combination of R5 and the photorelay provide 120Ω of bus impedance to the for the CAN lines.

Bus termination: Figure 15 shows the termination scheme using the CSD87502Q2 and CSD17483F4 N_Channel MOSFETs. Once the FETs are biased R5 will provide the 120Ω termination resistance for the CAN bus lines.

Bypass and bulk capacitors should be placed as close as possible to the supply pins of transceiver. Examples include C2 and C3 (V_{CC}).

Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3, and R4.

To filter noise on the digital IO lines, a capacitor may be used close to the input side of the IO as shown by C1 and C4.

Because the internal pullup and pulldown biasing of the device is weak for floating pins, an external 1-kΩ to 10-kΩ pullup or pulldown resistor should be used to bias the state of the pin more strongly against noise during transient events.

Pin 1: If an open-drain host processor is used to drive the TXD pin of the device, an external pullup resistor between 1-kΩ and 10-kΩ should be used to drive the recessive input state of the device.

Pin 5: SPLIT should be connected to the center point of a split termination scheme to help stabilize the common-mode voltage to $V_{CC}/2$. If SPLIT is unused it should be left floating.

Pin 5: V_{IO} is input pin to a level shifter which controls the output voltage level of the RXD pin. R4 is an optional resistor and may not be needed in all applications.

Pin 8: Is shown assuming the mode pin, STB, will be used. If the device will only be used in normal mode, R3 is not needed and the pads of C4 could be used for the pulldown resistor to GND.

8.3.1 Layout Prints

To download the Layout Prints for each board, see the design files at http://www.ti.com/tool/TIDA-01238

TOP SILKSCREEN

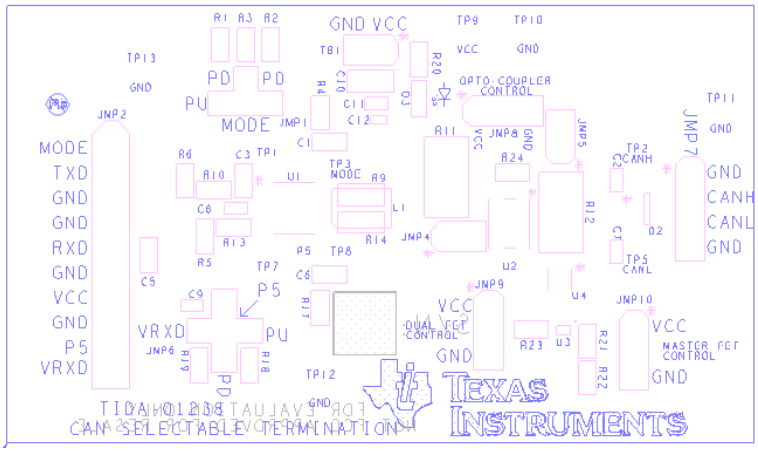


Figure 16: Top Silk

TOP SOLDER MASK

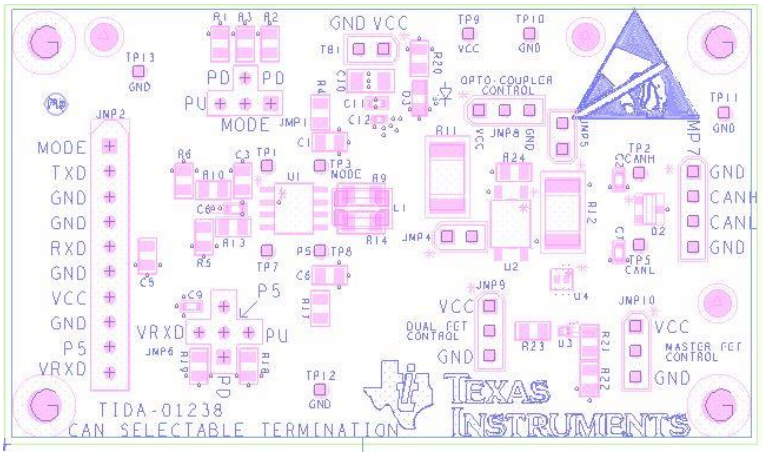


Figure 17: Top Solder Mask

TOP LAYER

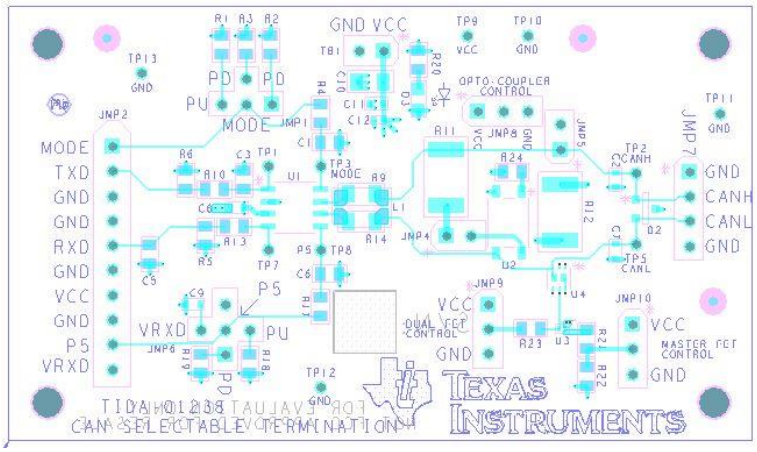


Figure 18: Top Layer

GROUND PLANE LAYER

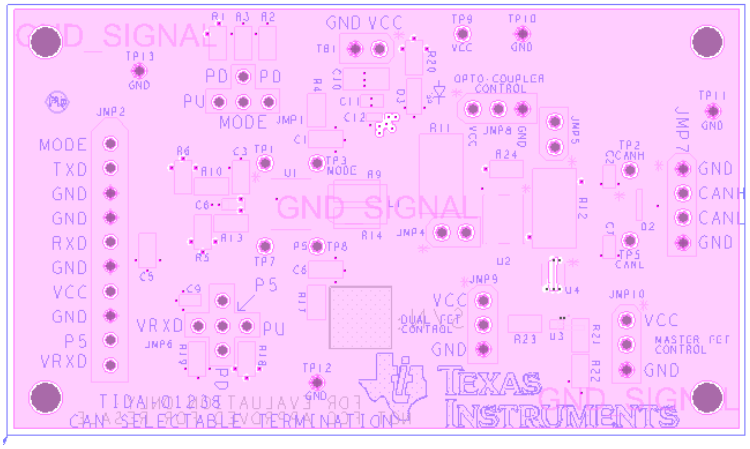


Figure 19: Ground Plane Layer 2

PWR PLANE LAYER3

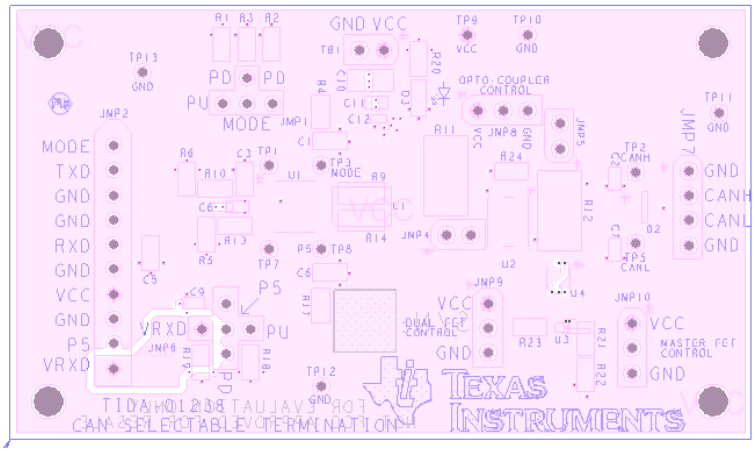


Figure 20: Power Plane Layer 3

BOTTOM LAYER

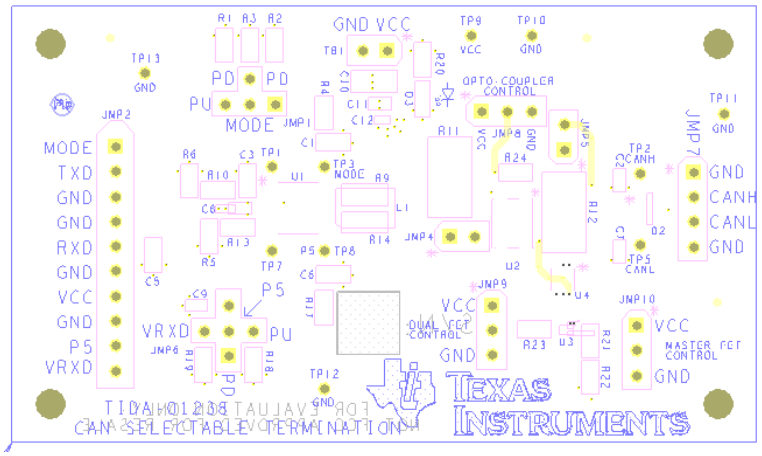


Figure 21: Bottom Layer

BOTTOM SOLDER MASK

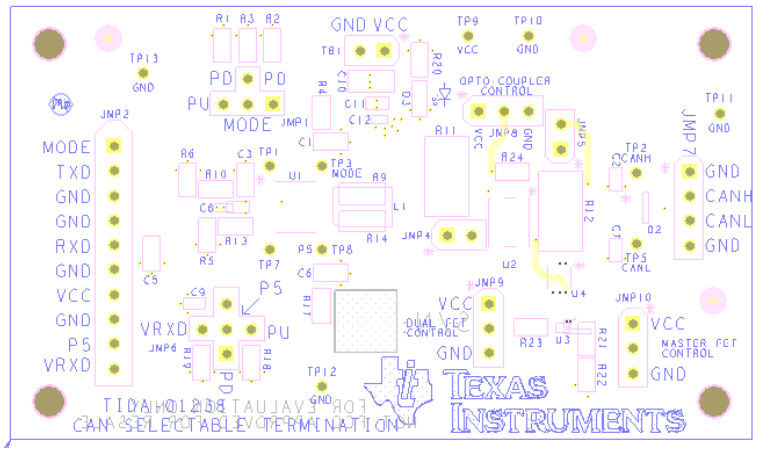


Figure 22: Bottom Layer Solder Mask

BOTTOM SILKSCREEN

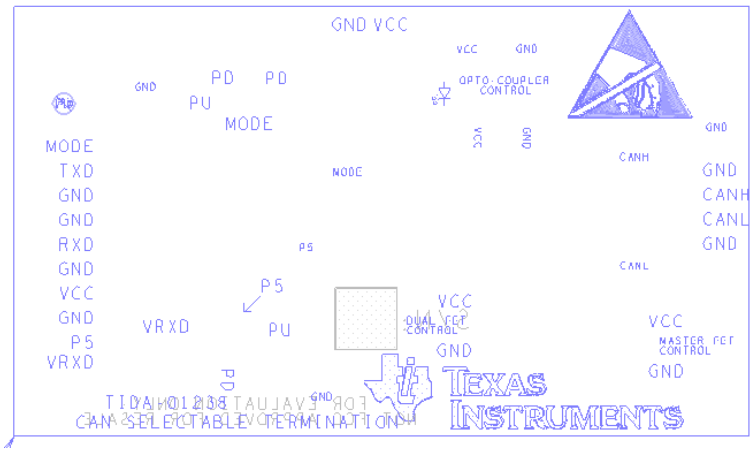


Figure 23: Bottom Silkscreen

MECHANICAL DIMENSIONS

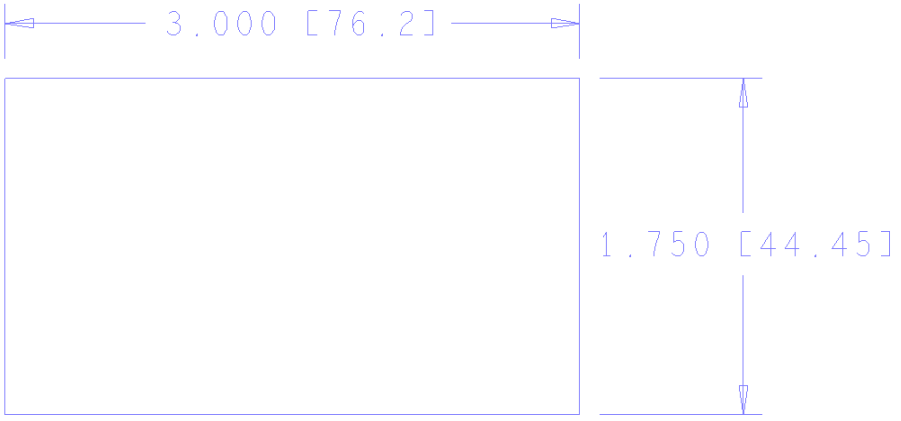


Figure 24: Mechanical Drawing

8.4 Gerber files

To download the Gerber files for each board, see the design files at http://www.ti.com/tool/TIDA-01238

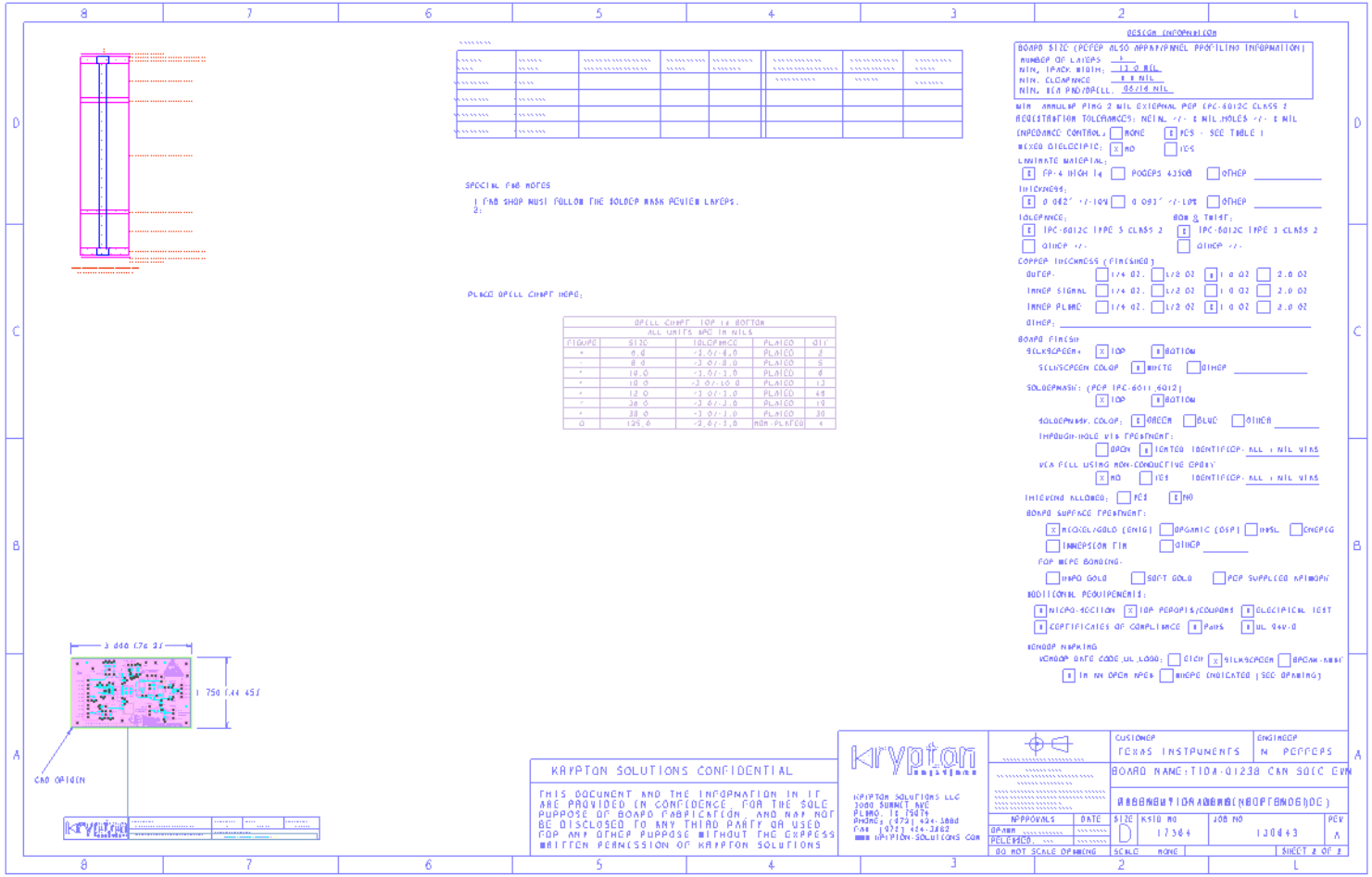


Figure 25: Gerbers

8.5 Assembly Drawings

To download the Assembly Drawings for each board, see the design files at http://www.ti.com/TIDA-01238

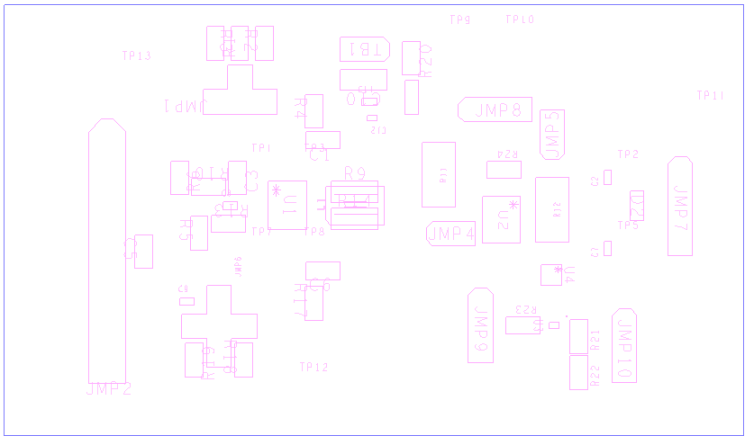


Figure 26: Assembly Drawing

9 References

1. Texas Instruments Application Report, Introduction to Controller Area Network (CAN), SLOA101A, 2002
2. Texas Instruments CAN Evaluation Module, TCAN EVM, 2015
3. Texas Instruments E2E Community, http://e2e.ti.com/support/interface/industrial_interface/

10 About the Author

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