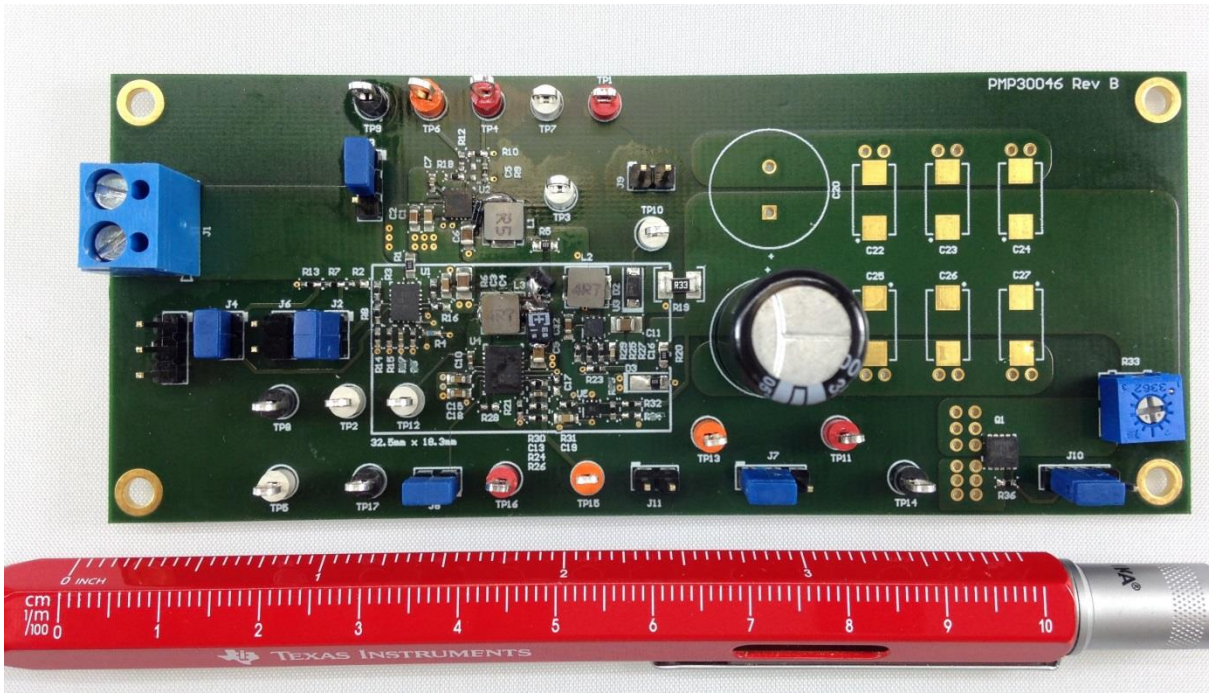
Enterprise SSD Backup Power Supply

- Input 5.0V or 12V
- Output 3.3V @ 2.5A, Backup Boost at 28V, Backup Buck 5V @ 2.5A
- Free-Running-Switching Frequency for TPS62130 2.5 MHz, for TPS61170 1.2MHz, for LM43603 500 kHz



1. Startup

The startup waveform at 5.0V input voltage and no load on the output is shown in Figure 1.

Channel Ch1 **5.0V Input Voltage**
5V/div, 2ms/div

Channel Ch2 **3.3V Output Voltage**
2V/div, 2ms/div

Channel Ch3 **28.0V Output Voltage**
20V/div, 2ms/div

Channel Ch4 **V Output Voltage**
1V/div, 2ms/div

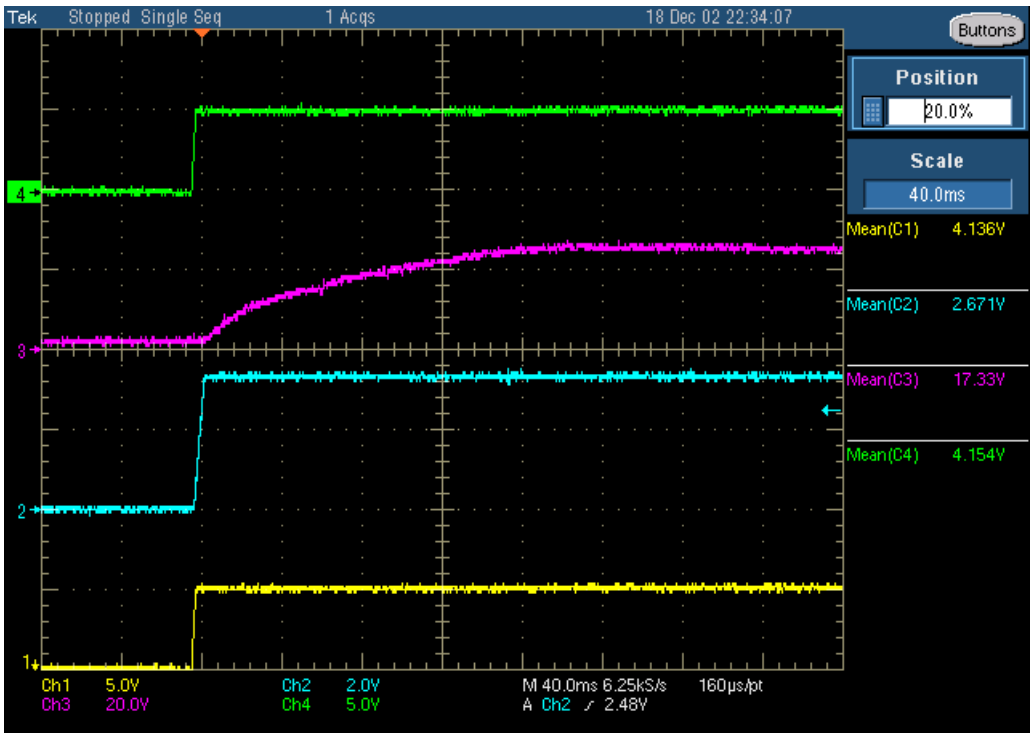


Figure 1

The startup waveform at 12.0V input voltage and no load on the output is shown in Figure 2.

Channel Ch1 **12.0V Input Voltage**
2V/div, 2ms/div

Channel Ch2 **3.3V Output Voltage**
2V/div, 2ms/div

Channel Ch3 **28.0V Output Voltage**
20V/div, 2ms/div

Channel Ch4 **3.3V Output Voltage**
1V/div, 2ms/div

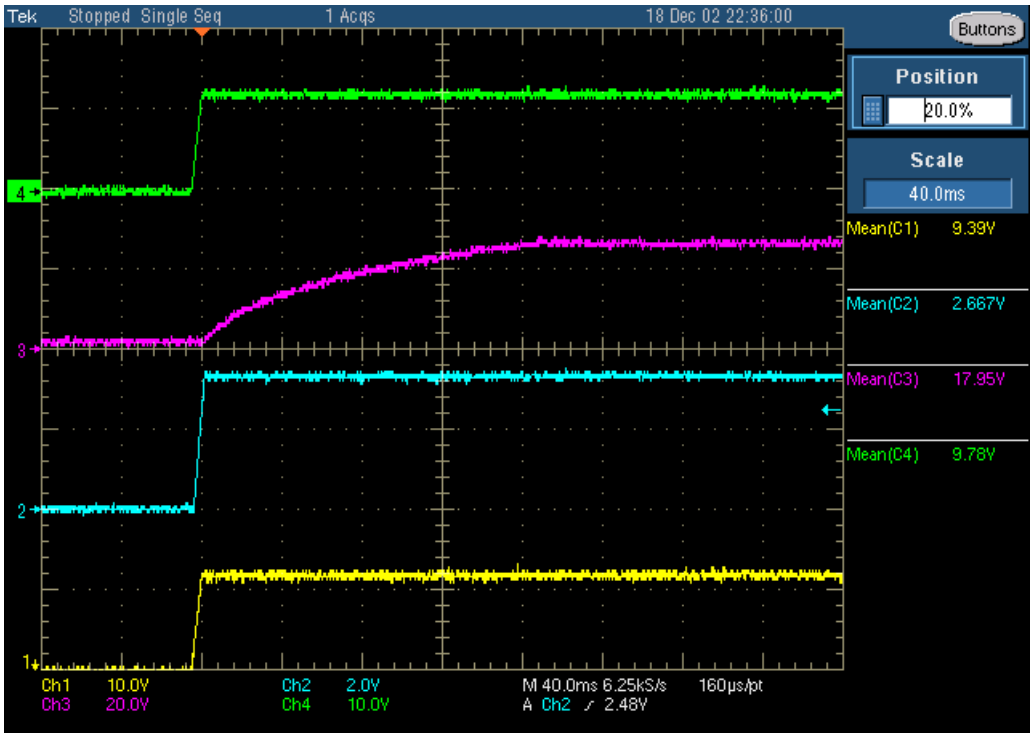


Figure 2

2. Shutdown

The shutdown waveform at 5.0V input voltage and 2.5A load on the 5V LM43603 output is shown in Figure 3.

Channel Ch1 **5.0V Input Voltage**
5V/div, 10ms/div

Channel Ch2 **3.3V Output Voltage**
2V/div, 10ms/div

Channel Ch3 **28.0V Output Voltage**
20V/div, 10ms/div

Channel Ch4 **LM43603 Switch Node**
20V/div, 10ms/div

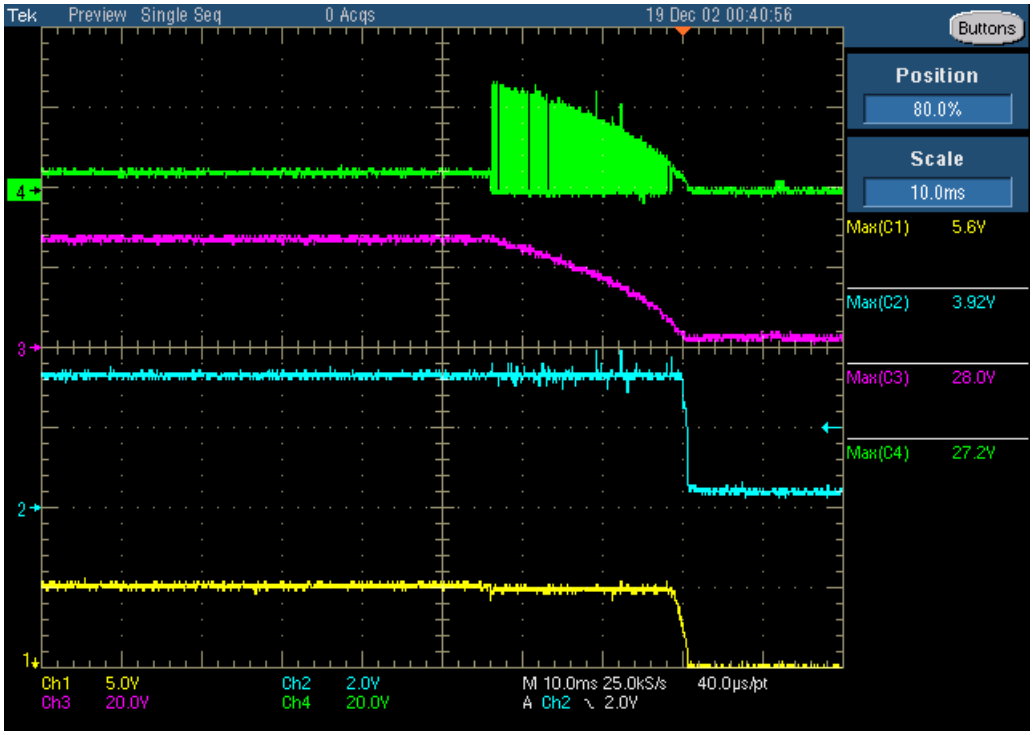


Figure 3

3. Efficiency

The efficiency and load regulation of the 3.3V TPS62130 Buck converter are shown in Figure 4 and Figure 5.

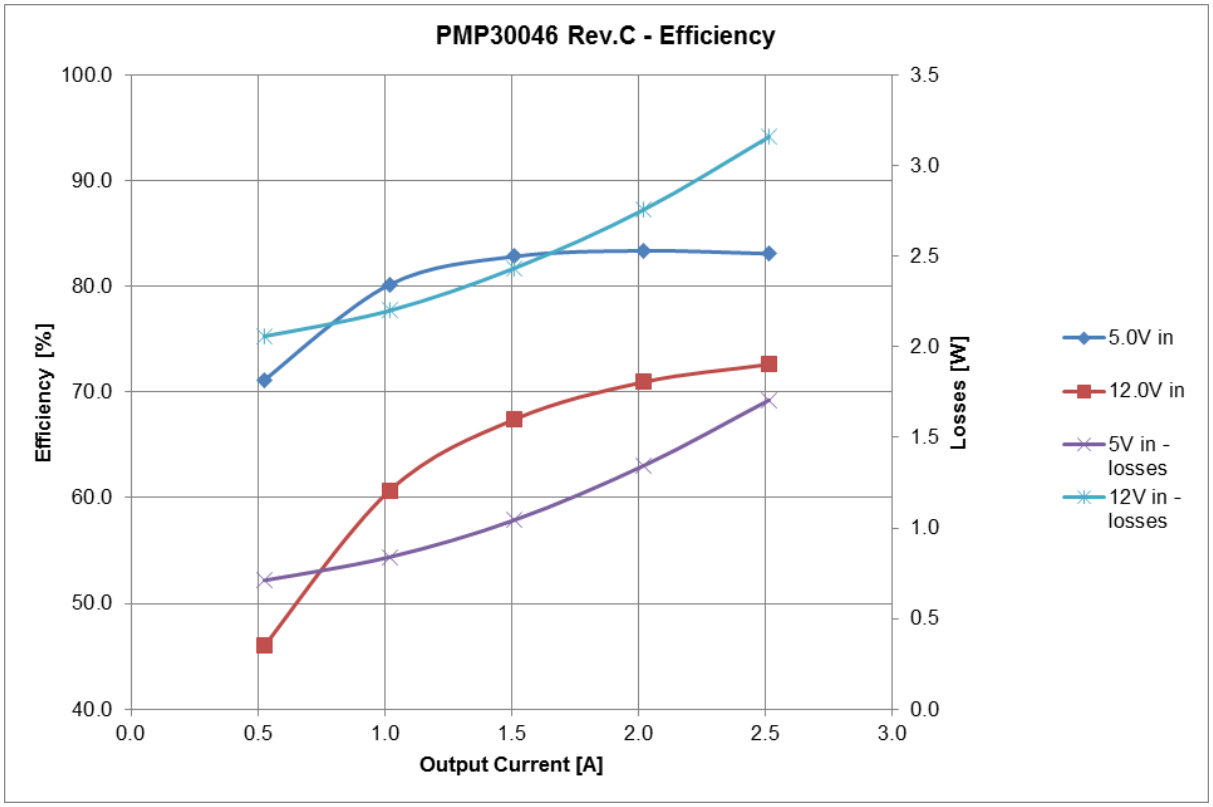


Figure 4

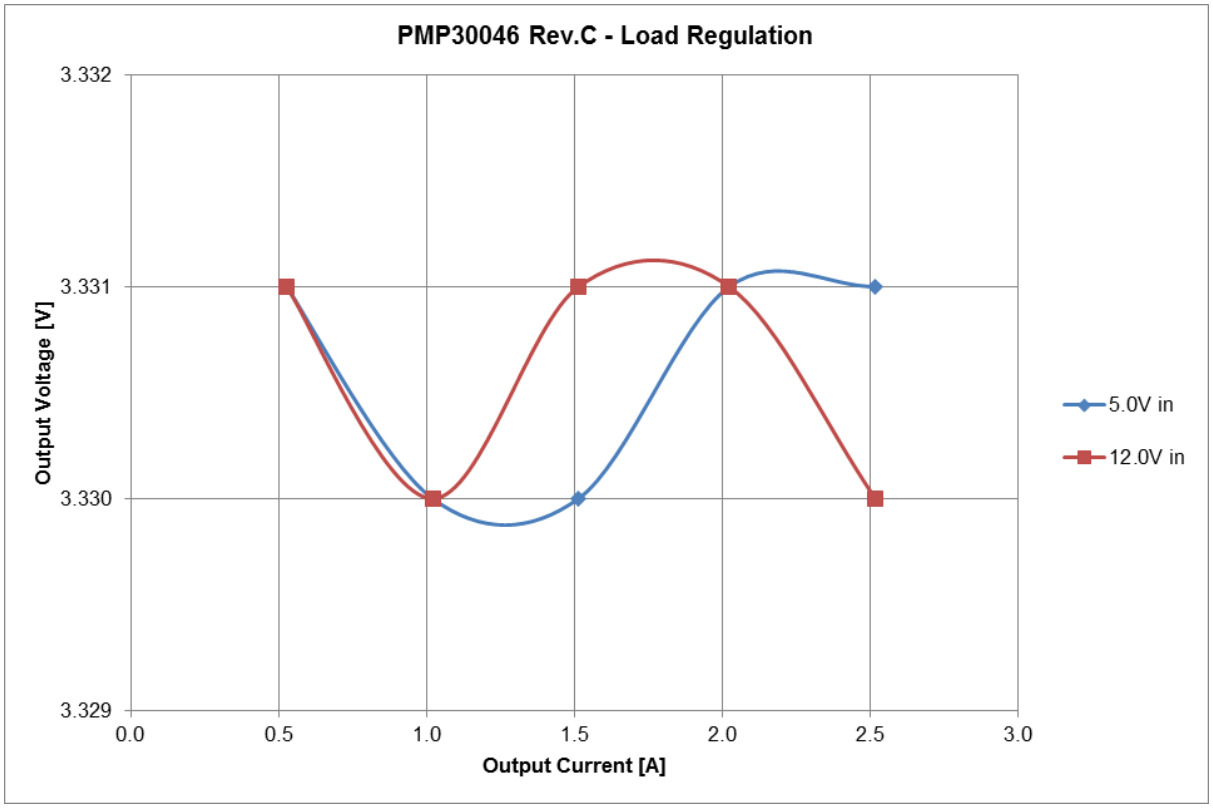

PMP30046 Rev.C - Load Regulation
3.332
3.331
3.330
3.329
Output Voltage [V]
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Output Current [A]
5.0V in
12.0V in

Figure 5

The efficiency and load regulation of the 5.0V LM43603 Buck converter are shown in Figure 6 and Figure 7.

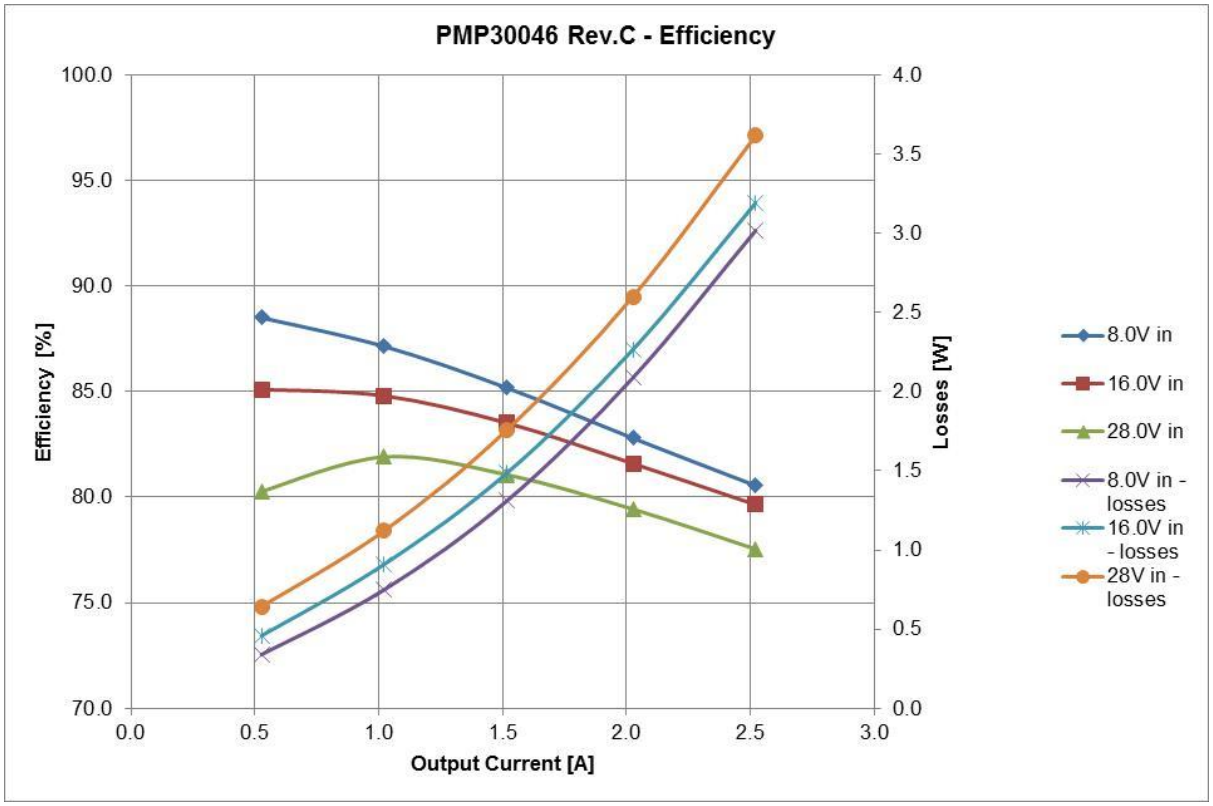


Figure 6

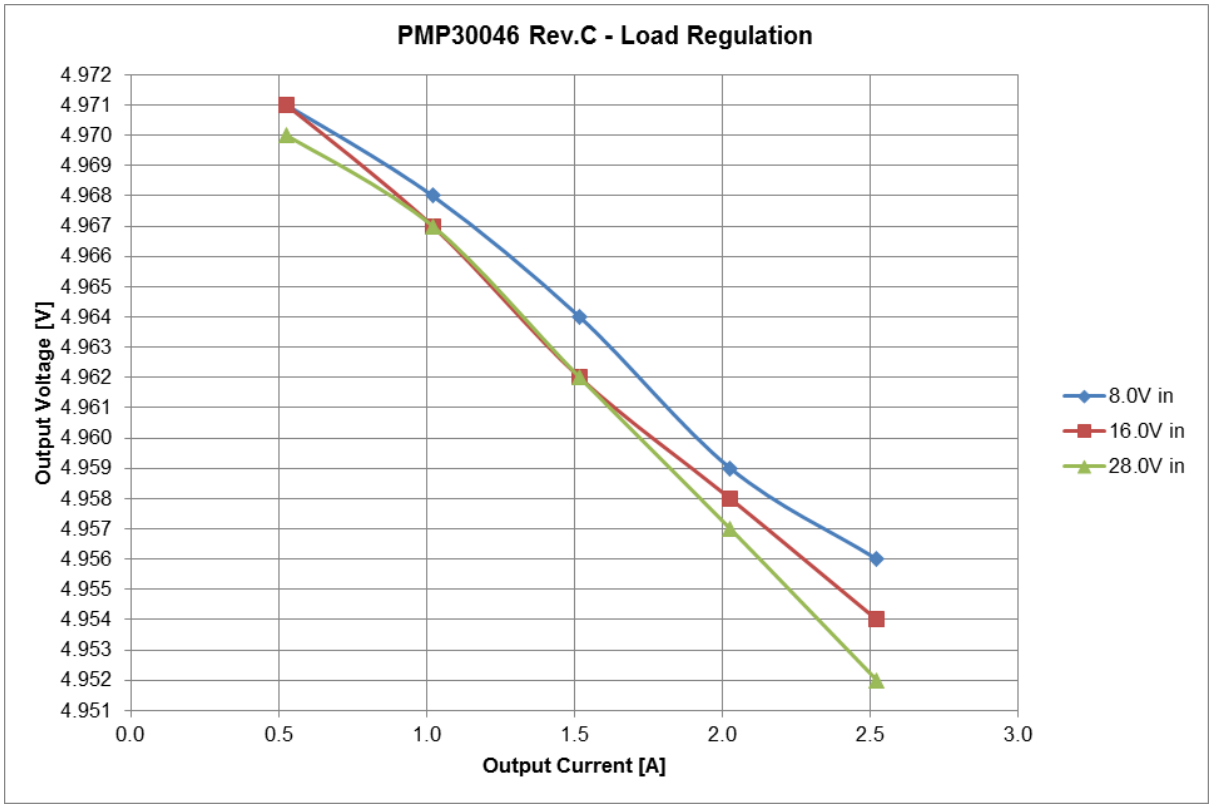

PMP30046 Rev.C - Load Regulation
Output Voltage [V]
4.972
4.971
4.970
4.969
4.968
4.967
4.966
4.965
4.964
4.963
4.962
4.961
4.960
4.959
4.958
4.957
4.956
4.955
4.954
4.953
4.952
4.951
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Output Current [A]
8.0V in
16.0V in
28.0V in

Figure 7

4. Transient Response

The response to a load step at 5.0V input voltage is shown in Figure 8.

Channel Ch3 **Output Current**, Load Step 1.25A to 2.5A
1A/div, 200µ s/div

Channel Ch1 **Output Voltage**, -24.8mV undershoot, 16mV overshoot
20mV/div, 200µs/div, AC coupled

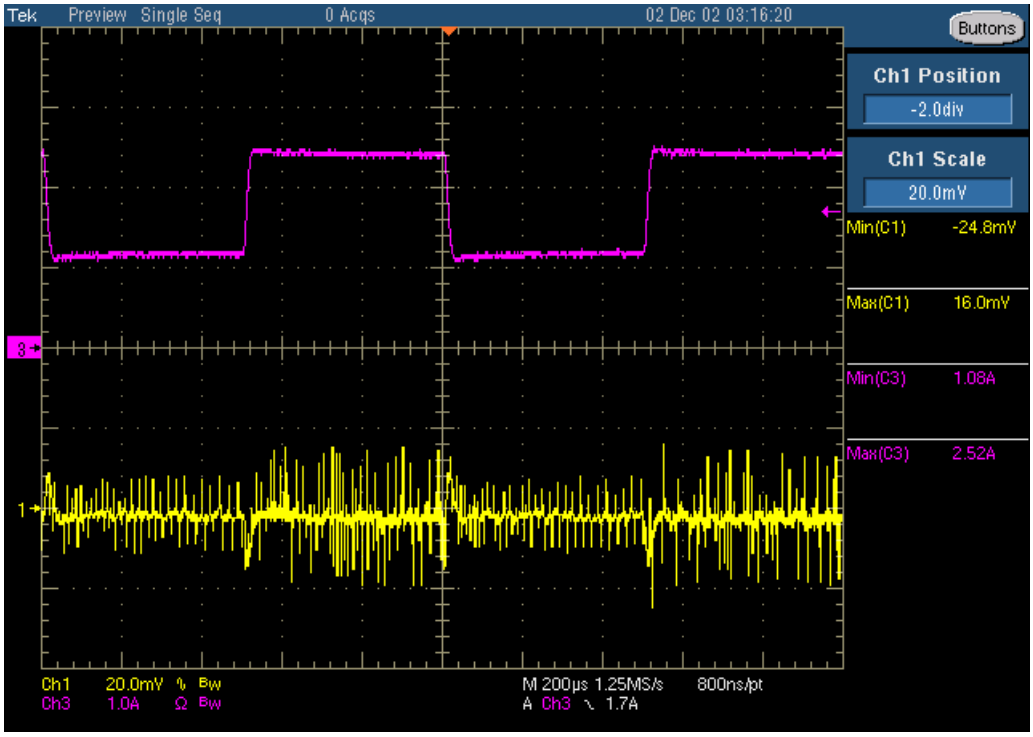


Figure 8

The response to a load step at 28.0V input voltage is shown in Figure 9.

Channel Ch3 **Output Current**, Load Step 0A to 2.5A
2A/div, 200µs/div

Channel Ch1 **Output Voltage**, -120mV undershoot, 88mV overshoot
200mV/div, 200µs/div, AC coupled

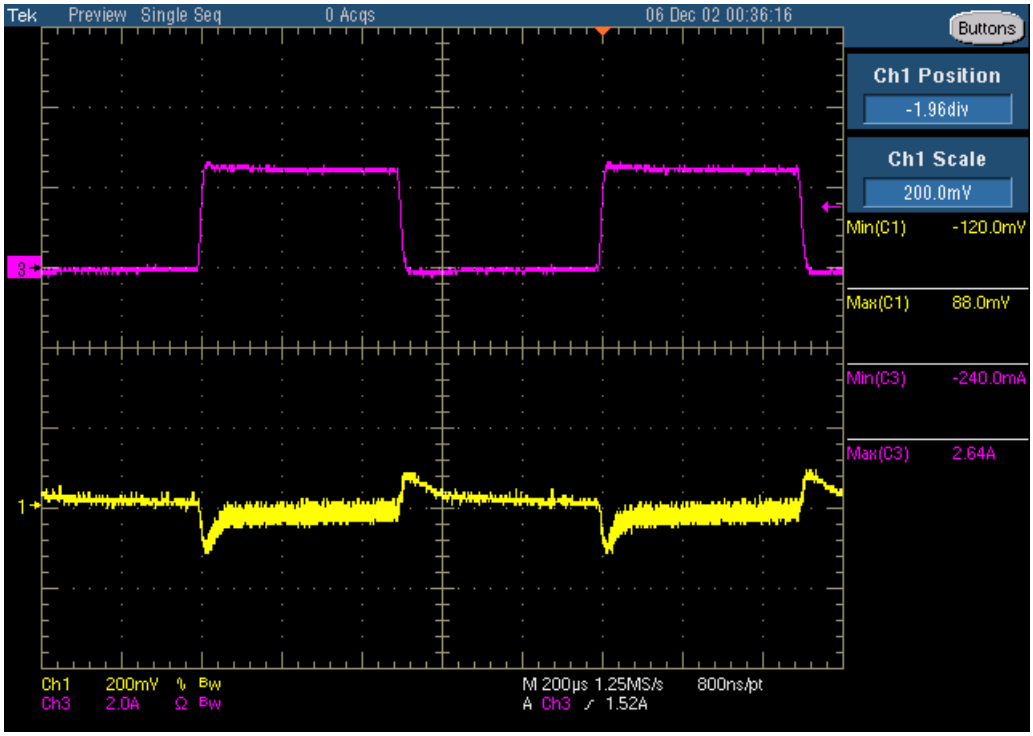


Figure 9

5. Frequency Response

The frequency response of the TPS62130 at 2.5A load is shown in Figure 10.

5.0V Input	21.2 kHz Bandwidth, 80 deg Phase Margin, -24 dB Gain Margin
12.0V Input	21.5 kHz Bandwidth, 80 deg Phase Margin, -25 dB Gain Margin

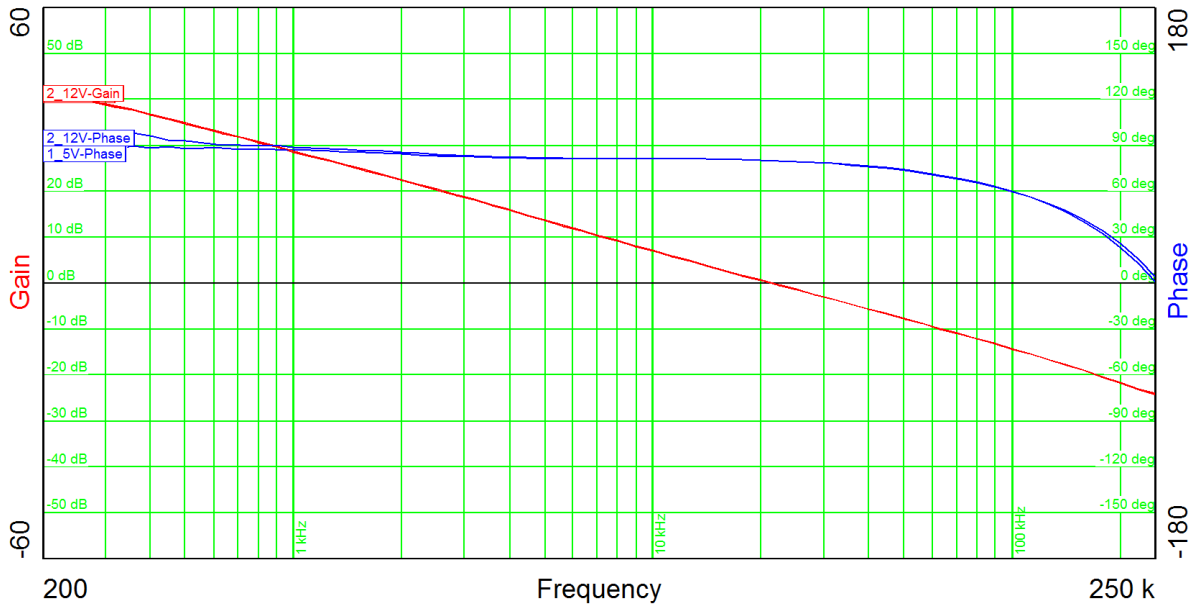


Figure 10

The frequency response of the TPS61170 at 0.07A load is shown in Figure 11.

3.3V Input 57.8 Hz Bandwidth, 75 deg Phase Margin, < -50 dB Gain Margin

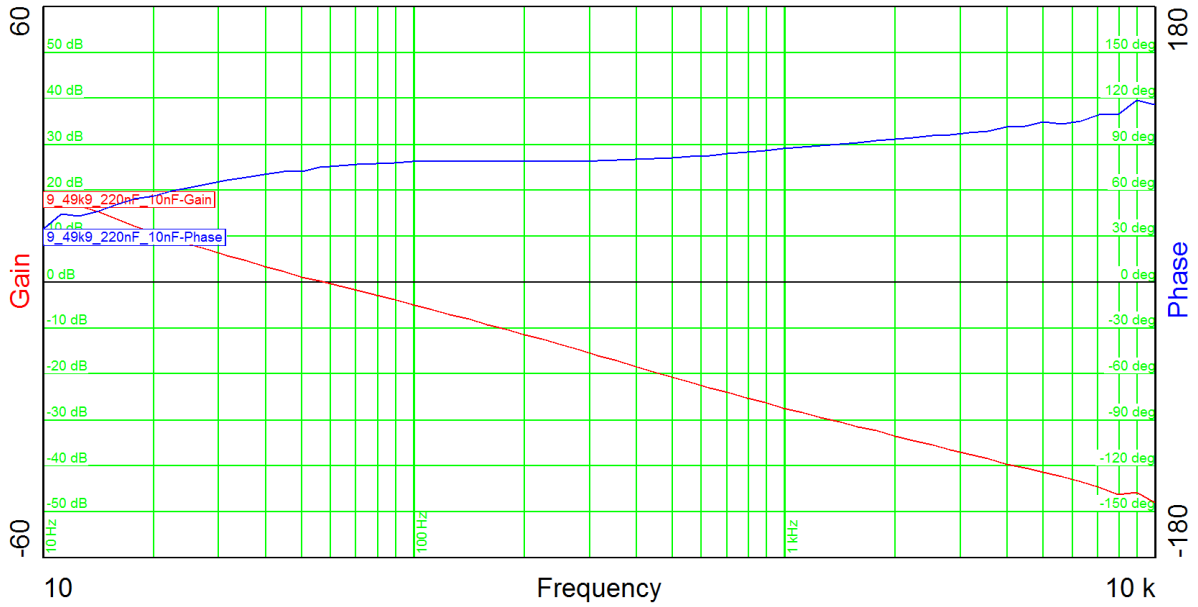


Figure 11

The frequency response at 16.0A load is shown in Figure 10.

8.0V Input	27.3 kHz Bandwidth, 81 deg Phase Margin, -14 dB Gain Margin
16.0V Input	25.1 kHz Bandwidth, 80 deg Phase Margin, -14 dB Gain Margin
28.0V Input	24.4 kHz Bandwidth, 79 deg Phase Margin, -15 dB Gain Margin

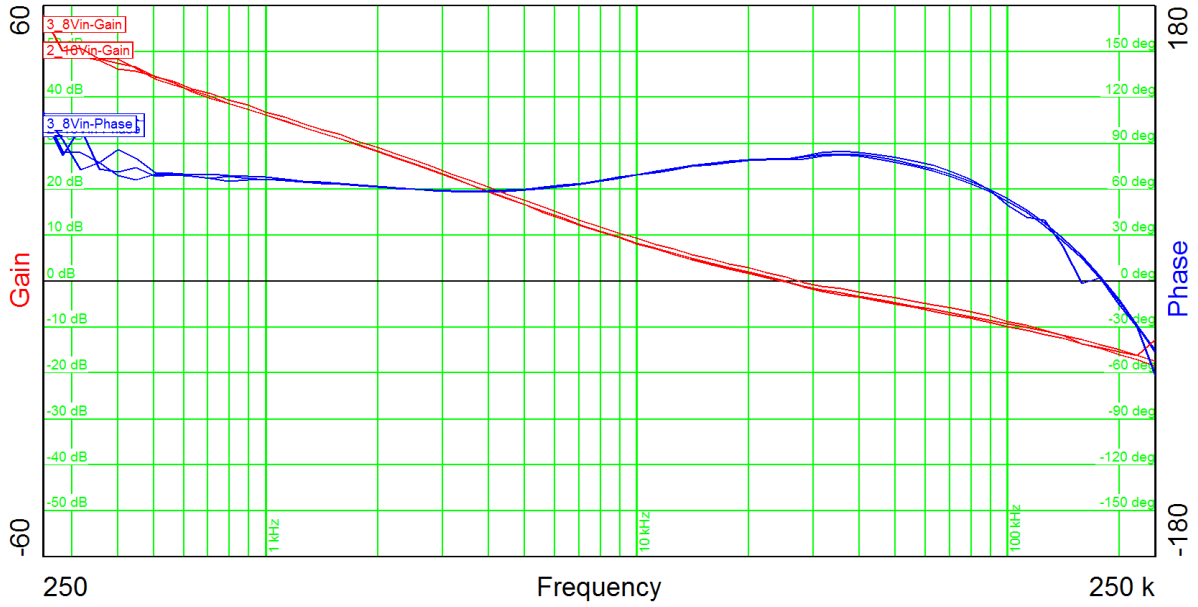


Figure 12

6. Output Ripple

The TPS62130 output ripple voltage at 2.5A load is shown in Figure 13.

Channel M1 **Output Voltage @ 5.0V Input**, 192mV peak-peak
200mV/div, 1us/div

Channel M2 **Output Voltage @ 12.0V Input**, 264mV peak-peak
200mV/div, 1us/div

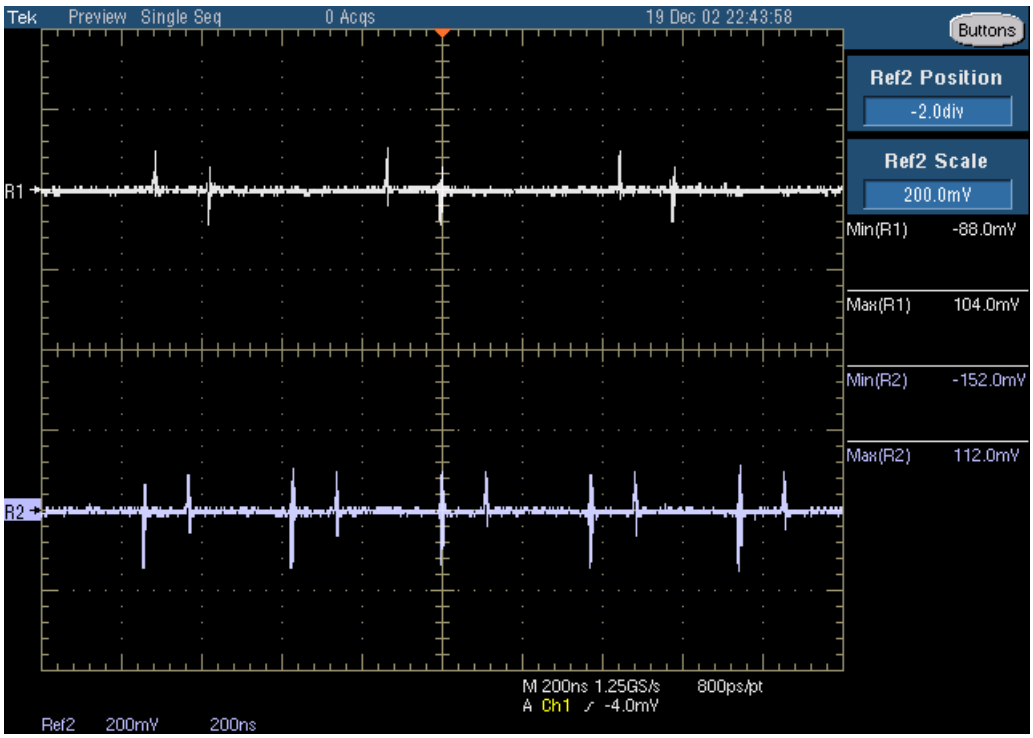


Figure 13

The LM43603 output ripple voltage at 2.5A load is shown in Figure 14.

Channel R1 **Output Voltage @ 8.0V Input**, 47.2mV peak-peak
50mV/div, 4us/div

Channel R2 **Output Voltage @ 16.0V Input**, 40.8mV peak-peak
50mV/div, 4us/div

Channel R3 **Output Voltage @ 28.0V Input**, 35.2mV peak-peak
50mV/div, 4us/div

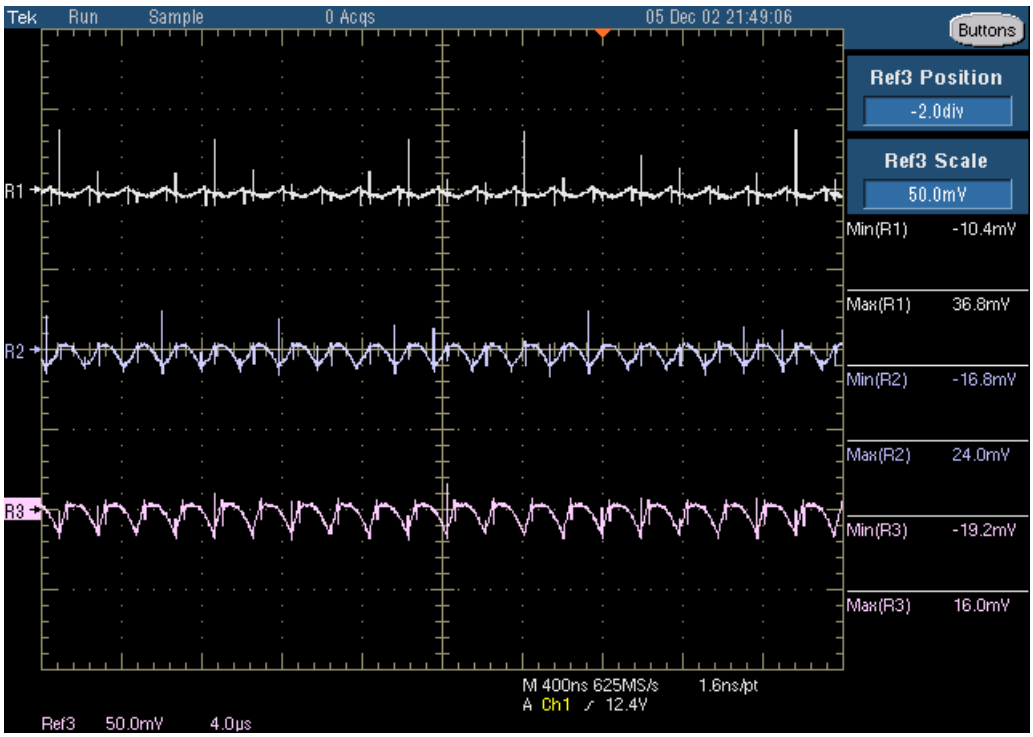


Figure 14

7. Switching Node

The drain-source voltage of the TPS62130 low-side FET at 12.0V input voltage and 2.5A load on the output is shown in Figure 15.

Channel Ch1 **Drain-Source Voltage**, -0.8V minimum, 13.4V maximum
5V/div, 80ns/div

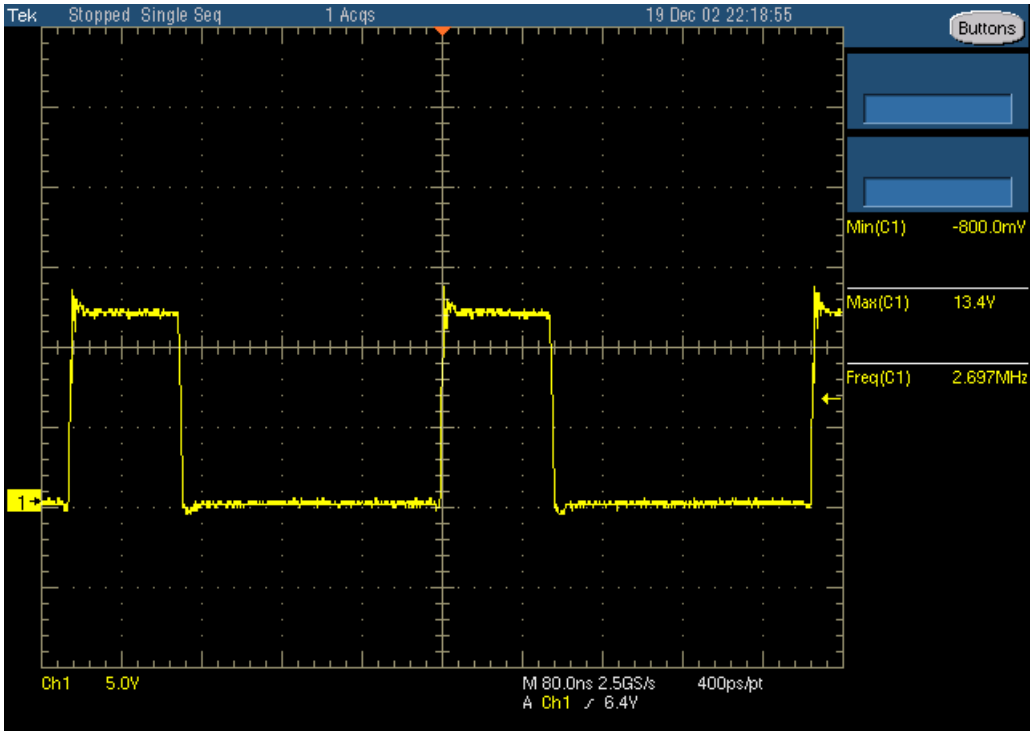


Figure 15

The drain-source voltage of the low-side FET at 28.0V input voltage and 2.5A load on the output is shown in Figure 16.

Channel Ch1 **Drain-Source Voltage**, -1.8V minimum, 29.0V maximum
5V/div, 400ns/div

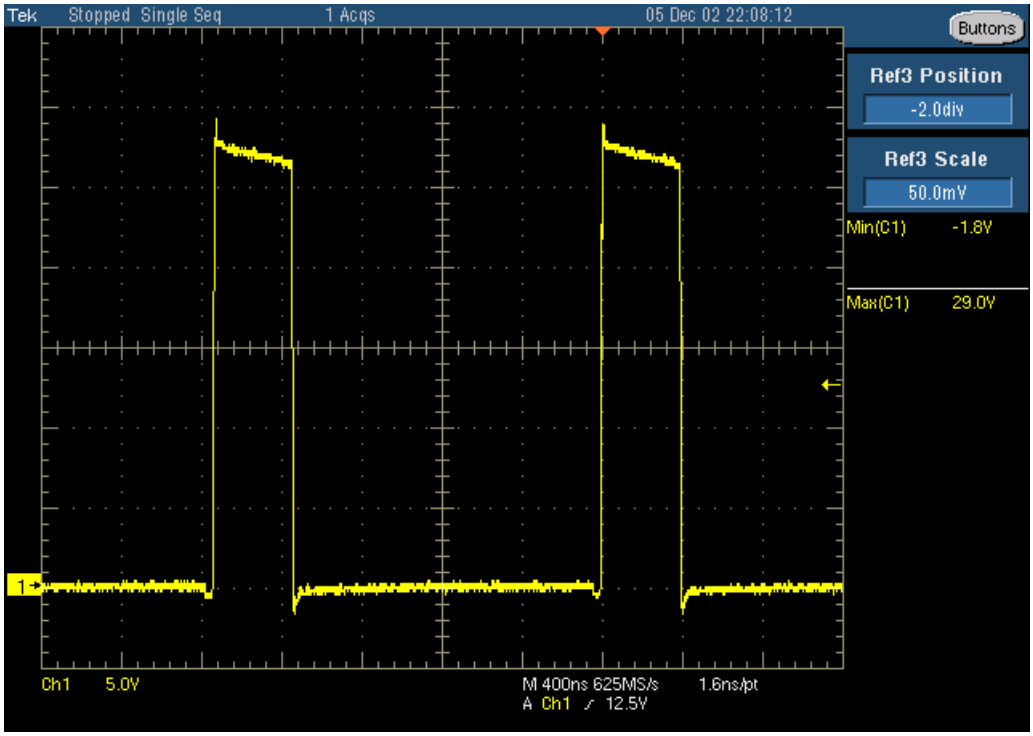


Figure 16

8. Thermal Image

The thermal image (Figure 17) shows the circuit at an ambient temperature of 20°C with an input voltage of 12.0V and 2.5A load on the 3.3V output.

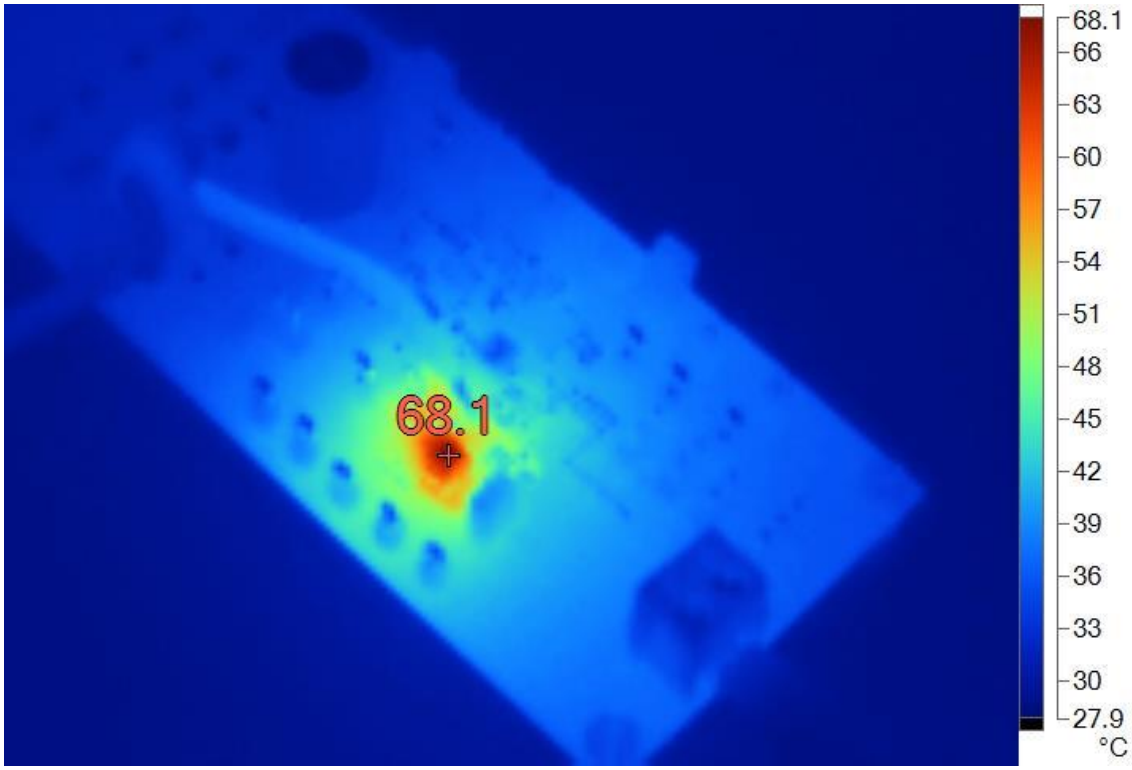


Figure 17

The thermal image (Figure 18) shows the circuit at an ambient temperature of 20°C with an input voltage of 5.0V and 2.5A load on the 3.3V output.

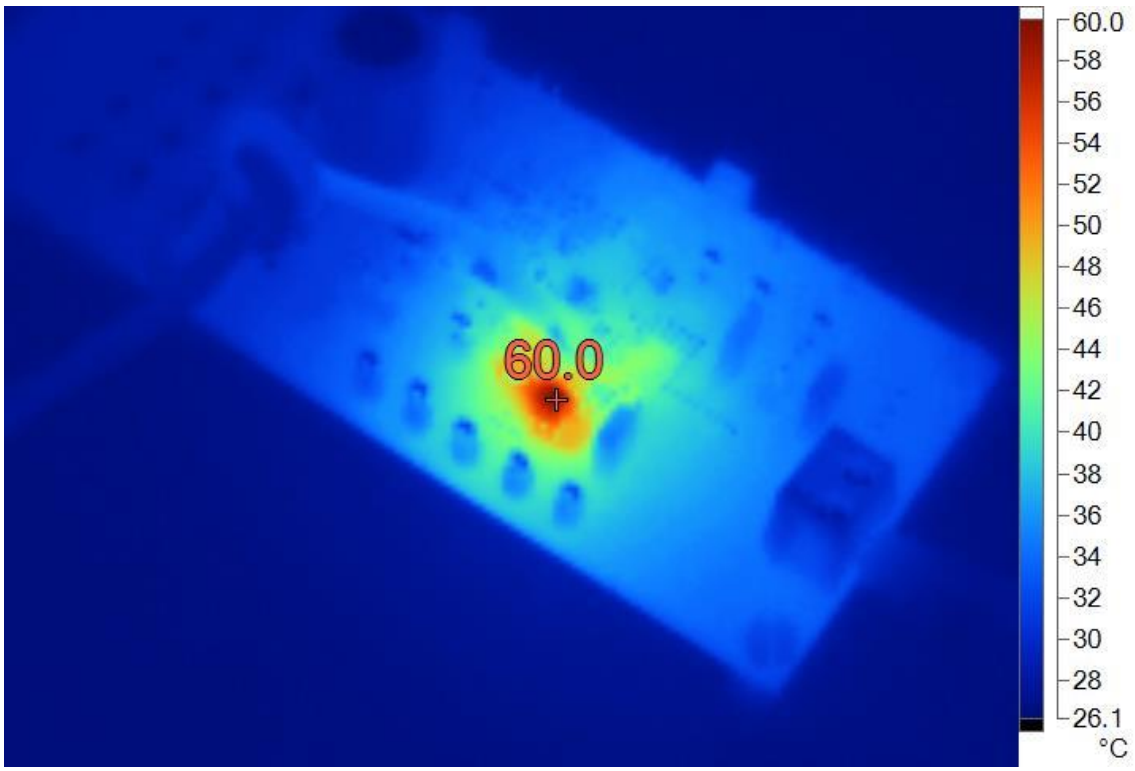


Figure 18

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