TI Designs

7.5-W, 1.25-A, Automotive Buck LED Driver Reference Design With Analog and PWM Dimming

Description

This TI Design showcases a TPS92515HV-Q1 small-form factor LED driver optimized to drive two LEDs for a fog light design. The buck topology is implemented as a direct-to-battery, single-stage LED driver to offer a simple and cost-effective lighting solution. Additional design flexibility includes analog and PWM dimming support as well as cycle-by-cycle current limit and integrated thermal shutdown protection. EMI filtering has been included and designed to meet CISPR-25, Class 3 conduction requirements.

Resources

PMP15004	Design Folder
TPS92515HV-Q1	Product Folder
TPS92515HV-Q1 Buck LED Driver EVM	Product Folder

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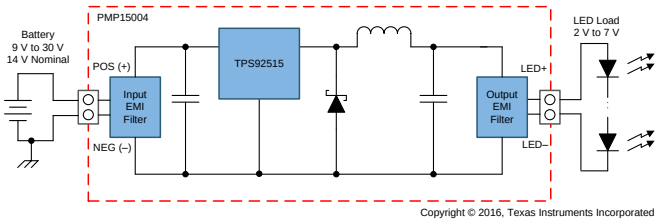
Features

- Optimized for Fog Lights and Other Small-Form Factor LED Lighting Applications
- CISPR-25 Tested EMI
- Stays Out of AM Band
- Analog and PWM Dimming
- Fast Transient Response With No Loop Compensation Required
- Cycle-by-Cycle Current Limit, Integrated Thermal Shutdown Protection, and Input Undervoltage Lockout
- Supports Load Dump up to 60 V

Applications

- Automotive Exterior Lighting:
  - Fog Lights, High and Low Beam Headlamps, DRL, Turn Signal, Side Marker
  - AFS LED Switched Matrix Headlamps
- Automotive Aftermarket Lighting
- Agricultural, Marine, Heavy Industry Lighting



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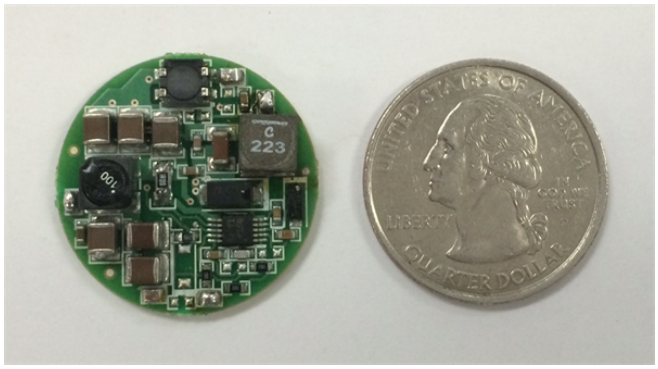

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1 System Overview

1.1 System Description

Styling, energy efficiency, and longevity are all factors that are causing widespread adoption of LEDs in place of incandescent light bulbs in automotive applications. Light-emitting diode (LED) lighting offers clear performance and reliability advantages over traditional light sources while enhancing the driver and passenger experience. However, short development cycles and intense competition puts pressure on automotive product vendors to reduce their time to market while still offering high-quality lighting solutions in terms of low electromagnetic interference (EMI), thermal efficiency, and light quality.

The PMP15004 reference design is a small-form factor, easy-to-adopt LED driver implementation that can be utilized in a broad range of automotive applications. This design uses the TPS92515HV-Q1, AEC-Q100-qualified LED converter, which has an integrated N-channel field-effect transistor (FET), contributing to a very streamlined design with a minimized printed-circuit board (PCB) footprint. The efficient buck topology accepts an input voltage range of 9 V to 30 V and has been optimized for driving one to two LEDs in series while meeting CISPR-25 Class 3 conducted EMI standards. Onboard analog and pulse-width modulation (PWM) dimming enables user-configured LED lighting calibration and precision dimming capability.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
VIN input voltage	—	9	14	30	V
VIN input voltage (load dump)	—	—	—	60	V
OUTPUT CHARACTERISTICS					
LED forward voltage	—	—	3	—	V
No. of LED in series	—	—	—	2	—
VLED output voltage	LED+ to LED–	—	6	8	V
ILED output current	—	—	1.25	—	A
Output power	—	—	7.5	—	W
Analog dimming range	V_{IADJ} = 0 V to 2.20 V	—	165:1	—	—
SYSTEM CHARACTERISTICS					
RR Inductor current ripple ratio	—	—	44	—	%
ΔIL-PP inductor current ripple	—	—	550	—	mA
ΔVIN-PP input voltage ripple	—	—	—	1.5	V
f_{SW} switching frequency	—	—	—	370	kHz
Efficiency	V_{IN} = 14 V, V_{OUT} = 6.1 V (two LEDs)	—	88.5		%
EMI (conducted)	—	CISPR-25 Class 3			
BASE BOARD CHARACTERISTICS					
Form factor	—	Diameter: 1 in (25.6 mm)			
No. of layers	—	2			
Height	—	0.26 in (6.6 mm)			

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1.3 Block Diagram

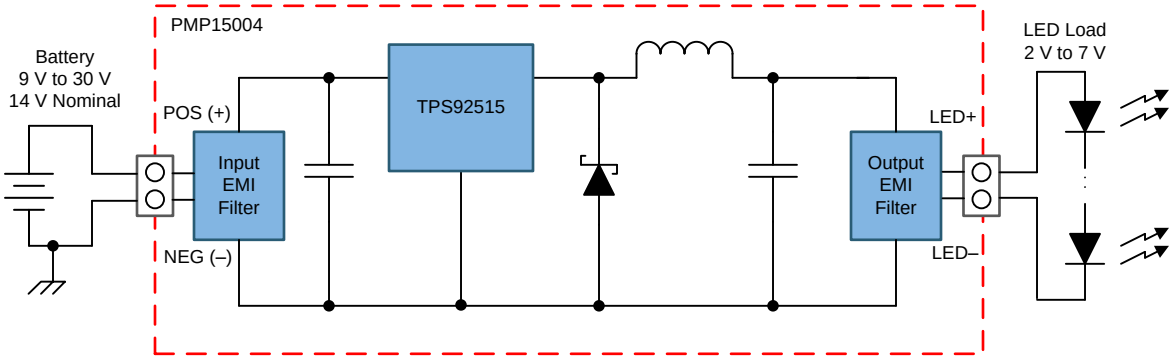

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Figure 1. PMP15004 Block Diagram

1.4 Highlighted Products

1.4.1 TPS92515HV-Q1

The TPS92515HV-Q1 is a compact, monolithic-switching regulator integrating a low-resistance N-Channel MOSFET (see Figure 2). The device is intended for high-brightness LED lighting applications where efficiency, high bandwidth, small size, PWM or analog dimming (or both) are important.

The regulator operates using a constant OFF-time, peak current control. The operation is simple: after an OFF-time based on the output voltage, an ON-time begins. The ON-time ends when the inductor peak current threshold has been reached. The TPS92515HV-Q1 device can be configured to maintain a constant peak-to-peak ripple during the ON and OFF periods of a shunt FET dimming cycle. This configuration is ideal for maintaining a linear response across the entire shunt FET dimming range.

Steady-state accuracy is aided by the inclusion of a low-offset, high-side comparator. LED current can be modulated using either analog dimming, PWM dimming, or both simultaneously. Other features include undervoltage lockout (UVLO), wide input voltage operation, open and overvoltage protection (OVP) operation, and wide-operating temperature range with thermal shut-down.

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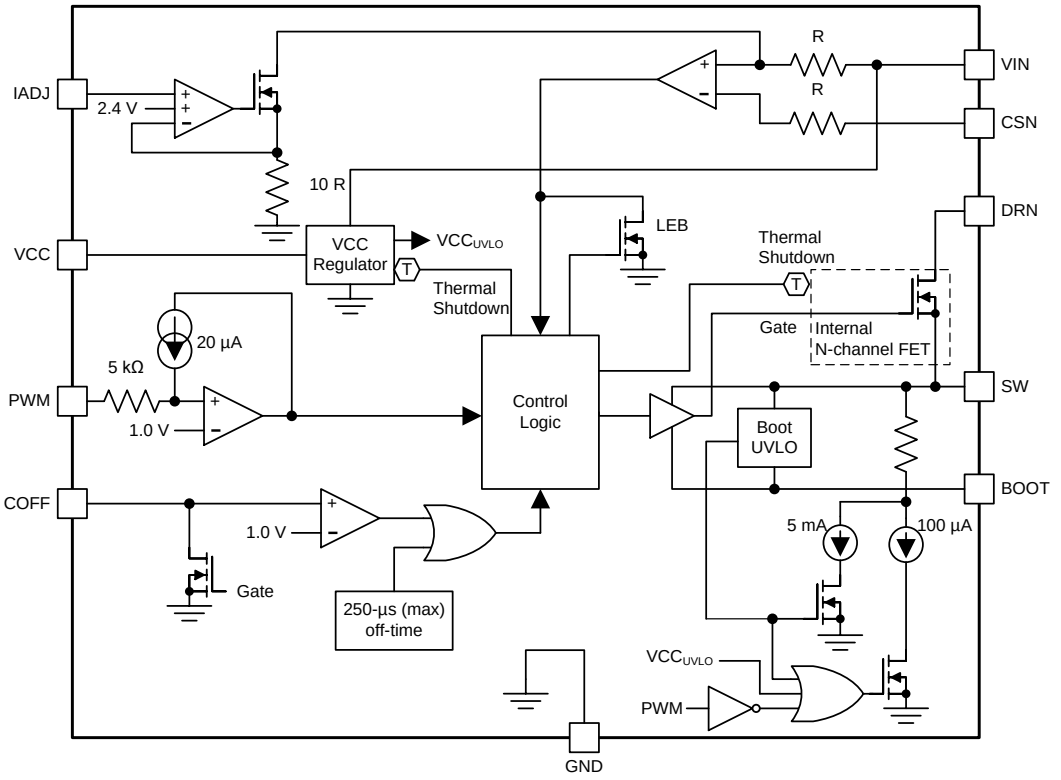

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Figure 2. TPS92515 Block Diagram

The TPS92515-Q1 device has an operational input range up to 42 V. The TPS92515HV-Q1 is a high-voltage option with an input range up to 65 V. Each device is available in a thermally enhanced 10-pin HVSSOP package.

Features:

- AEC-Q100 Grade 1 qualified
- Integrated 290-mΩ (typ) internal N-channel FET
- Input voltage range:
  - TPS92515x: 5.5 V to 42 V
  - TPS92515HVx: 5.5 V to 65 V
- Operation down to 5.15 V after start-up
- Low offset high-side peak current comparator
- Constant average current, up to 2 A
- Inherent cycle-by-cycle current limit
- Multiple dimming methods
- 10,000:1 shunt PWM dimming range
- 1000:1 PWM dimming range
- 200:1 analog dimming range
- Simple constant off-time control
- No loop compensation
- Fast transient response
- Thermally-enhanced HVSSOP package
- Integrated thermal protection

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2 System Design Theory

This design consists of a high-performance LED controller integrated circuit (IC) with an integrated FET configured in a buck (step-down) topology with EMI filtering at both the input and output (see Figure 3). The input voltage range is 9 V to 30 V, which makes this LED driver compatible for direct-to-battery type configurations. This design supports 1.25 A of output current and an output power rating of just under 8 W. The design has been optimized to drive two high-brightness LEDs in series (assuming an LED forward voltage of 3 V) from a typical voltage supply of 14 V. However, multiple combinations of input supplies and LED loads can easily be created using this TI Design as a starting point.

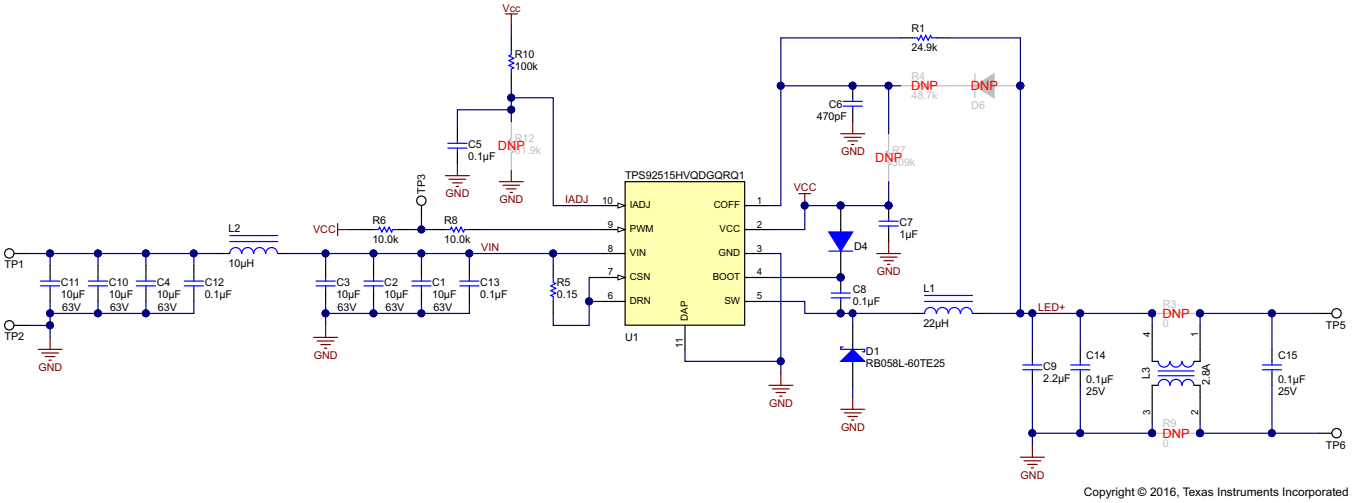

Figure 3. PMP15004 Schematic

2.1 Analog Adjust Input (IADJ) and Analog Dimming

The analog adjust pin (IADJ) provides the reference for the peak inductor current trip point. This threshold is then used to establish the default output current level for this design, which is 1.25 A. The IADJ voltage is tied to VCC through resistor R10, which results in the V_{IADJ} voltage being clamped internally to 2.4 V. Connecting the IADJ pin directly to VCC is the simplest configuration and the most accurate stand-alone implementation.

Other configurations utilizing the IADJ pin include thermal foldback, interfacing with a microcontroller (MCU), implementing a soft-start sequence, and so forth. Refer to the product data sheet for further details on these options.

If analog dimming is required, an external voltage between 0 V and 2.4 V can be applied directly to the IADJ pin to provide an analog dimming function. An analog dimming range of 165:1 is attainable with this TI Design.

2.2 PWM Dimming

The default PWM pin voltage for this design is approximately 2.5 V as set up by the resistor divider (consisting of R6 and R8), from VCC to GND. This default voltage ensures that the TPS92515HV-Q1 starts up and operates properly when input power has been applied.

Additionally, PWM dimming can be implemented by applying a signal above 1 V (typical) and below 900 mV (typical) at test point TP3. This design has been tested with PWM frequencies from 240 Hz to 5 kHz. When using higher frequencies (greater than 5 kHz), the delays from PWM to gate turn ON and turn OFF can begin to limit the achievable duty cycle. In this situation, TI recommends the designer consider using a shunt FET PWM solution with the TPS92515HV-Q1, which is further described in the product data sheet.

2.3 Switching Frequency and OFF Time

For a fixed LED load, the switching frequency of the TPS92515HV-Q1 increases as the input voltage, V_{IN}, increases, as Figure 4 shows.

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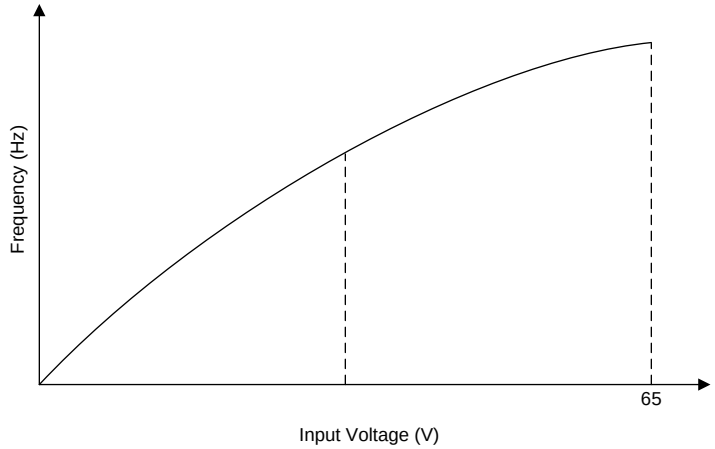

Figure 4. Frequency versus Input Voltage V_{IN} (Fixed LED Voltage)

To prevent this design from operating in the AM band (that is, below 540 kHz), the maximum specified V_{IN} and switching frequency are used to calculate the OFF time, t_{OFF}, and associated component values.

Using the following Equation 1, Equation 2, and Equation 3 (found in the product data sheet), duty cycle (D) and off-time (t_{OFF}) can be calculated. Component values can then be selected to meet the design criteria for this LED driver.

$$D = \frac{V_{LED}}{V_{IN} \times n} \tag{1}$$

$$t_{OFF} = \left(\frac{1}{f_{SW}}\right) \times (1 - D) \tag{2}$$

$$R_{OFF} = \frac{t_{OFF}}{-C_{OFF}\left(\ln\left(1 - \frac{V_{OFT}}{V_{LED}}\right)\right)} \tag{3}$$

From Equation 1 and using an output voltage (V_{LED}) of 6 V, maximum input voltage (V_{IN}) of 30 V, and a target efficiency (n) of 90%, the duty cycle (D) is calculated as 22.2%. With a maximum frequency (f_{SW}) of 370 kHz, the OFF time is calculated to be 2.10 µs using Equation 2. The typical OFF-time threshold (V_{OFT}) is 1 V, and by using the data sheet recommended 470 pF for the OFF-time capacitor C_{OFF} (C6), the OFF-time resistor R_{OFF} (R1) is calculated to be 24.5 kΩ using Equation 3.

For this design, a resistor value of 24.9 kΩ has been chosen for R1.

2.4 Inductor Selection and Current Ripple

Choosing an inductor requires a balance between inductor current ripple, efficiency, physical size, and thermal considerations. A higher inductance value reduces current ripple but may require a physically larger inductor to handle a specific inductor current and maintain acceptable efficiency (with a lower-winding resistance DCR) and thermal dissipation. However, implementing a physically larger inductor then impacts the overall PCB footprint, headroom, and the overall potential design cost.

The inductor and the current ripple specification have been carefully chosen to provide an optimized balance of LED regulation performance, physical size, PCB footprint, and thermal dissipation. With the 1.25-A LED current and 44% inductor ripple ratio specification, the peak-to-peak inductor current ripple (ΔI_{L-PP}) is set at 550 mA. Using Equation 4, the calculated inductance is 22.9 µH.

$$L = \frac{V_{LED} \times t_{OFF}}{\Delta I_{L-PP}} \tag{4}$$

For this LED driver, a 22-µH inductor has been chosen for L1.

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2.5 Calculating Sense Resistor

The sense resistor R5 in now calculated using Equation 5. Because the IADJ pin is tied to V_{CC}, the V_{IADJ} reference voltage is clamped at 2.4 V.

$$R_{SENSE} = \frac{\left(\frac{V_{IADJ}}{10}\right)}{I_{LED} + \frac{\left(\Delta I_{L-PP}\right)}{2}} \quad (5)$$

The calculated sense resistance is 0.157 Ω. For this design, a 0.15-Ω resistor has been chosen for R5.

2.6 Verify Peak Current for Inductor Selection

Using the selected sense resistor and Equation 6, the peak inductor current is calculated as 1.6 A. Inductor L1 has been selected to meet this minimum peak current rating.

$$IL_{PEAK} = \frac{\left(\frac{V_{IADJ}}{10}\right)}{R_{SENSE}} \quad (6)$$

2.7 Input Capacitance

Per the product data sheet, the voltage ripple (ΔV_{IN-PP}) must not exceed 10% of the input voltage (V_{IN}) or 2 V, whichever is lower. Because this design can operate up to an input voltage of 30 V, the maximum voltage ripple is 2 V. However, the minimum capacitance must also be based on the lowest-operating switching frequency, which occurs at an input voltage of 9 V for this design . Using Equation 1 and Equation 2 with the previously calculated off-time of 2.10 µs and an input voltage of 9 V results in a frequency of 123 kHz. Using this information with Equation 7, the minimum input capacitance is calculated as 3.8 µF.

$$C_{IN-MIN} = \frac{I_{LED} \times \left(\frac{1}{f_{SW}} - t_{OFF}\right)}{\Delta V_{IN-PP}} \quad (7)$$

If using PWM dimming, then a larger input capacitor is required to supply the initial current required for the LED driver to reach the current regulation set-point. A general rule for PWM dimming applications is to use a capacitance value that is ten times greater than the value calculated for non-PWM dimming designs.

For this particular design, an EMI input filter is required to pass CISPR-25 Class 3 limits. The input capacitor is therefore designed in conjunction with the EMI filter and the result is an input capacitance much greater than the minimum value calculated in the preceding Equation 7 and is also able to support PWM dimming requirements.

2.8 Output Capacitance

A capacitor placed in parallel with the LED load can be used to reduce ΔI_{LED-PP} while keeping the same average current through both the inductor and the LED load. With an output capacitor, the inductance can be lowered, making the magnetic smaller and less expensive. Alternatively, the circuit can be run at a lower frequency with the same inductor value, improving the efficiency and increasing the maximum allowable average output voltage. A parallel output capacitor is also useful in applications where the inductor or input voltage tolerance is poor. Adding a capacitor that reduces ΔI_{LED-PP} to well below the target provides headroom for changes in inductance or V_{IN} that might otherwise push the maximum ΔI_{LED-PP} too high.

Because the inductor value of this design has been chosen to meet the inductor current ripple specification, a minimum amount of output capacitance (2.2 µF) has been added.

Alternatively, because current is being regulated and is continuous, no output capacitance is required to supply the load and maintain output voltage. This feature is advantageous when designing for high-frequency PWM dimming on the LED load (that is, PWM shunt FET), which requires fast dimming edges.

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2.9 Thermal Protection

Internal thermal protection circuitry protects the controller in the event of exceeding the maximum junction temperature. At 175°C the converter typically shuts down, thus protecting all the circuitry in the reference design. The maximum junction temperature is a function of the system operating points (that is, efficiency, ambient temperature, and thermal management), component choices, and switching frequency.

2.10 Power Supply Recommendations

The TPS92515HV-Q1 has been designed with the consideration of two, main-input source possibilities: direct from battery or from the output of a boost stage. For either application, ensure input voltage ripple requirements have been met. The input ripple must go no higher than 10% of the input voltage to a maximum of 2 V.

2.10.1 Input Source Direct From Battery

Operation direct from battery has been considered when designing the TPS92515HV-Q1. The device ratings are such that load dump and other battery voltage excursions should not exceed the ratings of the device. When the battery voltage drops, the ability of the device to run in to dropout and various UVLO controls ensure a controlled recovery and no device damage. The BOOT UVLO protection allows duty cycles over 99%.

2.10.2 Input Source From Boost Stage

The TPS92515HV-Q1 maximum input voltage of 65 V makes it a suitable, second-stage buck regulator for a variety of applications and LED output configurations. Assuming a LED forward voltage of 3.4 V, and allowing for some headroom below the 65-V maximum input, the TPS92515HV-Q1 can successfully drive up to 12 LEDs connected in series.

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3 Designing for Low EMI

3.1 CISPR-25 Overview

CISPR-25 is the automotive EMI standard on which most original equipment manufacturers (OEMs) base their own requirements. The CISPR-25 standard is known as *Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers* [2]. Basically, the purpose of the standard is to limit the amount of emissions from a subsystem in a few important frequency bands to ensure it does not interfere with other systems that intentionally operate (or receive) in those bands.

For example, an AM radio receiver is “listening” (tuned) to a specific frequency (for example 710 kHz), picking up a radio station’s signal put out on that frequency. The receiver only wants to receive and amplify the signals intended for AM radio broadcast on that frequency; however, if another system on the car is unintentionally emitting a lot of energy (noise) at that frequency, the noise impedes the radios ability to cleanly resolve the radio station’s signal and the user may hear a lot of noise in the signal, or obscure the intentional signal altogether. Standards like CISPR-25 have been specifically designed to avoid these issues by setting acceptable limits on these systems; OEMs define their own limits but CISPR-25 provides examples.

The testing and limits are split into two separate types of emissions: conducted and radiated. Conducted emissions are coupled onto supply lines directly through conductors (traces, wires, and so forth), and radiated emissions are emitted as electromagnetic waves and can be picked up by intentional or unintentional antennas on other systems.

The test procedures, relevant frequency bands, and limits are different for both, but the basics are similar: The subsystem, or device under test (DUT), is placed in an isolated room or chamber and set up in a well-defined, reproducible electrical setup. All other possible emitters are removed from the chamber and the DUT is turned ON then allowed to operate normally. The DUT is powered through an artificial network (or LISN) and loaded per its normal operation. A spectrum analyzer is then used to measure its emissions across different frequencies (either through the LISN or from an antenna) and compared against the CISPR-25 limits. Both the peak and average values of the emissions are measured and both must pass.

Finally, the level of “passing” falls into several categories, or “classes”, which have different limits. OEMs define which class a specific subsystem must satisfy.

3.2 EMI Performance

Figure 5 shows the conducted EMI scan for this design at a nominal 14-V input voltage and driving a 6-V LED load (that is two LEDs in series) at 1.25 A of LED current. The blue trace is the peak scan and the blue lines denote the peak limits for CISPR-25 Class 3. The black trace is the average scan with the green lines denoting average limits for CISPR-25 Class 3. The scan covers the entire conducted frequency range of 150 kHz to 108 MHz.

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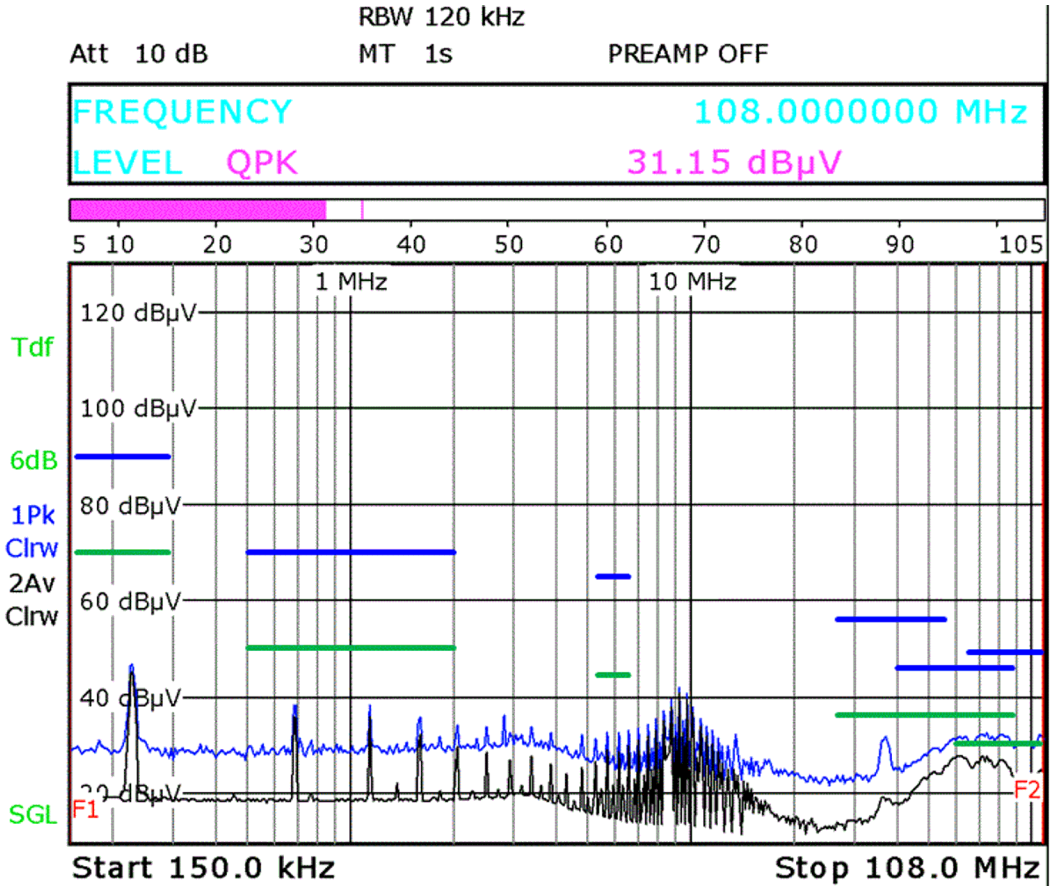

Figure 5. CISPR-25 Class 3 Conducted EMI Scan (Blue: Peak Limits, Green: Average Limits) V_{IN} = 14 V, Two LEDs, I_{LED} = 1.25 V

3.3 EMI Filter Design

The input EMI filter consists of a differential mode PI filter formed by the input capacitors (C1 through C4, C10 through C13) and the input inductor (L2). The primary purpose of the filter is to minimize EMI conducted from the circuit to prevent it from interfering with the electrical network supplying power to the LED driver. Frequencies in and around the LED driver switching frequency (that is, fundamental and harmonics) are primarily addressed with this filter and the filter cutoff frequency is determined by the inductor and capacitor resonance.

Sufficient differential mode noise filtering on the output is generally provided by the output capacitor assuming low equivalent-series-resistance (ESR) ceramics are used as in the design. This LED driver has been designed with the assumption that a connection to chassis ground is not available. To attenuate high frequency common-mode noise on the output, common-mode choke (L3) is placed in series with LED+ and LED–. If a chassis ground connection is available to the designer, then common-mode capacitors can be utilized, which increase the effectiveness of common-mode noise rejection and possibly reduce or eliminate the requirement for an output choke.

For more information on EMI filter design refer to TI literature numbers SNVA489C and SNVA538.

3.3.1 Additional EMI Considerations

Higher power levels may likely require increased EMI filtering to pass CISPR-25 class 3 limits. Options include increasing input capacitance, or output capacitance (or both), adding ferrite bead resistance to mitigate high frequency EMI, or increasing output choke inductance for common-mode noise reduction.

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4 Testing and Results

4.1 Test Setup

Figure 6 shows the test setup. The input voltage was supplied by a DC power supply connected to the onboard test points TP1 and TP2. The LED load was connected to the board using test points TP6 and TP5. Four digital multimeters (DMMs) were used to measure input voltage, input current, output voltage, and output current. To enable PWM dimming, an external signal generator was connected to the PWM using test point TP3. For analog adjustment and dimming measurements, an external voltage supply was connected to the IADJ pin at the node between R10 and R12.

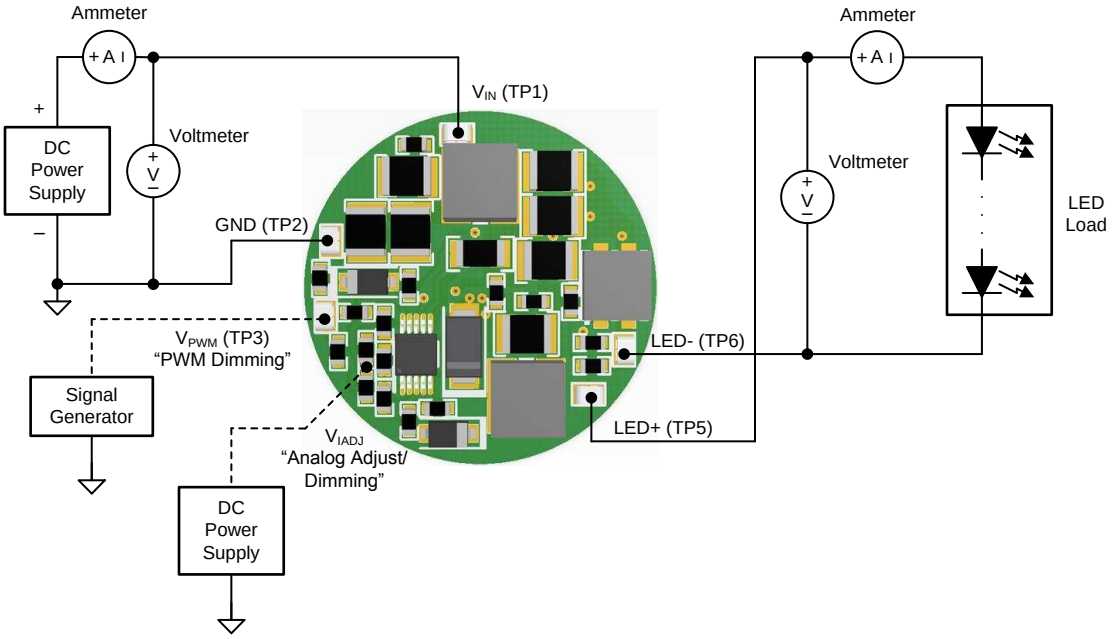

Figure 6. Test Setup Connections

4.2 Test Results

The test setup described in Figure 6 was used to generate the following data for efficiency, line regulation, analog dimming, and PWM dimming measurements.

4.2.1 Efficiency

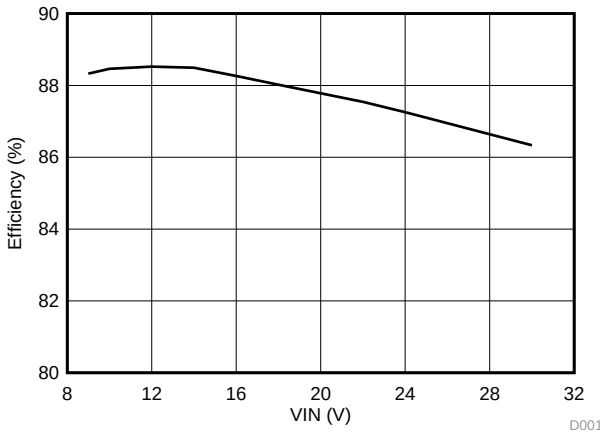

Figure 7. Efficiency versus Input Voltage (Two LEDs)

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4.2.2 Line Regulation

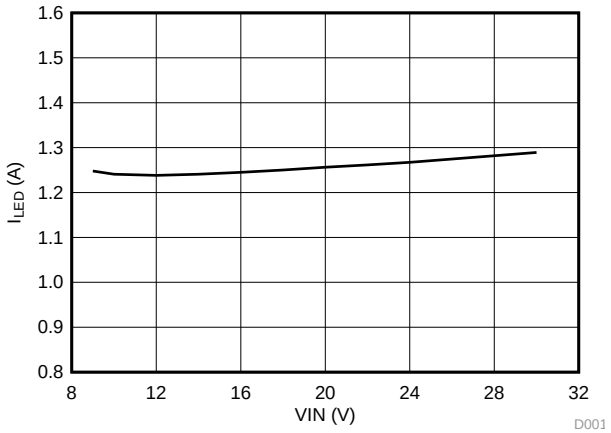

Figure 8. LED Current versus Input Voltage (Two LEDs)

4.2.3 Analog Dimming

An analog dimming range of 165:1 is supported by this design.

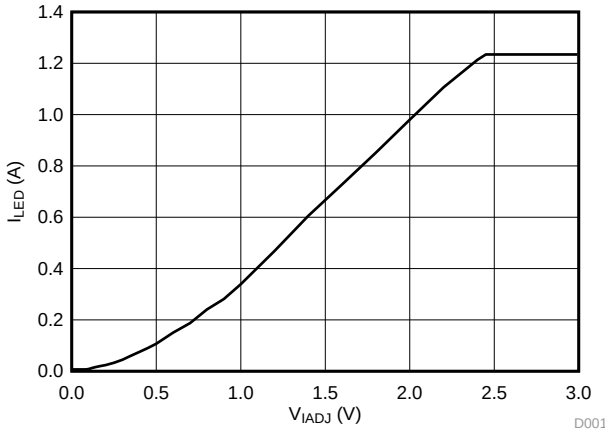

Figure 9. LED Current versus IADJ Pin Voltage (V_{IN} = 14 V, Two LEDs)

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4.2.4 PWM Dimming

Linear PWM dimming is achieved using dimming frequencies ranging from 240 Hz to 5 kHz.

Figure 10. LED Current versus Duty Cycle (f_{DIM} = 240 Hz) (V_{IN}= 14 V, Two LEDs)

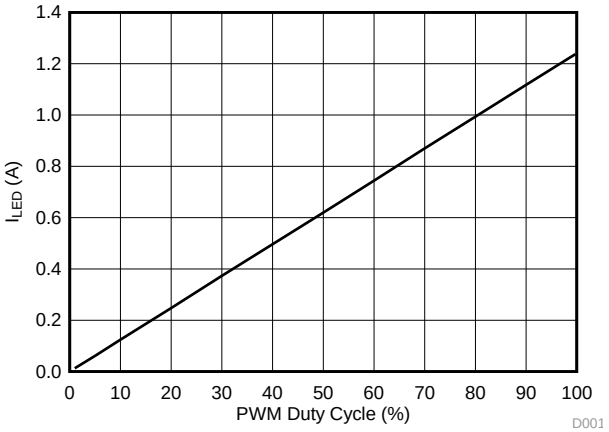

Figure 11. LED Current versus Duty Cycle (f_{DIM} = 1000 Hz) (V_{IN} = 14 V, Two LEDs)

Figure 12. LED Current versus Duty Cycle (f_{DIM} = 5000 Hz) (V_{IN} = 14 V, Two LEDs)

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4.2.5 Switching Waveforms (Steady-State)

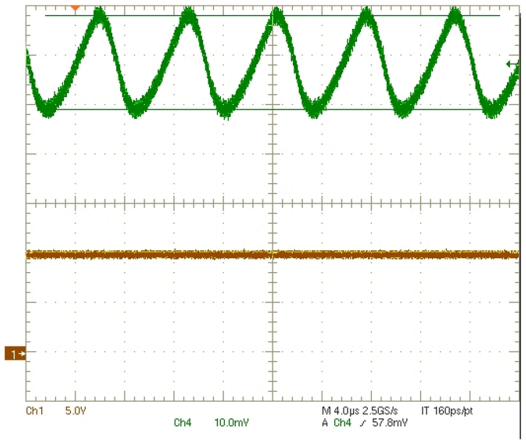

Figure 13. V_{IN} = 10 V, Two LEDs, Ch1: V_{IN}, Ch4: I_{LED} (200 mA/div)

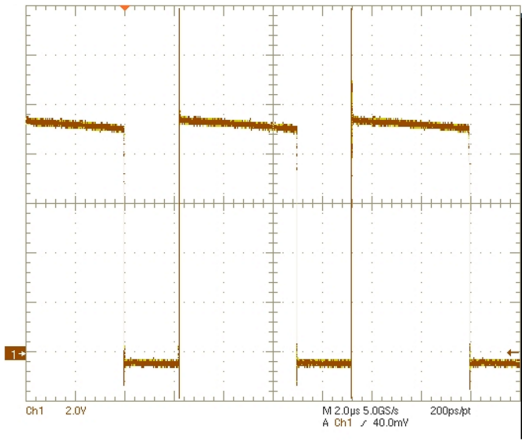

Figure 14. V_{IN} = 10 V, Two LEDs, Ch1: V_{SW} (Switch Node)

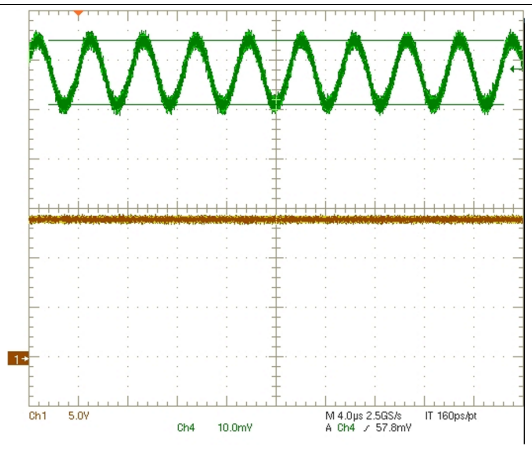

Figure 15. V_{IN} = 14 V, Two LEDs, Ch1: V_{IN}, Ch4: I_{LED} (200 mA/div)

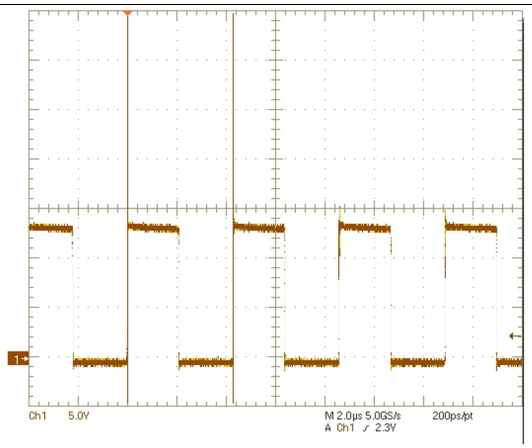

Figure 16. V_{IN} = 14 V, Two LEDs, Ch1: V_{SW} (Switch Node)

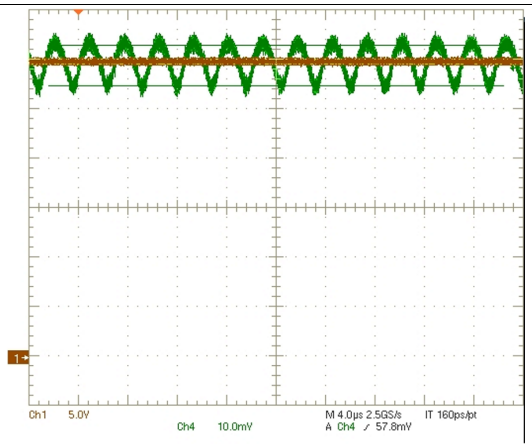

Figure 17. V_{IN} = 30 V, Two LEDs, Ch1: V_{IN}, Ch4: I_{LED} (200 mA/div)

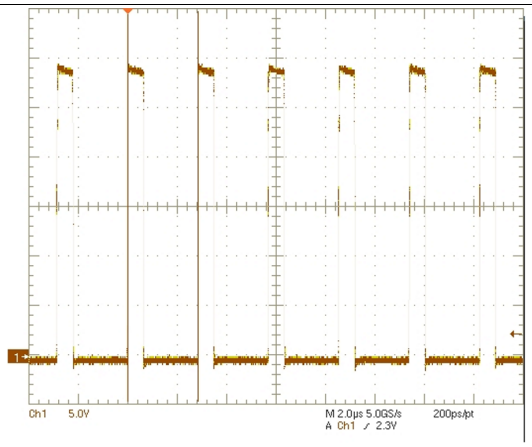

Figure 18. V_{IN} = 30 V, Two LEDs, Ch1: V_{SW} (Switch Node)

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4.2.6 Switching Waveforms (Start-up and Shutdown)

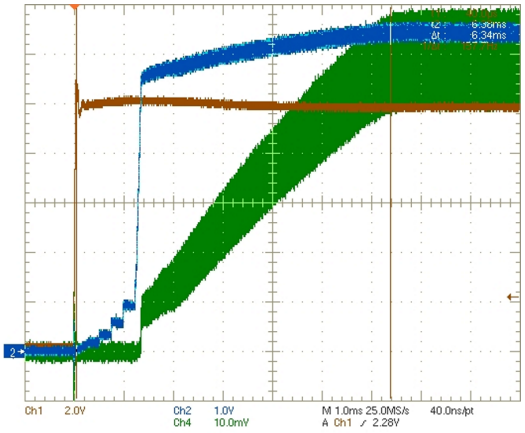

Figure 19. V_{IN} = 10 V, Two LEDs, Ch1: V_{IN}, Ch2: V_{OUT}, Ch4: I_{LED} (200 mA/div)

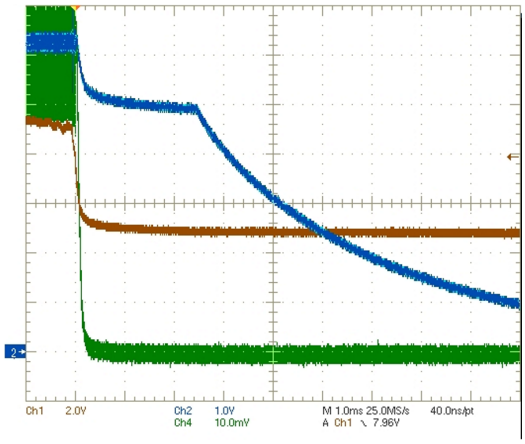

Figure 20. V_{IN} = 10 V, Two LEDs, Ch1: V_{IN}, Ch2: V_{OUT}, Ch4: I_{LED} (200 mA/div)

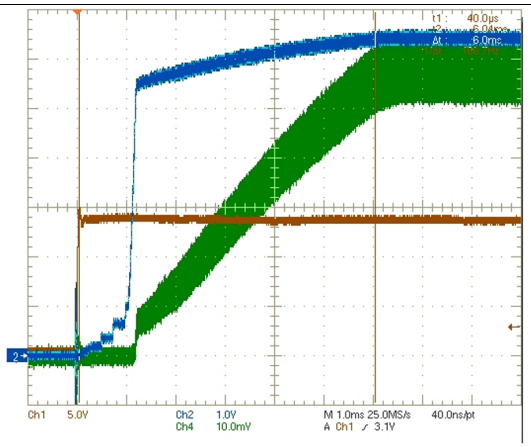

Figure 21. V_{IN} = 14 V, Two LEDs, Ch1: V_{IN}, Ch2: V_{OUT}, Ch4: I_{LED} (200 mA/div)

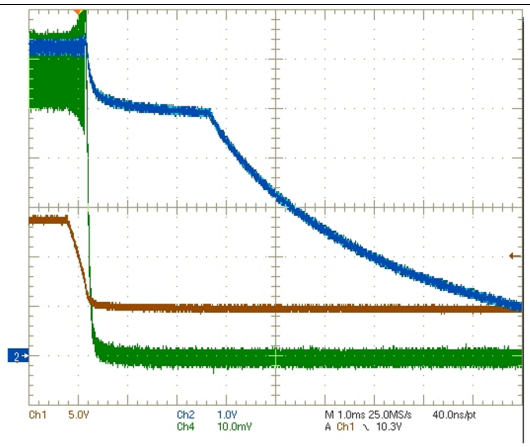

Figure 22. V_{IN} = 14 V, Two LEDs, Ch1: V_{IN}, Ch2: V_{OUT}, Ch4: I_{LED} (200 mA/div)

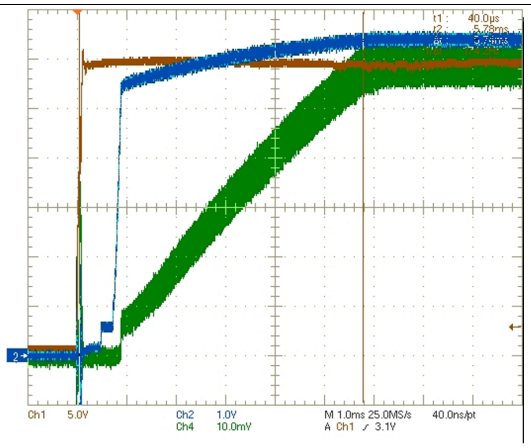

Figure 23. V_{IN} = 30 V, Two LEDs, Ch1: V_{IN}, Ch2: V_{OUT}, Ch4: I_{LED} (200 mA/div)

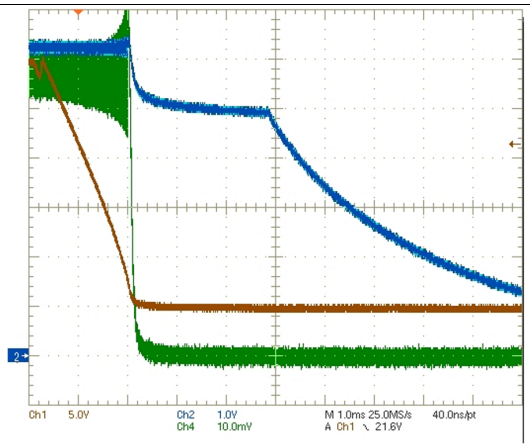

Figure 24. V_{IN} = 30 V, Two LEDs, Ch1: V_{IN}, Ch2: V_{OUT}, Ch4: I_{LED} (200 mA/div)

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4.2.7 PWM Dimming Waveforms

- PWM dimming frequency: 240 Hz
- Channel 1: PWM signal
- Channel 4: LED current

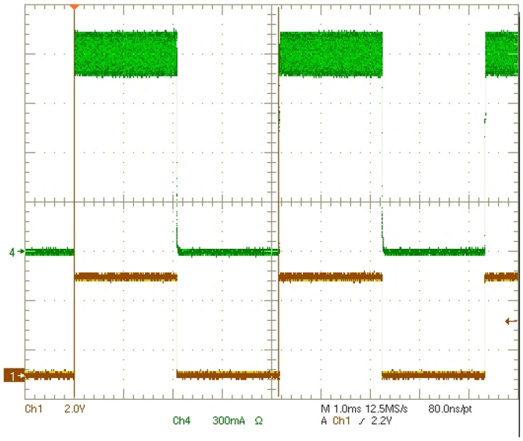

Figure 25. f_{DIM} = 240 Hz, Duty Cycle: 50%

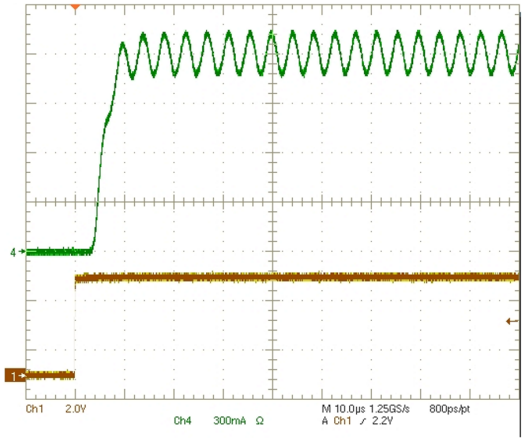

Figure 26. f_{DIM} = 240 Hz, Duty Cycle: 50%

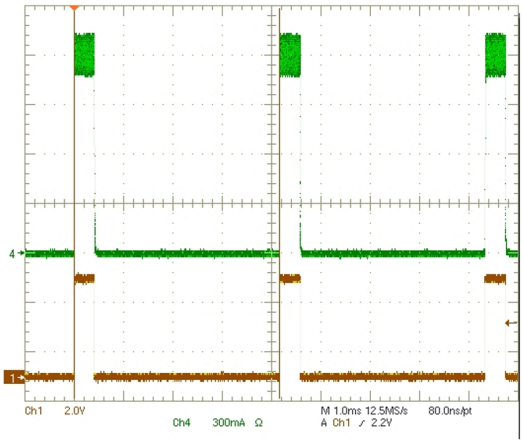

Figure 27. f_{DIM} = 240 Hz, Duty Cycle: 10%

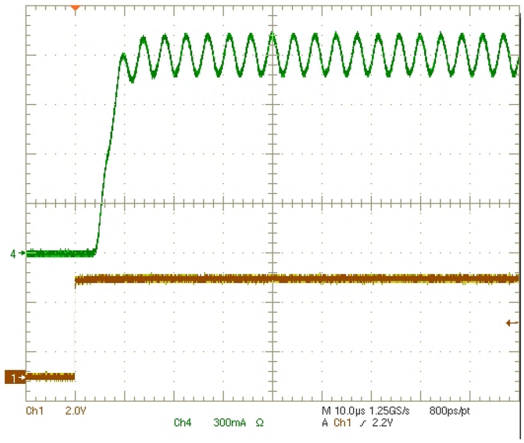

Figure 28. f_{DIM} = 240 Hz, Duty Cycle: 10%

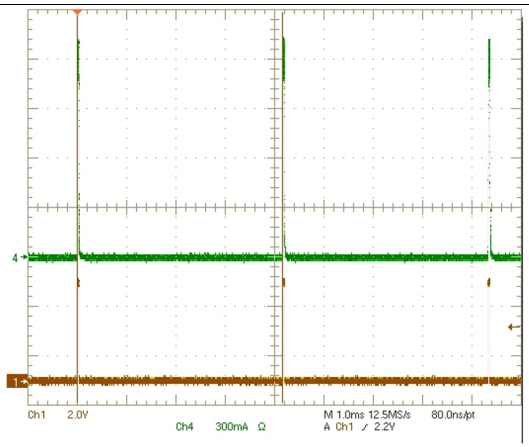

Figure 29. f_{DIM} = 240 Hz, Duty Cycle: 1%

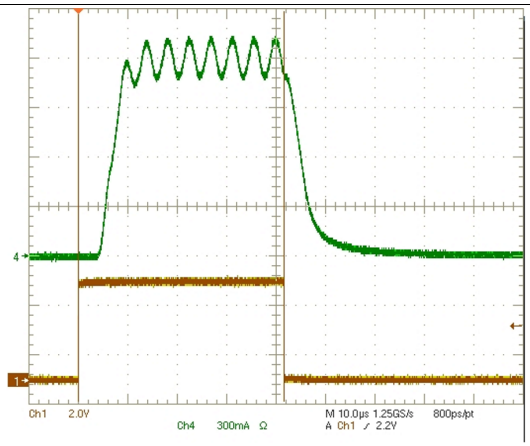

Figure 30. f_{DIM} = 240 Hz, Duty Cycle: 1%

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- PWM dimming frequency: 1000 Hz
- Channel 1: PWM signal
- Channel 4: LED Current

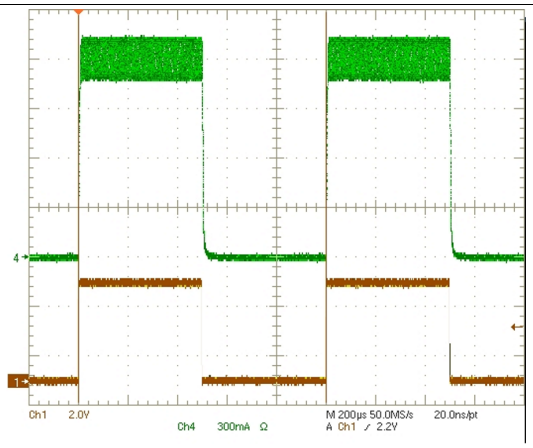

Figure 31. f_{DIM} = 1000 Hz, Duty Cycle: 50%

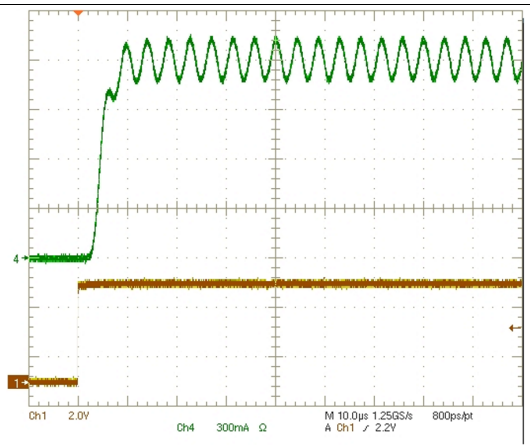

Figure 32. f_{DIM} = 1000 Hz, Duty Cycle: 50%

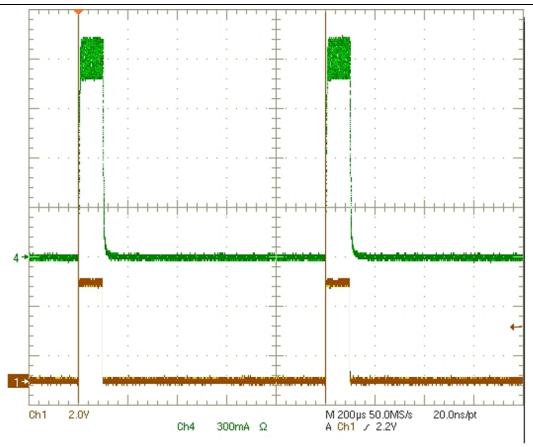

Figure 33. f_{DIM} = 1000 Hz, Duty Cycle: 10%

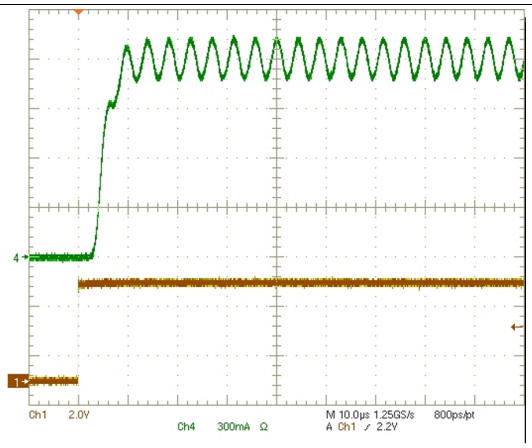

Figure 34. f_{DIM} = 1000 Hz, Duty Cycle: 10%

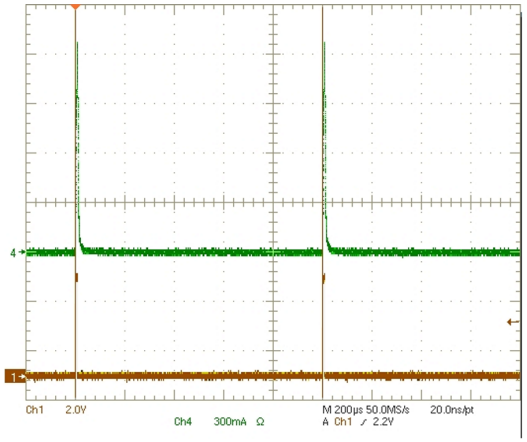

Figure 35. f_{DIM} = 1000 Hz, Duty Cycle: 1%

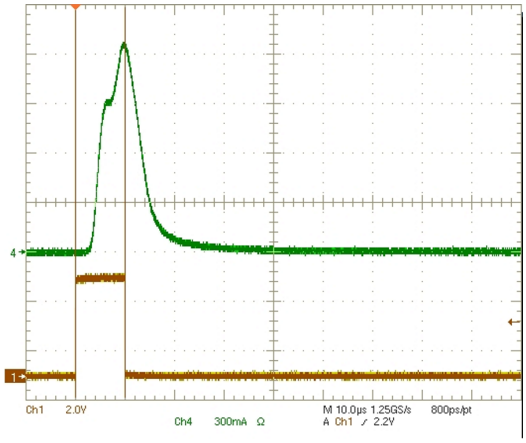

Figure 36. f_{DIM} = 1000 Hz, Duty Cycle: 1%

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- PWM dimming frequency: 5000 Hz
- Channel 1: PWM signal
- Channel 4: LED current

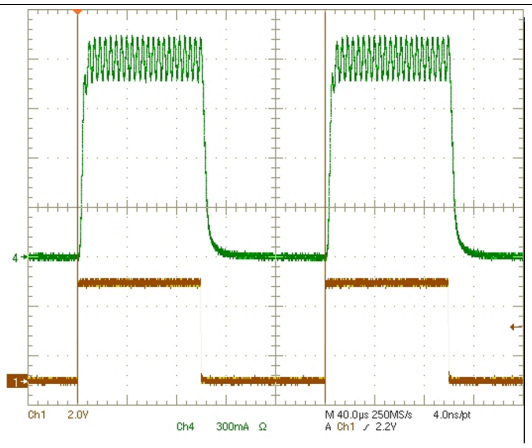

Figure 37. f_{DIM} = 5000 Hz, Duty Cycle: 50%

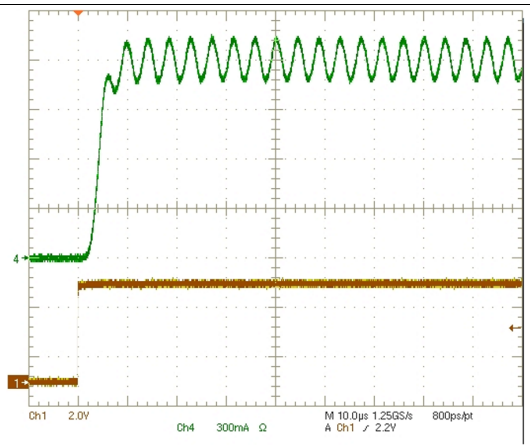

Figure 38. f_{DIM} = 5000 Hz, Duty Cycle: 50%

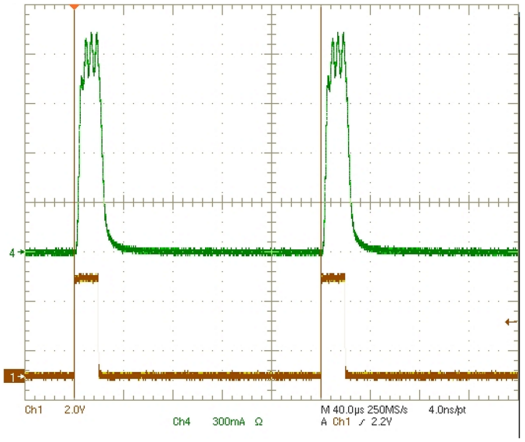

Figure 39. f_{DIM} = 5000 Hz, Duty Cycle: 10%

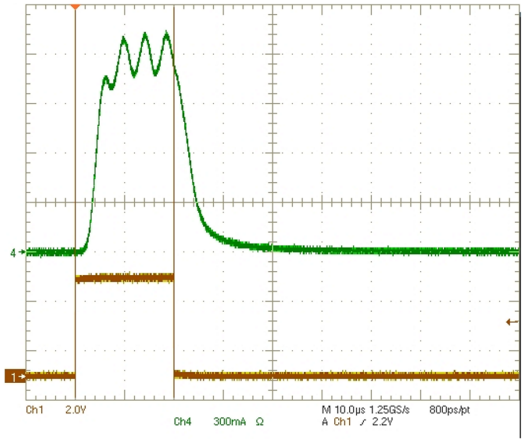

Figure 40. f_{DIM} = 5000 Hz, Duty Cycle: 10%

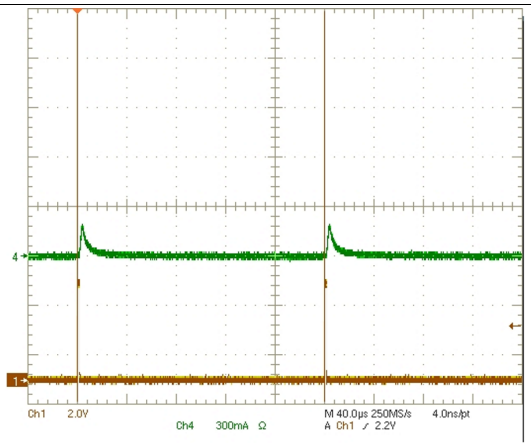

Figure 41. f_{DIM} = 5000 Hz, Duty Cycle: 1%

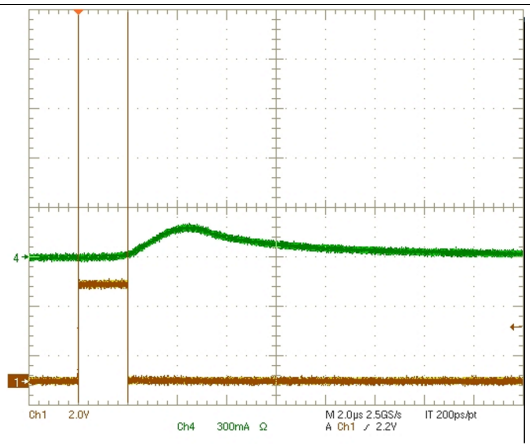

Figure 42. f_{DIM} = 5000 Hz, Duty Cycle: 1%

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5 Design Files

5.1 Schematics

To download the schematics, see the design files at PMP15004.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at PMP15004.

5.3 PCB Layout Recommendations

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. By carefully considering the PCB layout requirements, a designer can avoid noise issues, device misbehavior, as well as reducing EMI. Figure 43 shows a generic layout and the associated current loops.

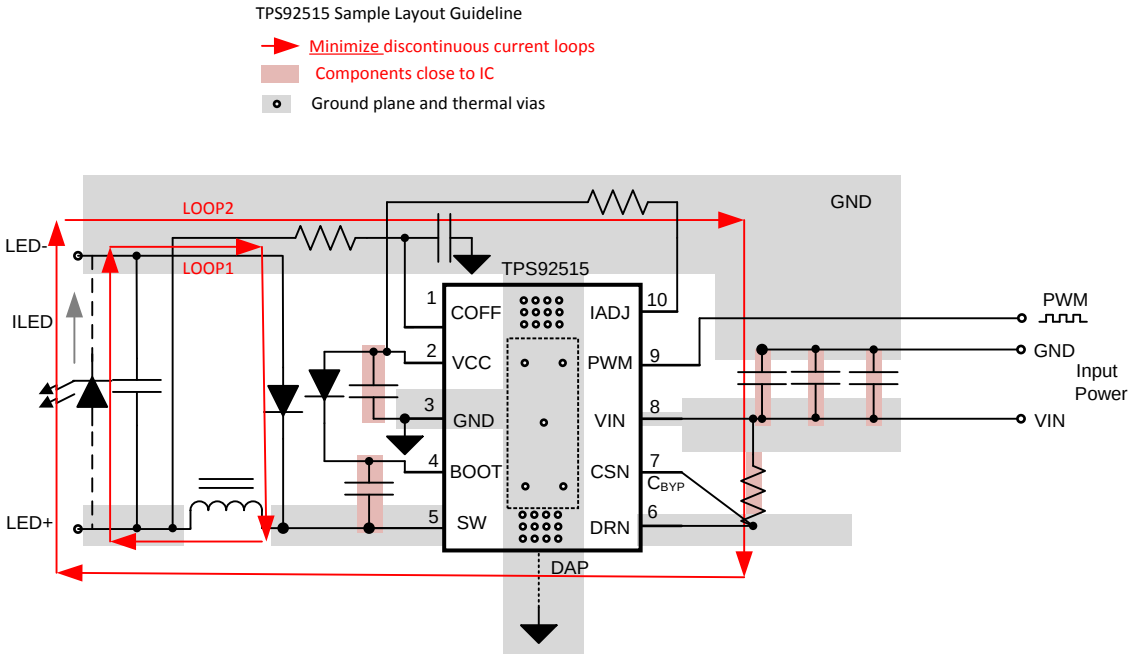

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Figure 43. PMP15004 Schematic and PCB Layout

Following a few simple guidelines maximizes noise rejection and minimizes the generation of EMI within this TI Design:

- Discontinuous currents are the type of current most likely to generate EMI; therefore, ensure to take care when routing these paths.
  - The main path for discontinuous current contains the input capacitor (C1, C2, C3), the recirculating diode (D1), the internal MOSFET (DRN pin to SW pin), and the sense resistor (R5) shown as LOOP2. Make LOOP2 as small as possible.
  - Make the connections between all three components short and thick to minimize parasitic inductance. In particular, the switch node (where L1, D1, and the SW pin connect, as LOOP1 shows) must only be large enough to connect the components without excessive heating from the current it carries.
- The IADJ, COFF, CSN, and VIN pins are all high-impedance control inputs; therefore, minimize the loops containing these high impedance nodes. The most sensitive loop contains the sense resistor (R5). Place the sense resistor as close as possible to the CSN and VIN pins to maximize noise

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rejection.

- Place the OFF-time capacitor (C6) close to the COFF and GND pins to maximize noise rejection.
- If external resistors are used to bias the IADJ pin, these resistors should also be placed close to the IADJ and GND pins and can then be decoupled with a small capacitor.
- In some applications the LED load can be far away from the device, several inches or more, or on a separate PCB connected by a wiring harness. When an output capacitor is used (such as C9) and the LED load is large or separated from the main converter, the output capacitor must be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.
- The TPS92515HV-Q1 has an exposed thermal pad to aid power dissipation. Adding several vias under the exposed pad helps conduct heat away from the device. The junction-to-ambient thermal resistance varies with application. The most significant variables are the area of copper in the PCB and the number of vias under the exposed pad. The integrity of the solder connection from the device exposed pad to the PCB is critical. Excessive voids greatly decrease the thermal dissipation capacity.

5.3.1 Thermal Scan

Figure 44 shows a thermal scan of the board running at a room temperature (≈25°C) with no air-flow. Table 2 lists measured temperatures of key components.

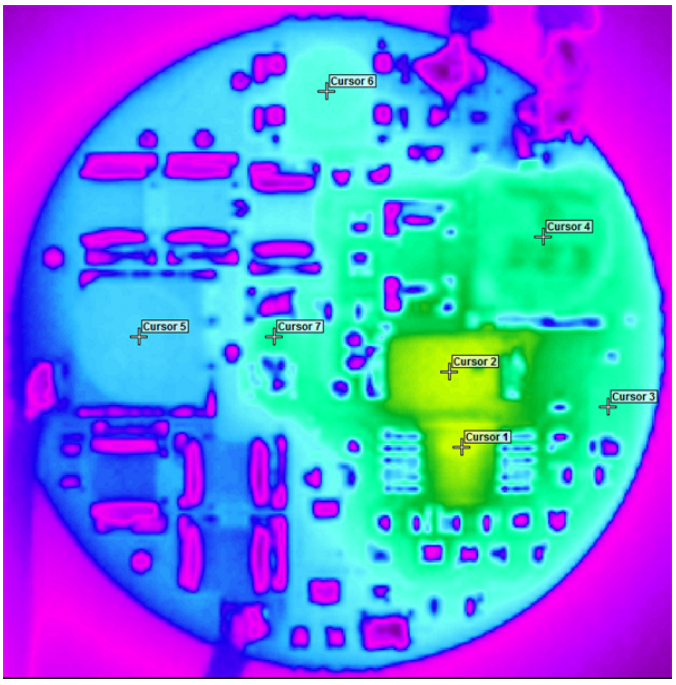

Figure 44. Thermal Scan—Top-View: V_{IN} = 14 V, Two LEDs, I_{LED} = 1.25 V

Table 2. Component Temperatures

CURSOR	COMPONENT	TEMPERATURE (°C)
1	U1	84.1
2	D1	83.1
3	D4	69.6
4	L1	71.7
5	L2	61.1
6	L3	66.2
7	R5	70.3

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5.3.2 Layout Prints

To download the layer plots, see the design files at PMP15004.

5.4 Altium Project

To download the Altium project files, see the design files at PMP15004.

5.5 Gerber Files

To download the Gerber files, see the design files at PMP15004.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at PMP15004.

6 References

1. Texas Instruments, *TPS92515x 2-A, Buck LED Driver with Integrated N-channel FET, High-Side Current Sense, and Shunt FET PWM Dimming Capability*, tps92515/Q1 and TPS92515HV/Q1 Data Sheet (SLUSBZ6)
2. International Electrotechnical Commission, *CISPR-25 Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers*, 3rd Edition 2008 (http://bit.ly/2cREucO)
3. ISO.org, *ISO 7637-2:2004 Road vehicles -- Electrical disturbances from conduction and coupling -- Part 2: Electrical transient conduction along supply lines only*, Section 5.6 2004 (http://www.iso.org/iso/iso_catalogue/catalogue_ics/catalogue_detail_ics.htm?csnumber=28533)
4. ISO.org, *16750-2:2010 Road vehicles -- Environmental conditions and testing for electrical and electronic equipment -- Part 2: Electrical loads*, Section 4.6 2010 (http://www.iso.org/iso/catalogue_detail.htm?csnumber=61280)

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