TI Designs

3.3-V, 1-A, Low EMI, 92% Efficiency DC/DC Module in Dual Layer TO-220 Form Factor Reference Design

Description

The TI Design TIDA-00947 demonstrates a small, high efficiency, low EMI DC/DC module to replace LDOs in major home appliance applications. This results in drastic improvement in efficiency, saving both size and cost, as no heat sink is required. With the same input current, the TPS54202, as a power converter, enables the supplying of higher output current as well as having lower power consumption at full load, low load, and standby operation.

This module is size and pin compatible with a TO-220 LDO enabling a quick evaluation and time to market.

Resources

TIDA-00947	Design Folder
TPS54202	Product Folder

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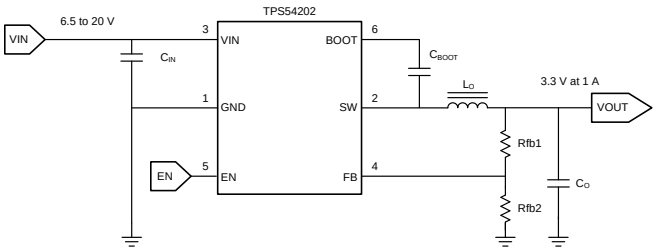
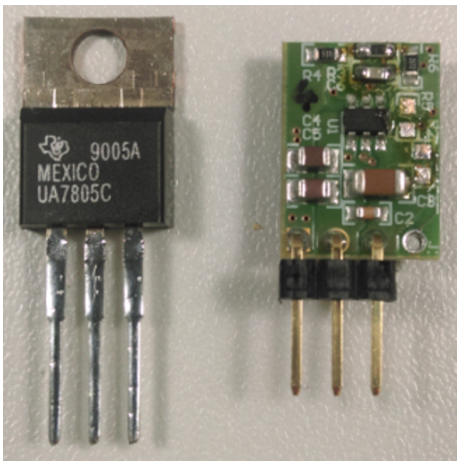
Features

- 3.3 V Regulated, up to 1-A Output Load
- 92% Efficiency
- 1.5-μA Standby Current and 84-μA No Load Current
- Small Form Factor: Size and Pin-Compatible and Smaller Than TO-220 (10.5 mm × 14.5 mm)
- Less Than 31ºC Increase at Full Load, Which Eliminates Need of Heat Sink
- Reduces Onboard DC/DC Design Complexity, Saves R&D Time and Efforts for Switching Power Supply EMC Design (Quicker to Market)

Applications

- Washing Machine and Dryer
- Refrigerator and Freezer
- Dishwasher
- Air Conditioner Indoor Units





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1 System Overview

1.1 System Description

Traditionally, low dropout regulators (LDO) are used in home appliances to generate 5 V or 3.3 V from the 12-V rail. These LDOs are chosen mainly for their cost and size.

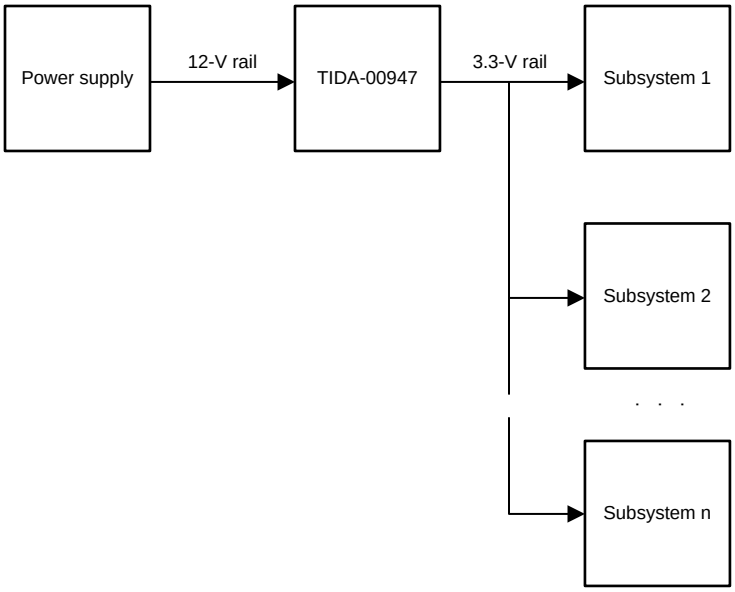

Figure 1. System Diagram

With the tightening requirements on active and standby power consumption and the increasing current needs due to the addition of new features (for example, the Wi-Fi module), the LDOs become an obstacle to achieving stringent energy ratings.

The TIDA-00947 was developed to answer this need of higher efficiency and current capability with the additional benefit of saving space by eliminating the heat sink, which is normally used in order to allow the LDOs to dissipate the losses.

1.2 Key System Specifications

The specifications of the TIDA-00947 are listed in Table 1:

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage range	6.5 to 20 V	—
Output voltage and max current	3.3 V at 1 A	—
Efficiency (full load, rated load, and light load)	90%: 12 V → 5 V at 1 A, 92%: 12 V → 5 V at 500 mA, 88%: 12 V → 5 V at 10 mA	Section 4.2.1
EMI performance	EN55022 class B, > 6-dB margin	Section 4.2.10
Regulation (line and load)	±1% across the input range and load current range	Section 4.2.3
Transient response	±5% from 0.1 to 1.0 A	Section 4.2.5
Protections	Short-circuit, hiccup mode OCP for both FETs, OTP, OVP	Section 4.2.7
Operating ambient temperature	–30°C to 65°C	Section 4.2.2

1.3 Block Diagram

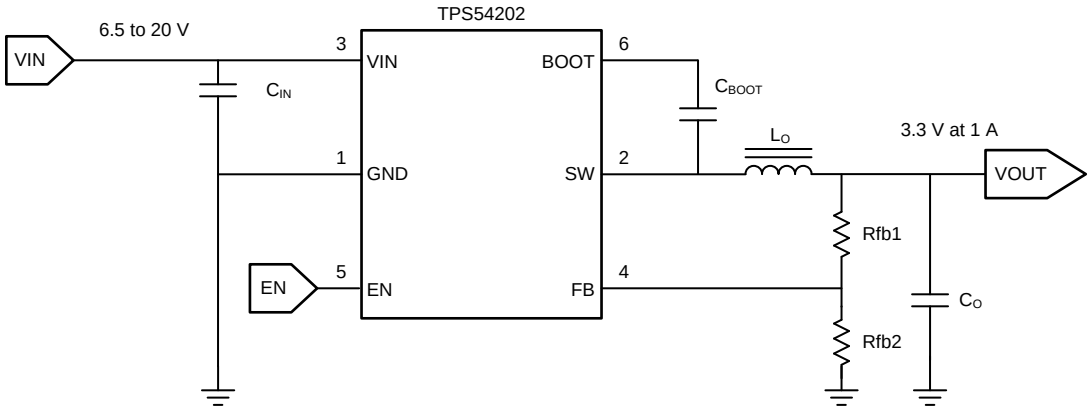

Figure 2. Block Diagram

1.4 Highlighted Products

1.4.1 TPS54202

The TPS54202 is a 4.5- to 28-V input voltage range, 2-A synchronous buck converter. The device includes two integrated switching FETs, internal loop compensation, and a 5-ms internal soft start to reduce component count.

By integrating the MOSFETs and employing the SOT-23 package, the TPS54202 achieves high power density and offers a small footprint on the PCB.

Advanced Eco-mode™ implementation maximizes light-load efficiency and reduces power loss.

In the TPS54202, the frequency spread spectrum operation is introduced for EMI reduction.

Cycle-by-cycle current limit in both high-side MOSFETs protect the converter in an overload condition and is enhanced by a low-side MOSFET freewheeling current limit, which prevents current runaway. Hiccup mode protection is triggered if the overcurrent condition has persisted for longer than the present time.

Features:

- 4.5- to 28-V wide input voltage range
- Integrated 148-mΩ and 78-mΩ MOSFETs for 2-A, continuous output current
- Low 2-μA shutdown, 45-μA quiescent current
- Internal 5-ms soft start
- Fixed 500-kHz switching frequency
- Frequency spread spectrum to reduce EMI
- Advanced Eco-mode pulse skip
- Peak current mode control
- Internal loop compensation
- Overcurrent protection for both MOSFETs with hiccup mode protection
- Overvoltage protection
- Thermal shutdown
- SOT-23 (6) package

1.5 System Design Theory

LDOs are devices that regulate the output voltage, while the output current is the same as the input current. This implies losses are proportional to the dropout between input and output voltage and the output current, as shown in Equation 1. These losses are the root cause of poor efficiency in LDOs. This translates to a limitation of the ratio between input and output voltage and maximum output current as well as the need of a heat sink. That heat sink will add cost and size to the overall solution.

A DC/DC switch mode power supply, including a Buck topology as in this project, present the advantage of having a higher efficiency, allowing them to be used in a wider variety of applications as well as being competitive with an LDO-based design with respect to cost and size (including all components and heat sink). More details on how a Buck topology works can be found in *Understanding Buck Power Stages In Switchmode Power Supplies* (SLVA057).

Compare the efficiency of the TIDA-00947 and an LDO based design. The efficiency data for the TIDA-00947 can be found in Section 4.2.1. In an LDO, the power to be dissipated can be estimated by Equation 1.

$$P_{DISSIPATED} = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} \quad (1)$$

Now calculate the power dissipated by a 12-V input, 3.3-V output design at 1 A, 500 mA, and 100 mA to see what the performances are for the TIDA-00947 and for the LDO-based design.

For 1 A, the efficiency of the TIDA-00947 is 90% (10% loss). With 3.3 W at the output, 0.33 W are dissipated. For the LDO-based design, Equation 1 gives 8.7 W to be dissipated by the LDO.

For 500 mA, the efficiency of the TIDA-00947 is 92% (8% loss). With 1.65 W at the output, 0.132 W are dissipated. For the LDO-based design, Equation 1 gives 4.35 W to be dissipated by the LDO.

Finally for 100 mA, 0.04 W needs to be dissipated for the TIDA-00947 (88% efficiency) versus 0.87 W for the LDO-based design.

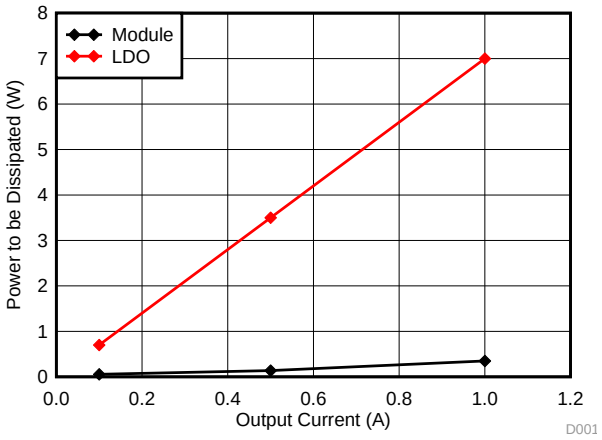

Figure 3. Comparison of Power Dissipated

As shown in Figure 3, the LDO-based design needs to dissipate much more power than the TIDA-00947 design, which impacts both power consumption and cost and size due to the necessity of a heat sink.

2 Circuit Design and Component Selection

2.1 Part and Topology Selection

The first step of the design is to select the circuit topology. As cost and space are key in home appliance design and no isolation is needed for the 12-V to 3.3-V conversion, a Buck topology is chosen. Still, with the aim to reduce bill of material cost and size, a synchronous converter with integrated FET is preferred.

With this in mind, as well as the specification in Section 1.2, the TPS54202 was chosen. The converter includes two integrated switching FETs, internal loop compensation, and a 5-ms internal soft start to reduce component count. It integrates a 148-mΩ and a 78-mΩ MOSFET for up to 2-A continuous output current operation with 2-µA shutdown and 45-µA quiescent current.

2.2 Design Steps and Passive Components Selection

The first step is to set the output voltage, which is adjusted by the resistor divider (R3 and R6). First set the range of the resistors; higher values will decrease the losses in the resistor divider but make the feedback signal more sensitive to noise, while lower values will make the feedback signal more robust against noise but increase losses. On this project, a good trade-off is setting R3 at 200 kΩ and use Equation 2 to calculate R6. A 51-Ω resistor (R4) was added to measure the loop stability. R4 is not needed in the final design.

$$R6 = \frac{R3 \times V_{REF}}{V_{OUT} - V_{REF}} \tag{2}$$

where

- R3 = 200 kΩ
- V_{OUT} = 3.3 V
- V_{REF} = 0.596 V

Equation 2 gives R6 = 44.08 kΩ. A resistor value of 44.2 kΩ is then used for R3. By reversing Equation 2, an effective output voltage of V_{OUT} = 3.294 V is given.

Then comes the choice of the inductor (L1). For this the inductance value, the RMS and peak current are considered.

The minimum inductor value of the inductor is calculated in Equation 3. To calculate the minimum inductor value, use the maximum input voltage (20 V), the maximum output voltage (3.3 V), the maximum output current (1 A), the switching frequency (500 kHz), and the coefficient that represents the amount of inductor ripple relative to the maximum output current (K_{IND}). For low ESR output capacitors, K_{IND} must be 0.3 (0.2 for higher ESR output capacitors). Equation 3 indicates that L1 must ideally be higher than 18.37 µH. 22 µH is used as value for L1 in this design.

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{V_{IN\_MAX} \times K_{IND} \times I_{OUT} \times F_{SW}} \tag{3}$$

With the output inductor value, the RMS and peak current can be calculated with Equation 4 and Equation 5, which respectively gives 1.004 A and 1.157 A. With these parameters in mind, the inductor can be selected. After reviewing the cost and performance of several inductor from various manufacturers, the THPC6045MF-220M from Taitech was selected.

$$I_{LRMS} = \sqrt{\left(I_{OUT}\right)^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{V_{IN\_MAX} \times L \times F_{SW}}\right)^2} \tag{4}$$

$$I_{L\_PEAK} = I_{OUT} \times \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{1.6 \times V_{IN\_MAX} \times L \times F_{SW}} \tag{5}$$

The maximum allowable output voltage ripple and the transient response to load changes determine the value of the output capacitors. C_{OUT} is selected based on the most stringent of the following equations.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{F_{SW} \times \Delta V_{OUT}} \quad (6)$$

where

- ΔI_{OUT} is the load step of the output current from the output current under light load (0.1 A) and full load (1 A)
- ΔV_{OUT} is the allowable change of output voltage during the load step

$$C_{OUT} > \frac{1}{8 \times F_{SW}} \times \frac{1}{\frac{V_{OUT\_RIPPLE}}{K_{IND} \times I_{OUT}}} \quad (7)$$

where

- V_{OUT_RIPPLE} is the maximum output ripple required

The output capacitors also influence the crossover frequency. In the case of the TPS54202, the crossover frequency must be lower than 40 kHz without considering the feed forward capacitor.

$$C_{OUT} > \frac{3.95}{V_{OUT} \times F_{CO}} \quad (8)$$

C_{OUT} must be selected based on the most stringent of the previous equations. Equation 6, Equation 7, and Equation 8 indicate that C_{OUT} must be higher than 30 μF. Including some margin for aging, temperature and DC bias, two 22 μF in parallel where chosen to fit the C_{OUT} requirements.

Equation 9 calculates the maximum ESR of the output capacitor needed to meet the maximum output ripple required. The equivalent ESR of the output capacitors C4 and C5 must be lower than 0.33 Ω.

$$R_{ESR} < \frac{V_{OUT\_RIPPLE}}{I_{L\_RIPPLE}} \quad (9)$$

A feed forward capacitor (C6) is used in parallel with R6 to improve the phase boost at the crossover frequency. Equation 10 shows the feed forward capacitor must be higher than 29 pF, so 30 pF was used.

$$C6 > \frac{V_{OUT} \times C_{OUT}}{2 \times \pi \times 3.95} \times \frac{1}{R3} \quad (10)$$

The last step is to set the enable threshold. If an external signal is used, then no additional components are required. But if no external enable signal is used, then the resistor divider, composed of R2 and R5, is used. Equation 11 and Equation 12 are used to select R2 and R5 values.

$$R2 = \frac{V_{START} \times \frac{V_{EN\_FALLING}}{V_{EN\_RISING}} - V_{STOP}}{I_P \times \left(1 - \frac{V_{EN\_FALLING}}{V_{EN\_RISING}}\right) + I_H} \quad (11)$$

$$R5 = \frac{R2 \times V_{EN\_FALLING}}{V_{STOP} - V_{EN\_FALLING} + R2 \times \left(I_P + I_H\right)} \quad (12)$$

where

- V_{START} is the voltage at which the converter begin operation (7.5 V here)
- $V_{STOP}$is the voltage below which the converter should be turned off (6.5 V here)
- $V_{EN\_FALLING}$ and V_{EN_RISING} are the falling and rising values of the internal UVLO (1.19 V and 1.21 V, respectively)
- I_P is the enable input current (0.7 μA)
- I_H is the hysteresis current (1.55 μA)

Equation 11 gives 561 kΩ for R2, so 562 kΩ was used. This makes Equation 12 result in 101.7 kΩ for R5, so 102 kΩ was used.

As required, a bootstrap capacitor (C1) of 0.1 μF (X7R or X5R) has to be added between the BOOT pin and the SW pin.

Finally a 0-Ω resistor (R1) was added next to the bootstrap for test purpose (EMC tests). Results of the tests show that this resistor is not needed.

3 Getting Started Hardware

3.1 PCB Overview

A picture of the PCB with the functional blocks is shown in Figure 4.

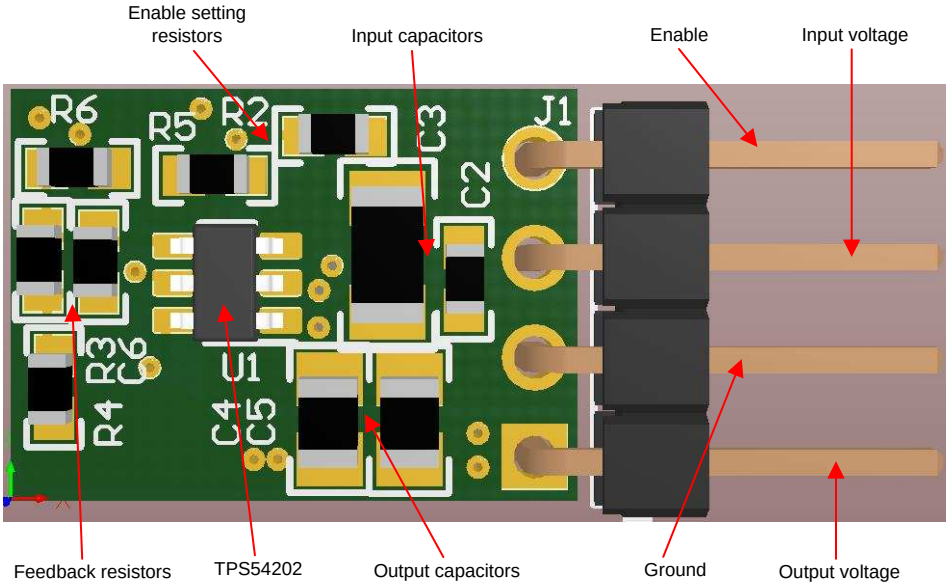

Figure 4. TIDA-00947 PCB With Functional Blocks

The inductor and bootstrap capacitor are placed on the bottom side of the board.

3.2 Connectors Settings

Table 2. Connector Settings

CONNECTOR	FUNCTION
J1-1	V_{OUT}
J1-2	GND
J1-3	V_{IN}
J1-4	EN

4 Testing and Results

4.1 Setup

Figure 5 shows the setup and the test equipment used.

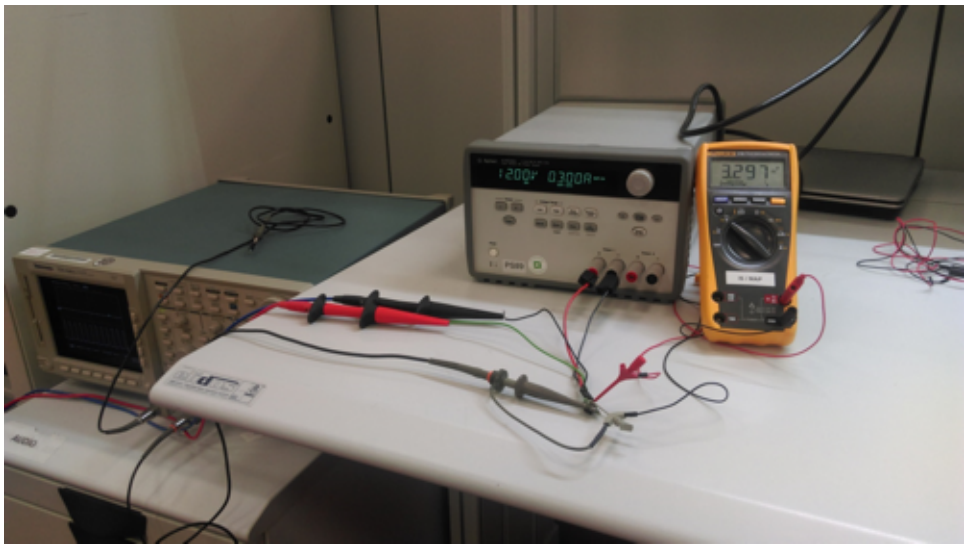

Figure 5. Test Setup for TIDA-00947

Table 3 lists the test equipment used to test the TIDA-00947.

Table 3. Test Equipment

TEST EQUIPMENT	PART NUMBER
Oscilloscope	Tektronix TDS 640A
Voltage probe	Tektronix P6139A
Current probe	LEM PR 30
Multimeter	Fluke 179 and 87 III
Power supply	Agilent E3648A
Electronic load	Chroma 63103 and 6314
Passive load	SNE350x40S2 D040
Temperature chamber	Voetsch VT4002
Thermal camera	Fluke TI40

4.2 Test Results

4.2.1 Efficiency

To test the efficiency, four multimeters are used; two are set up as voltmeters to measure the input and output voltages, and two are set up as ampmeters to measure the input and output currents.

The measurements are done at a room temperature of 22.5ºC.

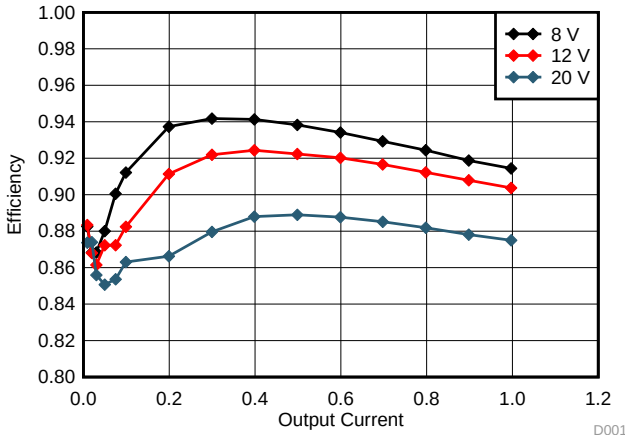

Figure 6. TIDA-00947 Efficiency

Table 4, Table 5, and Table 6 list the details of the efficiency curves shown in Figure 6.

Table 4. Efficiency With 8-V Input

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	η
7.905	0.4534	3.2880	0.9968	0.914443
7.915	0.4062	3.2890	0.8981	0.918751
7.920	0.3585	3.2900	0.7978	0.924433
7.930	0.3114	3.2900	0.6975	0.929284
7.940	0.2657	3.2910	0.5988	0.934109
7.950	0.2200	3.2920	0.4985	0.938286
7.960	0.1750	3.2920	0.3983	0.941280
7.970	0.1314	3.2930	0.2995	0.941748
7.980	0.0877	3.2930	0.1992	0.937300
7.990	0.0447	3.2940	0.0989	0.912149
7.990	0.0343	3.2950	0.0749	0.900526
7.990	0.0232	3.2955	0.0495	0.880018
7.990	0.0143	3.2960	0.0301	0.868302
8.000	0.0093	3.2960	0.0196	0.868301
8.000	0.0042	3.2950	0.0090	0.882589

Table 5. Efficiency With 12-V Input

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	η
11.93	0.3039	3.2870	0.9968	0.903726
11.94	0.2724	3.2880	0.8981	0.907915
11.95	0.2407	3.2890	0.7978	0.912250
11.95	0.2095	3.2900	0.6975	0.916618
11.96	0.1790	3.2900	0.5988	0.920224
11.97	0.1486	3.2910	0.4985	0.922317
11.97	0.1185	3.2920	0.3983	0.924395
11.98	0.0893	3.2930	0.2995	0.921892
11.98	0.0601	3.2940	0.1992	0.911343
11.99	0.0308	3.2950	0.0989	0.882433
11.99	0.0236	3.2955	0.0749	0.872312
11.99	0.0156	3.2960	0.0495	0.872265
12.00	0.0096	3.2970	0.0301	0.861456
12.00	0.0062	3.2950	0.0196	0.868038
12.00	0.0028	3.2980	0.0090	0.883393

Table 6. Efficiency With 20-V Input

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	η
19.950	0.1876	3.285	0.9969	0.875006
19.960	0.1684	3.286	0.8982	0.878088
19.960	0.1490	3.287	0.7979	0.881863
19.970	0.1298	3.289	0.6976	0.885151
19.970	0.1111	3.289	0.5988	0.887674
19.970	0.0924	3.290	0.4986	0.888993
19.975	0.0739	3.291	0.3983	0.887988
19.980	0.0561	3.292	0.2995	0.879627
19.980	0.0379	3.293	0.1992	0.866256
19.990	0.0189	3.297	0.0989	0.863059
19.990	0.0145	3.299	0.0750	0.853616
19.990	0.0096	3.298	0.0495	0.850691
19.990	0.0058	3.297	0.0301	0.855943
19.990	0.0037	3.298	0.0196	0.873961
19.990	0.0017	3.299	0.0090	0.873702

4.2.2 Thermal

The thermal pictures in Figure 7 and Figure 8 were taken at a room temperature of 22.5°C, with a 12-V input, and 3.3 V at a 1-A output without airflow.

The hottest point of the design is the TPS54202 at 53.2°C; this is an increase of 30.7°C. Because the acceptable ambient temperature range is –30°C to 65°C, no heat sink is required for the TIDA-00947 to function properly.

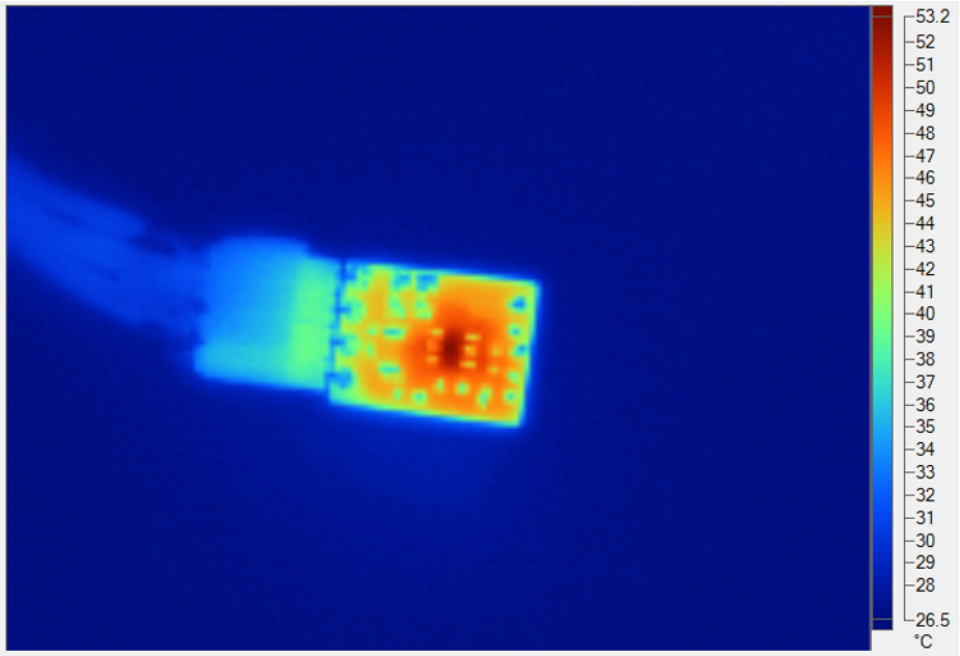

Figure 7. Top-Side Thermal Picture With 12-V_{IN}, 3.3 V at 1-A Output

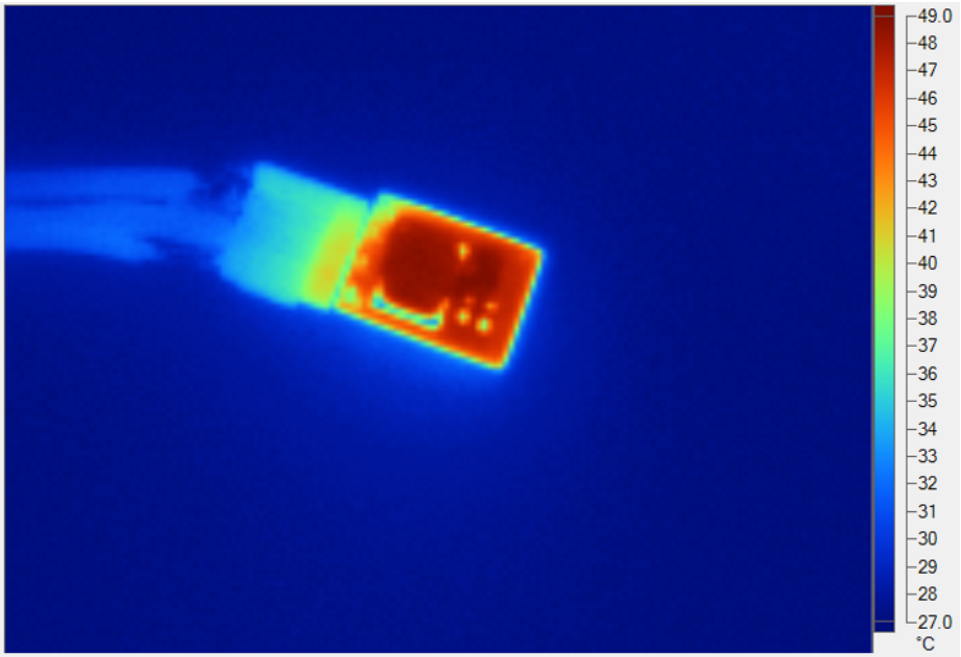

Figure 8. Bottom-Side Thermal Picture With 12-V_{IN}, 3.3 V at 1-A Output

4.2.3 Line and Load Regulation Over Temperature

Figure 9, Figure 10, and Figure 11 show the output voltage variation, depending load current and input voltage across –30ºC to 65ºC.

Across all input voltages, output currents, and temperature conditions, the output voltage varies between 3.274 and 3.303 V. This is 0.88% of the output voltage, which is well below the initial target of ±1%.

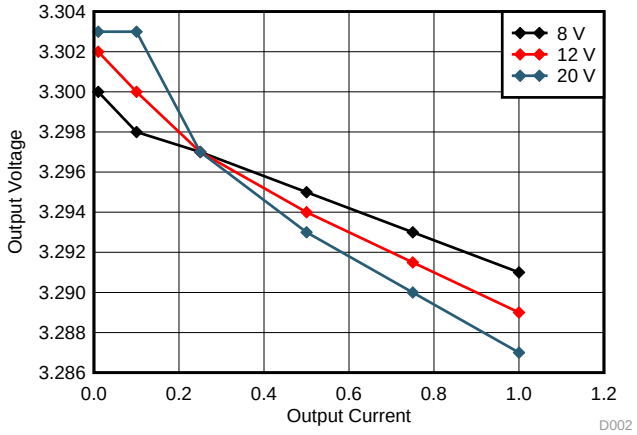

Figure 9. Line and Load Regulation at 65ºC

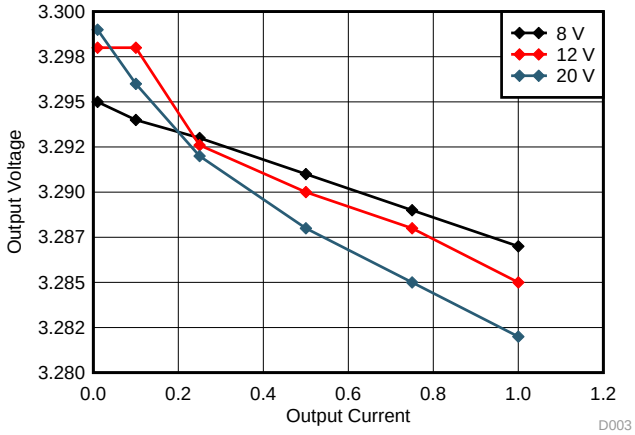

Figure 10. Line and Load Regulation at 22.5ºC

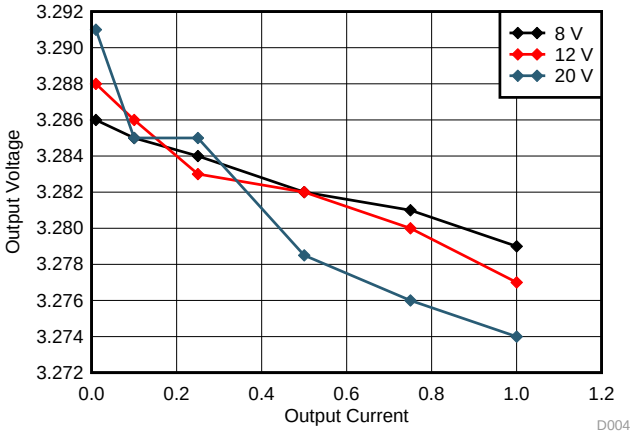

Figure 11. Line and Load Regulation at –30ºC

Table 7, Table 8, and Table 9 list the details of the line and load regulation over temperature curves shown in Figure 9, Figure 10, and Figure 11.

Table 7. Line and Load Regulation at 65ºC

V_{IN}	V_{OUT}	I_{OUT}
20	3.287	1.00
20	3.290	0.75
20	3.293	0.50
20	3.297	0.25
20	3.303	0.10
20	3.303	0.01
12	3.289	1.00
12	3.292	0.75
12	3.294	0.50
12	3.297	0.25
12	3.300	0.10
12	3.302	0.01
8	3.291	1.00
8	3.293	0.75
8	3.295	0.50
8	3.297	0.25
8	3.298	0.10
8	3.300	0.01

Table 8. Line and Load Regulation at 22.5ºC

V_{IN}	V_{OUT}	I_{OUT}
20	3.282	1.00
20	3.285	0.75
20	3.288	0.50
20	3.292	0.25
20	3.296	0.10
20	3.299	0.01
12	3.285	1.00
12	3.288	0.75
12	3.290	0.50
12	3.293	0.25
12	3.298	0.10
12	3.298	0.01
8	3.287	1.00
8	3.289	0.75
8	3.291	0.50
8	3.293	0.25
8	3.294	0.10
8	3.295	0.01

Table 9. Line and Load Regulation at –30ºC

V_{IN}	V_{OUT}	I_{OUT}
20	3.2740	1.00
20	3.2760	0.75
20	3.2785	0.50
20	3.2850	0.25
20	3.2850	0.10
20	3.2910	0.01
12	3.2770	1.00
12	3.2800	0.75
12	3.2820	0.50
12	3.2830	0.25
12	3.2860	0.10
12	3.2880	0.01
8	3.2790	1.00
8	3.2810	0.75
8	3.2820	0.50
8	3.2840	0.25
8	3.2850	0.10
8	3.2860	0.01

4.2.4 Output Voltage Ripple

The output voltage ripple remains below 20 mVpp under full load (1 A), low load (10 mA), or no load. This is well below the initial requirements of ±1%.

Measurements were done at 22.5ºC room temperature with 12-V input voltage. The upper curve (1) is the output voltage with oscilloscope in AC-coupling mode with 50 mV/div. The lower curve (2) is the switch node (pin 2 of the TPS54202) with 5 V/div.

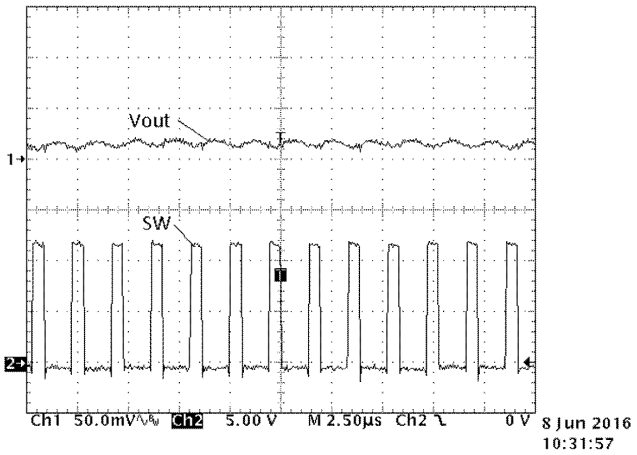

Figure 12. Output Voltage Ripple at 1-A Output Load

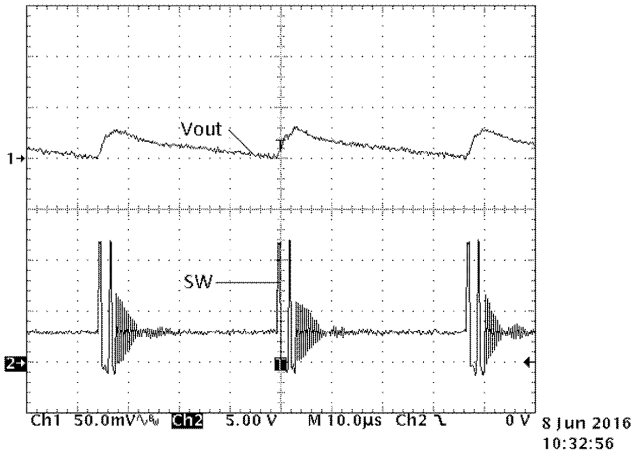

Figure 13. Output Voltage Ripple at 10-mA Output Load

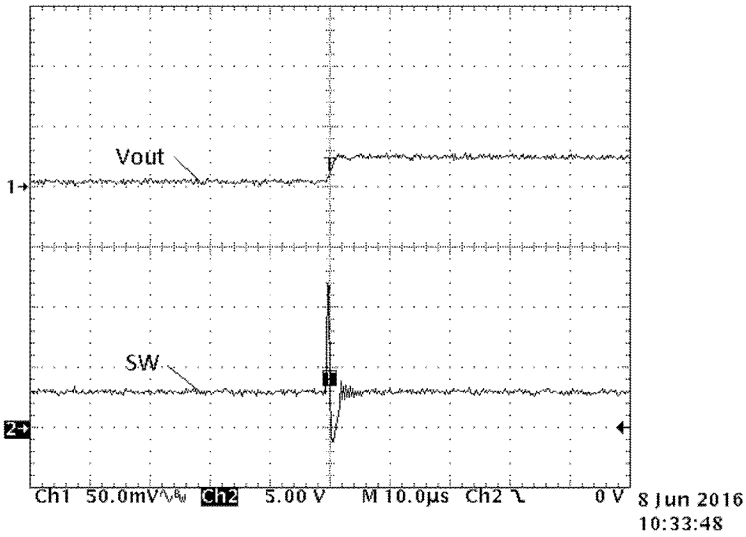

Figure 14. Output Voltage Ripple at No Load Output

4.2.5 Transient Response

The transient response is below ±200 mV for load steps between 10 mA and 1 A, which were the design requirements (±5%).

Measurements were done at 22.5°C room temperature with 12-V input voltage. The upper curve (1) is the output voltage with oscilloscope in AC-coupling mode with 100 mV/div. The lower curve (2) is the output current with the current probe 100 mV/A with 200 mV/div. The load step is applied with a 250-mA/μs slew rate.

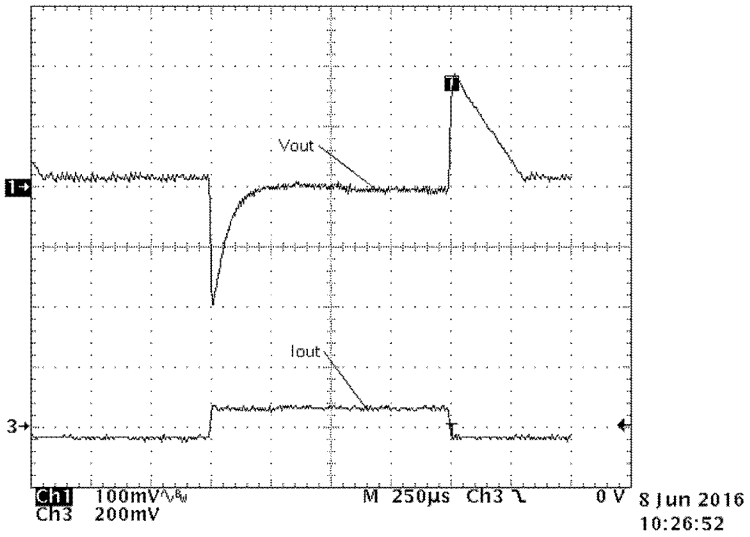

Figure 15. Transient Response From 10-mA to 1-A Output Load

4.2.6 Start-up and Shutdown

For the start-up and the shutdown behavior, 12 V is applied at the input with a 1-A load at the output.

The EN setting resistors (R2 and R5) are not populated, and the Enable pin is controlled with a 5-V signal.

Measurements were done at 22.5ºC room temperature. The upper curve (1) is the output voltage with oscilloscope in DC-coupling mode with 2 V/div. The lower curve (2) is the Enable signal with 5 V/div.

The TIDA-00947 takes 7 ms to provide 3.3 V at the output after the EN pin is enable. The output voltage is reached without overshoot.

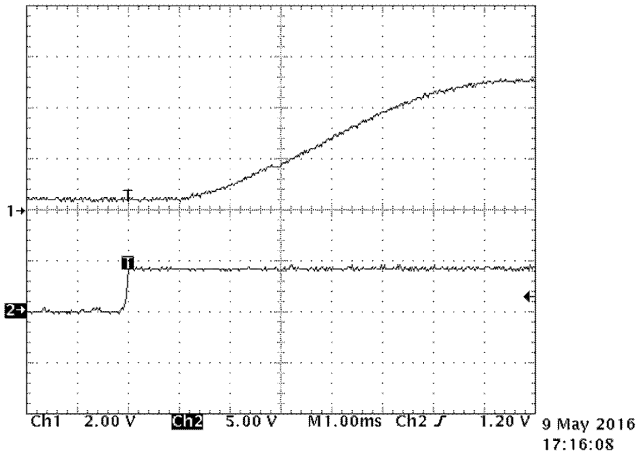

Figure 16. Start-up at 12-V Input and 1-A Output Load

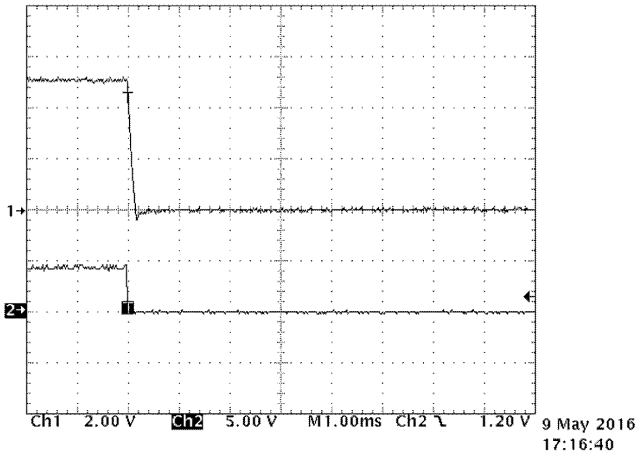

Figure 17. Shutdown at 12-V Input and 1-A Output Load

4.2.7 Overcurrent and Short-Circuit Test

The overcurrent protection was tested by having a transient load from 1- to 3-A output current while the board is supplied with 12 V. The short-circuit protection was tested by shorting the output pin to ground.

The upper curve (1) is the output voltage with oscilloscope in DC-coupling mode with 2 V/div (Figure 18) and 100 mV/div (Figure 19). The lower curve (2) is the output current with the current probe 100 mV/A with 200 mV/div.

As shown in Figure 18 and Figure 19, when the current is rising to the current limit level, the device enters overcurrent protection as described in the TPS54202 datasheet (SLVSD26). After waiting the pre-programmed time, the device tries to restart. Once the fault condition is removed, the device starts normally.

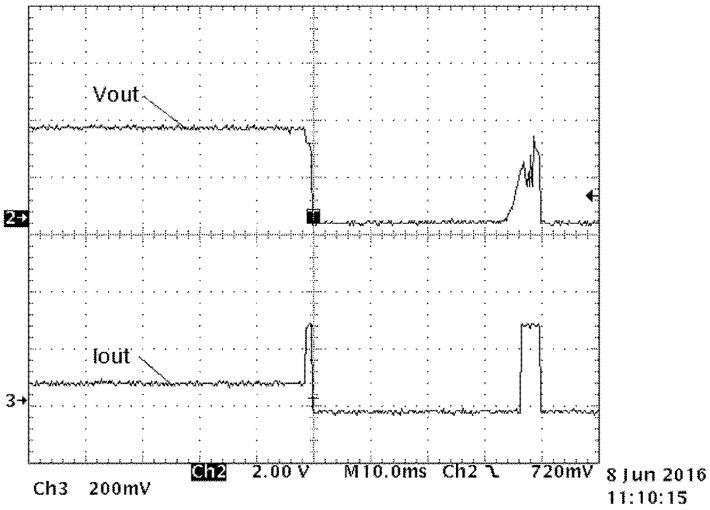

Figure 18. Overcurrent Protection

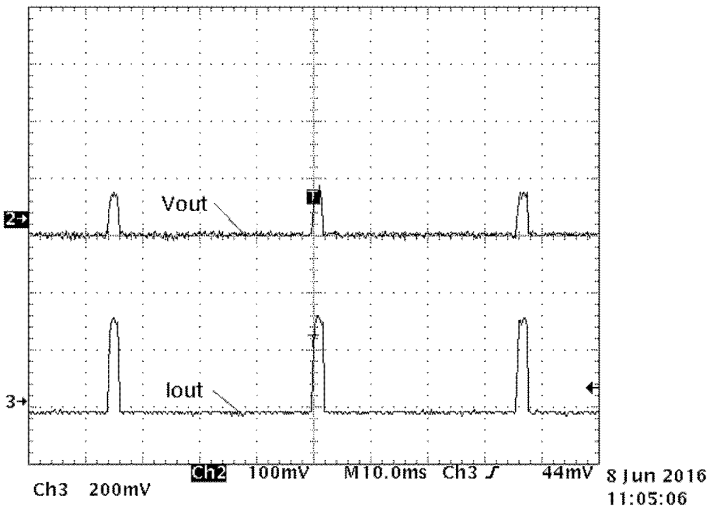

Figure 19. Short-Circuit Protection

4.2.8 Overvoltage Test

The overvoltage protection was tested by applying 3.65 V at the output of the TIDA-00947 board while the board is supplied with 12 V and with a 1-A output load.

The upper curve (4) is the output voltage with oscilloscope in DC-coupling mode with 2 V/div. The middle curve (3) is the current coming out of the TIDA-00947 with the current probe at 100 mV/A with 50 mV/div. The lower curve (2) is voltage at the switch node with 5 V/div.

As described in page 11 of the TPS54202 datasheet (SLVSD26), if the voltage on the FB pin is higher than 108% of the V_{REF}, the high-side MOSFET is turned off. Once the fault condition is removed, the device starts switching normally again.

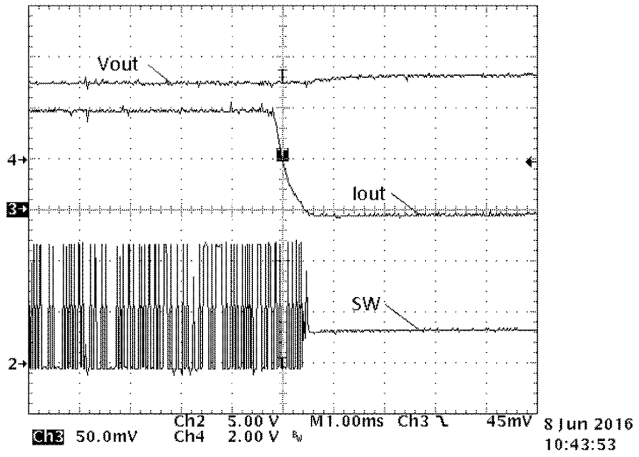

Figure 20. Overvoltage Protection From 3.3 to 3.65 V

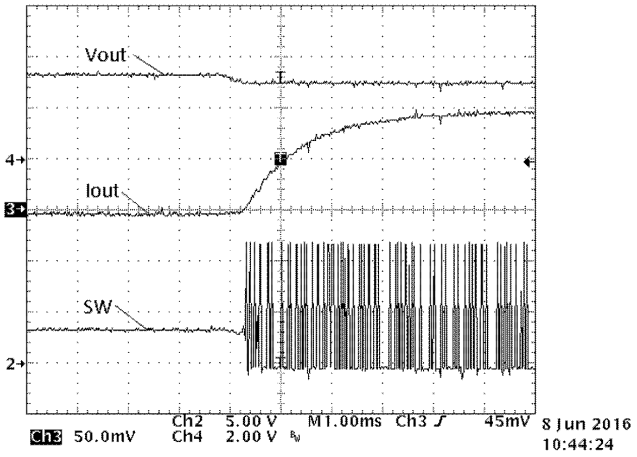

Figure 21. Overvoltage Protection From 3.65 to 3.3 V

4.2.9 Standby and No-Load Currents

The standby current was measured with an ampmeter at 22.5°C room temperature with a 12-V input voltage. The enable pin was set low through the connector, and the enable setting resistors (R2 and R5) not populated. The standby current was measured at 1.5 μA.

The no-load current was measured with an ampmeter at 22.5°C room temperature with a 12-V input voltage, with the enable setting resistors (R2 and R5) populated and no load attached at the output. The no-load current was measured at 84 μA.

4.2.10 EMC Tests

The TIDA-00947 TI Design has been tested for EMI according to EN55022 Class B conducted and radiated emissions. The EMC tests were performed by CSA Group Bayern GmbH (Germany).

4.2.10.1 Conduction Emission

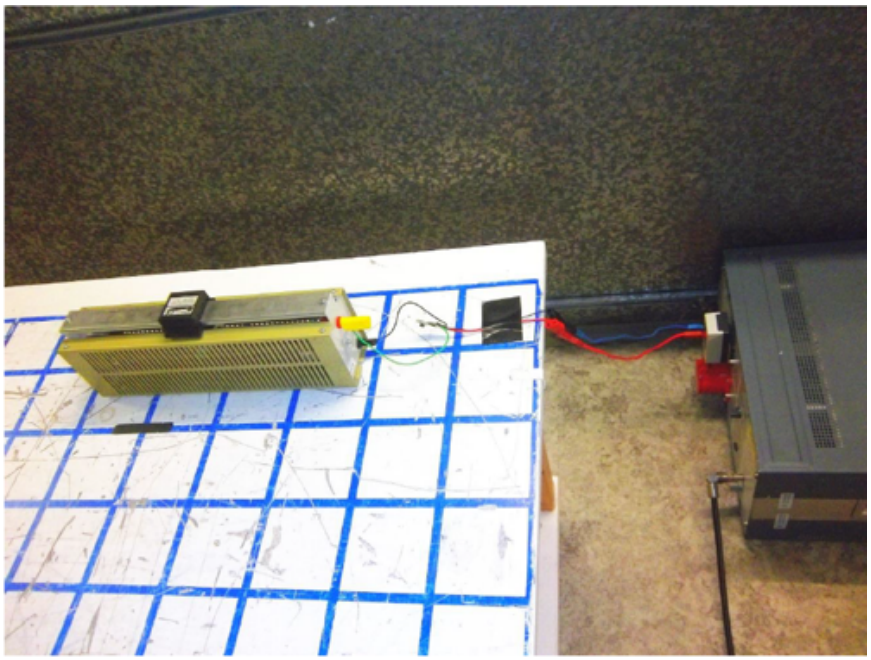

Figure 22. Conducted Emission Test Setup

The first test was performed without an input filter, and the conducted test did not pass.

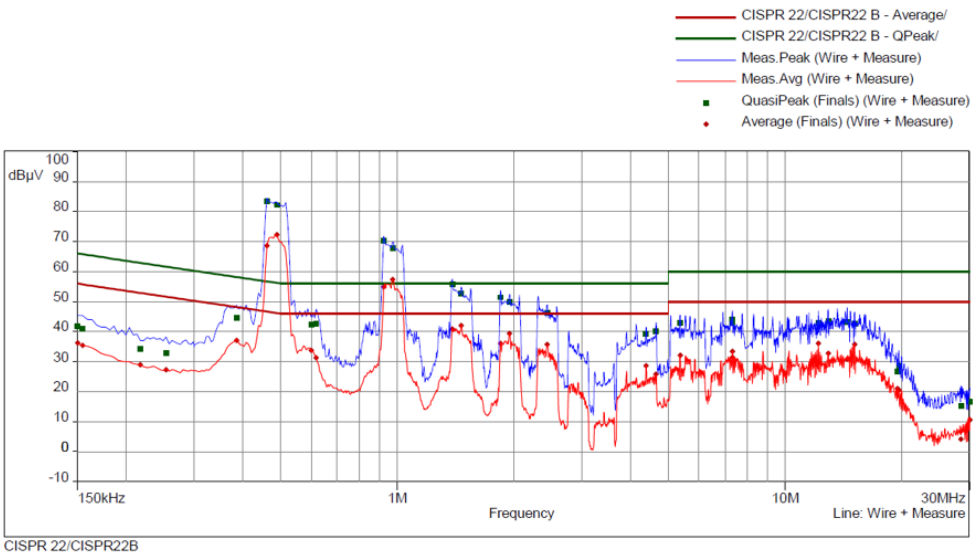

Figure 23. Conducted Emission Test Result Without Filter

Table 10. Conducted Emission Test Result Without Filter

FREQ (MHz)	SR	QP (dBµV)	MARGIN (dB)	LIMIT (dB)	AV (dBµV)	MARGIN (dB)	LIMIT (dB)	LINE	CORR (dB)
0.1500	1	41.85	24.15	66.00	36.19	19.81	56.00	Wire +	10.06
0.1545	1	40.81	24.95	65.75	35.35	20.40	55.75	Wire +	10.06
0.2175	1	34.34	28.57	62.91	29.01	23.90	52.91	Wire +	10.06
0.2535	1	32.93	28.71	61.64	27.39	24.25	51.64	Wire +	10.06
0.3855	2	44.74	13.42	58.16	37.05	11.11	48.16	Wire +	10.06
0.4620	2	83.47	–26.81	56.66	68.68	–22.02	46.66	Wire +	10.06
0.4890	2	82.13	–25.94	56.18	72.22	–26.04	46.18	Wire +	10.06
0.6000	3	42.34	13.66	56.00	33.78	12.22	46.00	Wire +	10.07
6.1800	3	42.64	13.36	56.00	31.36	14.64	46.00	Wire +	10.07
0.9240	3	70.28	–14.28	56.00	54.89	–8.89	46.00	Wire +	10.07
0.9735	3	67.88	–11.88	56.00	57.35	–11.35	46.00	Wire +	10.07
1.3890	4	55.70	0.30	56.00	40.84	5.16	46.00	Wire +	10.07
1.4610	4	52.62	3.38	56.00	42.10	3.90	46.00	Wire +	10.07
1.8480	4	51.44	4.56	56.00	36.16	9.84	46.00	Wire +	10.08
1.9470	4	49.82	6.18	56.00	39.32	6.68	46.00	Wire +	10.08
2.4360	5	46.31	9.69	56.00	35.77	10.23	46.00	Wire +	10.09
4.3890	5	39.20	16.80	56.00	28.61	17.39	46.00	Wire +	10.11
4.6545	5	40.30	15.70	56.00	25.80	20.20	46.00	Wire +	10.12
5.3670	6	42.94	17.06	60.00	32.19	17.81	50.00	Wire +	10.13
7.3200	6	43.99	16.01	60.00	33.45	16.55	50.00	Wire +	10.16
7.3245	6	43.10	16.90	60.00	31.49	18.51	50.00	Wire +	10.16
12.1965	7	43.02	16.98	60.00	36.09	13.91	50.00	Wire +	10.25
12.9255	7	43.54	16.46	60.00	32.84	17.16	50.00	Wire +	10.27
14.4870	7	43.25	16.75	60.00	30.85	19.15	50.00	Wire +	10.31
15.1170	7	42.58	17.42	60.00	35.72	14.28	50.00	Wire +	10.32
19.5015	8	26.63	33.37	60.00	21.01	28.99	50.00	Wire +	10.43
19.6545	8	28.69	31.31	60.00	20.52	29.48	50.00	Wire +	10.43
28.4295	8	15.24	44.76	60.00	4.27	45.73	50.00	Wire +	10.56
29.9865	8	16.67	43.33	60.00	10.67	39.33	50.00	Wire +	10.59

A small filter (10-µF capacitor and 5-µH inductor) was then added at the input, which allowed the board to pass the conducted emission test with more than 12 dB of margin.

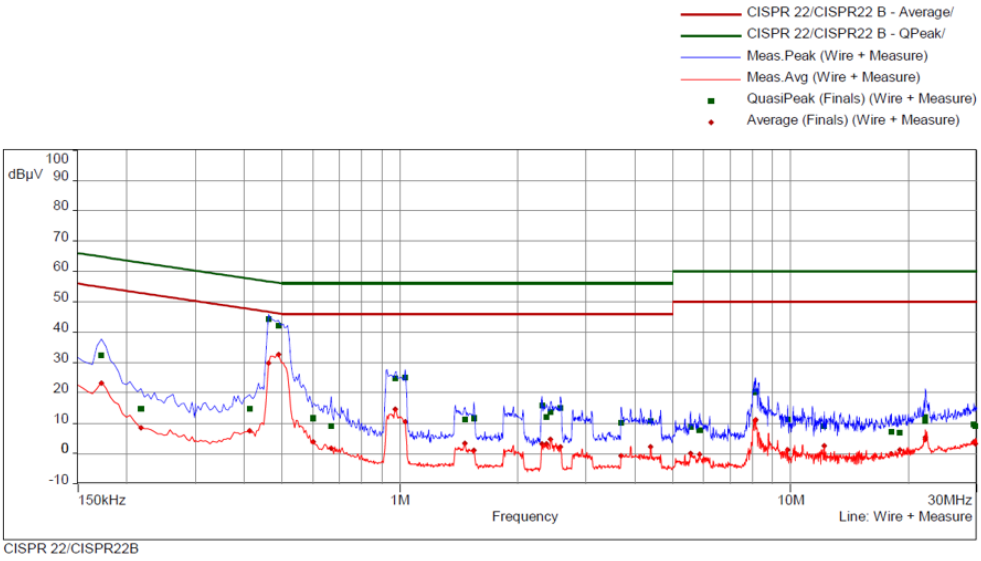

Figure 24. Conducted Emission Test Result With Filter (Wire +)

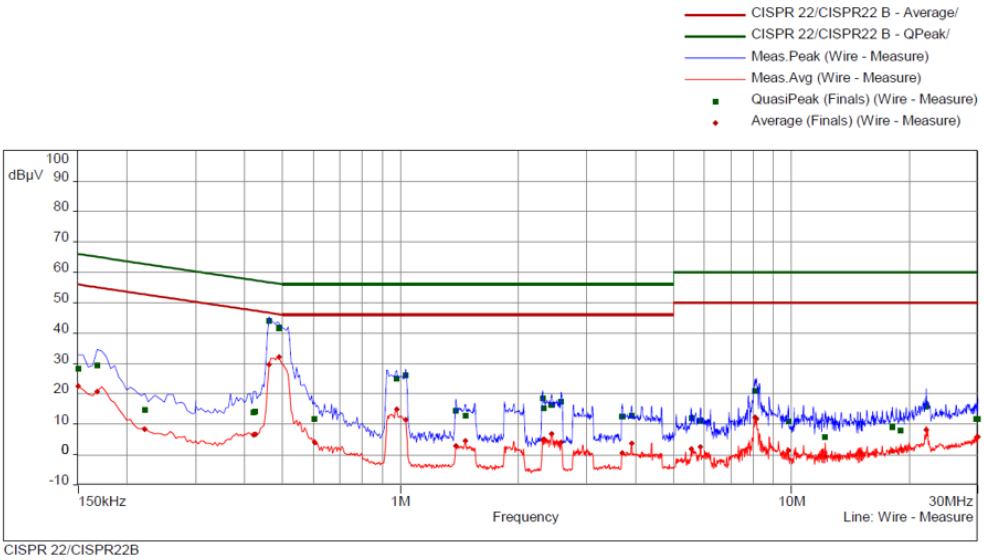

Figure 25. Conducted Emission Test Result With Filter (Wire –)

Table 11. Conducted Emission Test Result With Filter

FREQ (MHz)	SR	QP (dBµV)	MARGIN (dB)	LIMIT (dB)	AV (dBµV)	MARGIN (dB)	LIMIT (dB)	LINE	CORR (dB)
0.1500	1	28.35	37.65	66.00	22.53	33.47	56.00	Wire –	10.06
0.1680	1	29.40	35.66	65.06	20.78	34.28	55.06	Wire –	10.06
0.2220	1	14.54	48.20	62.74	8.33	44.42	52.74	Wire –	10.06
0.4215	2	13.87	43.54	57.42	6.50	40.91	47.42	Wire –	10.06
0.4260	2	14.27	43.06	57.33	6.64	40.69	47.33	Wire –	10.06
0.4620	2	44.04	12.62	56.66	29.61	17.05	46.66	Wire –	10.06
0.4890	2	41.78	14.40	56.18	62.16	14.02	46.18	Wire –	10.06
0.6045	3	11.64	44.36	56.00	4.11	41.89	46.00	Wire –	10.07

Table 11. Conducted Emission Test Result With Filter (continued)

FREQ (MHz)	SR	QP (dBµV)	MARGIN (dB)	LIMIT (dB)	AV (dBµV)	MARGIN (dB)	LIMIT (dB)	LINE	CORR (dB)
0.9780	3	24.96	31.04	56.00	14.95	31.05	46.00	Wire –	10.07
1.0320	3	26.02	29.98	56.00	11.43	34.57	46.00	Wire –	10.07
1.3890	4	14.51	41.49	56.00	2.81	43.19	46.00	Wire –	10.07
1.4655	4	12.88	43.12	56.00	4.58	41.42	46.00	Wire –	10.07
2.3115	4	18.54	37.46	56.00	4.92	41.08	46.00	Wire –	10.08
2.3340	4	15.24	40.76	56.00	5.07	40.93	46.00	Wire –	10.08
2.4360	5	16.48	39.52	56.00	6.83	39.17	46.00	Wire –	10.09
2.5800	5	17.40	38.60	56.00	4.11	41.89	46.00	Wire –	10.09
3.6915	5	12.42	43.58	56.00	0.57	45.43	46.00	Wire –	10.10
3.9030	5	12.74	43.26	56.00	3.75	42.25	46.00	Wire –	10.11
5.5425	6	11.92	48.08	60.00	1.87	48.13	50.00	Wire –	10.13
5.8530	6	11.37	48.63	60.00	2.53	47.47	50.00	Wire –	10.13
8.0670	6	21.01	38.99	60.00	12.28	37.72	50.00	Wire –	10.17
8.1345	6	21.02	38.98	60.00	11.82	38.18	50.00	Wire –	10.17
9.8340	7	10.93	49.07	60.00	1.37	48.63	50.00	Wire –	10.19
12.2100	7	5.74	54.26	60.00	–0.49	50.49	50.00	Wire –	10.25
18.1095	7	9.24	50.76	60.00	1.20	48.80	50.00	Wire –	10.40
19.0365	7	7.96	52.04	60.00	1.99	48.01	50.00	Wire –	10.42
22.1565	8	15.97	44.03	60.00	8.19	41.81	50.00	Wire –	10.48
29.7435	8	11.63	48.37	60.00	5.78	44.22	50.00	Wire –	10.59
29.9955	8	11.70	48.30	60.00	5.79	44.21	50.00	Wire –	10.59
0.1725	9	32.36	32.48	64.84	23.21	31.63	54.84	Wire +	10.06
0.2175	9	14.77	48.14	62.91	8.54	44.38	52.91	Wire +	10.06
0.4125	10	14.73	42.86	57.60	7.52	40.07	47.60	Wire +	10.06
0.4620	10	44.40	12.26	56.66	29.87	16.79	46.66	Wire +	10.06
0.4890	10	42.27	13.92	56.18	32.63	13.56	46.18	Wire +	10.06
0.6000	11	11.72	44.28	56.00	3.91	42.09	46.00	Wire +	10.07
0.6675	11	9.18	46.82	56.00	1.69	44.31	46.00	Wire +	10.07
0.9735	11	24.63	31.37	56.00	14.61	31.39	46.00	Wire +	10.07
1.0320	11	25.02	30.98	56.00	10.53	35.47	46.00	Wire +	10.07
1.4655	12	11.23	44.77	56.00	3.38	42.62	46.00	Wire +	10.07
1.5465	12	11.69	44.31	56.00	1.02	44.98	46.00	Wire +	10.07
2.3115	12	16.02	39.98	56.00	3.23	42.77	46.00	Wire +	10.08
2.3700	12	12.01	43.99	56.00	3.26	42.74	46.00	Wire +	10.08
2.4315	13	13.71	42.29	56.00	4.65	41.35	46.00	Wire +	10.08
2.5800	13	15.10	40.90	56.00	2.22	43.78	46.00	Wire +	10.09
3.6870	13	10.14	45.86	56.00	–0.75	46.75	46.00	Wire +	10.10
4.3890	13	10.70	45.30	56.00	2.22	43.78	46.00	Wire +	10.11
5.5425	14	8.90	51.10	60.00	0.02	49.98	50.00	Wire +	10.13
5.8485	14	7.77	52.23	60.00	–0.23	50.23	50.00	Wire +	10.13
8.1300	14	20.09	39.91	60.00	10.88	39.12	50.00	Wire +	10.17
8.1345	14	20.53	39.47	60.00	11.23	38.77	50.00	Wire +	10.17
9.8340	15	11.22	48.78	60.00	1.18	48.82	50.00	Wire +	10.19
12.2010	15	9.24	50.76	60.00	2.52	47.48	50.00	Wire +	10.25
18.1095	15	7.16	52.84	60.00	–0.16	50.16	50.00	Wire +	10.40
19.0320	15	6.90	53.10	60.00	1.25	48.75	50.00	Wire +	10.42
22.1610	16	12.09	47.91	60.00	5.34	44.66	50.00	Wire +	10.48

Table 11. Conducted Emission Test Result With Filter (continued)

FREQ (MHz)	SR	QP (dBµV)	MARGIN (dB)	LIMIT (dB)	AV (dBµV)	MARGIN (dB)	LIMIT (dB)	LINE	CORR (dB)
22.1655	16	10.73	49.27	60.00	4.79	45.21	50.00	Wire +	10.48
29.4960	16	9.50	50.50	60.00	3.93	46.07	50.00	Wire +	10.58
29.7705	16	9.07	50.93	60.00	3.15	46.85	50.00	Wire +	10.59

4.2.10.2 Radiated Emission

The radiated emission was tested first with a prescan test with an antenna at 3 m and a threshold higher from 10 dB. This pretest identifies the critical points (less than 20 dB of margin) for the 10-m test.

Figure 26. Radiated Emission 3-m Prescan Test Setup

CAUTION

For the prescan, due to the shorter distance (3 m instead of 10 m), the threshold for radiated EMI of EN55022 is higher by 10 dB.

During the prescan, the board passed the radiated emission test with more than 8 dB of margin.

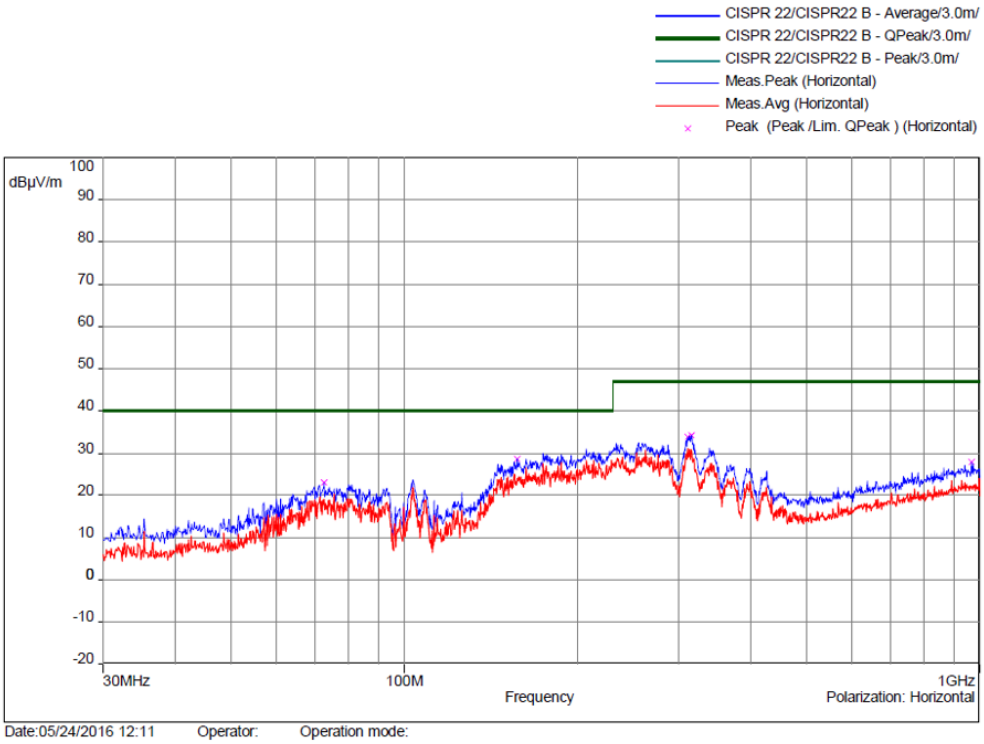

Figure 27. Radiated Emission 3-m Prescan Test Horizontal Polarization

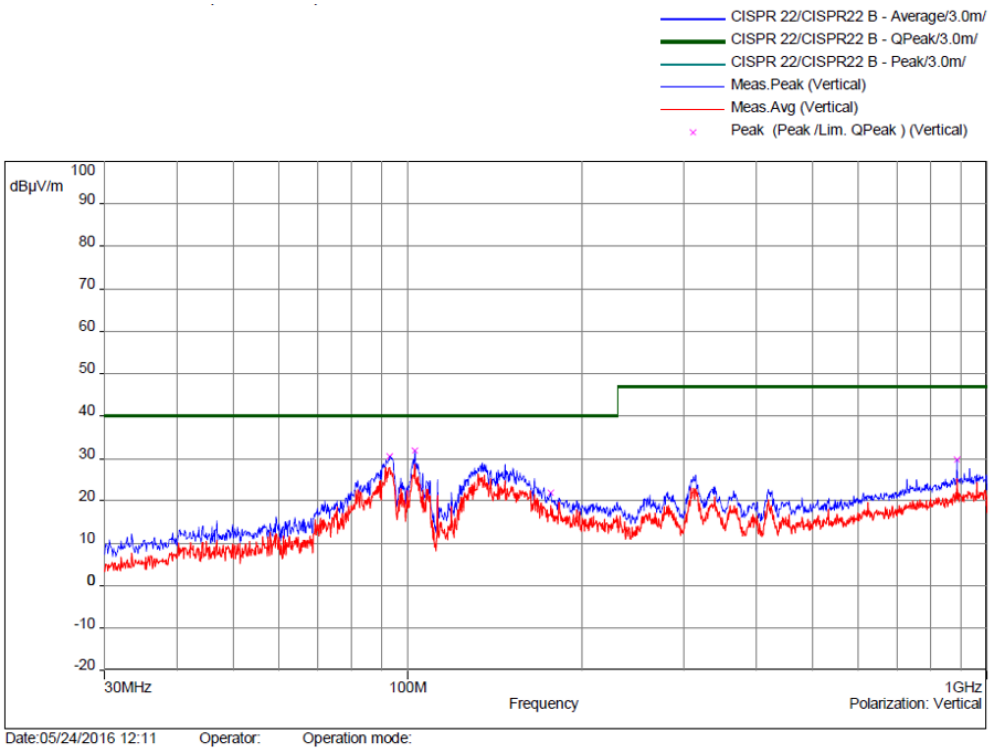

Figure 28. Radiated Emission 3-m Prescan Test Vertical Polarization

Table 12. Radiated Emission 3-m Prescan List of Critical Points

FREQ (MHz)	SR	PK (dBµV/m)	LIMIT QP (dBµV/m)	MARGIN (dB)	ANGLE	POLARIZATION	CORR
72.58725873	1	23.01	40.00	–16.99	69.30	Horizontal	–8.54
157.17971800	1	28.63	40.00	–11.37	259.30	Horizontal	–5.88
310.74607460	1	33.81	47.00	–13.19	209.40	Horizontal	–4.67
315.30553060	1	34.15	47.00	–12.85	239.40	Horizontal	–4.62
967.21072110	1	27.78	47.00	–19.22	189.50	Horizontal	7.42
93.15331533	2	30.44	40.00	–9.56	129.30	Vertical	–10.10
103.04830480	2	31.86	40.00	–8.14	169.30	Vertical	–8.65
176.87268730	2	21.85	40.00	–18.15	229.40	Vertical	–6.34
887.46874690	2	29.67	47.00	–17.33	319.30	Vertical	6.01

Those critical points are then tested in the typical 10-m setup.

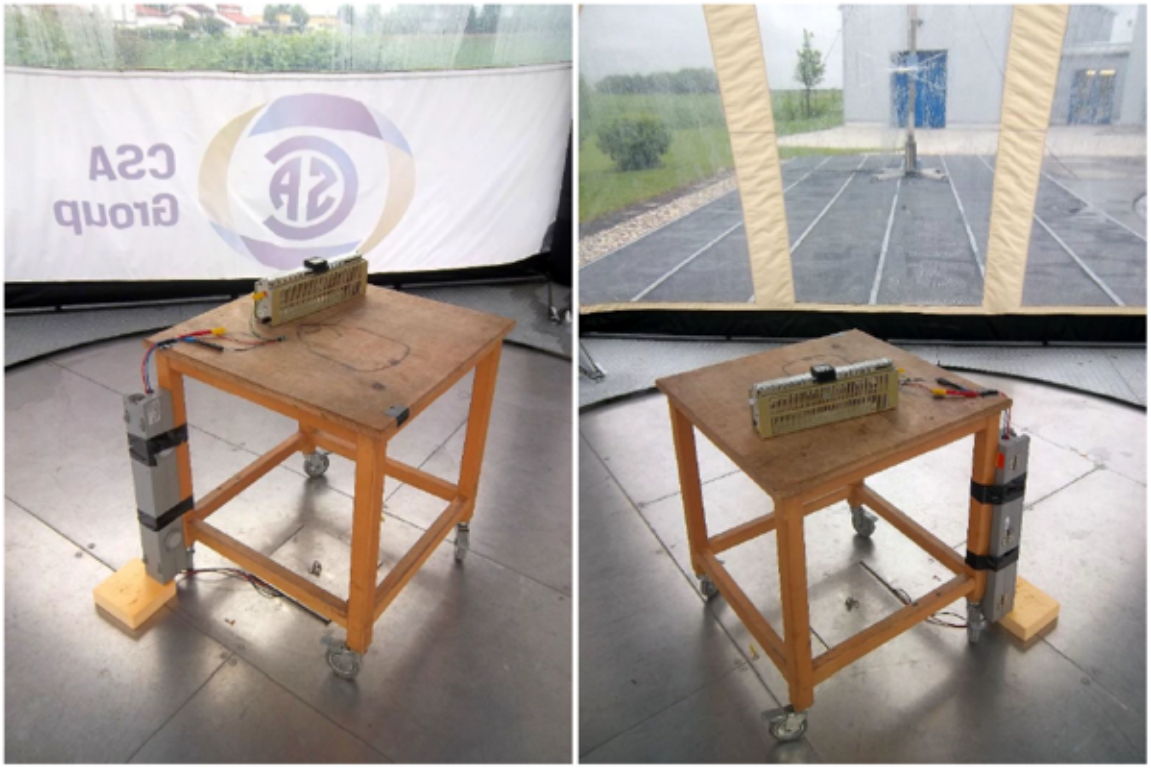

Figure 29. Radiated Emission 10-m Test Setup

During the 10-m setup, the board passed the radiated emission test with more than 13 dB of margin.

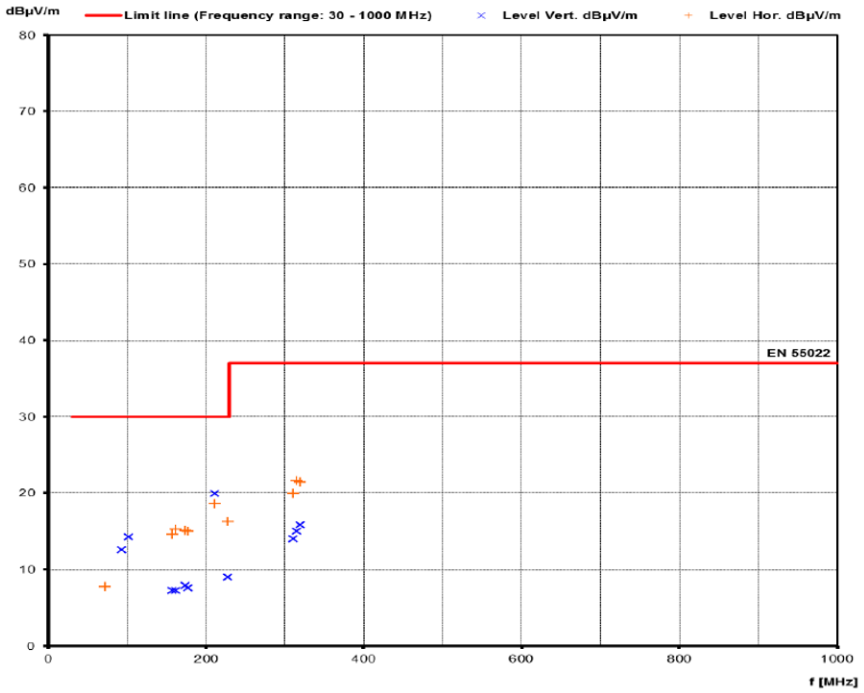

Figure 30. Radiated Emission 10-m Test Result

Table 13. Radiated Emission 10-m Test Result

FREQ (MHz)	READING VERT (dBµV)	READING HOR (dBµV)	CORRECT VERT (dB/m)	CORRECT HOR (dB/m)	LEVEL VERT (dBµV/m)	LEVEL HOR (dBµV/m)	LIMIT (dBµV/m)	D_{LIMIT} (dB)
72.60	—	–2.6	—	10.3	—	7.7	30.0	–22.3
93.30	0.6	—	12.0	—	12.6	—	30.0	–17.4
102.80	1.2	—	13.0	—	14.2	—	30.0	–15.8
157.00	–3.3	4.1	10.5	10.5	7.2	14.6	30.0	–15.4
162.00	–3.5	4.5	10.7	10.7	7.2	15.2	30.0	–14.8
174.00	–3.6	3.6	11.4	11.4	7.8	15.0	30.0	–15.0
177.00	–4.1	3.3	11.7	11.7	7.6	15.0	30.0	–15.0
212.00	6.2	4.8	13.7	13.7	19.9	18.5	30.0	–10.1
228.00	–5.4	1.9	14.3	14.3	8.9	16.2	30.0	–13.8
310.70	–3.1	2.9	17.0	17.0	13.9	19.9	37.0	–17.1
315.70	–2.2	4.4	17.2	17.2	15.0	21.6	37.0	–15.4
320.00	–1.5	4.1	17.3	17.3	15.8	21.4	37.0	–15.6

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00947.

5.2 Bill of Materials

To download the bill of materials, see the design files at TIDA-00947.

5.3 PCB Layout Recommendations

In switch mode DC/DC, special care must be taken to avoid coupling between the different loops. In a Buck topology, the input loop is particularly critical; for this reason, the input capacitors must be placed as close as possible to the TPS54202.

This is done by separating the noise sensitive loop (Feedback and Enable) from the high di/dt loops (input, switch node, bootstrap). This is done by placing the components and traces of the feedback and enable loop as far as possible from components and traces with high di/dt.

Special attention was also given to the ground plane; trying to make it as large and as solid as possible, to both reduce noise sensitivity, and help thermal dissipation.

With regards to thermal dissipation, the input and output voltage planes must also made as large and solid as possible to help keep the board as cool as possible.

Lastly, the soldering pad for the inductor was slightly enlarged to allow the tests of several inductors.

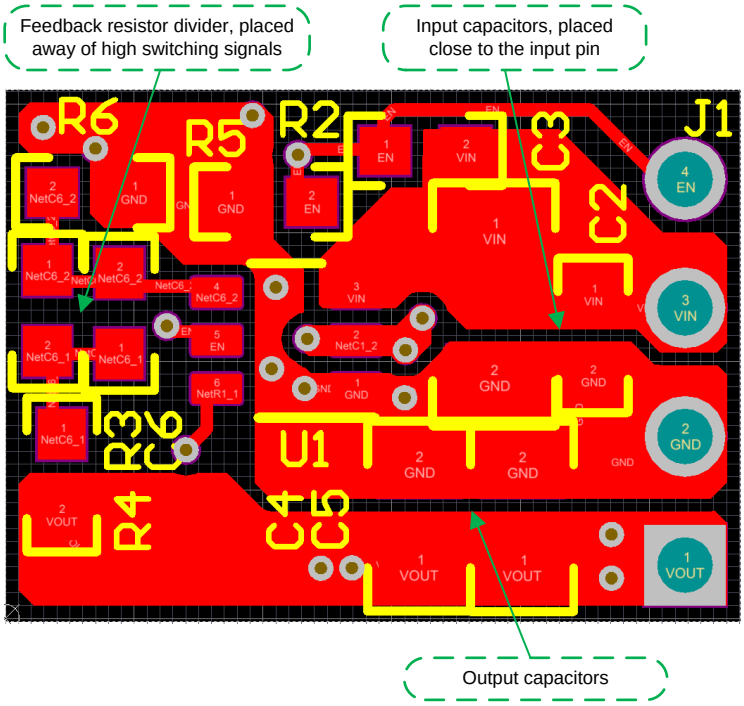

Figure 31. Top Layer

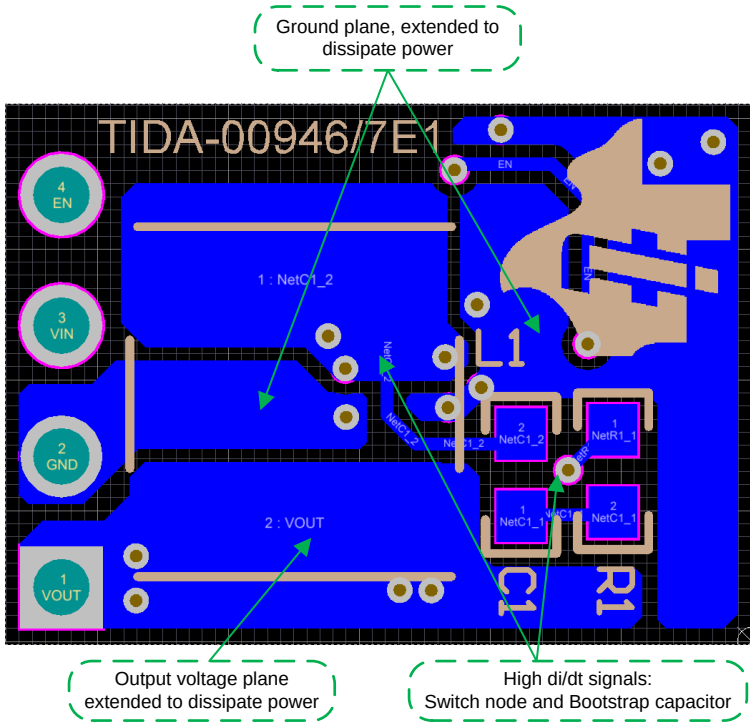

Figure 32. Bottom Layer (Flipped)

5.3.1 Layout Prints

To download the layout prints, see the design files at TIDA-00947.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00947.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00947.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00947.

6 References

1. Texas Instruments, *Understanding Buck Power Stages In Switchmode Power Supplies*, Application Report (SLVA057)
2. Texas Instruments, *Layout Tips for EMI Reduction in DC / DC Converters*, AN-2155 Application Report (SNVA638)
3. Texas Instruments, *Simple Success With Conducted EMI From DCDC Converters*, AN-2162 Application Report (SNVA489)

6.1 Trademarks

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7 About the Author

KEVIN STAUDER is a system engineer in the Industrial Systems team at Texas Instruments, responsible for developing TI Designs for industrial applications.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2016) to A Revision	Page
• Changed from preview page	1

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