PMP9767 Test Report – Efficient, LDO-free Power Supply for a 12-bit 500-MSPS ADC

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ABSTRACT

The electrical performance of data converters depends on the cleanliness of their supply voltages, particularly the analog domain supply. In order to quickly achieve a clean enough power supply solution that is sure to not degrade the data converter's performance, linear regulators (LDOs) are widely used to lower the input supply voltage to the various voltages needed by the data converter. LDOs are relatively simple to design. However, LDOs have high power dissipation across them. To overcome this, engineers sometimes use a switch mode power supply (SMPS), also known as a 'DC/DC' or 'switcher', to efficiently step down the input voltage, followed by an LDO to make a cleaner output voltage. This two-chip approach combines good efficiency and power cleanliness but adds cost. A single-chip solution using just a SMPS is a cost-effective and efficient power supply solution which does not degrade the performance of the 12-bit ADS540x family of analog to digital converters (ADCs). This application report applies to the ADS5401 through ADS5409 and ADS54T01 through ADS54T04.

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1 ADS540x Power Requirements

The ADS540x family has straightforward power requirements, as shown in Figure 1.

POWER SUPPLY					
I_{AVDD33}	3.3V Analog supply current		239	270	mA
I_{AVDD18}	1.8V Analog supply current		79	90	mA
I_{AVDDC}	1.8V Clock supply current		27	35	mA
I_{DVDD}	1.8V Digital supply current	Auto Correction Disabled	117	140	mA
I_{DVDD}	1.8V Digital supply current	Auto Correction Enabled	207		mA
I_{DVDD}	1.8V Digital supply current	Auto Correction Disabled, decimation filter enabled	142		mA
$I_{DVDDLVDS}$	1.8V LVDS supply current	Unused LVDS outputs Disabled	104	120	mA
I_{IOVDD}	1.8V I/O Voltage supply current		1	2	mA

Figure 1. The power requirements of the ADS5407

While there are separate pins for the different sub-system voltages, it is generally recommended to combine digital supply circuits which operate at the same voltage (1.8 V in this case). For the ADS540x, the 1.8 V rails are further combined off of one common regulator with ferrite bead plus capacitor filters placed between the common voltage rail and each sub-system. This allows the ADS540x to be powered with just two regulators—a very common 1.8 V and 3.3 V. See Reference 1 for details of this implementation.

Table 1 shows the resulting four sub-systems, two supply voltages and the typical current required by each. Auto correction is assumed to be enabled to get a worst case power budget.

Table 1. The ADS5407's four voltage domains

<table>
<tr><td>Voltage Sub-system</td><td>Typical Current Required (mA)</td><td>Combined Current Required (mA)</td></tr>
<tr><td>3.3 V Analog</td><td>239</td><td>239</td></tr>
<tr><td>1.8 V Analog</td><td>79</td><td rowspan="3">418</td></tr>
<tr><td>1.8 V Clock</td><td>27</td></tr>
<tr><td>1.8 V Digital</td><td>312</td></tr>
</table>

2 ADS540x Power Solutions

2.1 Linear Regulators

The ADS540x Evaluation Module (EVM) uses two TPS79601 LDOs to power the ADS540x. (A third LDO is used to power an LVDS buffer and therefore does not affect the performance of the ADC. It is not relevant to this report.)

2.2 Switch Mode Power Supplies

The TPS62231 and TPS62237 were tested as the SMPS solutions. These are very small solution size, high efficiency step-down converters which require just three passive components external to the IC. The output voltage is fixed on the IC, so two different part numbers are required for the 1.8-V and 3.3-V rails.

2.3 Performance Comparison (Test Results)

The LDO power solution and SMPS power solution were compared on the ADS5407 EVM. Input current consumption was measured, as well as the most commonly-used performance measurements of Signal to Noise Ratio (SNR) and Spurious-Free Dynamic Range (SFDR). The ferrite bead and capacitor configuration was kept the same for each test. The only variable was the power supply topology, an LDO or SMPS.

A 5-V input voltage was used for all tests. A 500-MHz clock was fed to the ADS5407 and measurements were taken at 230 MHz, 170 MHz, and 5 MHz signal frequencies. Auto-correction was enabled and bandpass filters were used on both the clock and signal inputs.

2.3.1 SNR

Figure 2 shows the differences in measured SNR between the LDO and SMPS power solutions. No significant difference is seen. Besides the power supply topology, there are other possible sources of performance differences such as the actual voltage applied to the ADS540x, as shown in Figure 25 and 26 of Reference 2.

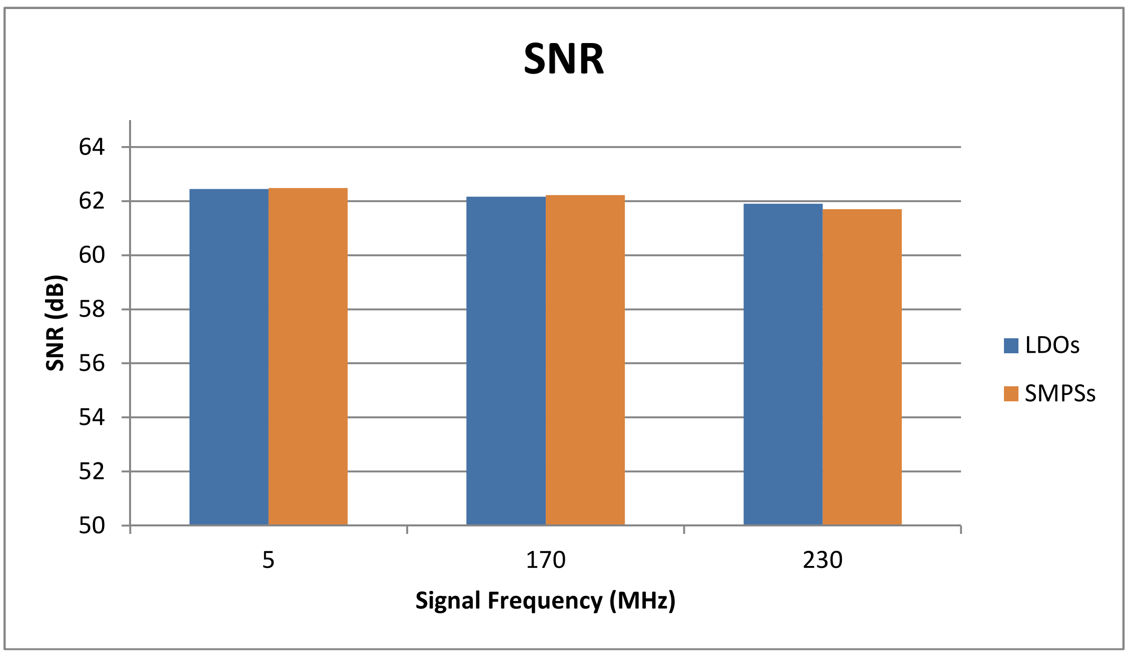

Figure 2. SNR comparison of the LDO power solution to the SMPS power solution

2.3.2 SFDR

Figure 3 shows the SFDR difference between the LDO and SMPS power solutions. No significant difference is seen. Besides the power supply topology, there are other possible sources of performance differences such as the actual voltage applied to the ADS540x, as shown in Figure 25 and 26 of Reference 2.

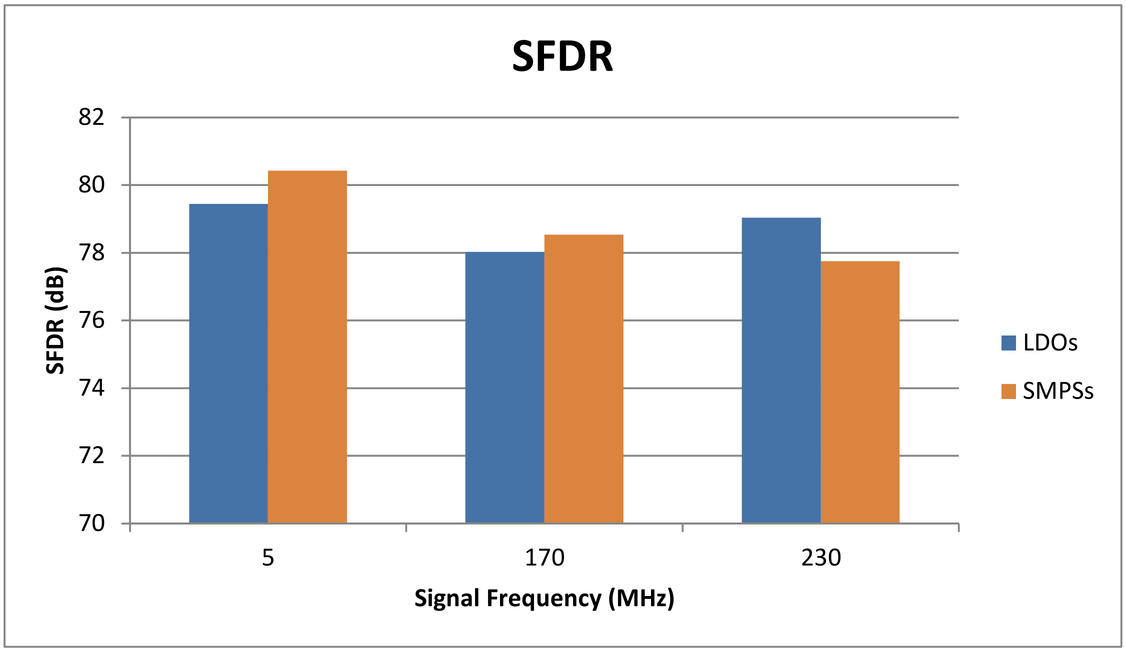

Figure 3. SFDR comparison of the LDO power solution to the SMPS power solution

2.3.3 Input Current Consumption

Figure 4 shows the input current consumption while Figure 5 shows the resulting efficiency difference between the LDO and SMPS power solutions. The LDO power solution reflects the total current draw of the ADS5407 (typically 657 mA), while the SMPS power solution reflects the advantage of the higher efficiency SMPS. The 5-V input voltage supply current is significantly lower than the current into the ADS5407, which gives an efficiency over 80% compared to the sub-50% of the LDO.

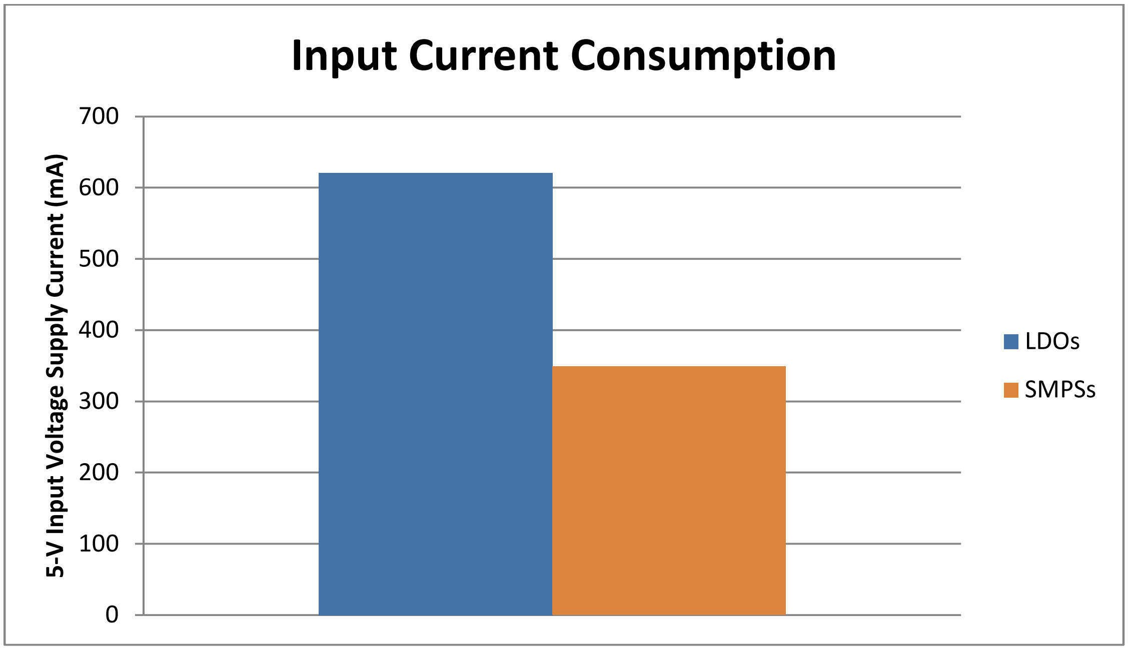

Figure 4. Input current consumption comparison of the LDO power solution to the SMPS power solution

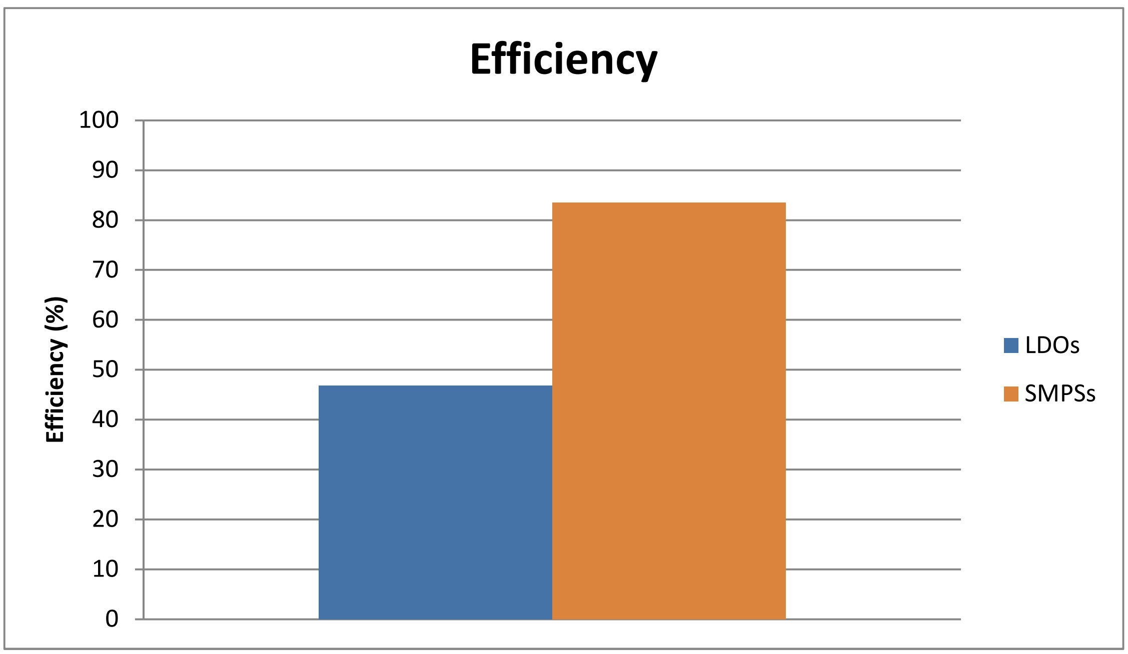

Figure 5. Efficiency comparison of the LDO power solution to the SMPS power solution

3 Conclusion

The TPS62231 and TPS62237 SMPSs power the ADS540x without any SNR or SFDR loss compared to an LDO power solution. Efficiency is nearly doubled to over 80% and the total solution size is decreased. PMP9767 shows a proven SMPS solution for powering a data converter with higher efficiency, a clean enough voltage, and reasonable cost.

References

1. *ADS540x EVM Design Package: SLAR069*
2. *ADS5407 data sheet: SLAS934*
3. *TPS62231 data sheet: SLVS941*
4. *TPS62237 data sheet: SLVS941*

Appendix A. Raw SNR and SFDR Test Results

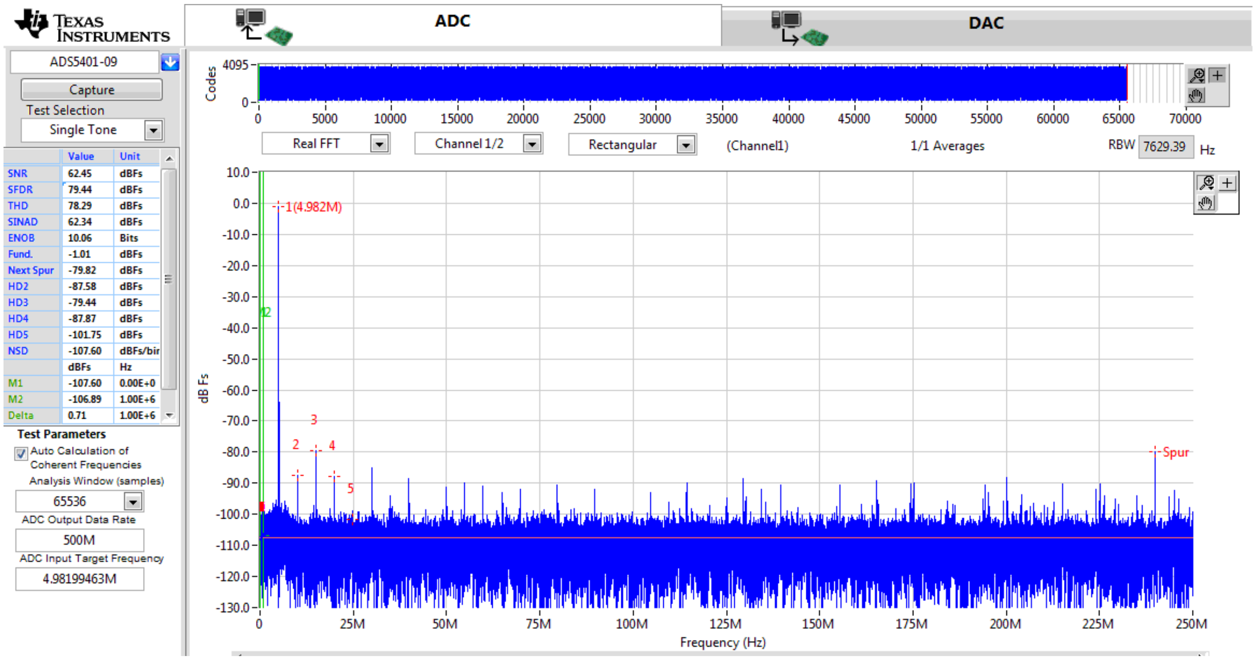

Figure A-1. ADS5407 powered with LDOs and 5-MHz signal frequency

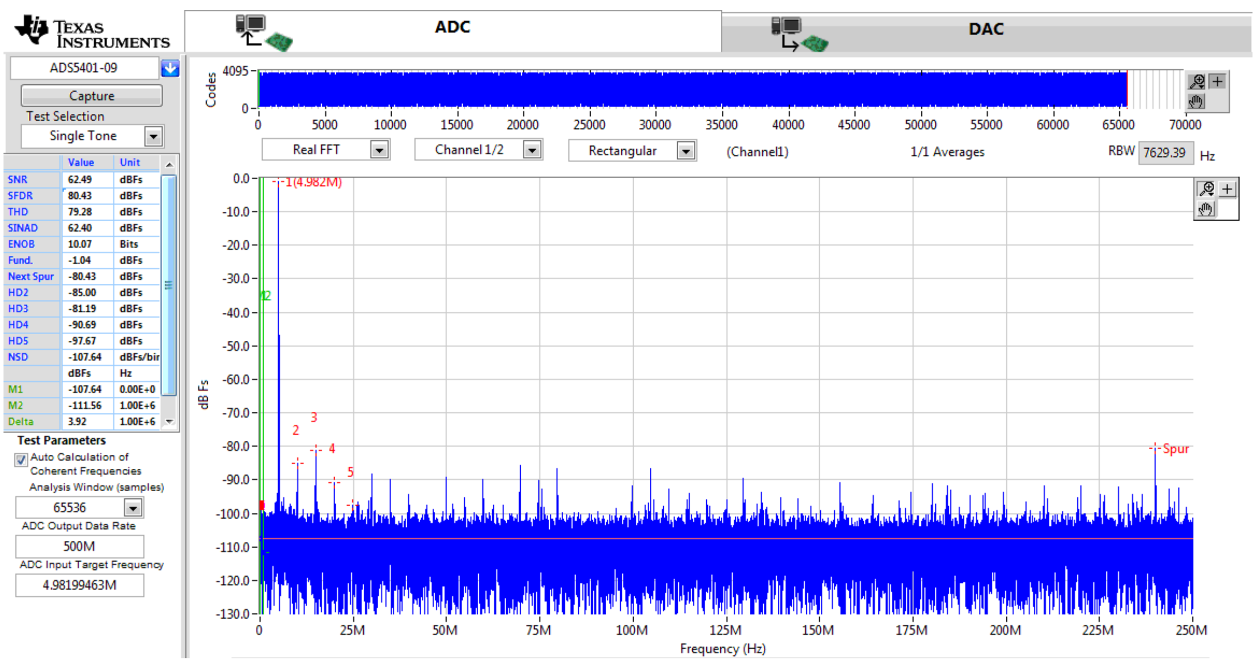

Figure A-2. ADS5407 powered with SMPSs and 5-MHz signal frequency

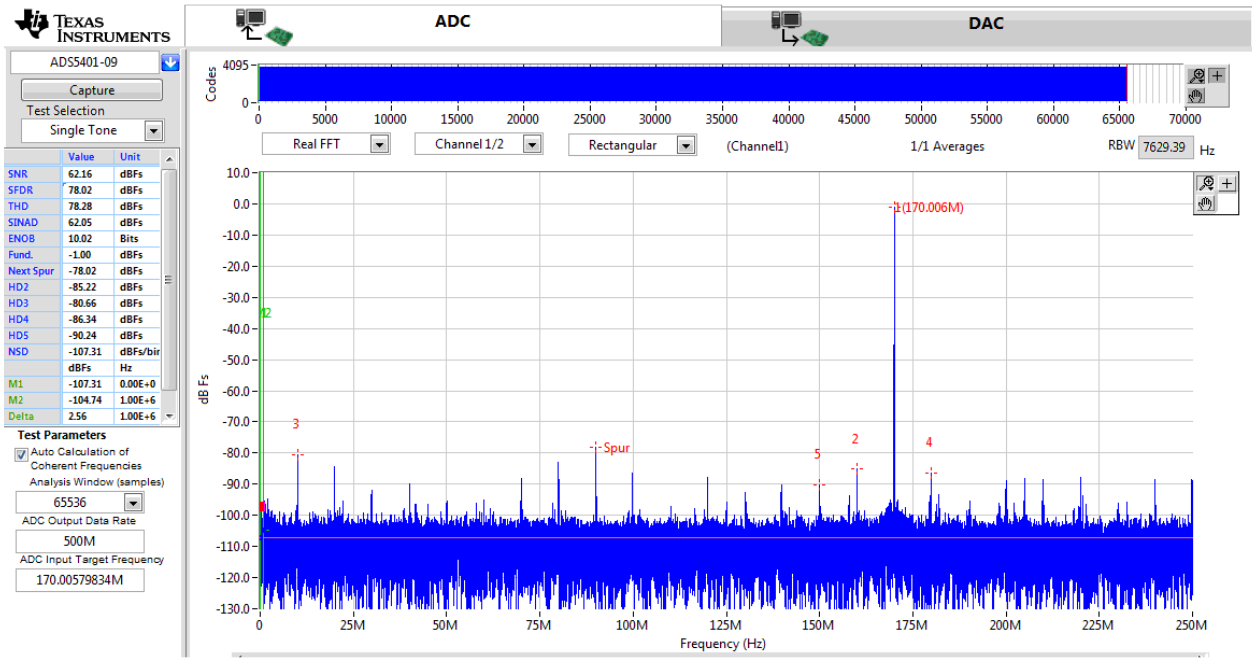

Figure A-3. ADS5407 powered with LDOs and 170-MHz signal frequency

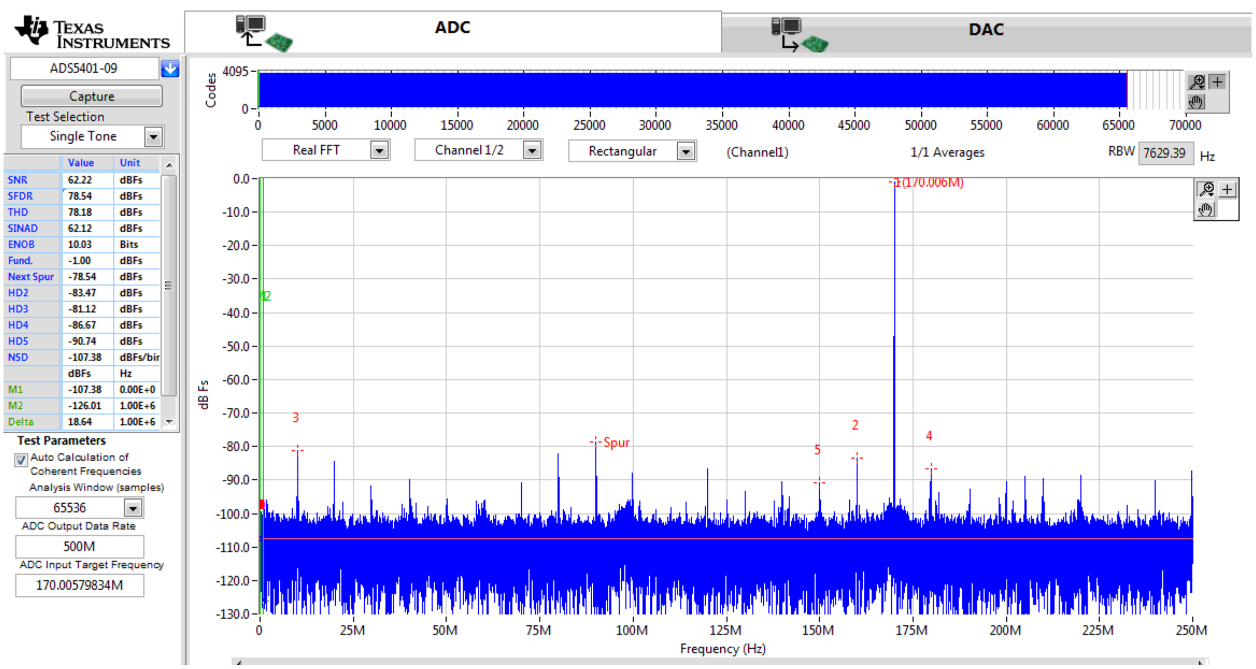

Figure A-4. ADS5407 powered with SMPSs and 170-MHz signal frequency

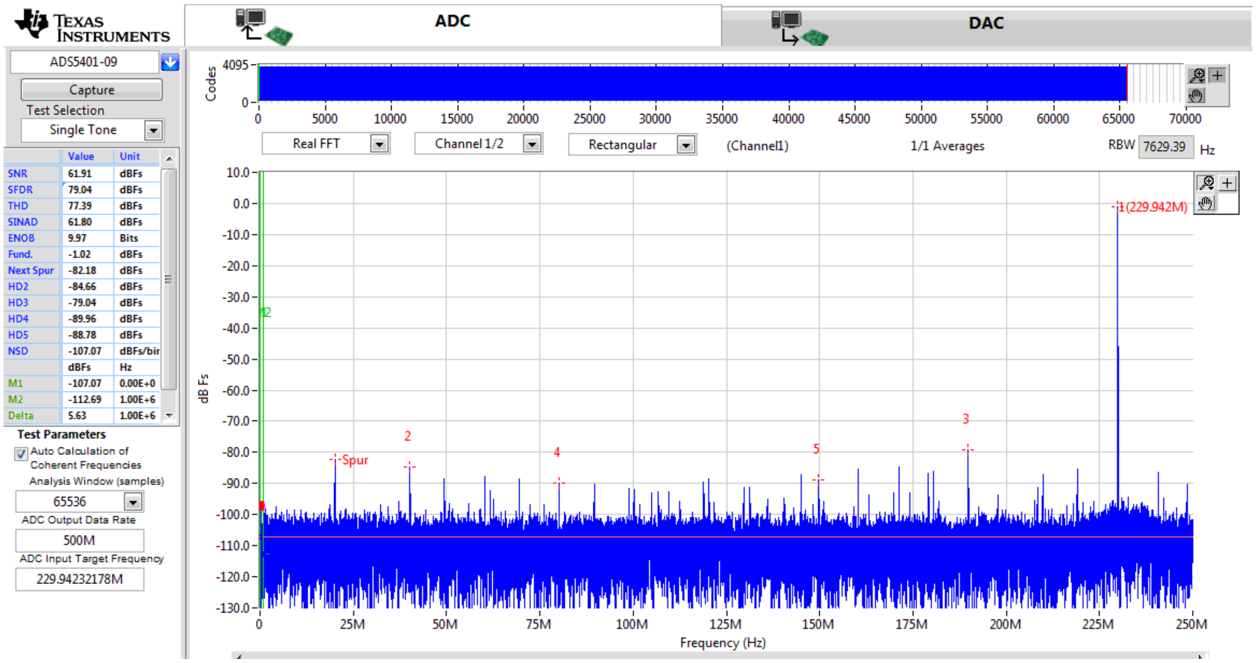

Figure A-5. ADS5407 powered with LDOs and 230-MHz signal frequency

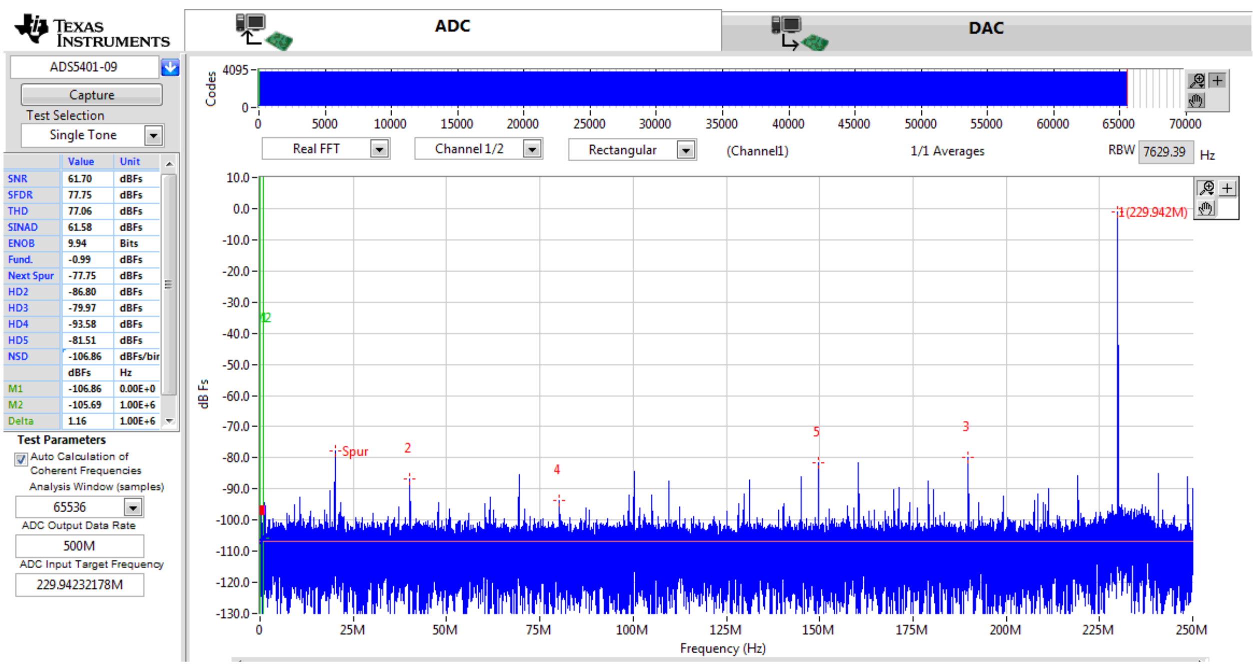

Figure A-6. ADS5407 powered with SMPSs and 230-MHz signal frequency