TI Designs

Total Harmonic Distortion Measurement For Energy Monitoring

TI Designs

This reference design implements power quality analysis in a three-phase energy measurement system. Power quality monitoring and analysis has an increasingly large role in improving the reliability of the electricity grid. The design measures total harmonic distortion (THD), monitors voltage sags and swells, and measures phase-to-phase angles to help determine phase sequence and prevent accidental phase swapping. Four-quadrant energy measurement is supported for net metering systems with bi-directional energy flow.

Design Resources

TIDM-THDREADING	Design Folder
MSP430F67791A	Product Folder
TPS54060	Product Folder
EVM4340-F6779	Tool Folder

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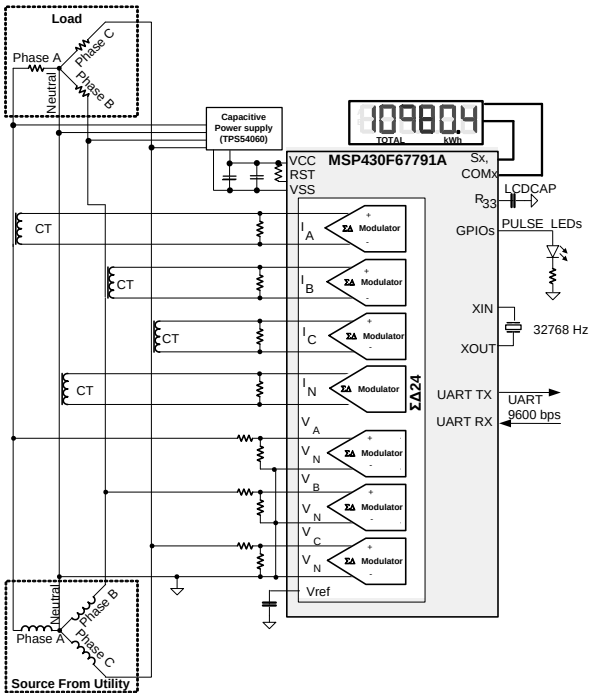
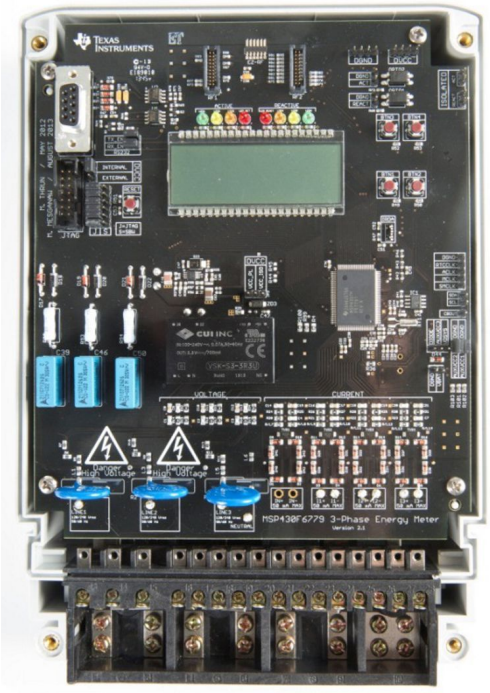
Design Features

- THD Calculated for Voltage and Current
- Voltage Sag and Swell Events Logged With Programmable Threshold Levels
- Phase-to-Phase Angle Measurement
- Four-Quadrant Energy Measurement With Class 0.2 Accuracy
- Complete Energy Library With Fundamental Voltage and Current, Fundamental Active and Reactive Power, Active and Reactive Energy, Root Mean Square (RMS) Current and Voltage, Power Factor, and Line Frequency

Featured Applications

- Metering
- Street Lighting





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1 System Description

The presence of harmonics can have a negative impact on both consumer loads and the electricity grid. This design implements a Class 0.2 three-phase energy measurement system that measures the total harmonic distortion, which can ensure that the current drawn by a customer's load does not significantly degrade the voltage delivered from the utility to other customers. For additional power quality information on the supply, voltage sags and swells are also logged. In addition, this design measures phase-to-phase angles, which can help in determining phase sequence and prevent accidentally swapping phases when installing an energy measurement system. This design supports four quadrant energy measurement for logging energy consumption and generation in systems that could both provide electricity to the utility company or consume the energy generated from the utility companies.

This design guide has a complete metrology source code provided as a downloadable zip file.

1.1 MSP430F67791A

For sensing and calculating the metrology parameters, the MSP430F67791A e-meter SoC is used. This device is the latest metering system on chip (SoC) that belongs to the MSP430F67xxA family of devices. In regards to metrology, the MSP430F67791A energy library software has support for calculation of various parameters for up to three-phase energy measurement. The key parameters calculated during energy measurements are: RMS current and voltage, fundamental current and voltage, current and voltage THD, phase-to-phase angles, active and reactive power and energies, power factor, and frequency.

1.2 TPS54060

The TPS54060 is used in the power supply to help provide a 3.3-V output from an input mains voltage of 120/230-V_{RMS} AC at 50 or 60 Hz. Figure 5 shows how the TPS54060 is used to create the 3.3-V output from the 120/230-V_{RMS} AC input.

2 Block Diagram

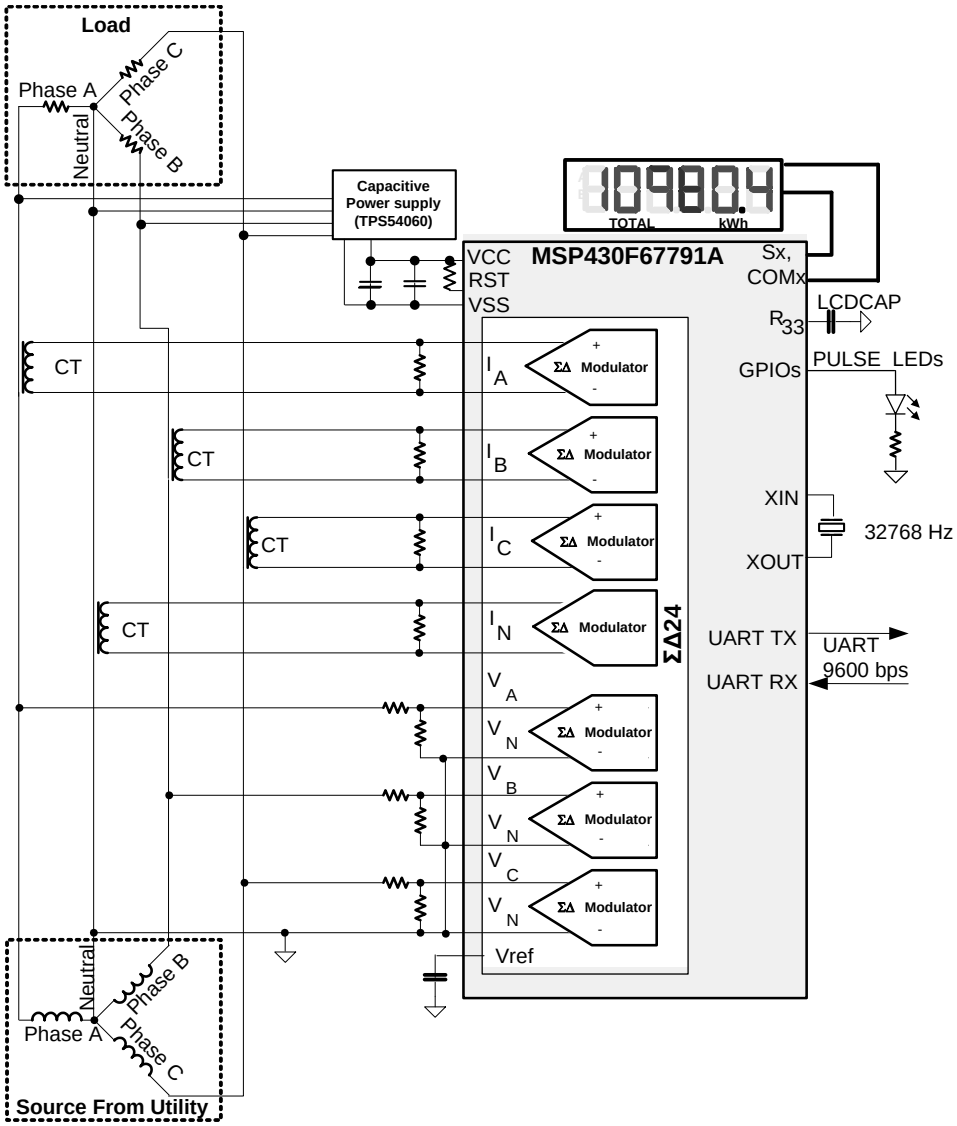


Figure 1. System Block Diagram

Figure 1 shows the high-level interface used for a three-phase energy measurement application that uses the MSP430F67791A. A three-phase four-wire star connection to the AC mains is shown in this case. Current sensors are connected to each of the current channels, and a simple voltage divider is used for corresponding voltages. The CT has an associated burden resistor that has to be connected at all times to protect the measuring device. The choice of the CT and the burden resistor is done based on the manufacturer and current range required for energy measurements. The CTs can be easily replaced by Rogowski coils with minimal changes to the front-end. The choice of voltage divider resistors for the voltage channel is selected to ensure the mains voltage is divided down to adhere to the normal input ranges that are valid for the MSP430ΣΔ24. Refer to the MSP4305xx/6xx user's guide (SLAU208) and device specific datasheet (SLAS983) for these numbers.

2.1 Highlighted Products

2.1.1 MSP430F67791A

The MSP430F67791A belongs to the powerful 16-bit MSP430F6xx platform. This device finds its application in energy measurement and has the necessary architecture to support it. The MSP430F67791A has a powerful 25-MHz CPU with MSP430CPUx architecture. The analog front-end (AFE) consists of seven independent 24-bit ΣΔ analog-to-digital converters (ADC) based on a second order sigma-delta architecture that supports differential inputs. The sigma-delta ADCs (ΣΔ24_B) operate independently and are capable of 24-bit results. They can be grouped together for simultaneous sampling of voltages and currents on the same trigger. In addition, it also has an integrated gain stage to support gains up to 128 for amplification of low-output current sensors. A 32×32-bit hardware multiplier on this chip can be used to further accelerate math intensive operations during energy computation.

For more info on the features of the MSP430F67791A, a block diagram of the chip is shown in Figure 2.

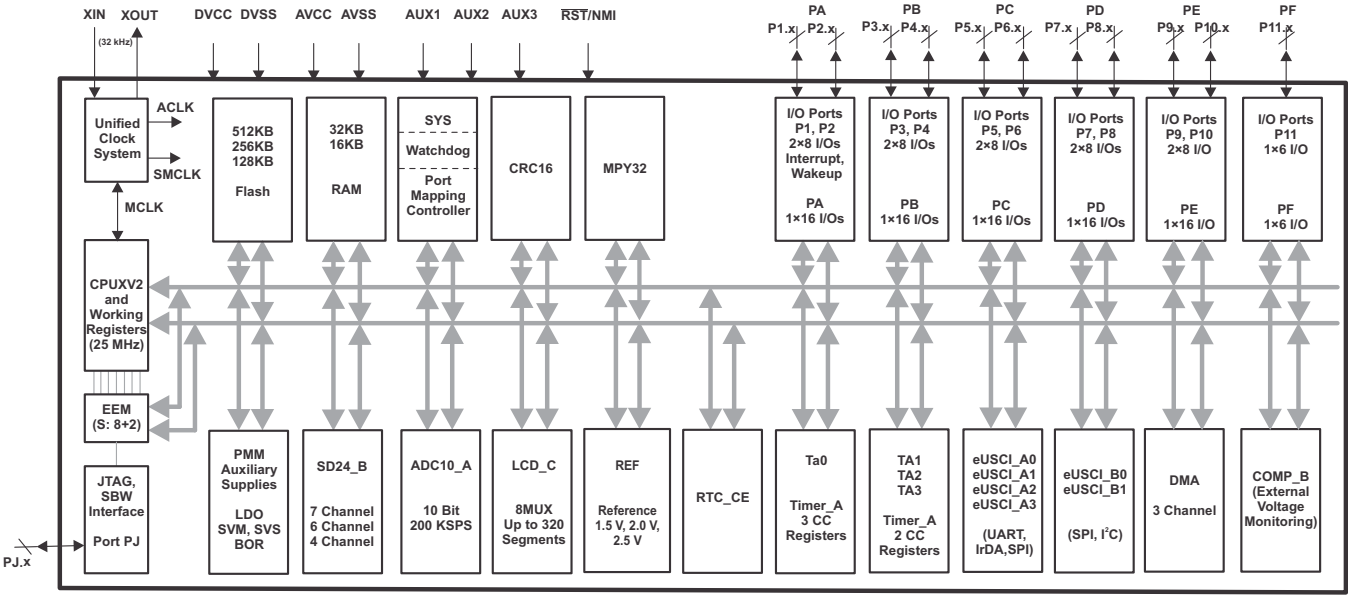


Figure 2. MSP430F67791A Block Diagram

2.1.2 TPS54060

The TPS54060A is a 60-V, 0.5-A, step-down regulator with an integrated high-side MOSFET. Current mode control provides simple external compensation and flexible component selection. A low-ripple pulse skip mode reduces the no load, regulated output supply current to 116 µA. Using the enable pin, shutdown supply current is reduced to 1.3 µA, when the enable pin is low.

Undervoltage lockout is internally set at 2.5 V, but can be increased using the enable pin. The output voltage startup ramp is controlled by the slow start pin that can also be configured for sequencing or tracking. An open-drain power good signal indicates the output is within 94% to 107% of its nominal voltage.

3 System Design Theory

3.1 Design Hardware Implementation

3.1.1 Analog Inputs

The MSP430 AFE, which consists of the ΣΔ ADC, is differential and requires that the input voltages at the pins do not exceed ±930 mV (gain = 1). To meet this specification, the current and voltage inputs need to be divided down. In addition, the ΣΔ24 allows a maximum negative voltage of –1 V. Therefore, AC signals from mains can be directly interfaced without the need for level shifters. This subsection describes the AFE used for voltage and current channels.

3.1.1.1 Voltage Inputs

The voltage from the mains is usually 230 V or 120 V and for optimal accuracy is usually scaled down within 930 mV. In the AFE for voltage, there consists a spike protection varistor, EMI filter beads (which should help for ESD testing), a voltage divider network, and a RC low-pass filter that acts like an anti-alias filter. Note that the anti-alias resistors on the positive and negative sides are different because the input impedance to the positive terminal is much higher; therefore, a lower value resistor is used for the anti-alias filter. If this is not maintained, a relatively large phase shift would result.

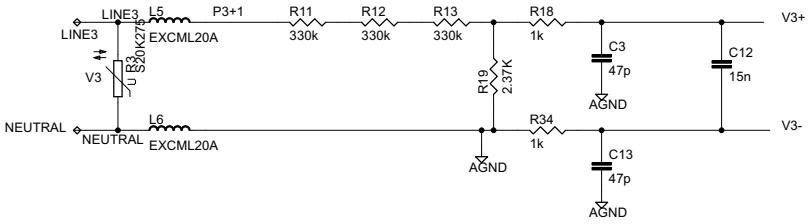


Figure 3. AFE for Voltage Inputs

Figure 3 shows the AFE for voltage inputs for a mains voltage of 230 V for the case that no harmonics present. The voltage is brought down to approximately 549 mV_{RMS}, which is 779 mV at its peak, and fed to the positive input. This voltage is within the MSP430ΣΔ analog limits by a safety margin greater than 15%. This safety margin ensures that spikes and harmonics can be accurately sensed up to a certain magnitude. To properly sense the RMS voltage when there is a lot of harmonic content, the front-end design should be designed with an even greater safety margin.

3.1.1.2 Current Inputs

The AFE for current inputs is slightly different from the AFE for the voltage inputs. Figure 4 shows the AFE used for a current channel. The AFE for current consists of diodes and transorbs for transient voltage suppression (TVS). In addition, the front-end consists of EMI filter beads (which should help for ESD testing), burden resistors for current transformers, and also a RC low-pass filter that acts like an anti-alias filter.

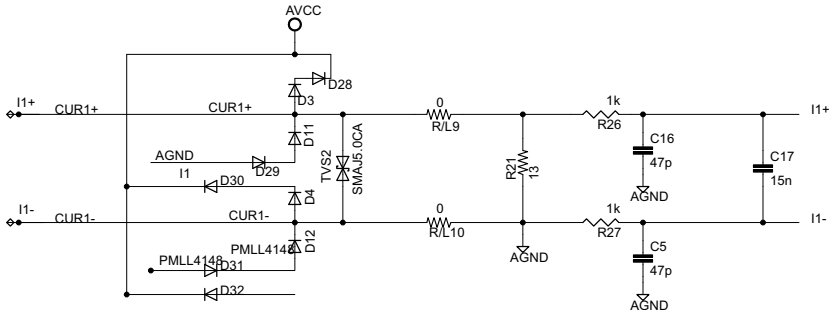


Figure 4. AFE for Current Inputs

In Figure 4, footprints for suppressant inductors are available. These inductor footprints are shown below as R/L1 and R/L2 and by default are populated with 0 Ω. In addition, in the figure, resistor R104 is the burden resistor that would be selected based on the current range used and the turns ratio specification of the CT (CTs with a turns ratio of 2000:1 are used for this design). The value of the burden resistor for this design is around 13 Ω. The antialiasing circuitry, consisting of resistors and capacitors, follow the burden resistor. Based on this EVM's maximum current of 100 A, CT turns ratio of 2000:1, and burden resistor of 13 Ω, the input signal to the converter is a fully differential input with a voltage swing of ±919 mV maximum when the maximum current rating of the energy measurement system (100 A) is applied if no harmonics are present. If a significant amount of harmonics will be expected in the system, to properly sense the harmonic content, either the maximum current rating should be derated or the burden resistor should be reduced.

3.1.2 Power Supply

The MSP430 family of microcontrollers support a number of low-power modes in addition to low-power consumption during active (measurement) mode when the CPU and other peripherals are active. Since an energy meter is always interfaced to the AC mains, the DC supply required for the measuring element (MSP430F67791A) can be easily derived using an AC to DC conversion mechanism. The reduced power requirements of this device family allow design of power supplies to be small, extremely simple and cost-effective. The power supply allows the operation of the energy measurement system by being powered directly from the mains. The next subsections discuss the various power supply options that are available to users to support their design.

3.1.2.1 Resistor Capacitor (RC) Power Supply

Figure 5 shows a capacitor power supply that provides a single output voltage of 3.3 V directly from the mains of 120/230-VRMS AC at 50 or 60 Hz.

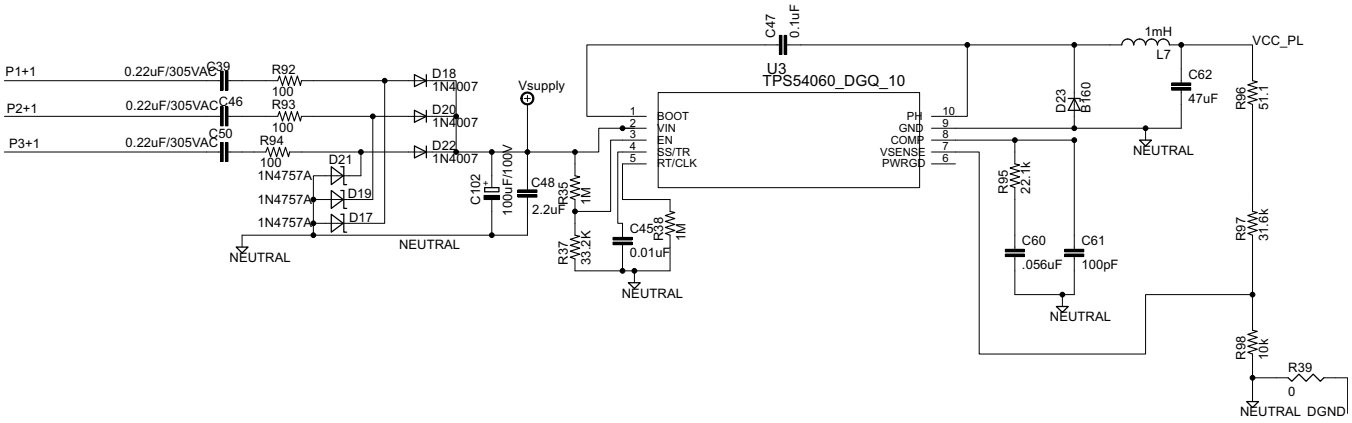


Figure 5. Simple Capacitive Power Supply for the MSP430 Energy Measurement System

Appropriate values of resistors (R92, R93, and R94) and capacitors (C39, C46, and C50) are chosen based on the required output current drive of the power supply. Voltage from mains is directly fed to an RC-based circuit followed by a rectification circuitry to provide a DC voltage for the operation of the MSP430. This DC voltage is regulated to 3.3 V for full-speed operation of the MSP430. The design equations for the power supply are given in SLVA491. The configuration shown in Figure 5 allows all three phases to contribute to the current drive, which is approximately three times the drive available from only one phase. If even higher output drive is required, the same circuitry can be used followed by an NPN output buffer. Another option would be to replace the above circuitry with a transformer or switching-based power supply.

3.1.2.2 Switching-Based Power Supply

Figure 6 shows a switching-based power supply that provides a single output voltage of 3.3 V directly from the AC mains 100 to 230 V_{RMS}. In the configuration shown in Figure 6, the energy measurement system is powered as long as there is AC voltage on Phase C, corresponding to pad "LINE 3" on the HW and P1/P3+1 on the schematic. The internal circuitry of a switching power supply is omitted from this design guide. For the drive of the power supply, see the documentation of the power supply module.

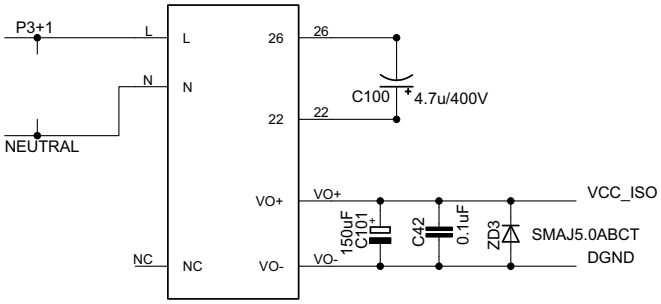


Figure 6. Switching-Based Power Supply for the MSP430 Energy Measurement System

3.2 Metrology Software Implementation

This section discusses the software for the implementation of three-phase metrology. The first subsection discusses the setup of various peripherals of the MSP430F67791A. Subsequently, this section describes the entire metrology software as two major processes: the foreground process and background process.

3.2.1 Peripherals Setup

The major peripherals of the MSP430F67791A are the 24-bit sigma delta (SD24_B) ADC, clock system, real-time clock (RTC), LCD, and watchdog timer (WDT).

3.2.1.1 SD24_B Setup

For a three-phase system, at least six ΣΔs are necessary to independently measure three voltages and currents. The code accompanying this design guide addresses the metrology for a three-phase system with limited discussion to anti-tampering; however, the code supports the measurement of the neutral current.

The clock to the SD24 (f_M) ADCs and trigger generator derives from the digitally controlled oscillator (DCO) running at 25 MHz. The sampling frequency is defined as $f_S = f_M / OSR$, the oversampling ratio (OSR) is chosen to be 256, and the modulation frequency, f_M, is chosen as 1.048576 MHz, resulting in a sampling frequency of 4096 samples per second. The SD24s are configured to generate regular interrupts every sampling instant.

The following are the ΣΔ channels associations:

- A0.0+ and A0.0– → Voltage V1
- A1.0+ and A1.0– → Voltage V2
- A2.0+ and A2.0– → Voltage V3
- A4.0+ and A4.0– → Current I1
- A5.0+ and A5.0– → Current I2
- A6.0+ and A6.0– → Current I3

Optional neutral channel can be processed through channel A3.0+ and A3.0–.

3.2.1.2 Real Time Clock (RTC_C)

The RTC_C is an RTC module that is configured to give precise one-second interrupts.

3.2.1.3 LCD Controller (LCD_C)

The LCD controller on the MSP430F67791A can support up to 8-mux displays and 320 segments. The LCD controller is also equipped with an internal charge pump that can be used for good contrast. In the current design, the LCD controller is configured to work in 4-mux mode using 160 segments with a refresh rate set to ACLK/64, which is 512 Hz.

3.2.2 Foreground Process

The initialization routines involve the setup of the SD24_B module, clock system, general purpose input/output (GPIO port) pins, RTC module for clock functionality, LCD and the USCI_A0 for UART functionality.

After the hardware is setup, any received frames from the GUI are processed. Subsequently, the foreground process checks whether the background process has notified it to calculate new metering parameters. This notification is done through the assertion of the "PHASE_STATUS_NEW_LOG" status flag whenever a frame of data is available for processing. The data frame consists of the processed dot products that were accumulated for one second in the background process. This is equivalent to accumulation of 50 or 60 cycles of data synchronized to the incoming voltage signal. In addition, a sample counter keeps track of how many samples have been accumulated over this frame period. This count can vary as the software synchronizes with the incoming mains frequency.

The processed dot products include the V_{RMS}, I_{RMS}, active power, reactive power, fundamental voltage, fundamental active power, and fundamental reactive power. These dot products are used by the foreground process to calculate the corresponding metrology readings in real-world units. Processed voltage and fundamental voltage dot products are accumulated in 48-bit registers. In contrast, processed current dot products, active energy dot products, fundamental active energy dot products, reactive energy dot products, and fundamental reactive energy dot products are accumulated in separate 64-bit registers to further process and obtain the RMS and mean values. Using the foreground's calculated values of active and reactive power, the apparent power is calculated. Similarly, using the foreground's calculated values for the fundamental voltage, fundamental reactive power, and fundamental active power, the fundamental current, voltage THD, and current THD are calculated. The frequency (in Hertz) and power factor are also calculated using parameters calculated by the background process using the formulas in Section 3.2.2.1.

The foreground process also takes care of updating the LCD. The LCD display item is changed every two seconds. For more information, about the different items displayed on the LCD, see Section 7.1.

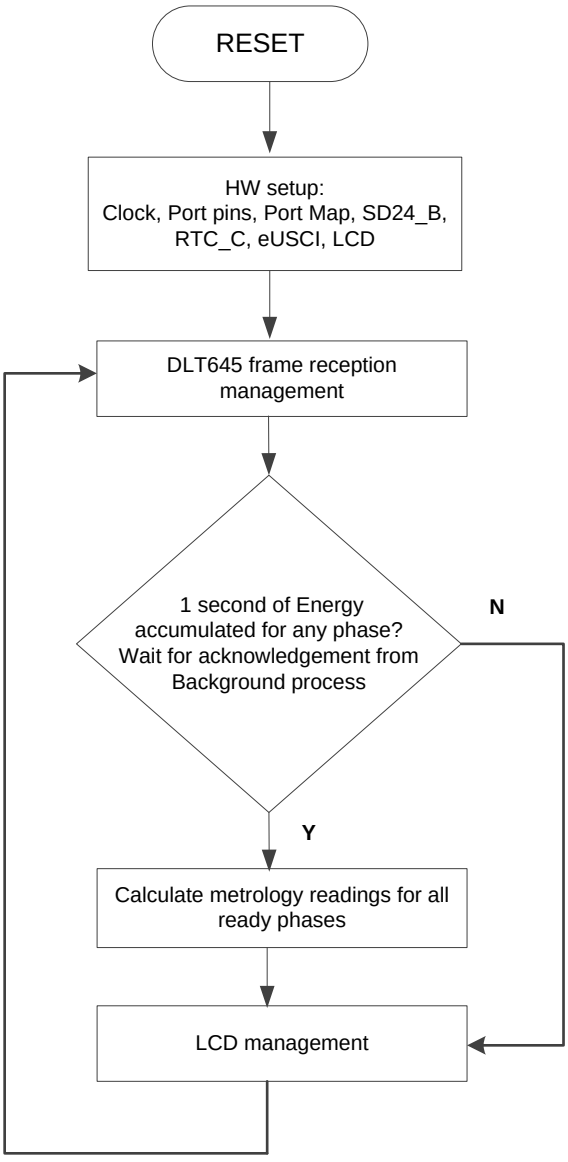


Figure 7. Foreground Process

3.2.2.1 Formulae

3.2.2.1.1 Standard Metrology Parameters

This section briefly describes the formulas used for the voltage, current, and energy.

As previous sections describe, voltage and current samples are obtained at a sampling rate of 4096 Hz. All of the samples that are taken in one second are kept and used to obtain the RMS values for voltage and current for each phase. The RMS values are obtained by the following formulas:

$$V_{RMS,ph} = K_{v,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} v_{ph}(n) \times v_{ph}(n)}{\text{Sample count}}} - v_{offset,ph} \quad (1)$$

$$I_{RMS,ph} = K_{i,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} i_{ph}(n) \times i_{ph}(n)}{\text{Sample count}}} - i_{offset,ph} \quad (2)$$

where

- ph = Phase parameters that are being calculated [that is, Phase A(= 1), B(= 2), or C(= 3)]
- $v_{ph}(n)$ = ADC sample from the ph phases's voltage channel, taken at sample instant n
- $v_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the voltage converter
- $i_{ph}(n)$ = ADC sample from the ph phases's current channel, taken at sample instant n
- $i_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the current converter
- Sample count = Number of samples in one second
- $K_{v,ph}$ = Scaling factor for voltage
- $K_{i,ph}$ = Scaling factor for current

Power and energy are calculated for a frames worth of active and reactive energy samples. These samples are phase corrected and passed on to the foreground process, which uses the number of samples (sample count) to calculate phase active and reactive powers through the following formulas:

$$P_{ACT,ph} = K_{ACT,ph} \frac{\sum_{n=1}^{\text{Sample count}} v(n) \times i_{ph}(n)}{\text{Sample count}} \quad (3)$$

$$P_{REACT,ph} = K_{REACT,ph} \frac{\sum_{n=1}^{\text{Sample count}} v_{90}(n) \times i_{ph}(n)}{\text{Sample count}} \quad (4)$$

$$P_{APP,ph} = \sqrt{P_{ACT,ph}^2 + P_{REACT,ph}^2} \quad (5)$$

where

- $v_{90,ph}$ (n) = Voltage sample of the waveform that results from shifting $v_{ph}(n)$ by 90°, taken at a sample instant n
- $K_{ACT,ph}$ = Scaling factor for active power
- $K_{REACT,ph}$ = Scaling factor for reactive power

Note that for reactive energy, the 90° phase shift approach is used for two reasons:

1. This approach allows accurate measurement of the reactive power for very small currents.
2. This approach conforms to the measurement method specified by IEC and ANSI standards.

The calculated mains frequency calculates the 90° shifted voltage sample. Because the frequency of the mains varies, it is important to first measure the mains frequency accurately to phase shift the voltage samples accordingly (see Section 3.2.3.1.4 for details).

To get an exact 90° phase shift, interpolation is used between two samples. For these two samples, the design uses a voltage sample slightly more than 90° before the current sample and a voltage sample slightly less than 90° before the current sample. The design's phase shift implementation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap FIR filter. In the software, a lookup table provides the filter coefficients that are used to create the fractional delays.

In addition to calculating the per-phase active and reactive powers, the cumulative sum of these parameters are also calculated by the following equations:

$$P_{ACT,\,Cumulative} = \sum_{ph=1}^{3} P_{ACT,ph} \tag{6}$$

$$P_{REACT,\,Cumulative} = \sum_{ph=1}^{3} P_{REACT,ph} \tag{7}$$

$$P_{APP,\,Cumulative} = \sum_{ph=1}^{3} P_{APP,ph} \tag{8}$$

Using the calculated powers, energies are calculated by the following formulas:

$$E_{ACT,\,ph} = P_{ACT,\,ph} \times \text{Sample count} \tag{9}$$

$$E_{REACT,\,ph} = P_{REACT,\,ph} \times \text{Sample count} \tag{10}$$

$$E_{APP\,ph} = P_{APP\,ph} \times \text{Sample count} \tag{11}$$

From there, the energies are also accumulated to calculate the cumulative energies, by the following equations:

$$E_{ACT,\,Cumulative} = \sum_{ph=1}^{3} E_{ACT,ph} \tag{12}$$

$$E_{REACT,\,Cumulative} = \sum_{ph=1}^{3} E_{REACT,ph} \tag{13}$$

$$E_{APP,\,Cumulative} = \sum_{ph=1}^{3} E_{APP,ph} \tag{14}$$

The calculated energies are then accumulated into buffers that store the total amount of energy consumed since the system reset. Note that these energies are different from the working variables used to accumulate energy for outputting energy pulses. There are four sets of buffers that are available: one for each phase and one for the cumulative of the phases. Within each set of buffers, the following energies are accumulated:

1. Active import energy (active energy when active energy ≥ 0)
2. Active export energy (active energy when active energy < 0)
3. React. Quad I energy (reactive energy when reactive energy ≥ 0 and active power ≥ 0; inductive load)
4. React. Quad II energy (reactive energy when reactive energy ≥ 0 and active power < 0; capacitive generator)
5. React. Quad III energy (reactive energy when reactive energy < 0 and active power < 0; inductive generator)
6. React. Quad IV energy (reactive energy when reactive energy < 0 and active power ≥ 0; capacitive load)
7. App. import energy (apparent energy when active energy ≥ 0)
8. App. export energy (apparent energy when active energy < 0)

The background process also calculates the frequency in terms of samples per mains cycle. The foreground process then converts this samples per mains cycle to Hertz by Equation 15:

$$\text{Frequency (Hz)} = \frac{\text{Sampling Rate (samples / second)}}{\text{Frequency (samples / cycle)}} \tag{15}$$

After the active power and apparent power have been calculated, the absolute value of the power factor is calculated. In the system's internal representation of power factor, a positive power factor corresponds to a capacitive load; a negative power factor corresponds to an inductive load. The sign of the internal representation of power factor is determined by whether the current leads or lags voltage, which is determined in the background process. Therefore, the internal representation of power factor is calculated by Equation 16:

$$\text{Internal representation of power factor} = \begin{cases} \dfrac{P_{ACT}}{P_{APPARENT}}, \text{ if capacitive load} \\ -\dfrac{P_{ACT}}{P_{APPARENT}}, \text{ if inductive load} \end{cases} \tag{16}$$

3.2.2.1.2 Power Quality Formulas

For calculating the fundamental RMS voltage, a pure sine wave is generated and tightly locked to the fundamental of the incoming voltage waveform. Using the generated waveform, the fundamental voltage, fundamental active power, and fundamental reactive power are calculated by the following equations:

$$V_{fund,ph} = K_{v\_fund,ph} \frac{\sum_{n=1}^{\text{Sample count}} v_{pure,ph}(n) \times v_{ph}(n)}{\text{Sample count}} \tag{17}$$

$$P_{ACT\_fund,ph} = K_{ACT\_fund,ph} \frac{\sum_{n=1}^{\text{Sample count}} v_{pure,ph}(n) \times i_{ph}(n)}{\text{Sample count}} \tag{18}$$

$$P_{REACT\_fund,ph} = K_{REACT\_fund,ph} \frac{\sum_{n=1}^{\text{Sample count}} v_{90\_pure,ph}(n) \times i_{ph}(n)}{\text{Sample count}} \tag{19}$$

where

- $V_{pure,ph}(n)$ = Voltage sample of the pure sine wave generated, taken at a sample instant n
- $V_{90\_pure,ph}(n)$ = Voltage sample of the waveform that results from shifting $V_{pure,ph}(n)$ by 90° , taken at a sample instant n
- $K_{v\_fund,ph}$ = Scaling factor for fundamental voltage
- $K_{ACT\_fund,ph}$ = Scaling factor for fundamental active power
- $K_{REACT\_fund,ph}$ = Scaling factor for fundamental active power

After calculating the fundamental voltage, fundamental active power, and fundamental reactive power, the fundamental current is calculated by the following formula:

$$I_{fund,ph} = K_{i\_fund,ph} \times \frac{\sqrt{P_{ACT\_fund,ph}^{\,2} + P_{REACT\_fund,ph}^{\,2}}}{V_{fund,ph}} \tag{20}$$

Where $K_{i\_fund,ph}$ = Scaling factor for fundamental current.

Once the fundamental current and fundamental voltage are calculated, the voltage THD and current THD can also be calculated. This software supports three different methods of calculating THD that are referred to in the following equations as THD_{IEC_F}, THD_{IEC_R}, and THD_{IEEE}. The formulas used to calculate voltage THD(V_THD) and current THD(I_THD) with the different methods is shown as follows:

$$V\_THD_{IEC\_F,ph} = \frac{\sqrt{V_{RMS,ph}^2 - V_{fund,ph}^2}}{V_{fund,ph}} \qquad I\_THD_{IEC\_F,ph} = \frac{\sqrt{I_{RMS,ph}^2 - I_{fund,ph}^2}}{I_{fund,ph}} \tag{21}$$

$$V\_THD_{IEC\_R,ph} = \frac{\sqrt{V_{RMS,ph}^2 - V_{fund,ph}^2}}{V_{RMS,ph}} \qquad I\_THD_{IEC\_R,ph} = \frac{\sqrt{I_{RMS,ph}^2 - I_{fund,ph}^2}}{I_{RMS,ph}} \tag{22}$$

$$V\_THD_{IEEE,ph} = \frac{V_{RMS,ph}^2 - V_{fund,ph}^2}{V_{fund,ph}^2} \qquad I\_THD_{IEEE,ph} = \frac{I_{RMS,ph}^2 - I_{fund,ph}^2}{I_{fund,ph}^2} \tag{23}$$

The method for calculating THD can be selected by defining the proper macro in the meterology-template.h file. To use the THD_{IEC_R} method, define the IEC_THD_R_SUPPORT macro in metrology-template.h file undefine the IEC_THD_F_SUPPORT macro. For using the THD_{IEC_F} method, define the IEC_THD_F_SUPPORT macro in metrology-template.h and undefine the IEC_THD_R_SUPPORT macro. To enable the THD_{IEEE} method, undefine both the IEC_THD_F_SUPPORT and IEC_THD_R_SUPPORT macros. To calculate THD correctly, select the proper method of THD calculation and ensure that any reference meter used for measuring THD uses the same THD method as the method selected in software.

3.2.3 Background Process

The background function deals mainly with timing critical events in software. It uses the ΣΔ interrupt as a trigger to collect voltage and current samples. The ΣΔ interrupt is generated when a new voltage or current sample is ready. All voltage channels are delayed so that the voltage samples for all channels are ready at the same time. Once the voltage samples are ready and collected, sample processing is done on the voltage samples and the previous current samples. This sample processing is done by the "per_sample_dsp()" function. After sample processing, the background process uses the "per_sample_energy_pulse_processing()" for the calculation and output of energy-proportional pulses. Figure 8 shows the flowchart for this process.

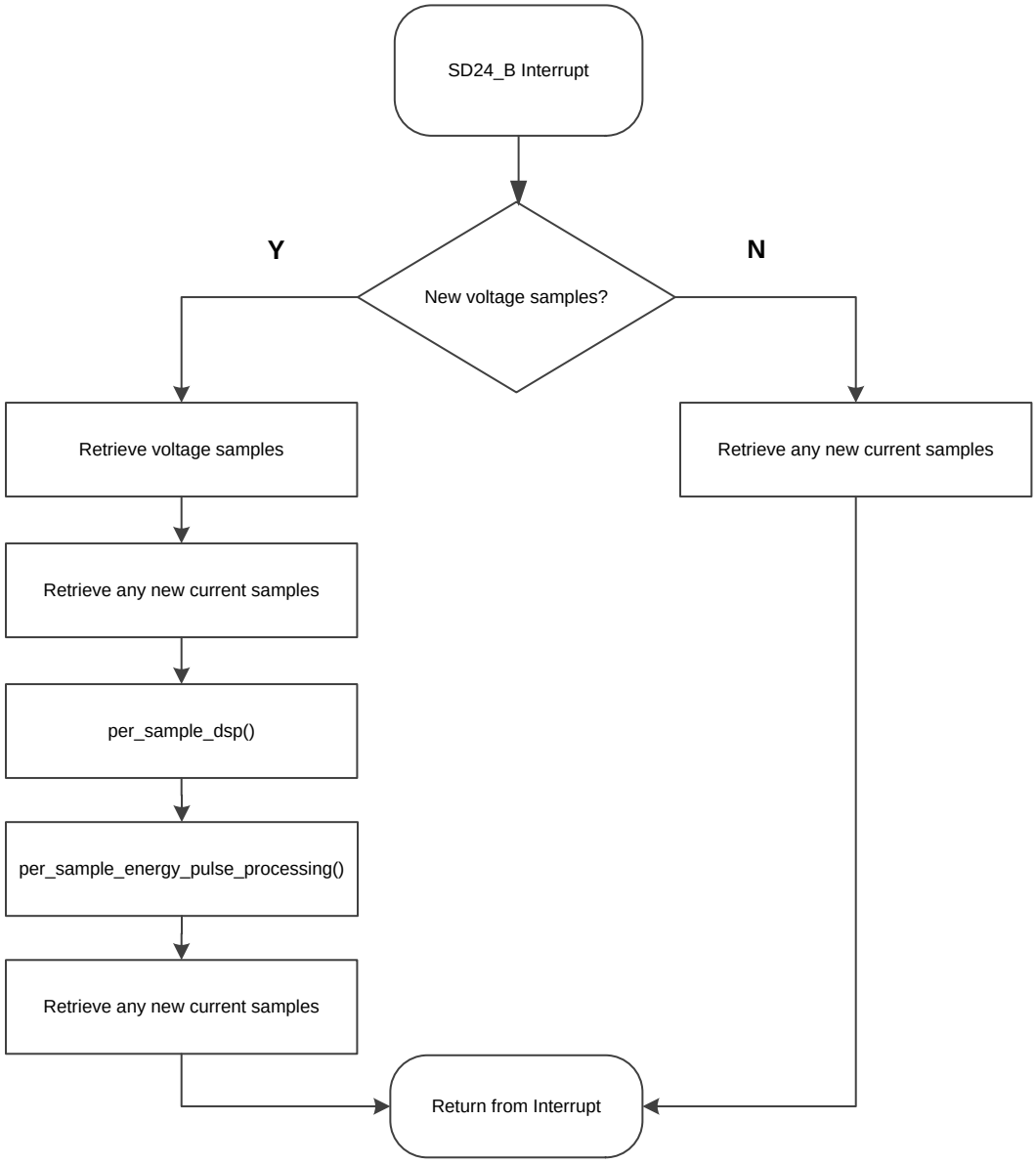


Figure 8. Background Process

3.2.3.1 per_sample_dsp()

Figure 9 shows the flowchart for the per_sample_dsp() function. The per_sample_dsp() function calculates intermediate dot product results that are fed into the foreground process for the calculation of metrology readings. Since 16-bit voltage samples are used, the voltage samples and fundamental voltage samples are further processed and accumulated in dedicated 48-bit registers. In contrast, since 24-bit current samples are used, the current samples are processed and accumulated in dedicated 64-bit registers. Per-phase active power, fundamental active power, fundamental reactive power, and reactive power are also accumulated in 64-bit registers.

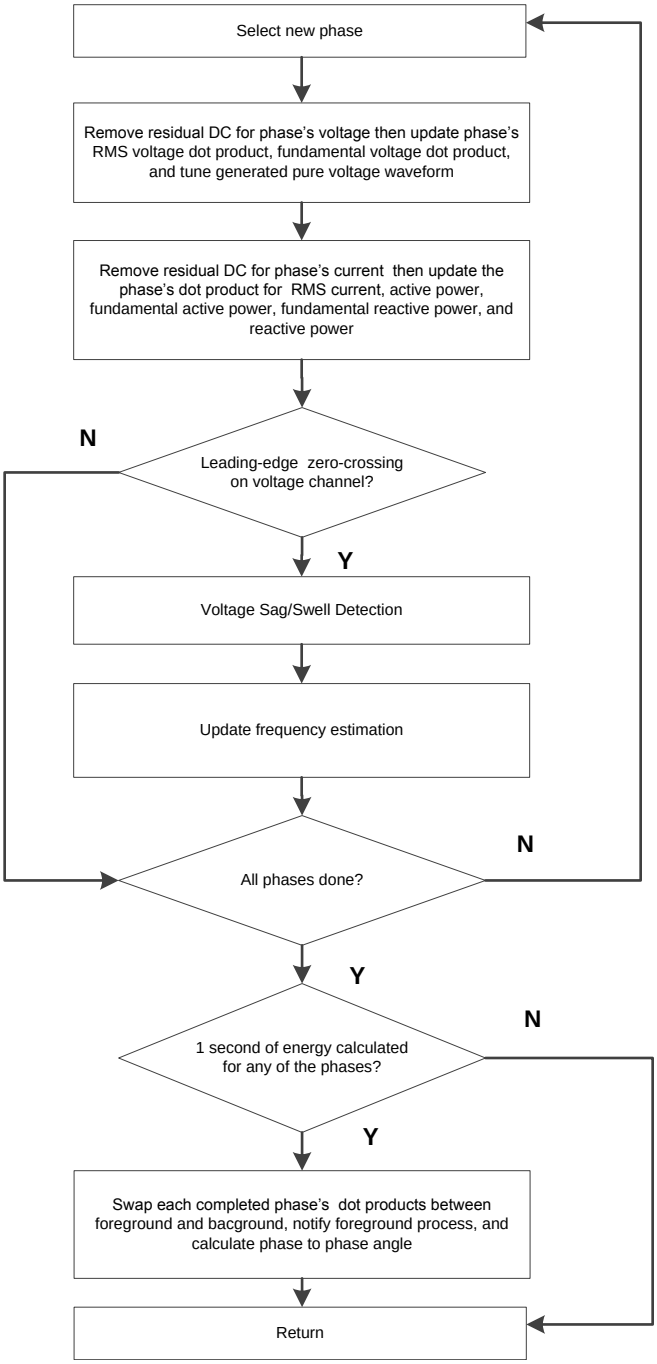


Figure 9. per_sample_dsp()

After sufficient samples (approximately one second's worth) have been accumulated, the background process triggers the foreground function to calculate the final values of RMS voltage; RMS current; active, reactive, and apparent powers; active, reactive, and apparent energy; frequency; power factor; fundamental voltage, fundamental current, fundamental active power, and fundamental reactive power; and voltage and current THD. In the software, there are two sets of dot products: at any given time, one is used by the foreground for calculation and the other used as the working set by the background. After the background process has sufficient samples, it swaps the two dot products so that the foreground uses the newly acquired dot products that the background process just calculated and the background process uses a new empty set to calculate the next set of dot products. In addition, after swapping the dot products for a particular phase, the angle between the previous phase voltage to that particular phase voltage is calculated.

Whenever there is a leading-edge zero-crossing (− to + voltage transition) on a voltage channel, the per_sample_dsp() function is also responsible for updating the corresponding phase's frequency (in samples per cycle) and voltage sag and swell conditions. For the sag and swell conditions, the RMS voltage is monitored over a rolling window of a certain number of mains cycles (this user-defined number of mains cycles is defined by the SAG_SWELL_WINDOW_LEN macro in the metrology-template.h file). Whenever the RMS voltage that is calculated over the duration of the current sag or swell window is less than the system's nominal voltage (as defined by the MAINS_NOMINAL_VOLTAGE macro in metrology-template) by a percentage larger than the swell threshold macro (defined as SAG_THRESHOLD in metrology-template), a sag event is defined as occurring. The number of mains cycles where this condition persists is logged as the sag duration and the number of sag condition occurrences is logged as the sag events count. Note that the sag duration corresponds to the total number of cycles in a sag condition since being reset and is therefore not cleared for every sag event. Similarly, if the measured RMS voltage is greater than the nominal voltage by a percentage larger than the swell threshold (defined as SWELL_THRESHOLD in metrology-template.h), a swell event is defined as occurring and the number of mains cycles where this condition persists is logged as the swell duration.

The following sections describe the various elements of electricity measurement.

3.2.3.1.1 Voltage and Current ADC Samples

The output of each SD24_B digital filter is a signed integer and any stray DC or offset value on these converters are removed using a DC tracking filter. A separate DC estimate for all voltages and currents is obtained using the filter, voltage, and current samples, respectively. This estimate is then subtracted from each voltage and current sample.

The resulting instantaneous voltage and current samples are used to generate the following intermediate results:

- Accumulated squared values of voltages and currents, which is used for V_{RMS} and I_{RMS} calculations, respectively
- Accumulated energy samples to calculate active energy
- Accumulated energy samples using current and 90° phase-shifted voltage to calculate reactive energy

The foreground process processes these accumulated values.

3.2.3.1.2 Pure Waveform Samples

To calculate the fundamental and THD readings, the software generates a pure sinusoid waveform for each phase and locks it to the fundamental of the incoming voltage waveform for that particular phase. Because the generated waveform is locked to the fundamental of the incoming voltage, the correlation of this pure waveform with the waveform from the voltage ADC can be used to find the amplitude of the fundamental component of the waveform sensed by the voltage ADC. Similarly, the correlation of the current and the pure voltage waveform can calculate the fundamental active power. For fundamental reactive power, the correlation of the 90° shifted pure waveform and the current can be used for calculating this parameter.

To generate a sine wave, information on the amplitude, phase, and frequency of the desired waveform is necessary. For the generated pure waveform, the amplitude is set to full scale to maximize the value of the fundamental dot products, the frequency is set to the measured frequency (in units of cycles per sample) that is used to calculate the mains frequency in final real-world units of Hertz, and the phase of the generated waveform is iteratively adjusted so that it is locked to the phase of the fundamental voltage. After the frequency is correctly calculated and the generated waveform's phase is locked to the fundamental voltage's phase, the fundamental readings can then be correctly calculated.

3.2.3.1.3 Phase-to-Phase Angle Readings

The samples of the generated pure sine waves are obtained by indexing into a lookup table of sine wave samples. In the software, there is one lookup table, but each phase has a different index into that same lookup table. Based on the value of the lookup table indexes of the different phases, the angle between the different fundamental voltage waveforms can be calculated. In the firmware, the phase-to-phase angle between a phase's voltage waveform and the previous phase's voltage waveform is calculated (that is, ϕ13, ϕ21, and ϕ32) . This phase to phase angle variable is internally represented in the firmware as a signed integer and is in units of $180°/2^{15}$.

Based on the expected value of the phase-to-phase angle readings, it can be determined whether an incorrect phase sequence is being registered by a meter by comparing the expected values of the phase-to-phase readings to the actual measured value. As an example, if ϕ13, ϕ21, and ϕ33 are all expected to be 240° but are reading 120°, this may indicate that two of the voltage connections have been accidentally swapped.

3.2.3.1.4 Frequency Measurement and Cycle Tracking

The instantaneous voltages are accumulated in a 48-bit register. In contrast, the instantaneous currents, active powers, reactive powers are accumulated in 64-bit registers. A cycle tracking counter and sample counter keep track of the number of samples accumulated. When approximately one second's worth of samples have been accumulated, the background process stores these accumulation registers and notifies the foreground process to produce the average results, such as RMS and power values. Cycle boundaries trigger the foreground averaging process because this process produces very stable results.

For frequency measurements, a straight line interpolation is used between the zero crossing voltage samples. Figure 10 shows the samples near a zero cross and the process of linear interpolation.

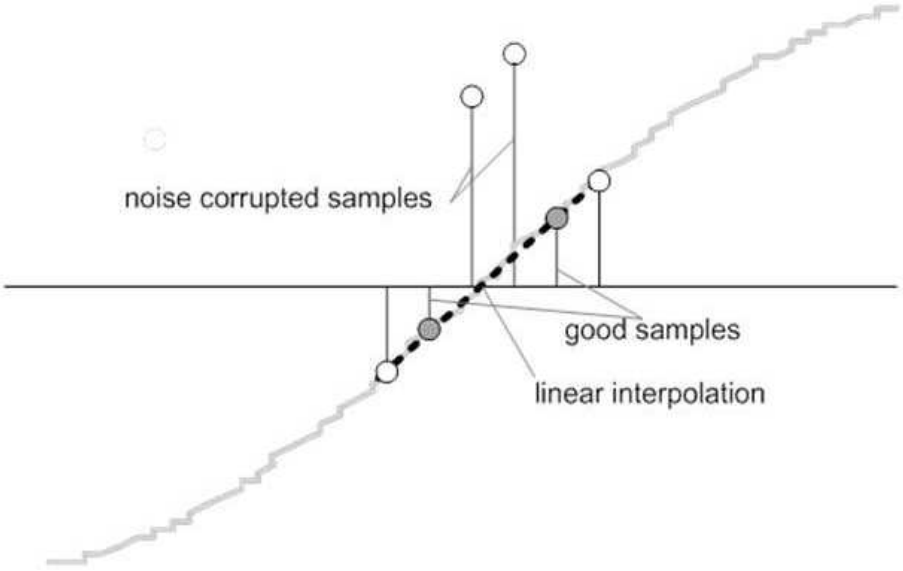


Figure 10. Frequency Measurement

Because noise spikes can also cause errors, the application uses a rate of change check to filter out the possible erroneous signals and make sure that the two points are interpolated from genuine zero crossing points. For example, with two negative samples, a noise spike can make one of the samples positive, thereby making the negative and positive pair appear as if there is a zero crossing.

The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out any cycle-to-cycle variations. This filtering results in a stable and accurate frequency measurement that is tolerant of noise.

3.2.3.2 LED Pulse Generation

In electricity meters, the energy consumption of the load is normally measured in a fraction of kilowatt-hour (kWh) pulses. This information can be used to accurately calibrate any meter for accuracy measurement. Typically, the measuring element (the MSP430 microcontroller) is responsible for generating pulses proportional to the energy consumed. To serve both these tasks efficiently, the pulse generation must be accurate with relatively little jitter. Although time jitters are not an indication of bad accuracy, time jitters give a negative indication of the overall accuracy of the meter. The jitter must be averaged out due to this negative indication of accuracy.

This application uses average power to generate these energy pulses. The average power (calculated by the foreground process) accumulates at every ΣΔ interrupt, thereby spreading the accumulated energy from the previous one-second time frame evenly for each interrupt in the current one-second time frame. This accumulation process is equivalent to converting power to energy. When the accumulated energy crosses a threshold, a pulse is generated. The amount of energy above this threshold is kept and a new energy value is added on top of the threshold in the next interrupt cycle. Because the average power tends to be a stable value, this way of generating energy pulses is very steady and free of jitter.

The threshold determines the energy "tick" specified by meter manufacturers and is a constant. The tick is usually defined in pulses per kWh or just in kWh. One pulse must be generated for every energy tick. For example, in this application, the number of pulses generated per kWh is set to 6400 for active and reactive energies. The energy tick in this case is 1 kWh/6400. Energy pulses are generated and available on a header and also through LEDs on the board. GPIO pins produce the pulses.

In the EVM, the LED labeled "Active" corresponds to the active energy consumption for the cumulative three-phase sum. "Reactive" corresponds to the cumulative three-phase reactive energy sum. The number of pulses per kWh and each pulse duration can be configured in software. Figure 11 shows the flow diagram for pulse generation. This flow diagram is valid for pulse generation of active and reactive energy.

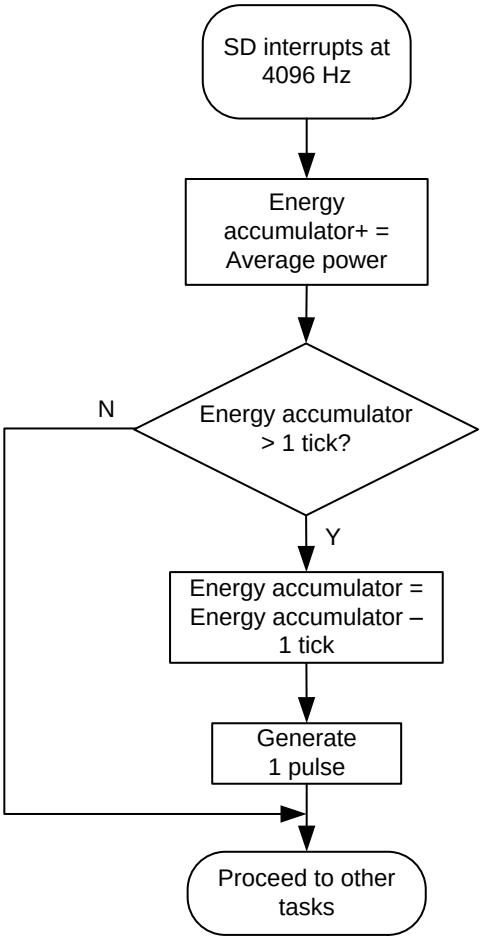


Figure 11. Pulse Generation for Energy Indication

The average power is in units of 0.001 W and a 1-kWh threshold is defined as:

$$\text{1-kWh threshold} = 1 / 0.001 \times 1\ \text{kW} \times (\text{Number of interrupts per sec}) \times (\text{number of seconds in one hour}) = 1000000 \times 4096 \times 3600 = 0\text{xD693A400000} \quad (24)$$

3.2.3.3 Phase Compensation

When a CT is used as a sensor, it introduces additional phase shift on the current signals. Also, the passive components of the voltage and current input circuit may introduce another phase shift. The user must compensate the relative phase shift between voltage and current samples to ensure accurate measurements. The ΣΔ converters have programmable delay registers (ΣΔ24PREx) that can be applied to a particular channel. This built-in feature (PRELOAD) provides the required phase compensation. Figure 12 shows the usage of PRELOAD to delay sampling on a particular channel.

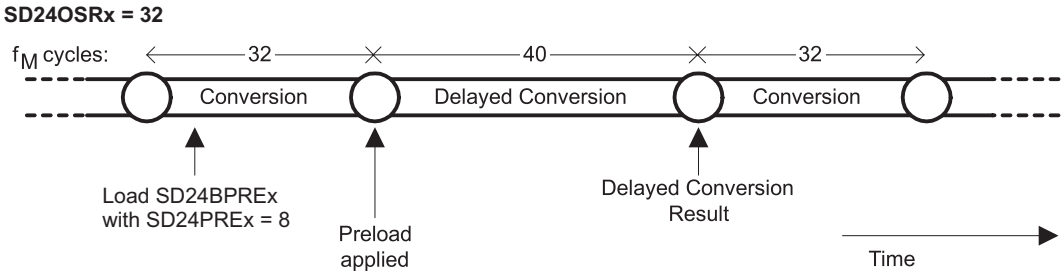


Figure 12. Phase Compensation Using PRELOAD Register

The fractional delay resolution is a function of input frequency (f_{IN}), OSR, and the sampling frequency (f_S).

$$\text{Delay resolution}_{Deg} = \frac{360^o \times f_{IN}}{OSR \times f_S} = \frac{360^o \times f_{IN}}{f_M} \quad (25)$$

In the current application, for an input frequency of 60 Hz, OSR of 256, and sampling frequency of 4096, the resolution for every bit in the PRELOAD register is about 0.02° with a maximum of 5.25° (maximum of 255 steps). When using CTs that provide a larger phase shift than this maximum, sample delays along with fractional delay must be provided.

4 Getting Started Hardware

For testing this design, the EVM430-F6779 is used and its MSP430F67791 is replaced with a MSP430F67791A. The following figures of the EVM best describe the hardware: Figure 13 is the top view of the energy measurement system, and Figure 14 then shows the location of various pieces of the EVM based on functionality.

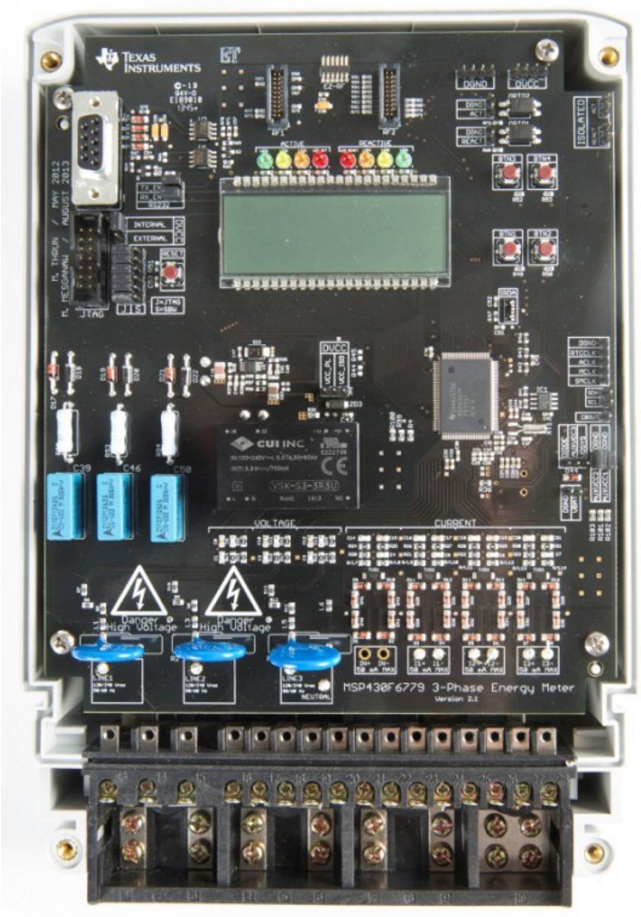


Figure 13. Top View of the TIDM-THDREADING Board

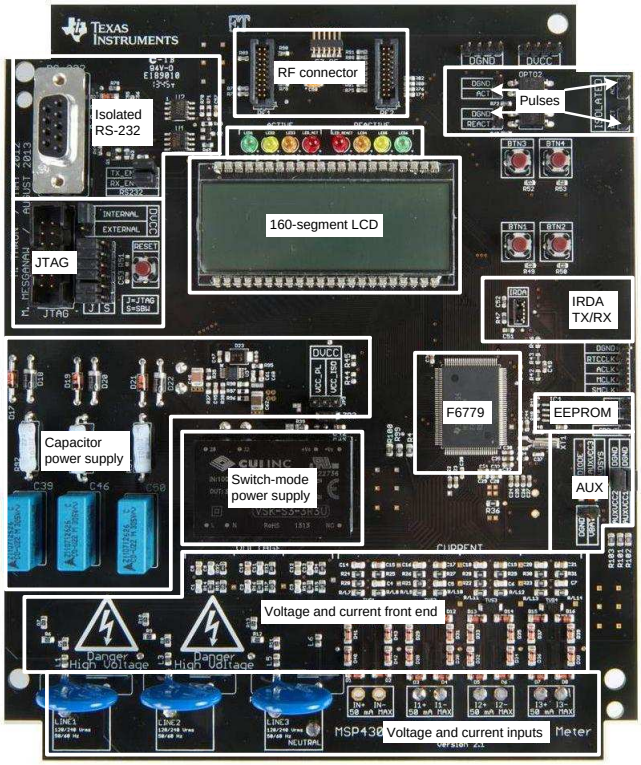


Figure 14. Top View of TIDM-THDREADING Board With Components Highlighted

4.1 Connections to the Test Setup for AC Voltages

AC voltage or currents can be applied to the board for testing purposes at these points:

- Pad "LINE1" corresponds to the line connection for phase A.
- Pad "LINE2" corresponds to the line connection for phase B.
- Pad "LINE3" corresponds to the line connection for phase C.
- Pad "Neutral" corresponds to the Neutral voltage. The voltage between any of the three line connections to the neutral connection should not exceed 230-V AC at 50 or 60 Hz.
- I1+ and I1– are the current inputs after the sensors for phase A. When a current sensor is used, make sure the voltages across I1+ and I1– does not exceed 930 mV. *This is currently connected to a CT on the EVM.*
- I2+ and I2– are the current inputs after the sensors for phase B. When a current sensor is used, make sure the voltages across I2+ and I2– does not exceed 930 mV. *This is currently connected to a CT on the EVM.*
- I3+ and I3– are the current inputs after the sensors for phase C. When a current sensor is used, make sure the voltages across I3+ and I3– does not exceed 930 mV. *This is currently connected to a CT on the EVM.*
- IN+ and IN– are the current inputs after the sensors for the neutral current. When a current sensor is used, make sure the voltages across IN+ and IN– does not exceed 930 mV. *This is currently not connected to the EVM.*

Figure 15 and Figure 16 show the various connections that need to be made to the test setup for proper functionality of the EVM. When a test AC source needs to be connected, the connections have to be made according to the EVM design.

Figure 15 shows the connections from the top view. V_A+ , V_B+, and V_C+ corresponds to the line voltage for phases A, B, and C, respectively. V_N corresponds to the neutral voltage from the test AC source.

Figure 16 shows the connections from the front view. I_A+ and I_A– correspond to the current inputs for phase A, I_B+, and I_B– correspond to the current inputs for phase B, and I_C+, and I_C– correspond to the current inputs for phase C. V_N corresponds to the neutral voltage from the test setup. Although the EVM hardware and software supports measurement for the neutral current, the EVM obtained from Texas Instruments do not have a sensor connected to the neutral ADC channel.

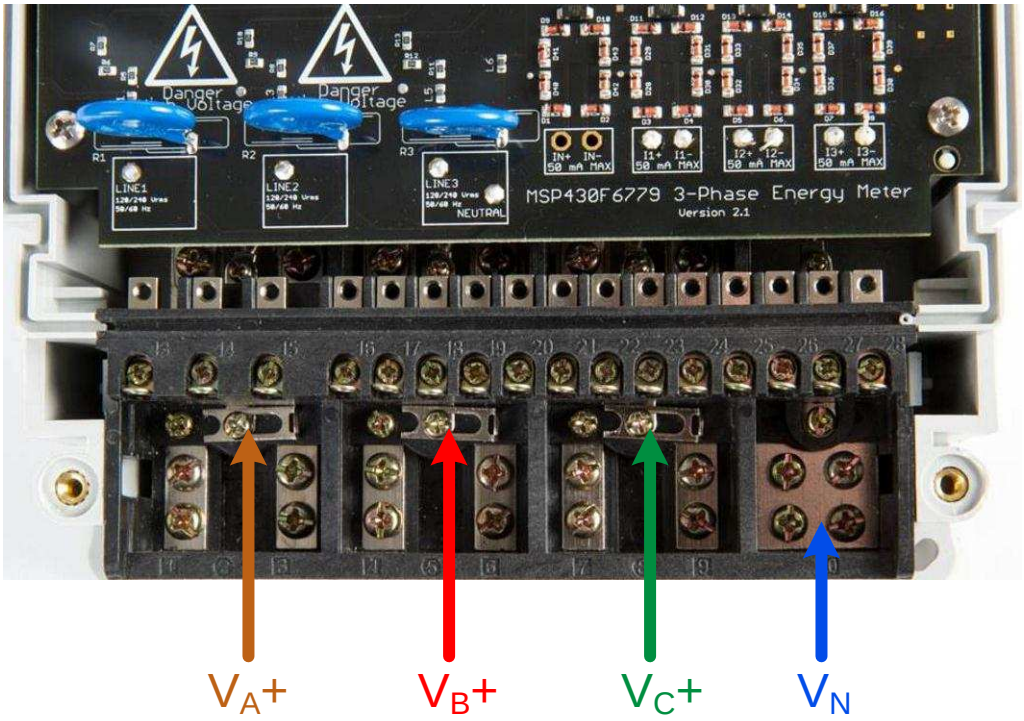


Figure 15. Top View of the EVM With Test Setup Connections

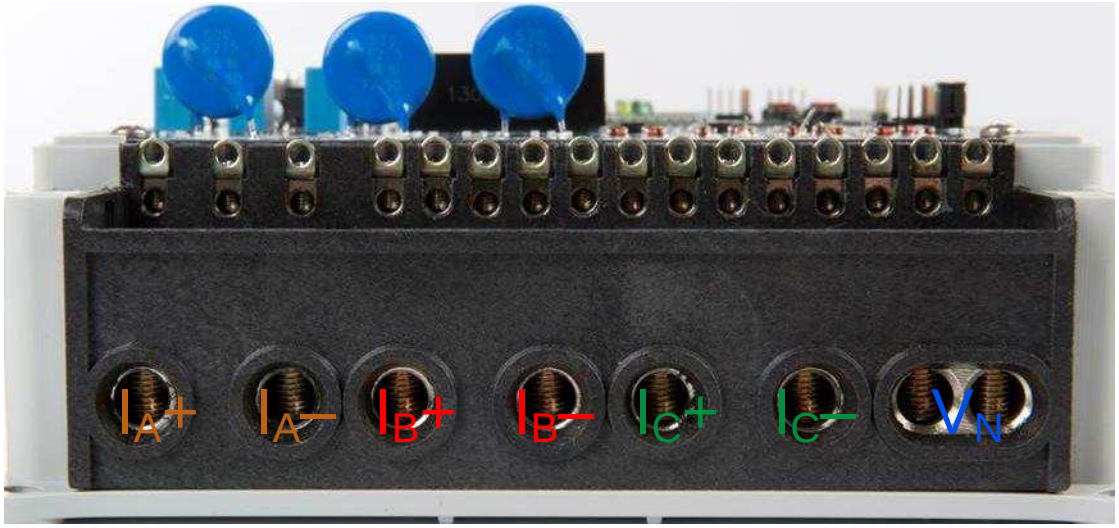


Figure 16. Front View of the EVM With Test Setup Connections

4.2 Power Supply Options and Jumper Settings

The EVM can be configured to operate with different sources of power. The entire board can be powered by a single DC voltage rail (DVCC), which can be derived either through JTAG, external power, or AC mains through either the capacitive or switching power supplies. Various jumper headers and settings are present to add to the flexibility to the board. Some of these headers require that jumpers be placed appropriately for the board to correctly function. Table 1 indicates the functionality of each jumper on the board and the associated functionality.

Table 1. Header Names and Jumper Settings

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
ACLK (Not isolated, do not probe)	1-pin header	ACLK output **(WARNING)**	Probe here to measure the frequency of ACLK.	This header is not isolated from AC voltage so do not connect any measuring equipment.
ACT (Not isolated, do not probe)	1-pin header	Active energy pulses **(WARNING)**	Probe between here and ground for cumulative three-phase active energy pulses	This header is not isolated from AC voltage so do not connect measuring equipments unless isolators external to the EVM are available. See Isolated ACT instead.
AUXVCC1 (Not isolated, do not probe)	2-pin header	AUXVCC1 selection or external power **(WARNING)**	Place a jumper here to connect AUXVCC1 to GND. This jumper must be present if AUXVCC1 is not used as a backup power supply. Alternatively, it can be used to provide a back-up power supply to the MSP430. To do so, simply connect the alternative power supply to this header and configure the software to use the backup power supply as needed. In addition, on the bottom of the board, a footprint is present that allows the addition of a super capacitor.	
AUXVCC2 (Not isolated, do not probe)	2-pin jumper Header	AUXVCC2 selection or AUXVCC2 external power **(WARNING)**	Place a jumper here to connect AUXVCC2 to GND. This jumper must be present if AUXVCC2 is not used as a backup power supply. Alternatively, it can be used to provide a back-up power supply to the MSP430. To do so, simply connect the alternative power supply to this header and configure the software to use this backup power supply as needed.	
AUXVCC3 (Not isolated, do not probe)	2-pin jumper Header	AUXVCC3 selection or external power **(WARNING)**	To power the RTC externally regardless of whether DVCC is available, provide external voltage at AUXVCC3, disable the internal AUXVCC3 charger in software, and do not connect a jumper at this header. Alternatively, place a jumper at the "VDSYS" option to connect AUXVCC3 to VDSYS so that it is powered from whichever supply (DVCC, AUXVCC1, or AUXVCC2) is powering the chip. If this jumper is placed, disable the internal charger in software. To power the RTC externally only when DVCC is not available, enable the internal charger, place a jumper at the "Diode", option and apply external voltage at the VBAT header.	
DGND (Not isolated, do not probe)	Header	Ground voltage header **(WARNING)**	Not a jumper header, probe here for GND voltage. Connect negative terminal of bench or external power supply when powering the board externally.	Do not probe if board is powered from AC mains, unless the AC mains are isolated. This voltage can be hot or neutral if AC wall plug is connected to the system.
DVCC (Not isolated, do not probe)	Header	VCC voltage header **(WARNING)**	Not a jumper header, probe here for VCC voltage. Connect positive terminal of bench or external power supply when powering the board externally.	Do not probe if board is powered from AC mains, unless the AC mains are isolated.
DVCC EXTERNAL (Do not connect JTAG if AC mains is the power source Isolated JTAG or supply is fine)	Jumper Header option	JTAG external power selection option **(WARNING)**	Place a jumper at this header option to select external voltage for JTAG programming.	This Jumper option and the DVCC INTERNAL jumper option comprise one three-pin header used to select the voltage source for JTAG programming.

Table 1. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
DVCC INTERNAL (Do not connect JTAG if AC mains is the power source).	Jumper Header option	JTAG internal power selection option **(WARNING)**	Place a jumper at this header option to power the board using JTAG and to select the voltage from the USB FET for JTAG programming.	This Jumper option and the DVCC EXTERNAL jumper option comprise one three-pin header used to select the voltage source for JTAG programming.
DVCC VCC_ISO ISO (Not isolated, do not probe)	Jumper Header option	Switching-mode supply select	Place a jumper at this header position to power the board through AC mains using the switching power supply	Place a jumper only if AC mains voltage is needed to power the DVCC rail. This header option and the DVCC VCC_PL header option comprise one 3-pin header that selects a capacitive power supply, a switching-mode power supply, or neither.
DVCC VCC_PL (Not isolated, do not probe)	Jumper Header option	Capacitor power supply select **(WARNING)**	Place a jumper at this header position to power the board through AC mains using the capacitor power supply	Place a jumper only if AC mains voltage is needed to power the DVCC rail. Do not debug using JTAG unless AC source is isolated or JTAG is isolated. This header option and the DVCC VCC_ISO header option comprise one three-pin header that selects a capacitive power supply, a switching-mode power supply, or neither
ISOLATED ACT	1-pin header	Isolated active energy pulses	Not a jumper header, probe between here and ground for cumulative three-phase active energy pulses	This header is Isolated from AC voltage so it is safe to connect to scope or other measuring equipment since isolators are already present.
ISOLATED REACT	1-pin header	Isolate reactive energy pulses	Not a jumper header, probe between here and ground for cumulative three-phase reactive energy pulses	This header is Isolated from AC voltage so it is safe to connect to scope or other measuring equipment since isolators are already present.
J (Do not connect JTAG if AC mains is the power source)	Jumper Header option	4-wire JTAG programming option **(WARNING)**	Place jumpers at the J header options of all of the six JTAG communication headers to select 4-wire JTAG.	There are six headers that jumpers must be placed at to select a JTAG communication option. Each of these six headers has a J option and an S option to select either 4-wire JTAG or SBW. To enable 4-wire JTAG, all of these headers must be configured for the J option. To enable SBW, all of the headers must be configured for the S option.
MCLK (Not isolated, do not probe)	1-pin header	MCLK output **(WARNING)**	Probe here to measure the frequency of MCLK.	The software does not output MCLK by default and will have to be modified to output MCLK. Probe only when AC mains is isolated
REACT (Not isolated, do not probe)	1-pin header	Reactive energy pulses **(WARNING)**	Not a jumper header, probe between here and ground for cumulative three-phase reactive energy pulses	This header is not isolated from AC voltage so do not connect measuring equipments unless isolators external to the EVM are available. See Isolated REACT instead.
RTCCLK	1-pin header	RTCCLK output	Probe here to measure the frequency of RTCCLK, which is used for calibrating the RTC.	The software does not output RTCCLK by default and will have to be modified to output RTCCLK.
RX_EN	Jumper Header	RS-232 Receive enable	Place a jumper here to enable receiving characters using RS-232.	—

Table 1. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
S (Do not connect JTAG if AC mains is the power source)	Jumper Header option	SBW JTAG programming option **(WARNING)**	Place jumpers at the S header options of all of the six JTAG communication headers to select SBW	There are six headers that jumpers must be placed at to select a JTAG communication. Each of these six headers that have a J option and an S option to select either 4-wire JTAG or SBW. To enable 4-wire JTAG, all of these headers must be configured for the J option. To enable SBW, all of the headers must be configured for the S option.
SCL (Not isolated, do not probe)	1-pin jumper Header	I^2C/EEPROM SCL probe point **(WARNING)**	Probe here to probe I^2C SCL line	Probe only when AC mains is isolated
SDA (Not isolated, do not probe)	1-pin jumper Header	I2C/EEPROM SDA probe point **(WARNING)**	Probe here to probe I^2C SDA line	Probe only when AC mains is isolated
SMCLK (Not isolated, do not probe)	1-pin header	SMCLK output **(WARNING)**	Probe here to measure the frequency of SMCLK.	The software does not output MCLK by default and will have to be modified to output SMCLK. Probe only when AC mains is isolated
TX_EN	Jumper Header	RS-232 transmit enable	Place a jumper here to enable RS-232 transmissions.	—
VBAT	2-pin jumper Header	AUXVCC3 external power for AUXVCC3 "Diode" option **(WARNING)**	When the "Diode" option is selected for AUXVCC3, apply voltage at this header so that the RTC could still be powered when the voltage at DVCC is removed.	—

5 Getting Started Firmware

The source code is developed in the IAR™ environment using the IAR Embedded Workbench® Integrated Development Environment (IDE) version 6.10.1 for the MSP430 IDE and version 7.0.5.3137 for IAR common components. Earlier versions of IAR cannot open the project files. When the project is loaded in IAR version 6.x or later, the IDE may prompt the user to create a backup. Click "YES" to proceed. The energy metrology software has three main parts:

- The toolkit that contains a library of mostly mathematics routines
- The metrology code that is used for calculating metrology parameters
- The application code that is used for the host-processor functionality of the system (that is communication, LCD, RTC setup, and so forth)

Figure 17 shows the contents of the source folder.

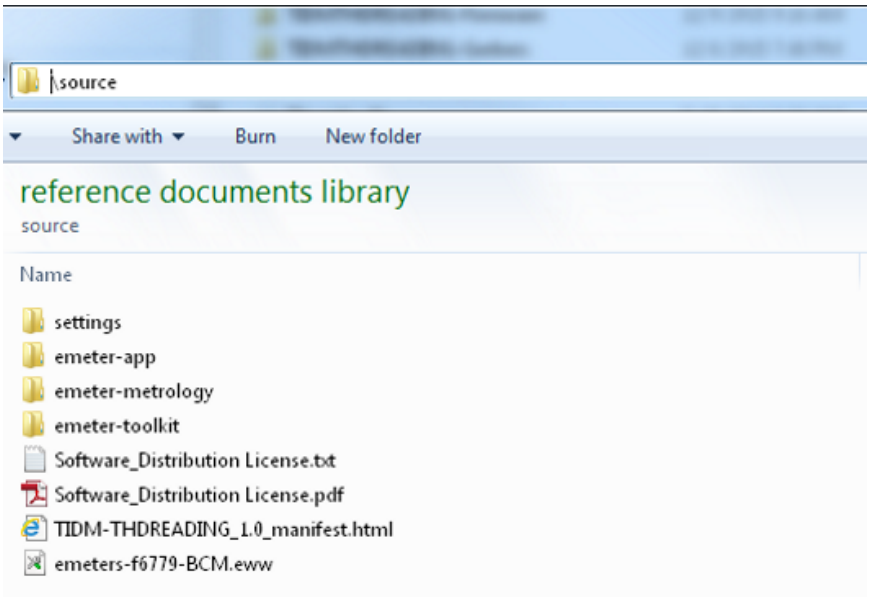


Figure 17. Source Folder Structure

Within the emeter-app-6779 folder in the emeter-app folder, the emeter-app-6779.ewp project corresponds to the application code. Similarly, within the emeter-metrology-6779 folder in the emeter-metrology folder, the emeter-metrology-6779.ewp project corresponds to the portion of the code for metrology. Additionally, the folder emeter-toolkit-6779 within the emeter-toolkit has the corresponding toolkit project file emeter-toolkit-6779.ewp. For first-time use, TI recommends to rebuild all three projects by performing the following steps:

1. Open the IAR IDE.
2. Open the F6779 workspace, which is located in the source folder.
3. Within IARs workspace window, click the Overview tab to have a list view of all the projects.
4. Right-click the emeter-toolkit-6779 option in the workspace window and select Rebuild All, as Figure 18 shows.
5. Right-click the emeter-metrology-6779 option in the workspace window and select Rebuild All, as Figure 19 shows.
6. Within IARs workspace window, click the emeter-app-6779 tab.
7. Within the workspace window, select emeter-app-6779, click Rebuild All as Figure 20 shows, and then download this project onto the MSP430F67791A.

NOTE: If any changes are made to any of the files in the toolkit project and the project is compiled, the metrology project must be recompiled. After recompiling the metrology project, the application project must then be recompiled. Similarly, if any changes are made to any of the files in the metrology project and the project is compiled, the application project must then be recompiled.

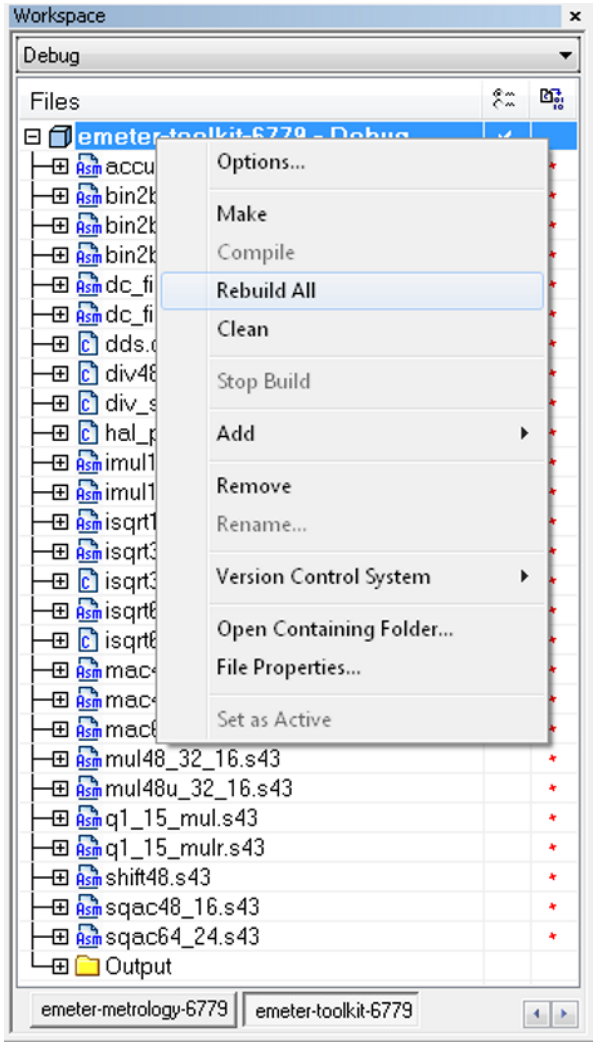


Figure 18. Toolkit Project Compilation

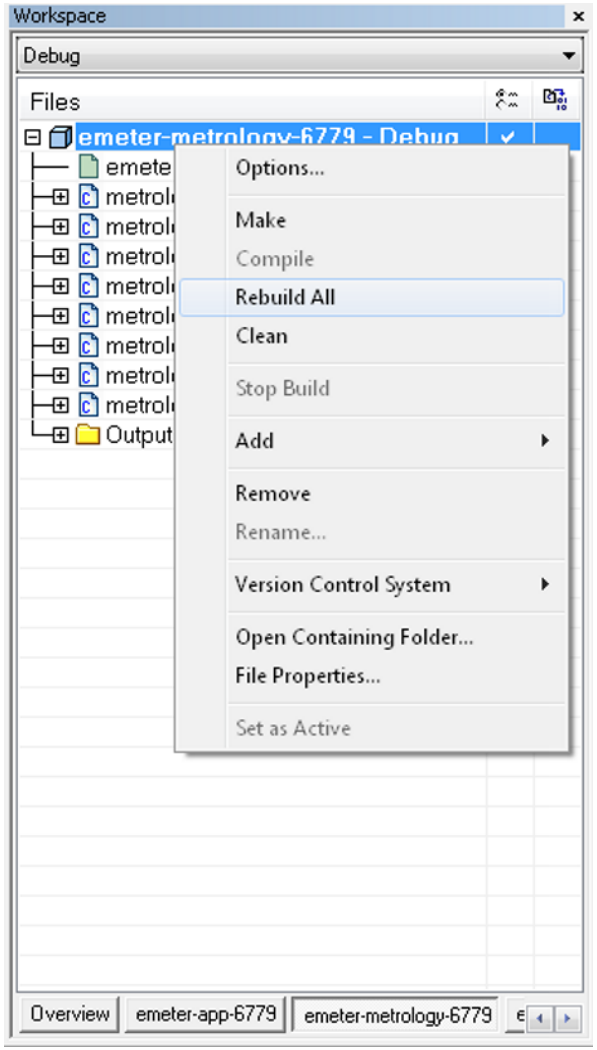


Figure 19. Metrology Project Compilation

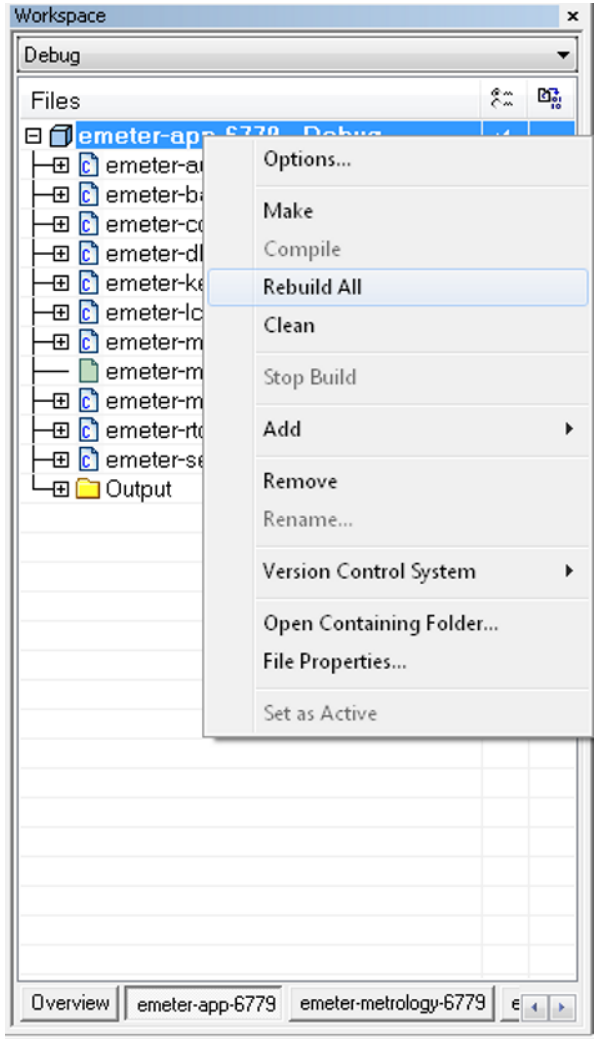


Figure 20. Application Project Compilation

6 Test Setup

To test metrology performance, a source generator provides the voltages and currents to the system at the proper locations mentioned in Section 4.1. A nominal voltage of 120 V, calibration current of 15 A, nominal frequency of 60 Hz, and power factor of 1 were used for each phase. In addition, for most test conditions, there is a fifth harmonic component added to both the fundamental voltage and current waveforms. For most tests, the fifth harmonic component of the current is set to 40% of the fundamental current and the fifth harmonic component of the voltage is set to 10% of the fundamental voltage. Also, because the used reference meter uses the THDR formula to calculate THD, the software is configured to also use this THDR formula for most of the test conditions. In the set of tests, eight different conditions were used for testing.

6.1 Condition 1: No Harmonics Present

In the first test condition, harmonics are not exposed to the system. Under this condition, active energy and reactive energy tests are conducted. For active and reactive energy testing, when the voltages and currents are applied to the system, the system outputs the cumulative active energy pulses at a rate of 6400 pulses/kWh. This pulse output is fed into a reference meter (in the test setup, this is integrated in the same equipment used for the source generator) that determines the active energy % error based on the actual energy provided to the system and the measured energy as determined by the system's active energy output pulse. Based on this, a plot of active energy % error versus current is created for 0°, 60°, and –60° phase shifts as shown in Section 8.1. Using a similar procedure, a plot of reactive energy % error versus current is created for 60° and –60°.

In addition to testing active and reactive energy % error, the phase-to-phase angle measurement is also tested. For this test, the phase-to-phase angle measurement on the GUI is compared to the reference meter's readings for these phase-to-phase angle readings.

6.2 Condition 2: Fifth Current Harmonic at 40%, Fifth Voltage Harmonic at 10%, 60 Hz

For the second test condition, a fifth harmonic component is added to both the voltage and current. The fifth harmonic component for voltage is set to 10% of the fundamental voltage and the fifth harmonic component for current is set to 40% of the fundamental current. The harmonic components are set so that they are aligned with the corresponding fundamental components. In addition, for this test the system uses a fundamental voltage of 120 V, frequency of 60 Hz, power factor of 1, and the THD_{IEC_R} formula for calculating the voltage and current THD.

Under these set of conditions, the voltage THD is measured using the reference meter and then compared to the calculated values of THD. For current THD calculations, multiple THD readings were taken from a fundamental current of 0.1 to 50 A. Over the same 0.1- to 50-A range, the % error of the fundamental active power is calculated using the measured fundamental active power and the fundamental active power reading from the reference meter.

6.3 Condition 3: Fifth Current Harmonic at 40%, Fifth Voltage Harmonic at 10%, 50 Hz

Condition 3 is similar to condition 2 except the fundamental frequency is 50 Hz instead of 60 Hz.

6.4 Condition 4: Combination of Harmonics

Condition 4 is similar to condition 2 except there are multiple harmonic components added to both the voltage and current channels. For voltage, third, fifth, seventh, and ninth harmonic components are added where each harmonic component is set to 2.5% of the fundamental voltage. For current, the third, fifth, seventh, and ninth harmonic components are each set to 10% of the fundamental current.

6.5 Condition 5: Fifth Current Harmonic at 4%, Fifth Voltage Harmonic at 2%

Condition 5 is similar to condition 2 except that instead of applying a fifth harmonic component at 40% for current, the fifth harmonic component is set to 4% of the fundamental. For voltage, the fifth harmonic component for this condition is set to 2% of the fundamental.

6.6 Condition 6: Power Factor = 0, Reactive Power Testing

In this condition, the fundamental reactive power % error is tested by applying a power factor of 0. The other parameters for this test condition are set as it is done for condition 2.

6.7 Condition 7: THD_{IEC_F} Calculations

In this condition, condition 2 is tested but the THD_{IEC_F} formula is used instead of the THD_{IEC_R} formula. Because the reference meter used for testing does not use this calculation formula for calculating THD, a THD_{IEC_F} calculation is calculated by looking at the reference meter's calculation of the amplitude of the fifth harmonic. Due to the source meter not being able to add a fifth harmonic component without adding a small portion of content at other harmonics, this measurement method would not be the most accurate because the system's THD reading would take into account the content at other harmonics while the calculation based on the reference meter's fifth harmonic content would not take this into account.

6.8 Condition 8: THD_{IEEE} Calculation

For condition 8, condition 2 is tested but the THD_{IEEE} is used instead of the THDR formula. The reference meter does not use this formula for calculating THD but the reference meter's THD_{IEC_R} calculation can be converted to be in the form of this alternative THD calculation.

7 Viewing Metrology Readings and Calibration

7.1 Viewing Results Through LCD

The LCD scrolls between metering parameters every two seconds. For each metering parameter that is displayed on the LCD, three items are usually displayed on the screen: a symbol used to denote the phase of the parameter, text to denote which parameter is being displayed, and the actual value of the parameter. The phase symbol is displayed at the top of the LCD and denoted by a triangle shape. The orientation of the symbol determines the corresponding phase. Figure 21 through Figure 23 shows the mapping between the different orientations of the triangle and the phase description:

Figure 21. Symbol for Phase A

Figure 22. Symbol for Phase B

Figure 23. Symbol for Phase C

Aggregate results (such as cumulative active and reactive power) and parameters that are independent of phase (such as time and date) are denoted by clearing all of the phase symbols on the LCD.

The bottom line of the LCD denotes the value of the parameter being displayed. The text to denote the parameter being shown is displayed on the top line of the LCD. Table 2 shows the different metering parameters that are displayed on the LCD and the associated units in which they are displayed. The **DESIGNATION** column shows which characters correspond to which metering parameter.

Table 2. Displayed Parameters

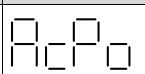
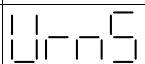
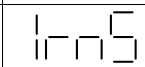
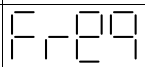
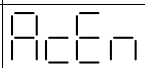
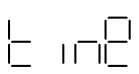
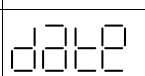
PARAMETER NAME	DESIGNATION	UNITS	COMMENTS
Active power		Watts (W)	This parameter is displayed for each phase. The aggregate active power is also displayed.
Reactive power		Volt-Ampere Reactive (VAR)	This parameter is displayed for each phase. The aggregate reactive power is also displayed.
Apparent power		Volt-Ampere (VA)	This parameter is displayed for each phase.
Power factor		Constant between 0 and 1	This parameter is displayed for each phase.
Voltage		Volts (V)	This parameter is displayed for each phase.
Current		Amps (A)	This parameter is displayed for each phase.
Frequency		Hertz (Hz)	This parameter is displayed for each phase.
Total consumed active energy		kWh	This parameter is displayed for each phase.
Total consumed reactive energy		kV_{ARH}	This parameter is displayed for each phase. This displays the sum of the reactive energy in quadrant 1 and quadrant 4.
Time		Hour:Minute:Second	This parameter is only displayed when the sequence of aggregate readings are displayed. It is not displayed once per phase.
Date		Year:Month:Day	This parameter is only displayed when the aggregate readings are displayed. It is not displayed once per phase.

Figure 24 shows an example of phase B's measured frequency of 49.99 Hz displayed on the LCD.

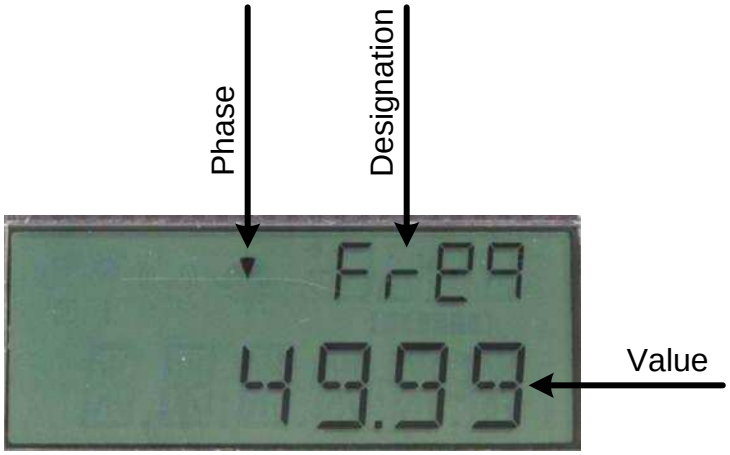


Figure 24. LCD

7.2 Calibrating and Viewing Results Through PC

7.2.1 Viewing Results

To view the metrology parameter values from the GUI, perform the following steps:

1. Connect the EVM to a PC using an RS-232 cable.
2. Open the GUI folder and open calibration-config.xml in a text editor.
3. Change the port name field within the meter tag to the COM port connected to the system. As Figure 25 shows, this field is changed to COM7.

```
260       </correction>
261     </phase>
262     <temperature/>
263     <rtc/>
264   </cal-defaults>
265   <meter position="1">
266     <port name="com7" speed="9600"/>
267   </meter>
268   <reference-meter>
269     <port name="USB0::0x0A69::0x0835::A66200101281::INSTR"/>
270     <type id="chroma-66202"/>
271     <log requests="on" responses="on"/>
272     <scaling voltage="1.0" current="1.0"/>
273   </reference-meter>
```

Figure 25. GUI Config File Changed to Communicate With Energy Measurement System

4. Run the calibrator.exe file, which is located in the GUI folder. If the COM port in the calibration-config.xml was changed in the previous step to the COM port connected to the EVM, the GUI opens (see Figure 26). If the GUI connects properly to the EVM, the top-left button is green. If there are problems with connections or if the code is not configured correctly, the button is red. Click the green button to view the results.

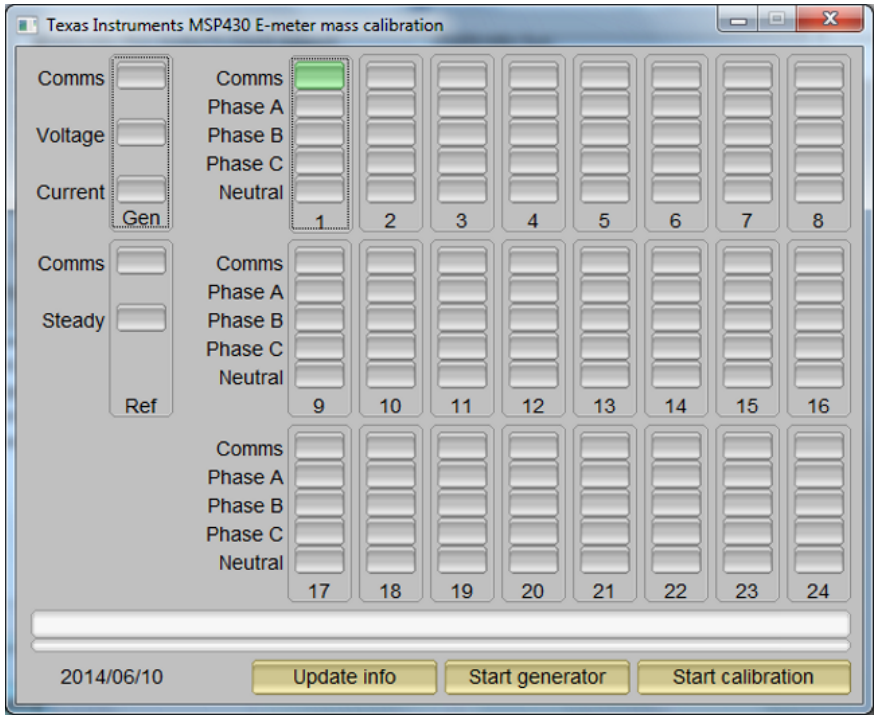


Figure 26. GUI Startup Window

Upon clicking on the green button, the results window opens (see Figure 27). In the figure, there is a trailing "L" or "C" on the Power factor values to indicate an inductive or capacitive load, respectively.

Figure 27. GUI Results Window

From Figure 27, the total-energy consumption readings and sag and swell logs can be viewed by clicking the Meter consumption button. After the user clicks this button, the Meter events and consumption window pops up, as Figure 28 shows.

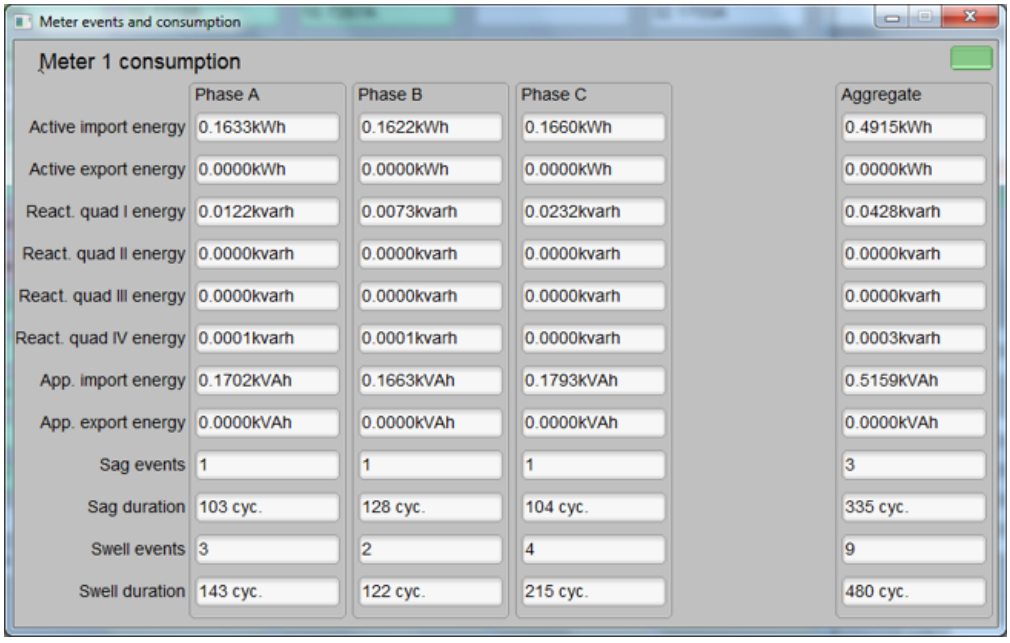


Figure 28. Meter Events and Consumption Window

From Figure 27, the user can view the system settings by clicking the "Meter features" button, view the system calibration factors by clicking the "Meter calibration factors" button, or open the window used for calibrating the system by clicking the "Manual cal." button.

7.2.2 Calibration

Calibration is key to any meter performance and it is absolutely necessary for every meter to go through this process. Initially, every meter exhibits different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify these effects, every meter must be calibrated. To perform calibration accurately there should be an accurate AC test source and a reference meter available. The source must be able to generate any desired voltage, current, and phase shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section discusses a simple and effective method of calibration of this three-phase EVM.

The GUI used for viewing results can easily be used to calibrate the EVM. During calibration, parameters called calibration factors are modified in software to give the least error in measurement. For this meter, there are six main calibration factors for each phase: voltage scaling factor, voltage AC offset, current scaling factor, current AC offset, power scaling factor, and the phase compensation factor. The voltage, current, and power scaling factors translate measured quantities in metrology software to real-world values represented in volts, amps, and watts, respectively. The voltage AC offset and current AC offset are used to eliminate the effect of additive white Gaussian noise (AWGN) associated with each channel. This noise is orthogonal to everything except itself; as a result, this noise is only present when calculating RMS voltages and currents. The last calibration factor is the phase compensation factor, which is used to compensate any phase shifts introduced by the current sensors and other passives. Note that the voltage, current, and power calibration factors are independent of each other. Therefore, calibrating voltage does not affect the readings for RMS current or power.

When the meter software is flashed with the code (available in the *.zip file), default calibration factors are loaded into these calibration factors. These values are to be modified through the GUI during calibration. The calibration factors are stored in INFO_MEM, and therefore, remain the same if the meter is restarted. However, if the code is re-flashed during debugging, the calibration factors may be replaced and the meter may have to be recalibrated. One way to save the calibration values is by clicking on the Meter calibration factors button (see Figure 27). The Meter calibration factors window (see Figure 29) displays the latest values, which can be used to restore calibration values.

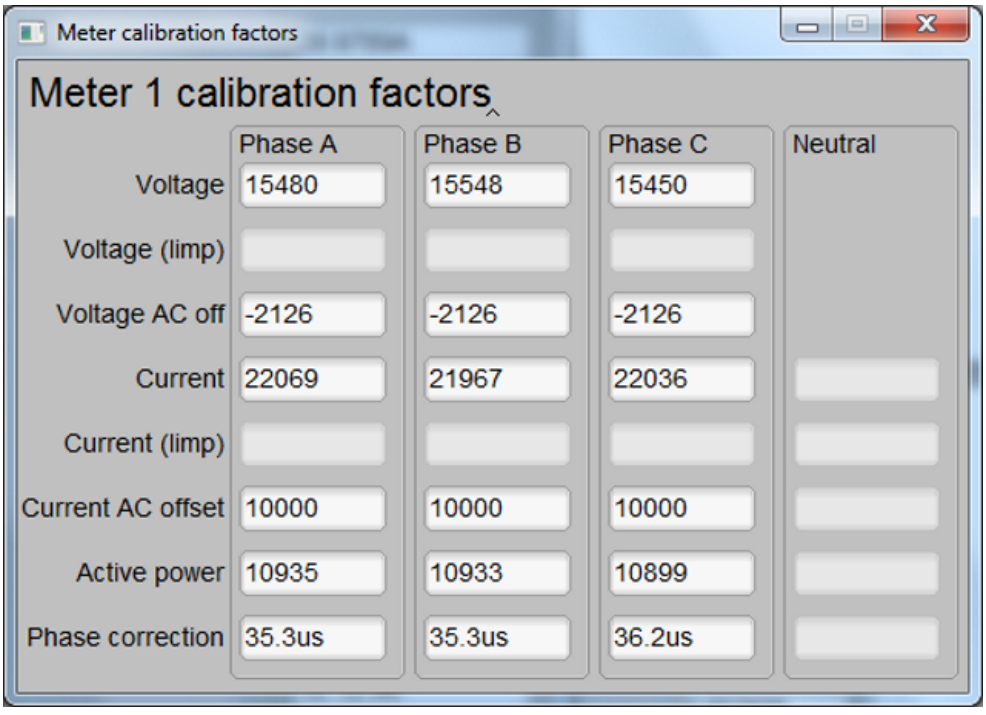


Figure 29. Calibration Factors Window

Calibrating any of the scaling factors is referred to as gain correction. Calibrating the phase compensation factors is referred to as phase correction. For the entire calibration process, the AC test source must be ON, meter connections consistent with Section 4.1, and the energy pulses connected to the reference meter.

7.2.2.1 Active Power Calibration

When performing active power calibration for any given phase, the other two phases must be disabled. Typically, switching only the currents OFF is good enough for disabling a phase.

Also, unlike current and voltage gain calibration, the active power error value that is used for active power gain calibration should be obtained from the reference meter and should not be calculated. This error is obtained by feeding the meter's energy pulse outputs to the reference meter, which would use these pulses to calculate the error. Although, conceptually, performing active power gain calibration can be done as it is done for voltage or current, this method is not the most accurate. The best option to get the proper error % used for calibration is to get it directly from the reference meters measurement error of the active energy.

7.2.2.1.1 Active Power Gain Calibration

Note that this example is for one phase. Repeat these steps for other phases.

1. Make sure the test source is OFF.
2. Connect the energy pulse output of the system to the reference meter. Configure the reference meter to measure the active power error based on these pulse inputs.
3. Connect the GUI to view results for voltage, current, active power, and the other metering parameters.
4. Turn on the test source and configure it to supply desired voltage for all phases and the desired current for only the phase being calibrated. Ensure that there is a zero-degree phase shift between the calibrating phase's voltage and current. For example, an example voltage, current, and phase shift can be 230 V, 10 A, 0º (PF = 1).
5. Click the "Manual cal." button that Figure 27 shows. The following screen pops up from Figure 30:

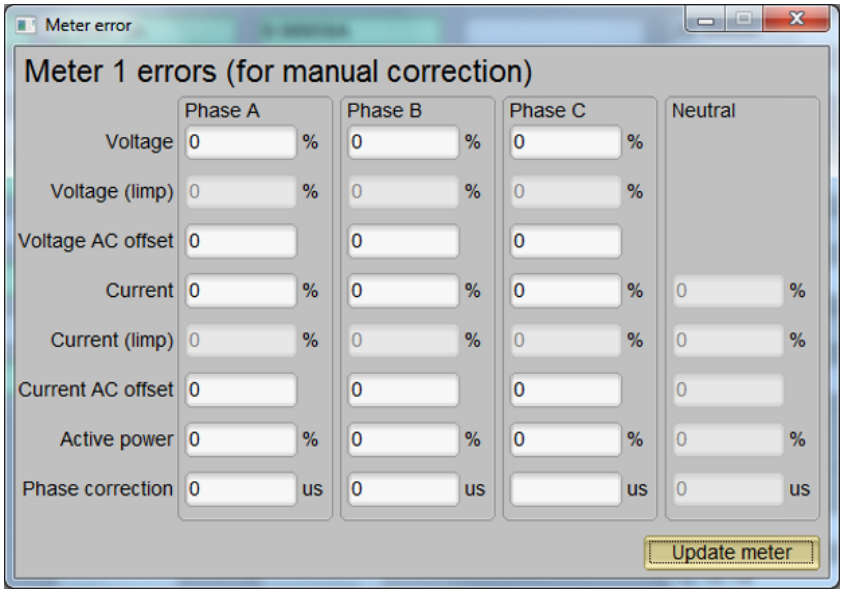


Figure 30. Manual Calibration Window

6. Obtain the % error in measurement from the reference meter. Note that this value may be negative.
7. Enter the error obtained in Step 4 into the Active Power field under the corresponding phase in the Figure 30 GUI window. This error is already the Correction (%) value and does not require calculation.
8. Click on Update meter button and the error values on the reference meter immediately settle to a value close to zero.

7.2.2.1.2 Active Power Phase Correction

After performing power gain correction, phase calibration must be performed. Similar to active power gain calibration, to perform phase correction on one phase, the other phases must be disabled. To perform phase correction calibration, perform the following steps:

1. If the AC test source has been turned OFF or reconfigured, perform Step 2 through Step 4 from Section 7.2.2.1.1 using the identical voltages and currents used in that section.
2. Disable all other phases that are not currently being calibrated by setting the current of these phases to 0 A.
3. Modify only the phase-shift to a non-zero value; typically, 60º is chosen. The reference meter now displays a different % error for active power measurement. Note that this value may be negative.
4. If this error from Step 3 is not close to zero, or is unacceptable, perform phase correction by following these steps:
   (a) In the Figure 30 GUI window, enter a value as an update for the Phase Correction field for the phase that is being calibrated. Usually, a small ± integer must be entered to bring the error closer to zero. Additionally, for a phase shift greater than 0 (for example: 60º), a positive (negative) error would require a positive (negative) number as correction.
   (b) Click on the "Update meter" button and monitor the error values on the reference meter.
   (c) If this measurement error (%) is not accurate enough, fine-tune by incrementing or decrementing by a value of 1 based on the previous Step 4a and Step 4b. Note that after a certain point, the fine-tuning only results in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.
   (d) Change the phase now to −60° and check if this error is still acceptable. Ideally, errors should be symmetric for same phase shift on lag and lead conditions.

After performing phase calibration, phase correction is complete for one phase. Repeat these steps to calibrate the other phases.

7.2.2.2 Voltage and Current Gain Calibration

After performing active power correction, gain correction should then be done for RMS voltage. When calibrating voltage, the voltages for all phases can be calibrated at the same time. Once voltage calibration has completed, RMS current should then be calibrated. Note that the calibration for RMS current should be done after active power and voltage are calibrated. Additionally, similar to RMS voltage, the currents for all phases can be calibrated at the same time. To perform either voltage or gain calibration, following these steps:

1. If the AC test source has been turned OFF or reconfigured, perform Step 2 through Step 4 from Section 7.2.2.1.1 using the identical voltages and currents used in that section.
2. Calculate the correction values for each voltage and current. The correction values that must be entered for the voltage and current fields are calculated by:

$$\text{Correction}\,(\%) = \left(\frac{\text{value}_{\text{observed}}}{\text{value}_{\text{desired}}} - 1 \right) \times 100 \tag{26}$$

   where
   - $\text{value}_{\text{observed}}$ is the value measured by the TI energy measurement system
   - $\text{value}_{\text{desired}}$ is the calibration point configured in the AC test source.
3. After calculating for all voltages and currents, input these values as is (±) into the Figure 30 window. This should be input into the fields Voltage and Current for the corresponding phases.
4. Click on the Update meter button and the observed values for the voltages and currents on the GUI settle to the desired voltages and currents.

This completes calibration of voltage, current, and power for all three phases. View the new calibration factors (see Figure 31) by clicking the "Meter calibration factors" button of the GUI metering results window in Figure 27.

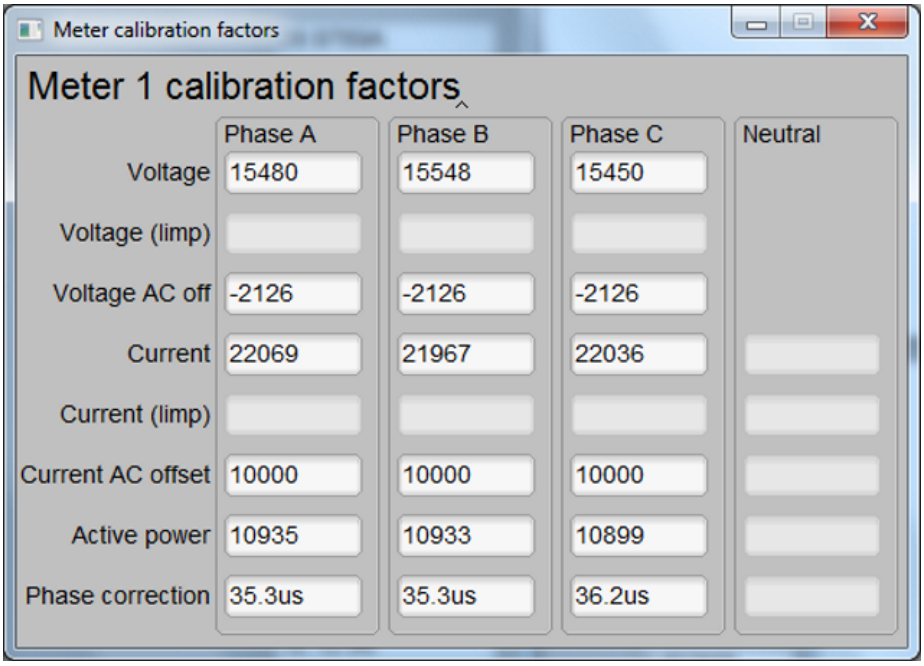


Figure 31. Calibration Factors Window

Also view the configuration of the system by clicking on the "Meter features button" in Figure 27 to get to the window that Figure 32 shows.

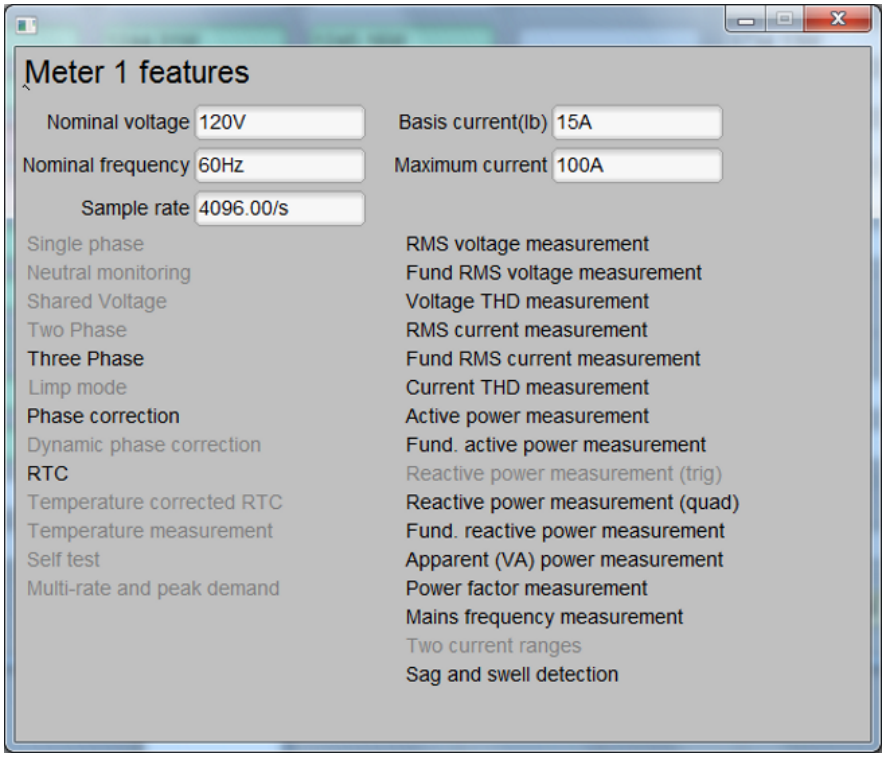


Figure 32. Meter Features Window

8 Test Data

8.1 Condition 1: No Harmonics Present

8.1.1 Active Energy

Table 3. Active Energy % Error

CURRENT (A)	0°	60°	–60°
0.05	–0.054	–0.008	–0.062
0.1	0.009	0.044	–0.067
0.25	0.005	0.040	–0.041
0.5	0.001	0.050	–0.039
1	0.005	0.046	–0.029
1.5	–0.007	0.045	–0.045
3	0.011	0.047	–0.032
10	0.015	0.025	0.010
15	0.008	0.011	0.003
30	0.020	–0.003	0.054
50	0.017	–0.062	0.091
75	0.020	–0.088	0.129
90	0.025	–0.107	0.167
100	0.024	–0.111	0.157

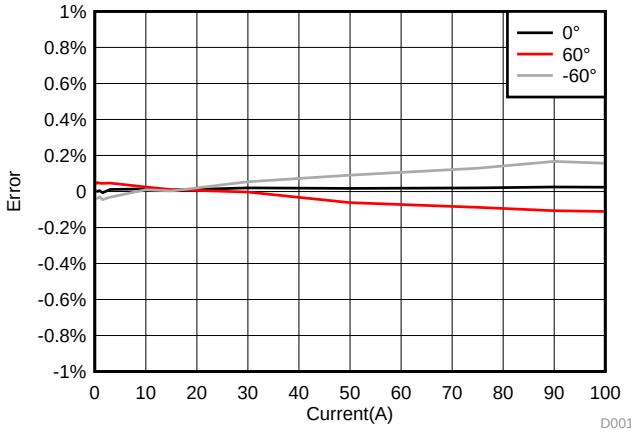


Figure 33. Active Energy % Error

8.1.2 Reactive Energy

Table 4. Reactive Energy % Error

CURRENT (A)	60°	–60°
0.05	–0.147	–0.058
0.1	–0.083	0.026
0.25	–0.070	0.006
0.5	–0.064	–0.005
1	–0.075	0.015
1.5	–0.070	–0.008
3	–0.052	–0.004
10	–0.048	–0.010
15	–0.051	–0.034
30	0.021	–0.024
50	–0.017	–0.051
75	0.002	–0.046
90	0.013	–0.036
100	0.019	–0.072

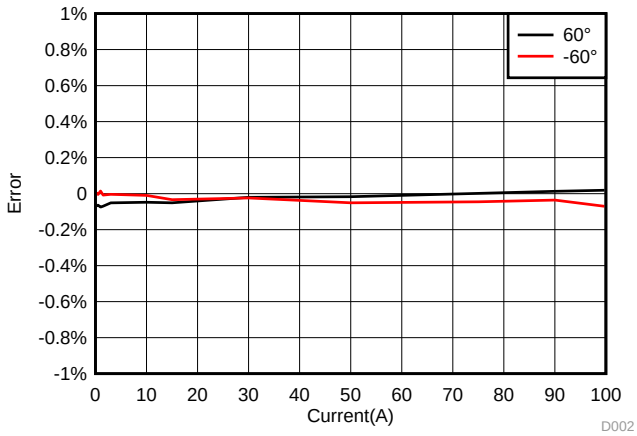


Figure 34. Reactive Energy % Error

8.1.3 Voltage Phase-to-Phase Delay

Table 5. Voltage Phase-to-Phase Delay

ANGLE	ACTUAL (°)	MEASURED (°)	DIFFERENCE (°)
ϕ13	239.849	240.18	–0.331
ϕ21	239.955	239.84	0.115
ϕ32	240.203	239.93	0.273

8.2 Condition 2: Fifth Current Harmonic at 40%, Fifth Voltage Harmonic at 10%, 60 Hz

8.2.1 Voltage THD

Table 6. Condition 2: Phase A Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	9.65	9.56

Table 7. Condition 2: Phase B Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	9.65	9.67

Table 8. Condition 2: Phase C Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	9.63	9.49

8.2.2 Current THD

Table 9. Condition 2: Phase A Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	37.442	36.34
0.25	37.348	36.29
1	37.330	36.27
10	37.296	36.28
50	37.302	36.28

Table 10. Condition 2: Phase B Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	37.420	36.36
0.25	37.336	36.29
1	37.320	36.27
10	37.323	36.27
50	37.317	36.26

Table 11. Condition 2: Phase C Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	37.446	36.37
0.25	37.358	36.28
1	37.327	36.28
10	37.339	36.27
50	37.328	36.27

8.2.3 Fundamental Active Power % Error

Table 12. Condition 2: Fundamental Active Power % Error

CURRENT (A)	PHASE A FUNDAMENTAL ACTIVE POWER % ERROR	PHASE B FUNDAMENTAL ACTIVE POWER % ERROR	PHASE C FUNDAMENTAL ACTIVE POWER % ERROR
0.1	–0.183073979	–0.199800200	–0.091666667
0.25	–0.196457112	–0.229785534	–0.066695568
1	–0.170648464	–0.213970527	–0.101658195
50	–0.170496170	–0.203486920	–0.043357180

8.3 Condition 3: Fifth Current Harmonic at 40%, Fifth Voltage Harmonic at 10%, 50 Hz

8.3.1 Voltage THD

Table 13. Condition 3: Phase A Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	9.8263	9.67

Table 14. Condition 3: Phase B Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	9.8534	9.67

Table 15. Condition 3: Phase C Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	9.8265	9.65

8.3.2 Current THD

Table 16. Condition 3: Phase A Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	37.343	36.61
0.25	37.283	36.55
1	37.257	36.52
10	37.229	36.53
50	37.259	36.53

Table 17. Condition 3: Phase B Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	37.342	36.64
0.25	37.269	36.56
1	37.255	36.55
10	37.278	36.55
50	37.270	36.56

Table 18. Condition 3: Phase C Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	37.354	36.58
0.25	37.283	36.48
1	37.291	36.47
10	37.282	36.48
50	37.270	36.46

8.3.3 Fundamental Active Power % Error

Table 19. Condition 3: Fundamental Active Power % Error

CURRENT (A)	PHASE A FUNDAMENTAL ACTIVE POWER % ERROR	PHASE B FUNDAMENTAL ACTIVE POWER % ERROR	PHASE C FUNDAMENTAL ACTIVE POWER % ERROR
0.1	–0.116579232	–0.116579232	–0.166555630
0.25	–0.133266700	–0.149925037	–0.119984002
1	–0.106586727	–0.168207178	–0.142405063
50	–0.104958017	–0.116645282	–0.116635564

8.4 Condition 4: Combination of Harmonics

8.4.1 Voltage THD

Table 20. Condition 4: Phase A Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	4.7724	4.50

Table 21. Condition 4: Phase B Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	4.9100	4.52

Table 22. Condition 4: Phase C Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	4.9355	4.55

8.4.2 Current THD

Table 23. Condition 4: Phase A Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	19.957	19.04
0.25	19.872	18.85
10	19.841	18.79
50	19.831	18.80

Table 24. Condition 4: Phase B Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	19.884	19.03
0.25	19.815	18.86
10	19.766	18.71
50	19.786	18.75

Table 25. Condition 4: Phase C Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	19.835	19.02
0.25	19.761	18.81
10	19.688	18.81
50	19.726	18.79

8.4.3 Fundamental Active Power % Error

Table 26. Condition 4: Fundamental Active Power % Error

CURRENT (A)	PHASE A FUNDAMENTAL ACTIVE POWER % ERROR	PHASE B FUNDAMENTAL ACTIVE POWER % ERROR	PHASE C FUNDAMENTAL ACTIVE POWER % ERROR
0.1	–0.141548709	–0.149875104	–0.149900067
0.25	–0.169892401	–0.179916039	–0.149950017
50	–0.137260128	–0.171414293	–0.129645059

8.5 Condition 5: Fifth Current Harmonic at 4%, Fifth Voltage Harmonic at 2%

8.5.1 Voltage THD

Table 27. Condition 5: Phase A Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	1.8946	2.08

Table 28. Condition 5: Phase B Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	1.8911	2.04

Table 29. Condition 5: Phase C Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	1.9269	1.99

8.5.2 Current THD

Table 30. Condition 5: Phase A Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	4.0500	5.07
0.25	4.0358	4.09
1	4.0354	3.85
10	4.0399	3.76
50	4.0282	3.71

Table 31. Condition 5: Phase B Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	4.0489	5.21
0.25	4.0278	4.29
1	4.0254	4.01
10	4.0334	4.13
50	4.0193	3.95

Table 32. Condition 5: Phase C Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	4.0240	5.03
0.25	4.0235	4.22
1	4.0215	3.99
10	4.0079	4.03
50	4.0086	3.94

8.5.3 Fundamental Active Power % Error

Table 33. Condition 5: Fundamental Active Power % Error

CURRENT (A)	PHASE A FUNDAMENTAL ACTIVE POWER % ERROR	PHASE B FUNDAMENTAL ACTIVE POWER % ERROR	PHASE C FUNDAMENTAL ACTIVE POWER % ERROR
0.1	–0.083277815	–0.183226451	–0.124916722
0.25	–0.136602919	–0.176572495	–0.166600027
1	–0.169858451	–0.181575879	–0.162378216
50	–0.114620818	–0.174912544	–0.133137820

8.6 Condition 6: Power Factor = 0, Reactive Power Testing

8.6.1 Voltage THD

Table 34. Condition 6: Phase A Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	9.9643	9.62

Table 35. Condition 6: Phase B Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	9.9818	9.63

Table 36. Condition 6: Phase C Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	9.9470	9.61

8.6.2 Current THD

Table 37. Condition 6: Phase A Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	37.424	36.35
0.25	37.334	36.29
1	37.318	36.28
10	37.295	36.28
50	37.290	36.26

Table 38. Condition 6: Phase B Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	37.413	36.34
0.25	37.345	36.27
1	37.324	36.27
10	37.324	36.27
50	37.315	36.27

Table 39. Condition 6: Phase C Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	37.463	36.38
0.25	37.376	36.29
1	37.346	36.27
10	37.339	36.27
50	37.290	36.26

8.6.3 Fundamental Reactive Power % Error

Table 40. Condition 6: Fundamental Active Power % Error

CURRENT (A)	PHASE A FUNDAMENTAL REACTIVE POWER % ERROR	PHASE B FUNDAMENTAL REACTIVE POWER % ERROR	PHASE C FUNDAMENTAL REACTIVE POWER % ERROR
0.1	–0.199766939	–0.208177200	–0.075012502
0.25	–0.219750949	–0.206494588	–0.080037351
1	–0.175643053	–0.204846365	–0.087521880
50	–0.182311611	–0.207670658	–0.057198126

8.7 Condition 7: THD_{IEC_F} Calculations

8.7.1 Voltage THD

Table 41. Condition 7: Phase A Voltage THD

VOLTAGE (V)	ESTIMATED ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	9.9981	9.65

Table 42. Condition 7: Phase B Voltage THD

VOLTAGE (V)	ESTIMATED ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	10.036	9.78

Table 43. Condition 7: Phase C Voltage THD

VOLTAGE (V)	ESTIMATED ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	10.019	9.60

8.7.2 Current THD

Table 44. Condition 7: Phase A Current THD

CURRENT (A)	ESTIMATED ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	40.367	39.08
0.25	40.257	38.98
1	40.238	38.96
10	40.200	38.94
50	40.198	38.93

Table 45. Condition 7: Phase B Current THD

CURRENT (A)	ESTIMATED ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	40.343	38.97
0.25	40.244	38.93
1	40.215	38.92
10	40.222	38.91
50	40.222	38.92

Table 46. Condition 7: Phase C Current THD

CURRENT (A)	ESTIMATED ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	40.386	39.03
0.25	40.279	38.96
1	40.254	39.04
10	40.238	38.92
50	40.237	38.91

8.8 Condition 8: THDIEEE Calculations Calculation

8.8.1 Voltage THD

Table 47. Condition 8: Phase A Voltage THD

VOLTAGE (V)	ESTIMATED ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	1.01364624	0.93

Table 48. Condition 8: Phase B Voltage THD

VOLTAGE (V)	ESTIMATED ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	1.00962304	0.91

Table 49. Condition 8: Phase C Voltage THD

VOLTAGE (V)	ESTIMATED ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
120	1.00881936	0.92

8.8.2 Current THD

Table 50. Condition 8: Phase A Current THD

CURRENT (A)	ESTIMATED ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	16.28122500	15.25
0.25	16.19982001	15.20
1	16.18372441	15.17
10	16.16602849	15.18
50	16.17648400	15.18

Table 51. Condition 8: Phase B Current THD

CURRENT (A)	ESTIMATED ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	16.28122500	15.24
0.25	16.19982001	15.14
1	16.18372441	15.14
10	16.16602849	15.14
50	16.17648400	15.13

Table 52. Condition 8: Phase C Current THD

CURRENT (A)	ESTIMATED ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.1	16.32160000	15.27
0.25	16.22236729	15.16
1	16.21109169	15.14
10	16.19660025	15.13
50	16.17648400	15.13

9 Design Files

9.1 Schematics

To download the schematics, see the design files at TIDM-THDREADING.

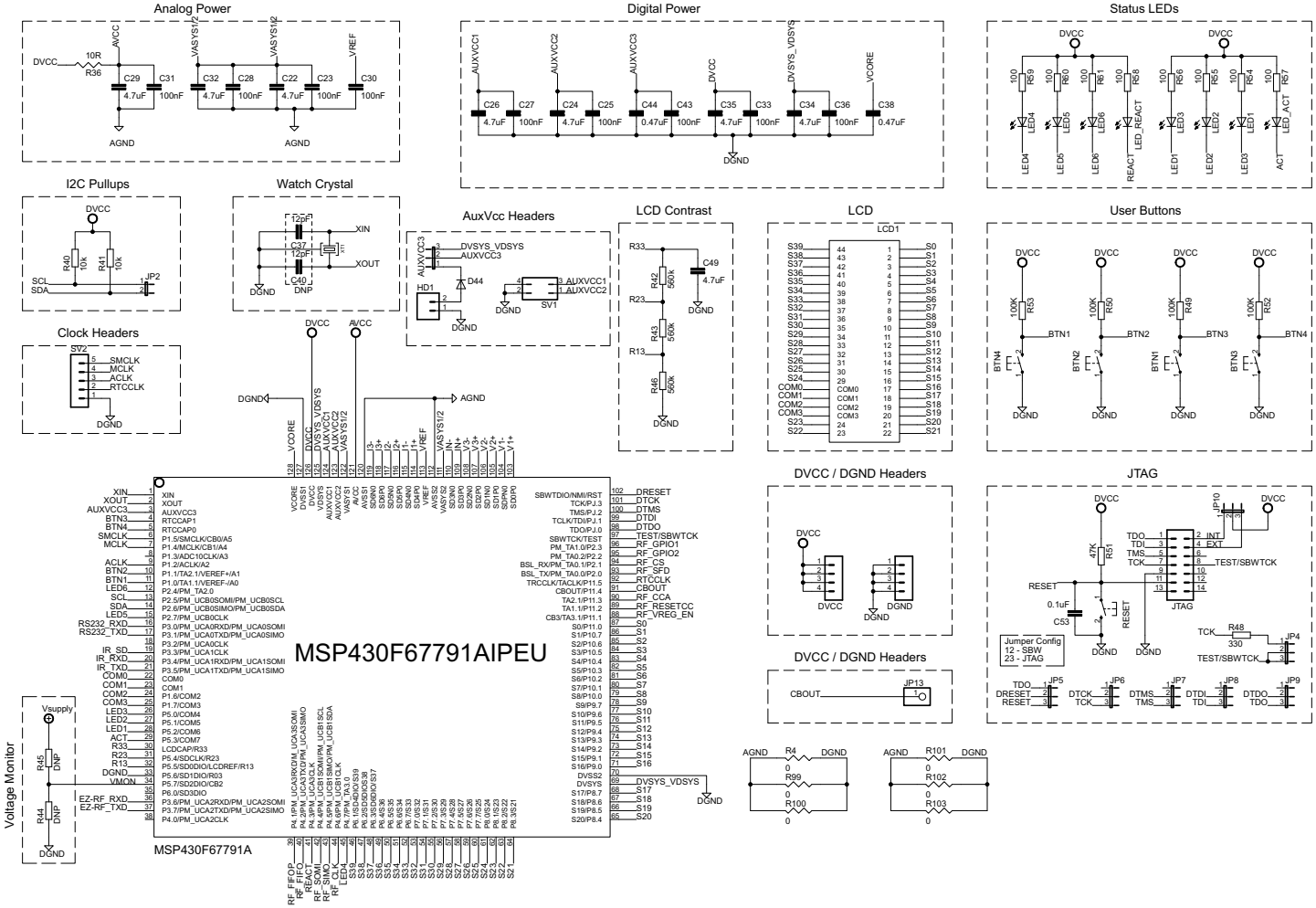


Figure 35. TIDM-THDREADING Schematics Page 1

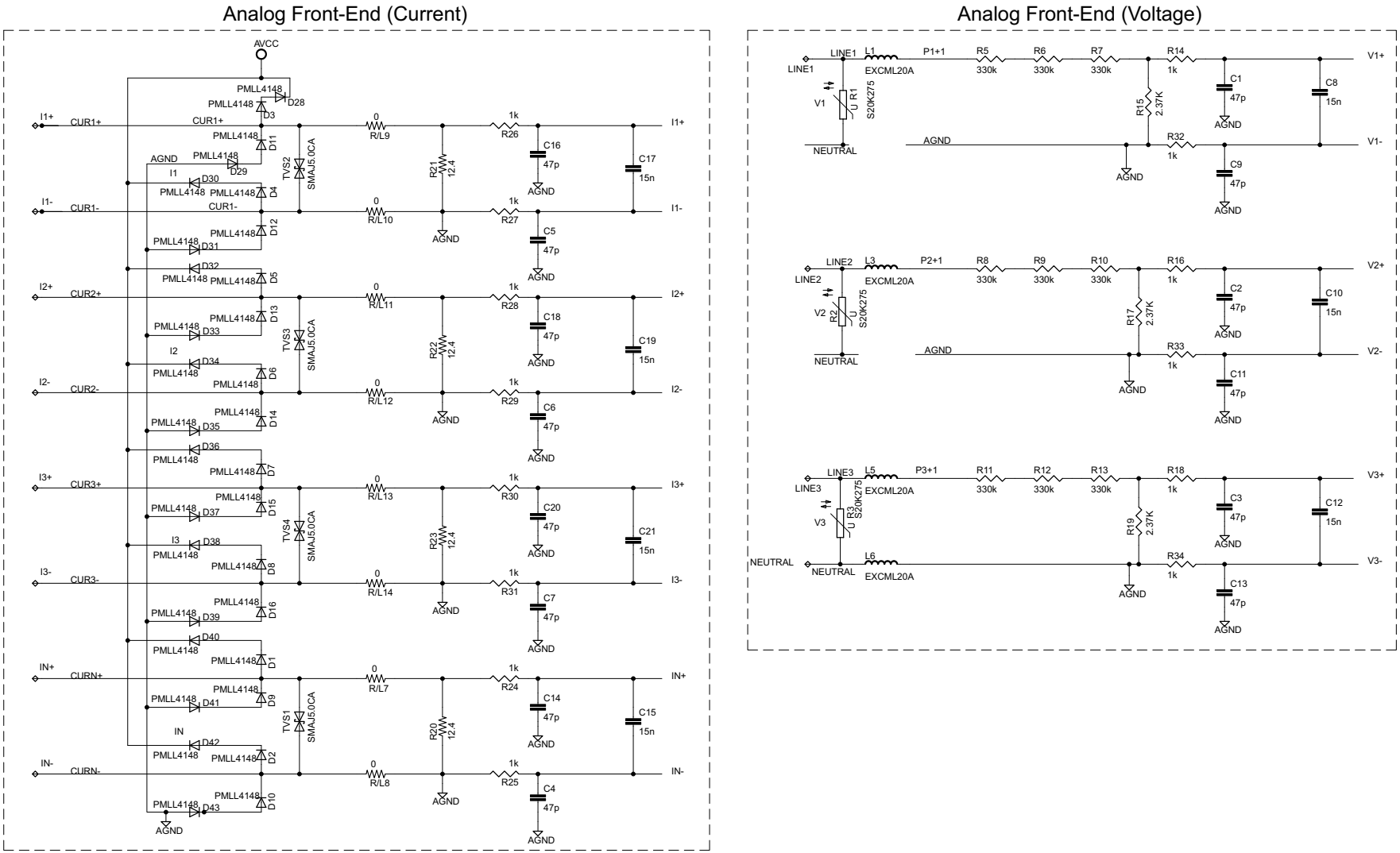


Figure 36. TIDM-THDREADING Schematics Page 2

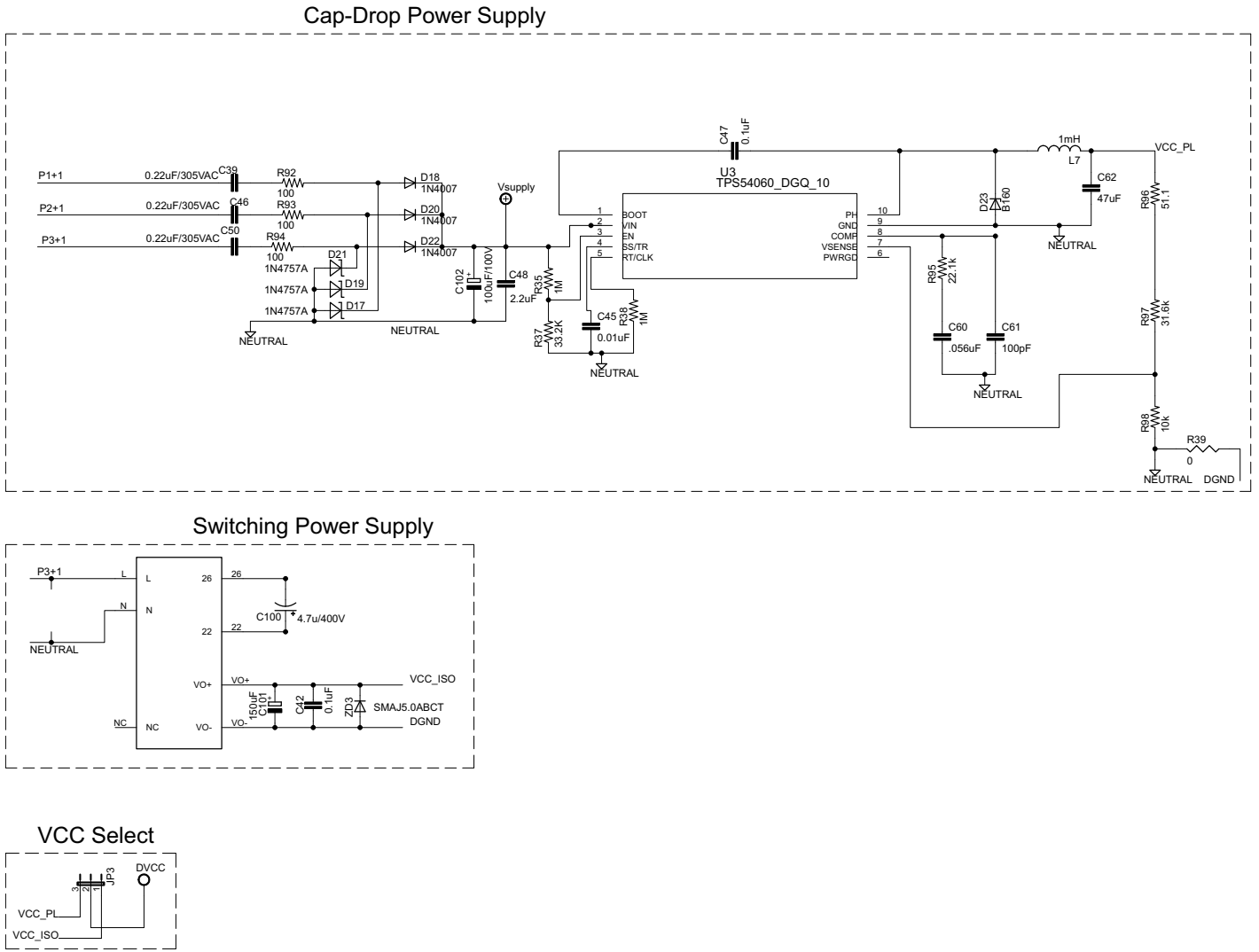


Figure 37. TIDM-THDREADING Schematics Page 3

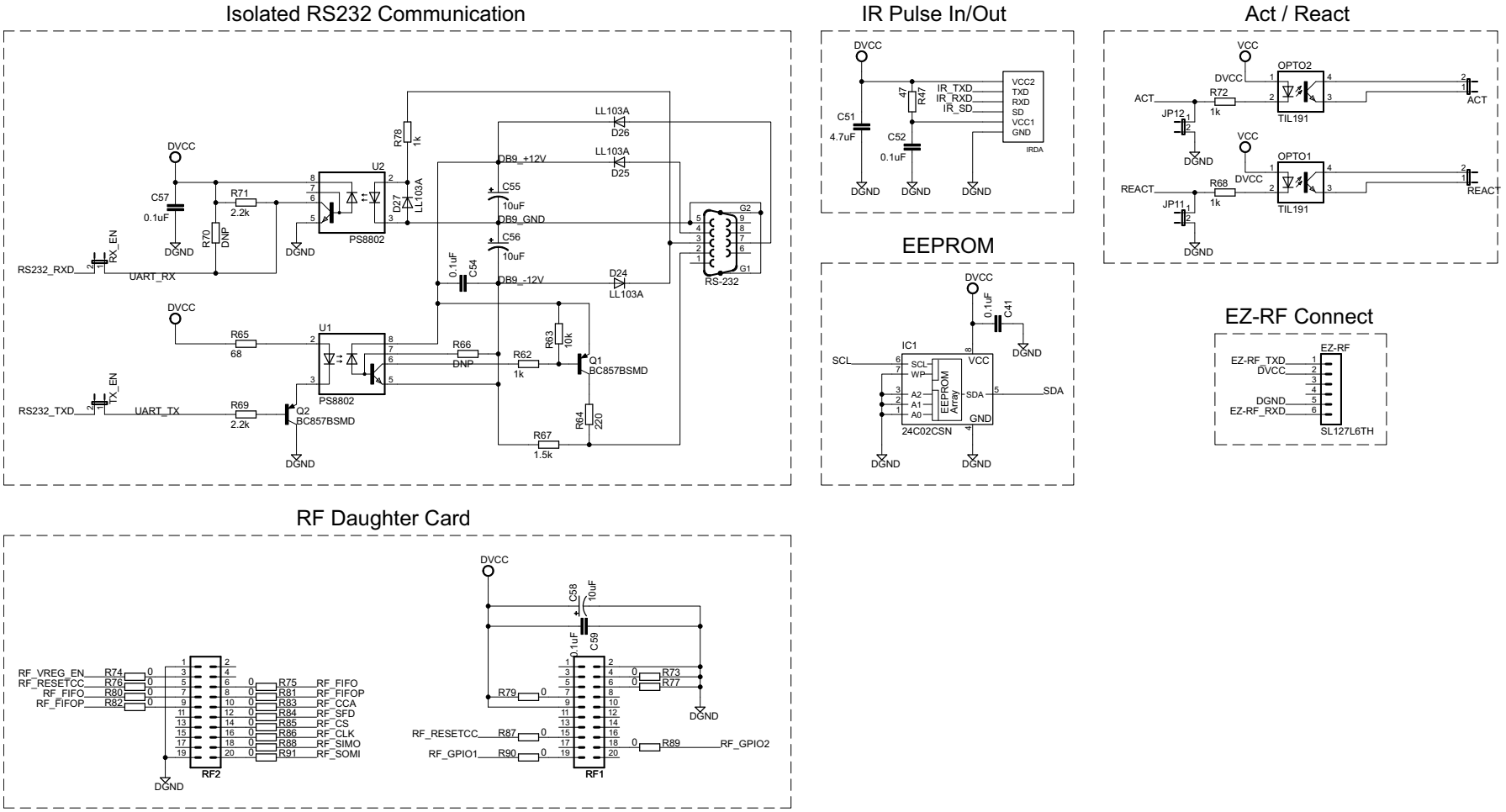


Figure 38. TIDM-THDREADING Schematics Page 4

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDM-THDREADING.

9.3 PCB Layout Recommendations

- Use ground planes instead of ground traces where possible and minimize the cuts in these ground planes (especially for critical traces) in the direction of current flow. Ground planes provide a low-impedance ground path, which minimizes induced ground noise. However, cuts in the ground plane can increase inductance. If there are cuts in the ground plane, they should be bridged on the opposite side with a 0-Ω resistor.
- When there is a ground plane on both top and bottom layers of a board (such as in our EVM) ensure there is good stitching between these planes through the liberal use of vias that connect the two planes.
- Keep traces short and wide to reduce trace inductance.
- Use wide VCC traces and star-routing for these traces instead of point-to-point routing.
- Isolate sensitive circuitry from noisy circuitry. For example, high voltage and low voltage circuitry should be separated.
- Use decoupling capacitors with low effective series resistance (ESR) and effective series inductance. Place decoupling capacitors close to their associated pins.
- Minimize the length of the traces used to connect the crystal to the microcontroller. Place guard rings around the leads of the crystal and ground the crystal housing. In addition, there should be clean ground underneath the crystal and placing any traces underneath the crystal should be prevented. Also, keep high frequency signals away from the crystal.

9.3.1 Layer Plots

To download the layer plots, see the design files at TIDM-THDREADING.

9.4 CAD Project

To download the CAD project files, see the design files at TIDM-THDREADING.

9.5 Gerber Files

To download the Gerber files, see the design files at TIDM-THDREADING.

10 Software Files

To download the software files, see the design files at TIDM-THDREADING.

11 About the Author

MEKRE MESGANAW is a Systems Engineer in the Smart Grid and Energy group at Texas Instruments, where he primarily works on grid monitoring customer support and reference design development. Mekre received his bachelor of science and master of science in computer engineering from the Georgia Institute of Technology.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2016) to A Revision	Page
• Changed sampling frequency of "4.096 samples per second" to "4096 samples per second"	8

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