# TI Design TIDA-00720

# *Power Cycling Reference Design to Extend Battery Life Using an Ultra-Low IQ LDO and Nano Timer*

## TI Designs

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## Design Resources

| | |
|---|---|
| TIDA-00720 | www.ti.com/tool/tida-00720 |
| LP38693 | www.ti.com/product/LP38693 |
| TPL5111 | www.ti.com/product/tpl5111 |
| Other TI Designs | TIDA-00484 |

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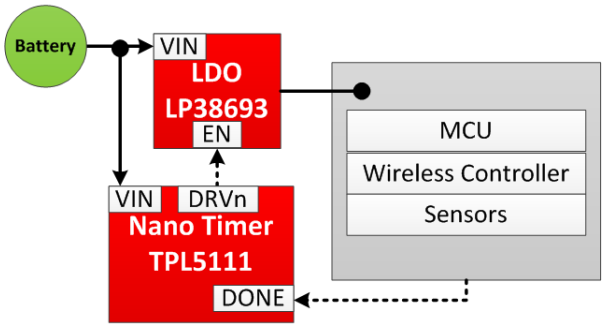
## Block Diagram



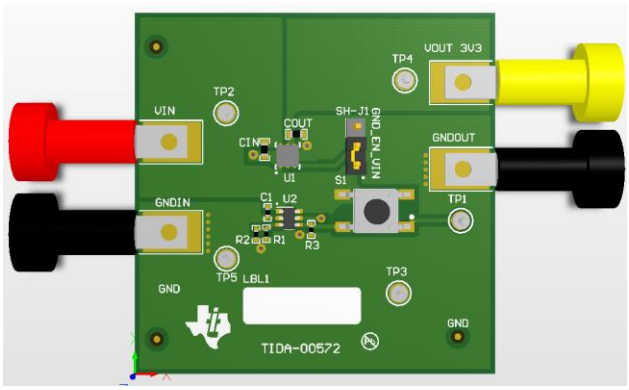

## Design Features

- Prolonged battery life by using power cycling. Sleep mode has an ultra-low quiescent
- Time intervals can be adjusted from 10ms to 2h with just an external resistor
- Ultra-low noise and ripple free 1.8V output voltage
- Fast power-up voltage supply. Output power supply is disabled as soon as the MCU sends a process completion signal.
- Cost efficient solution with only a few compensation components
- TIDA-00720 provides design guide and design files of the power management solution.

## Featured Applications

- Low power battery applications
- Sensor-data acquisition systems
- Home or office security monitoring
- Building automation

## Board Image



# 1 System Description

The TIDA-00720 reference design shows a method to extend battery life by power cycling. The power cycling concept consist in time interval period that enables the power management devices for just enough time for the microcontroller to execute the program, transmit data or collect data. Some of the MCUs have sleep modes with low stand-by currents, but the power management devices will continue to dissipate power if they are left enabled. The current leakage is higher during the enabled mode and will add up to the total power waste during the MCU sleep cycles.

The periodic time cycles are generated with a low stand-by current Nano-timer (TPL5111). At the beginning of the time cycle ($T_0$) the TPL5111 sends a high signal to the enable (EN) pin of a low dropout (LDO) linear regulator (LP38693). The LDO will enable its output to power the system.
At the end of the MCU program execution a signal high will send by the MCU to the DONE pin of the TPL5111; then the TPL5111 will pull low the signal at the LDO EN pin to disable the output voltage and begin the ultra-low quiescent current disable mode for the reminding of the programed power cycle, if the MCU does not finishes the program execution during the time interval period ($t_{IP}$) minus 50ms the Nano-clock will disable the LDO and restart the power cycle ($T_0$) after 50 ms.
Figure 1 shows a graphical representation of the process explained above.

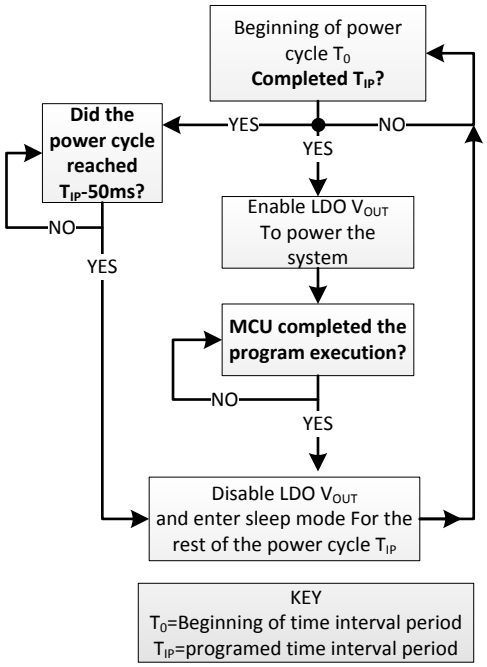



**Figure 1 Power Cycle Process**

One of the advantages of the LP38693 LDO is the ultra-low quiescent current, when the output voltage is disabled the quiescent current ($I_Q$) is basically zero ($I_{Q(VEN<0.4V)}$ < 1µA). An additional advantage is the fast power-up from sleep mode to enable mode.

This design is ideal for systems that operate for various years without replacing the battery; these systems do not need to run constantly instead they operate in periodic intervals of seconds, minutes or even an hour in between operating time.
These applications are sensor monitoring systems as water flow meters, temperature or humidity meters, heat meters, gas meters, motion monitoring systems and many more.

The TIDA-00720 reference design provides test data, design guide and Gerber files; all the files can be obtain from the design folder at www.ti.com/tool/TIDA-00720

## 2 Block Diagram

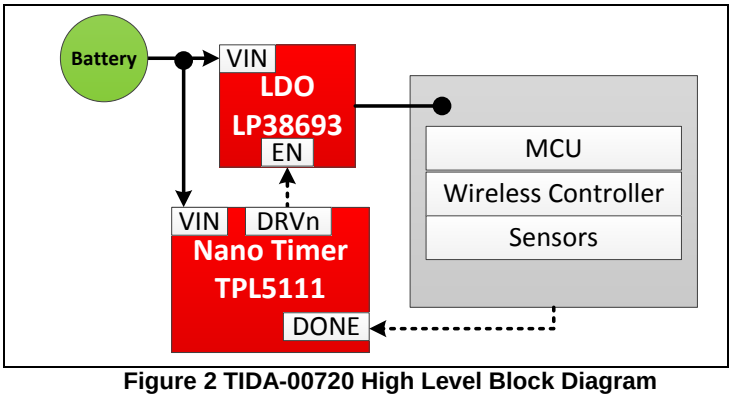



**Figure 2 TIDA-00720 High Level Block Diagram**

The **Figure 2** shows the comprehensive block diagram of the TIDA-00720 design. The red blocks represent the main components of this document.

- LP38693 LDO
- TPL5111 Nano Timer

### 2.1 LP38693 Low Dropout CMOS Linear Regulators Stable with Ceramic Output Capacitors

The LP38693 are designed to meet the requirements of portable, battery-powered digital systems providing an accurate output voltage with fast start-up. When disabled via a low logic signal at the enable pin (EN), the power consumption is reduced to virtually zero

The LP38693 perform well with a single 1-µF input capacitor and a single 1-µF ceramic output capacitor.

- 2% Output Accuracy (25°C)
- Precision (Trimmed) Bandgap Reference
- Ensured Specs for –40°C to 125°C
- 1-µA Off-State Quiescent Current
- Thermal Overload Protection
- Fold back Current Limiting
- Ground Pin Current: 55 µA (typical) at full load
- Enable Pin (LP38693)

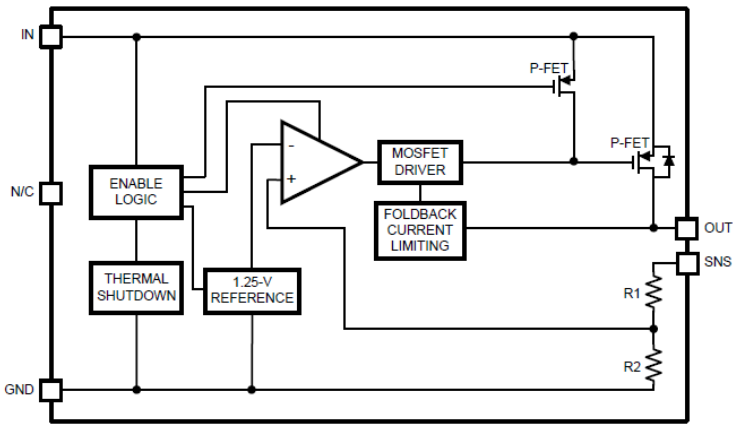



**Figure 3 LP38693 Functional Block Diagram**

## 2.2 TPL5111 Nano-Power System Timer for Power Gating

The TPL5111 is a timer with power gating feature. It is ideal for use in power-cycled applications and provides selectable timing from 100 ms to 7200 s.
When configured in timer mode (EN/ONE_SHOT= HIGH) the TPL5111 periodically asserts a DRVn signal to an LDO or DC-DC converter that is used to turn on a microcontroller. If the microcontroller replies with a DONE signal within the programmed time interval (< tDRVn) the TPL5111 de-asserts DRVn. Otherwise the TPL5111 asserts DRVn for a time equal to tDRVn.
The TPL5111 can also work in a one shot mode (EN/ONE_SHOT= LOW). In this mode the DRVn signal is asserted just one time at the power on of the TPL5111. If the µC replies with a DONE signal within the programmed time interval (< tDRVn) the TPL5111 de-asserts DRVn. Otherwise the TPL5111 asserts DRVn for a time equal to tDRVn.

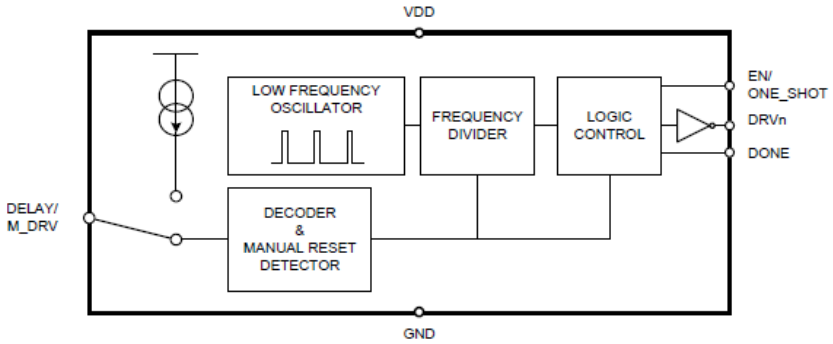



**Figure 4: TPL5111 Functional Block Diagram**

# 3 Design Implementation Guidelines

## 3.1 LP38693 Design Guidelines

The LP38693 was selected for its disabled mode low quiescent current, fast turn on time and easy to implement device in addition to the mentioned benefits the LP38693 has the inherit benefits of LDOs regulators of low output noise and high input power supply ripple rejection. This section mentions the 3.1 LP38693 design consideration for this application.

### 3.1.1 Enable and Disable Mode

The enable and disable modes are controlled by the signals form the TLV5111 pin 5 (DRVn). A High signal at the EN pin (3V @ 6V input voltage) will enable the output and vice versa a low signal (typically 0.4 V) will disable the output voltage.

### 3.1.2 Compensation Components

The LP38693 has a fixed 1.8V output voltage, which means that it does not requires a feedback resistive network. The only external components are the input and output capacitors.

***Output capacitors***

The LP38693 works with very small ceramic output capacitors. A 10-µF ceramic capacitor (temperature types Z5U, Y5V or X7R/X5R) with ESR between 5 mΩ to 500 mΩ is suitable for the application.

***Input Capacitors***

An input capacitor is required for stability. A 10 µF capacitor is placed close to the IN pin with a distance no more than 1 cm

## 3.2 TPL5111 Design Guidelines

The TPL5111 was selected for its ultra-low current consumption of 35 nA and programmable duty cycles. This section talks about the TPL5111 design considerations for this application.

### 3.2.1 Programmable Time Internal

The power cycles can be programed by means of a resistor ($R_{EXT}$) from the DELEY/M_DRV pin3 and ground. Equation 1 is used to select the resistors values. The equation below provides a theoretical value of 6.79 Ω for 2 second interval period, the closes real value is 6.788 kΩ by utilizing 12.4 kΩ and 15 kΩ in parallel. The time interval can be adjusted from 10 milliseconds to 2 hours

$$R_{EXT} = 100\left(\frac{-b+\sqrt{b^2-4a(c-100\,T)}}{2a}\right) \quad \textbf{Equation 1}$$

Table 1 shows an example of parallel resistor to set common time intervals. Higher current consumption can be achieved with longer sleep time intervals

**Table 1 Common Time Intervals**

| TIME INTERVAL | CALCULATED RESISTANCE (kΩ) | PARALLEL of TWO 1% TOLERANCE RESISTORS,(kΩ) |
|---|---|---|
| 1min | 22.02 | 40.2 // 48.7 |
| 10min | 57.44 | 107.0 // 124.0 |
| 30min | 92.43 | 182.0 // 187.0 |
| 60min | 124.91 | 221.0 // 287.00 |

During the on time of the time interval a high signal will be generated at DRVn equal to the programmed time interval period ($t_{IP}$) minus 50 ms. The $t_{IP}$ is shorter if a DONE signal is received from the MCU before $t_{IP}$ - 50 ms. If the DONE signal is not received within $t_{IP}$ - 50 ms, the DRVn signal will be LOW for the last 50 ms of $t_{IP}$ before the next cycle starts.

### 3.2.2 Startup up power cycle

During startup the TPL5111 does a onetime measurement of the resistance ($R_{EXT}$), during this measurement a constant current is temporarily flowing into the external resistor, the current is typically 200 µA

### 3.2.3 DONE Signal

As soon as the microcontroller finalizes the process a single will be send to the DONE pin 4 of the TLP5111. The TPL5111 recognizes a valid DONE signal as a low to high transition; if two or more DONE signals are received within the time interval, only the first DONE signal is processed. The minimum DONE signal pulse length is 100 ns. When the TPL5111 receives the DONE signal it asserts DRVn logic LOW.

## 3.3 System Parameters

| PARAMETER | VALUE | NOTES |
|---|---|---|
| Input Voltage Range ($V_{IN}$) | 1.88V to 5.5V @ 0.1A load<br>2.23 to 5.5 @ 0.5A load | $V_{IN}$ is limited by the Nano-timer maximum input and LDO dropout voltage |
| Output voltage ($V_{OUT}$) | 1.8V | The LP38693-ADJ can be used for other voltage options |
| Intermittent period ($T_{IP}$) | 2 seconds | $T_{IP}$ can be adjusted in a range of 10ms to 2h |
| Output Current | 500 mA | LDO maximum output voltage |
| Disabled mode quiescent current | ~77 nA | LDO + Nano timer |
| Output noise density | 0.7 µV/√Hz | BW = 10 Hz to 10 kHz |

### 3.3.1 Enabled and Disabled Mode Current Consumption

The Table 2 and Figure 5 show a comparison between current consumption during sleep mode and active mode. The measurements in this section were made with the Agilent 34410A Multimeter at room temperature and without any loads connected. The values are the average current of multiple sleep and active cycles. The nominal input voltage was 3.3V

**Table 2 Active Mode and Sleep Mode Quiescent Current**

| DEVICE | ACTIVE MODE | SLEEP MODE |
|---|---|---|
| LP38693 | 100 µA | 40 nA |
| TPL5111 | 37 nA[1] | 37 nA |
| **Total** | 100 µA | 77 nA |

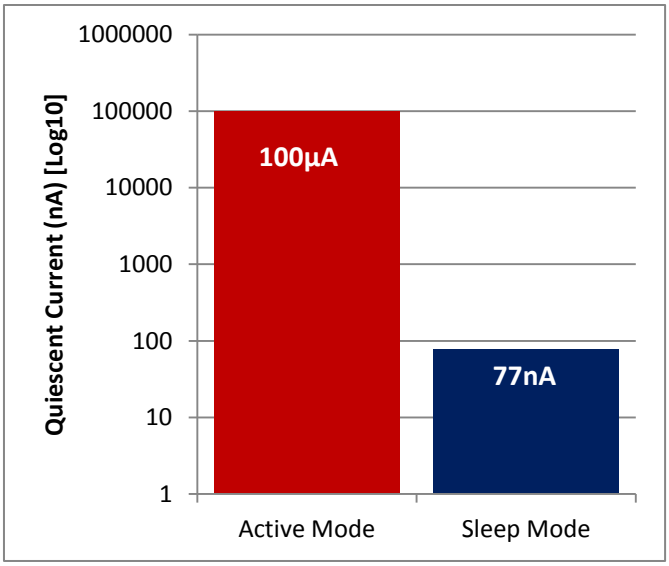



**Figure 5: Comparison between Sleep Mode and Active Mode (no load)**

[1] This value does not include the current needed to digitalize the external resistance ($R_{EXT}$). $R_{EXT}$ digitalization = (200µA•50µs)

### 3.3.2 Battery Life Approximation

The **Equation 2** can be used to approximate the battery life using the power cycling method. The equation does not take into account battery shelf life, but it does include a theoretical battery derating factor to take into account battery self-discharge and temperature changes.

**Equation 2:**

$$\text{Battery life (years)} = \left(\frac{\text{Battery capacity [mAh]} \bullet t_{TOTAL}}{(I_S \bullet t_S + I_{REXT} + I_A \bullet t_A}\right) \bullet \frac{1\ \text{year}}{8760\text{h}} \bullet (100\% - \text{DF}[\%])$$

All currents are in milliamps (mA) and time is in seconds (s)

## Battery life parameters

$I_A$ [mA]: --------- Total active mode current consumption = $I_{LP38693\_ACTIVE}$ + $I_{TPL5111\_ACTIVE}$ + $I_{SYSTEM}$
$T_A$[s]: ---------- Active mode duration
$I_S$ [mA]: --------- Sleep mode current consumption = ~0.077mA
$T_S$[s]:---------- Sleep mode duration minus $t_{R\_EXT}$
$I_{R\_EXT}$: ---------- is a constant 0.01 value to take into account the current required to digitalize ($R_{EXT}$)
$T_{TOTAL}$[s]: -------- $T_A$[s] + $T_S$[s] + $t_{R\_EXT}$[s] = $T_{IP}$ = Programed Intermittent period
DF =---------- Derating factor, the typical derating factor is 15%

**Table 3** Table 3 shows a comparison of the estimated battery life when taking advantage of the low sleep mode current of the TIDA-00720 and regular stand by current consumption

**Table 3 Battery Life with and without TIDA-00720 Method**

| PARAMETER | WITH TIDA-00720 METHOD | WITHOUT TIDA-00720 METHOD |
|---|---|---|
| batt [mAh] | 240 | 240 |
| $I_A$ [mA] | 20 | 20 |
| $T_A$[s] | 0.03 | 0.03 |
| $I_S$ [mA] | **(sleep mode) 0.00007** | **(no sleep mode) 0.1** |
| $T_S$[s] | 119.97 | 119.97 |
| $T_{TOTAL}$[s] | 120 | 120 |
| DF % | 0.85 | 0.85 |
| **Battery life (years)** | **4.6** | **0.22** |

# 4 Test Setup

**Note**

The TIDA-00720 board is not available for purchase, however the an EVMs for LP38693 and TPL5111 can be ordered at **www.ti.com**

Before applying power to the TIDA-00720 board, all external connections should be verified. The external power supply must be turned off before being connected. Confirm proper polarity to the $V_{IN}$ and $V_{OUT}$ terminals before turning the external power supply on.

## 4.1 Test Equipment

The following table shows the test equipment used to collect test data.

**Table 4 Test Equipment**

| TEST EQUIPMENT | PART NUMBER |
|---|---|
| Oscilloscope | Agilent DPO4014B |
| DC voltage supply | Agilent E3631A |
| Multimeter | Agilent E34401A |
| Network Analyzer | Agilent E5061B ENA |

# 5 Test Data

## 5.1 Power Cycling

Figure 6 shows the power cycling when the DONE signal is asserted, if for some reason the MCU does not completes the program execution the LDO will remain enable for the programed time interval minus 50 ms.

The DONE signal was generated using a function generator triggered externally by the DRVn. 50ms after the DRVn signal is detected the function generator sends a 1.8V square pulse to the DONE pin of the TPL5111.

**Test parameters**
$V_{IN}$ 4.5V
Load= 35 ohms
Vout = 1.8
Intermittent time: 2s
Active time: 50mS

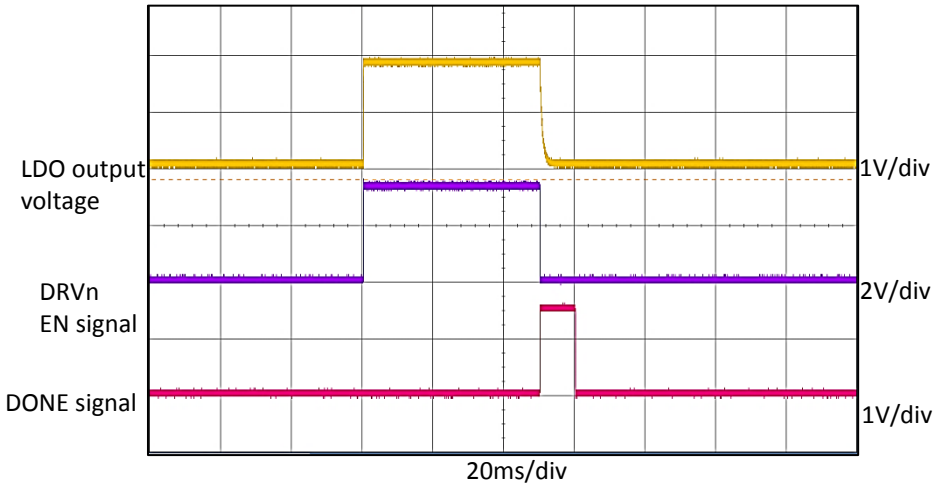



**Figure 6 DONE Signal Received**

Figure 7 shows the power cycling when the DONE signal is note generated

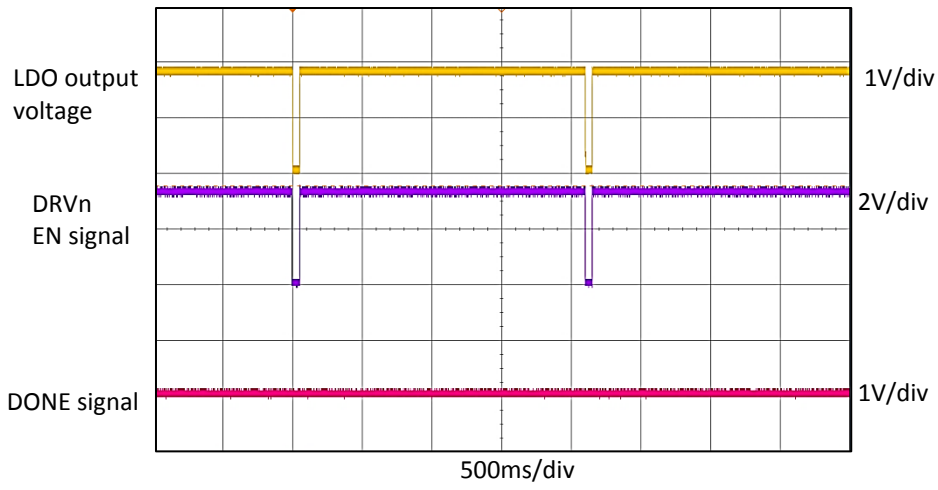



**Figure 7 DONE Signal Not Received Within Programed Time Interval**

## 5.2 Power-up time

Figure 8 shows the TPL5111 DRVn signal as the LP38693 enable signal. The LP38693 takes <100 µs to reach 95% of the nominal output voltage.

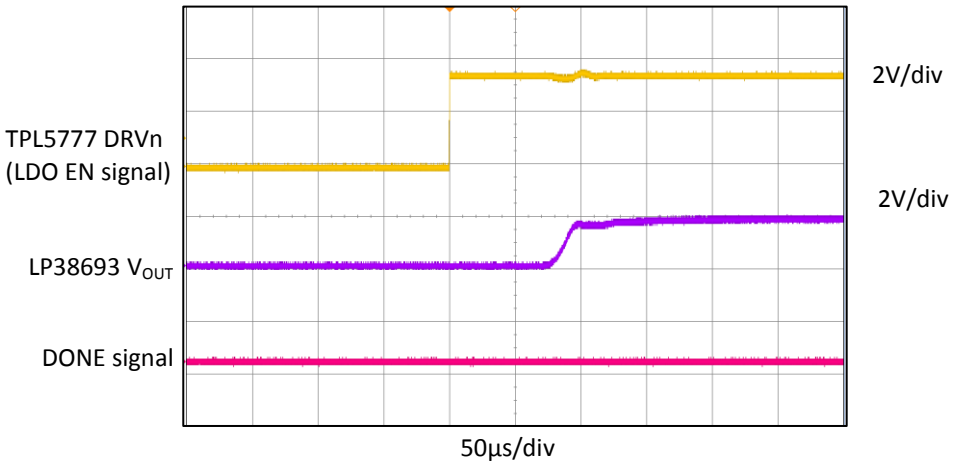



**Figure 8 TPL38693 Output Voltage Power-up Time**

## 5.3 Line and Load Transients response

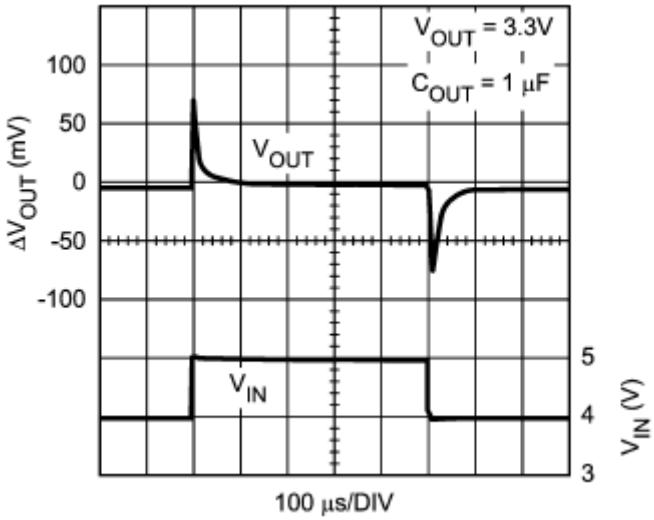



**Figure 9: Line Transient Response**

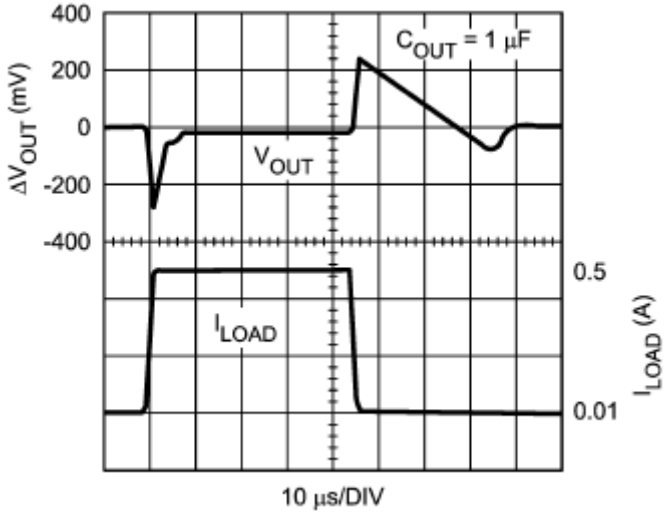



**Figure 10: Load Transient Response**

## 5.4 Power supply ripple rejection

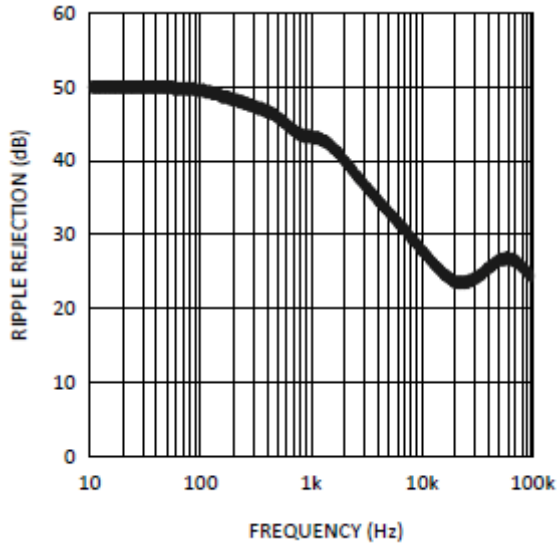



**Figure 11: Comparison between PSRR and Frequency**

## 5.5 Noise Density

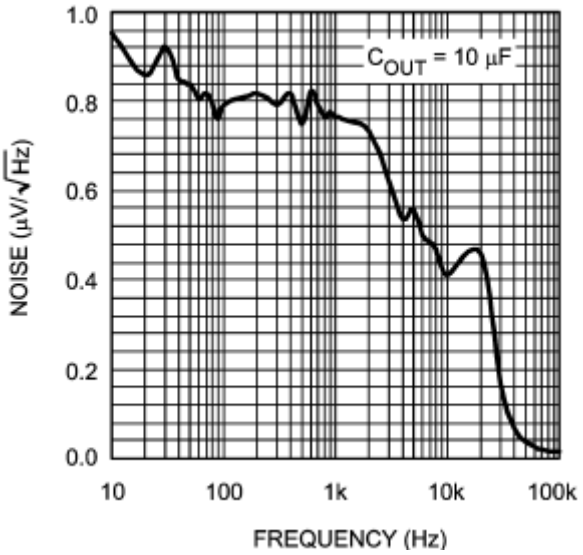



**Figure 12: Comparison between Noise and Frequency**

## 5.6 TPL5111 Supply Current Vs Supply Voltage

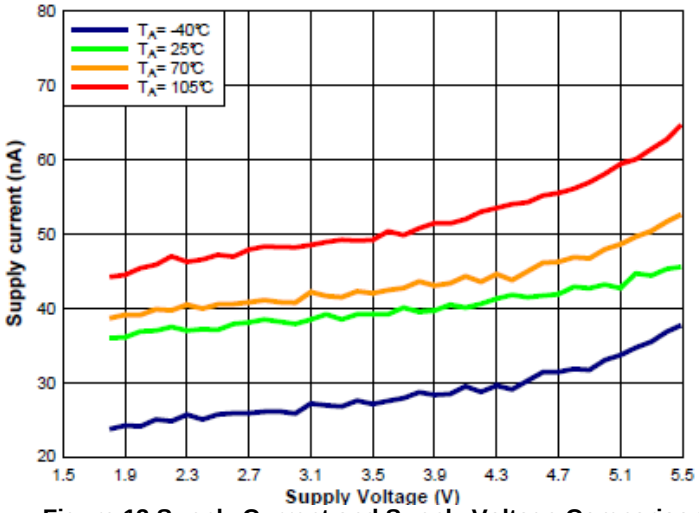



**Figure 13 Supply Current and Supply Voltage Comparison**

## 5.7 TPL5111 Comparison between Supply Current and Time

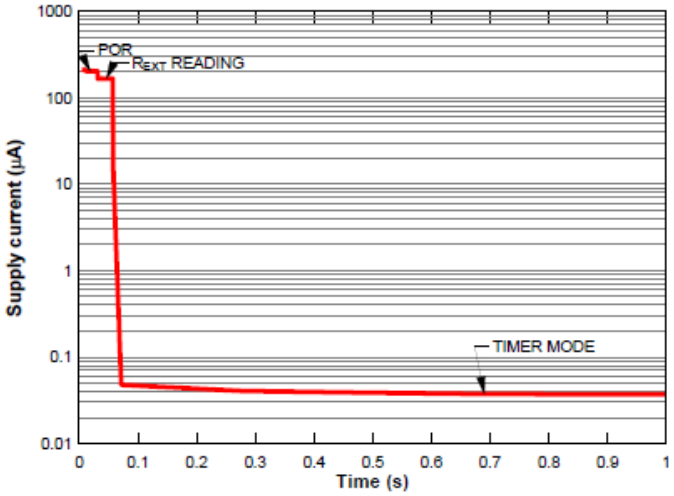



**Figure 14 Supply Current and Time Comparison**

## Design Files

### 5.8 Schematics

To download the Schematic, see the design files at http://www.ti.com/tool/TIDA-00572

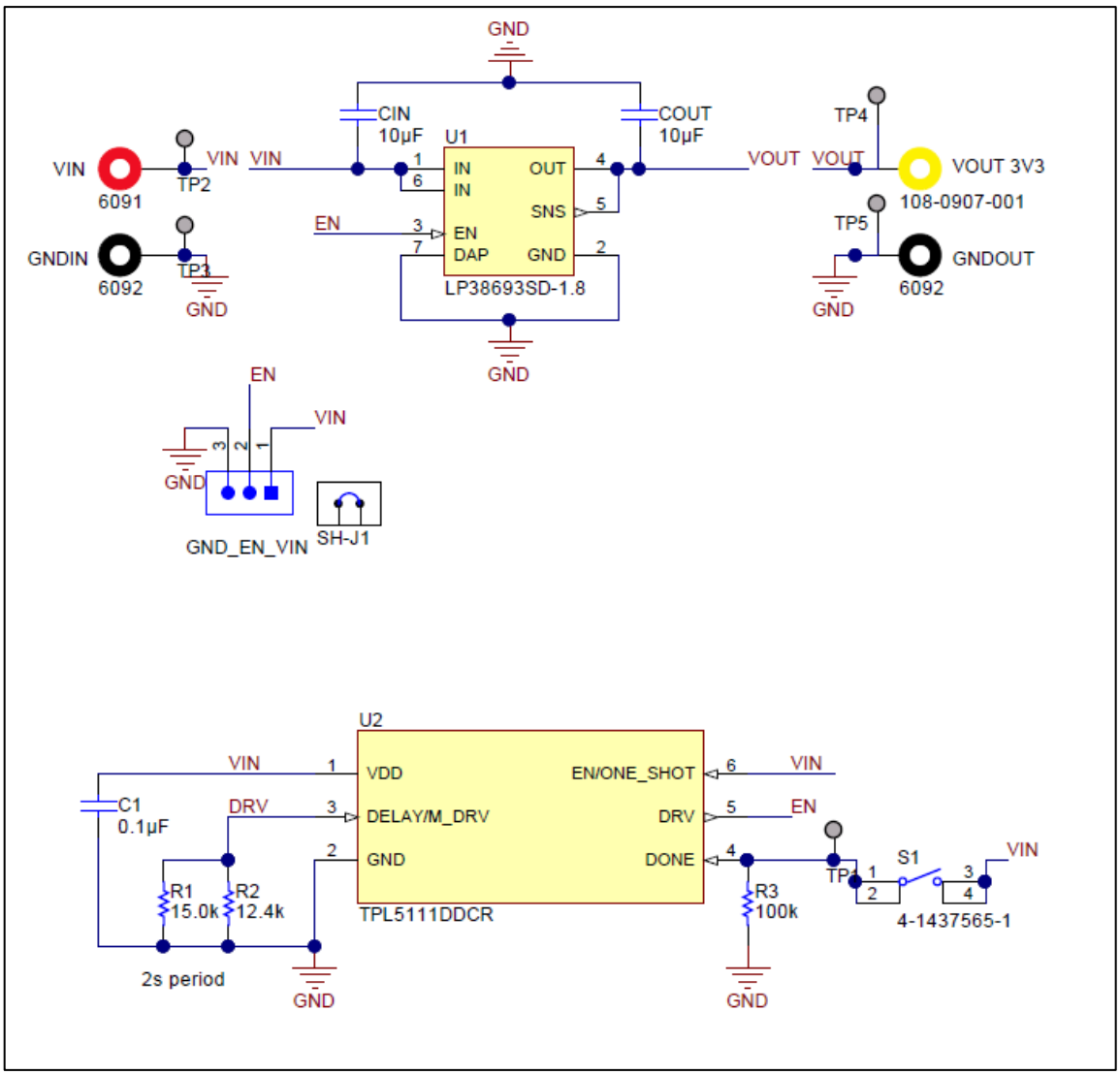



**Figure 15: TIDA-00720 Evaluation Board**

### 5.8.1 Altium Project

The Altium project files can be downloaded at the link below.
http://www.ti.com/tool/TIDA-00599

- Gerber and NC-drills
- Bill of Materials (BOM)
- Assembly Drawings

## 5.9 PCB Layout Recommendations

- As a rule of thumb avoid connections using long trace lengths and narrow trace widths. These will add parasitic inductances and resistance that resulting in inferior performance especially during transient conditions
- Avoid any sharp corners. Electric fields tend to build up on corners, increasing EMI coupling.
- The input and output capacitor must be place as close as possible to the components input and output pin
- Place the inductor and compensation components close to the feedback pin to minimize the current loop.
- Ensure low impedance path for grounds and return paths

### 5.9.1 Layout Guidelines

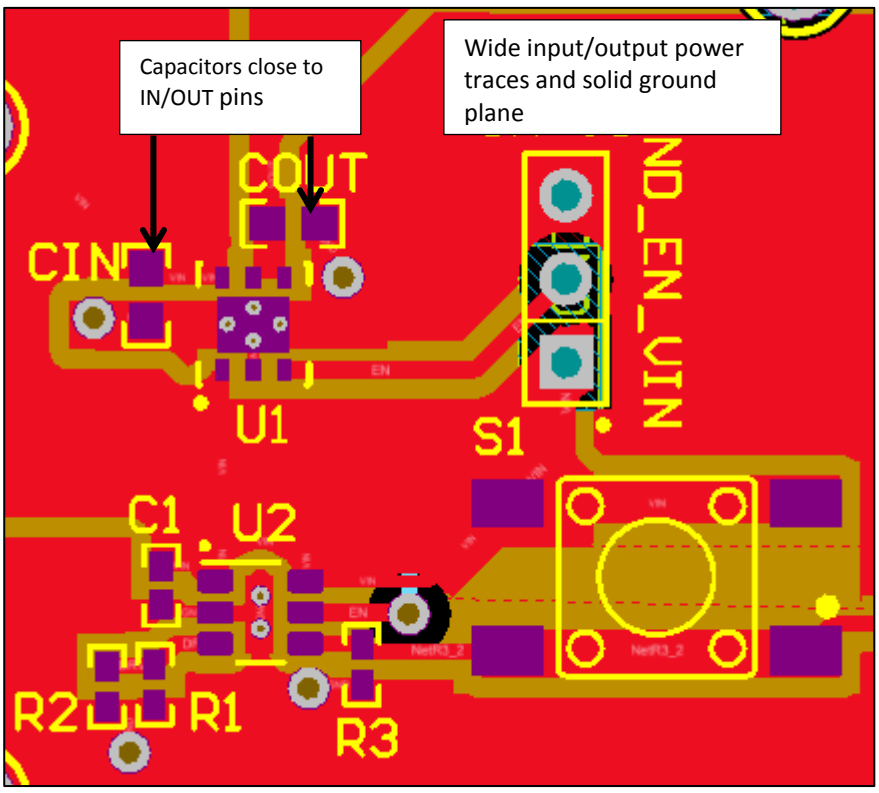



**Figure 16: TIDA-00720 Layout Guidelines**

## 6 References

1. Texas Instruments TI Designs: Humidity and Temperature Sensor Node for Sub-1GHz Star Networks Enabling 10+ Year Coin Cell Battery Life, http://www.ti.com/tool/TIDA-00484

## 7 Terminology

TI Glossary: SLYZ022 This glossary lists and explains terms, acronyms, and definitions.

## 8 About the Author

**Antony Pierre Carvajales**

Antony is a Systems and Applications Engineer at Texas Instruments Incorporated. Antony is responsible for developing reference design solutions for the mobile devices power RF (MDP-RF) power group. Antony brings to this role experience in system-level analog, mixed-signal, and power management design. Mr. Carvajales earned his bachelor of science (BS) in electrical engineering from the Florida International University in Miami FL. Antony is a member of the Institute of Electrical and Electronics Engineers (IEEE) and the Society of Hispanic Professional Engineers (SHPE).

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Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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