TI Designs

Flexible High Current IGBT Gate Driver With Reinforced Digital Isolator

TI Designs

This reference design is an isolated IGBT gate driver with bipolar gate voltages. This design is intended for driving high power IGBT's requiring high peak gate currents up to 40 A. TI's NexFET power blocks scale in this range with the same package to enable a single design to be used for multiple drive platforms with different power ratings. The ISO7842 Digital Isolator is used to achieve reinforced isolation with transient surge rating of 8-kV and 50-kV CMTI. The design incorporates DESAT protection using fast transient response comparator TLV3201. The DESAT detection threshold and the soft turn-off time are configurable. The design can interface with PWMs from 3.3-V and 5-V MCUs along with fault, reset, and UVLO signals.

Design Resources

TIDA-00448	Design Folder
ISO7842	Product Folder
TPS51604	Product Folder
CSD87353Q5D	Product Folder
TLV3201	Product Folder
TPS3700	Product Folder
TPS7A4201	Product Folder
CSD17313Q2	Product Folder
SN74LVC1G125	Product Folder

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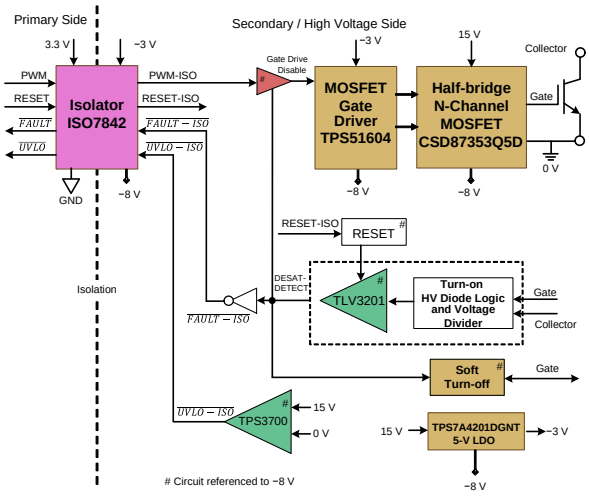
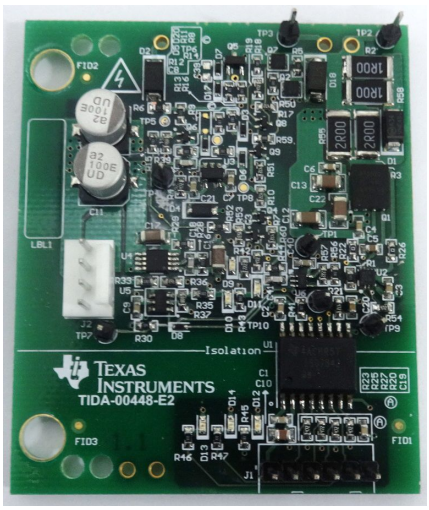
Design Features

- Designed for Low Voltage Drives With Input Supply up to 600-V AC
- Designed for Medium Power IGBT Modules With Rated Current up to 1000 A and Q_g up to 10 µC
- Bipolar (15 V and –8 V) Gate Drive Voltages
- Common MOSFET Footprint Enables to Choose Parts with 25-A, 32-A, and 40-A Rating for Flexible Source and Sink Currents
- Programmable DESAT and Soft Shutdown Feature
- 8-kV Reinforced Isolation and CMTI Greater Than 50 kV/µs
- Undervoltage Lockout (UVLO) on 15-V Rail
- Input PWM Signals Compatible with 3.3-V and 5-V MCUs
- Feedback Signals for Fault and UVLO and Control Signal to Reset Latched Fault State

Featured Applications

- Variable Speed AC Drives
- Servo Drives
- Solar Inverters
- Uninterruptible Power Supplies





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1 Introduction

This reference design is a reinforced isolated IGBT gate driver with bipolar gate drive voltages. This design is intended for driving high power IGBTs requiring high peak gate currents up to 40 A. TI's NexFET power blocks, which scales in this range with same package, enable single design to be used for multiple drive platforms with different power ratings. The ISO7842 Digital Isolator provides reinforced isolation with a transient surge rating of 8-kV and 50-kV CMTI. The design incorporates DESAT protection using fast transient response comparator TLV3201. The DESAT detection threshold and the soft turn-off time are configurable. The design can interface with PWMs from 3.3-V and 5-V MCUs along with fault, reset, and UVLO signals.

This isolated discrete gate driver is designed for low voltages and medium power drives, operating from a 3-phase AC supply up to 600 V. Medium power drives rated up to 250 kW can have IGBT modules with gate charges up to 10 µC, necessitating high peak currents to turn on and off the IGBT. Gate driver ICs have a limited peak current capability; typical values are 2.5 A for source and 5 A for sink. This reference design, built using discrete components with scalable gate drive currents up to 40 A, is suitable in such scenarios. Additionally, using a discrete gate driver allow the designer to have a configurable DESAT threshold and soft turn-off of time, which can be adjusted according to the characteristics of the IGBT module in use.

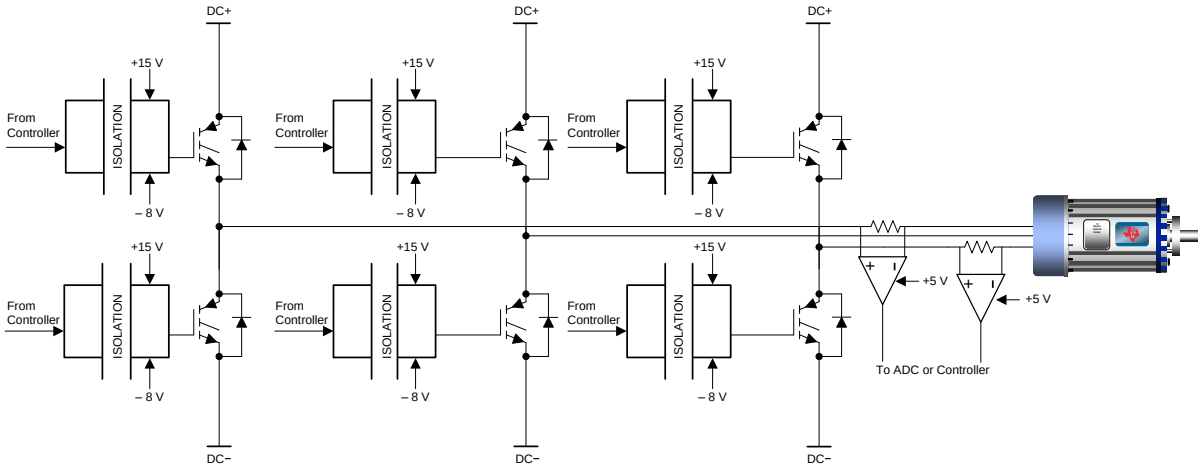

Figure 1. 3-Phase Inverter With Isolated Gate Driver

Figure 1 shows a typical three-phase inverter with six IGBTs. The inverter generates a pulse width modulated waveform by switching between the positive and negative voltage of the DC bus by the control of the IGBTs.

The IGBT is driven with bipolar voltages of 15 V to turn on and –8 V to turn-off with respect to the emitter of the IGBT. However, the emitter of the top IGBT is switching to the DC positive voltage and DC negative. An effective way to apply the turn-on and turn-off voltage is to use isolated 15 V and –8 V and to reference this to the emitter of the IGBT. Each IBGT gate driver board requires an external 15-V and –8-V power rail and provides galvanic isolation between input and output of the gate driver. The reference design has DESAT and undervoltage lockout for reliable operation of the inverter. The V_{CE} of the IGBT is monitored during ON time to detect overcurrent conditions, which will make the IGBT get into a linear mode of operation. On detecting V_{CE} higher than a DESAT threshold, the IGBT is shut off slowly (soft turn-off) to limit the V_{CE} overshoot, which otherwise may damage the IGBT.

The signals to and from the gate driver can be interfaced with a 3.3-V or 5-V MCU. Signals include PWM, fault, and undervoltage detect to indicate the state of the gate driver and RESET control signal to bring the gate driver out of latch after the fault state.

The testing of the gate drive was done with CM450DX-24S1 IGBT module from Mitsubishi. The form factor of the board was chosen to fit on top of this IGBT module.

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2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	
Gate drive	Voltage	15-V and –8-V bipolar drive voltage[1]
	Currents	Option of 25 A , 32 A , 40 A Sink and source currents
Protection	Configurable DESAT detection threshold with latched turn-off of the gate driver	
	Configurable soft turn-off time	
	UVLO on 15-V rail with option to disable the gate drive	
Isolation	Working voltage, V_{IORM}	2-kV peak
	Transient Over Voltage V_{IOTM}	8-kV peak
	CMTI	> 50 kV/µs
Interface	Voltage	3.3 V or 5 V
	Input signals	PWM and RESET
	Output signals	$\overline{\text{FAULT}}$ and $\overline{\text{UVLO}}$
System or drive specs	Input voltage	Up to 600 V_{AC}
IGBT modules	IGBT gate capacitance	Q_g up to 10 µC

(1) 15-V, –8-V isolated power supply is not generated on this board.

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3 System Description

The design consists of four sections: the isolated interface with the motor controller, the drive stage, the protections circuit, and the power supply of the gate drive.

The isolated interface is implemented using the ISO7842 digital isolator. This interfaces the low voltage MCU to PWM, RESET, $\overline{\text{FAULT}}$, and $\overline{\text{UVLO}}$ signals to the drive stage.

The drive stage uses the CSD877353Q5D, which are half-bride N-channel MOSFET power blocks. The CSD877353Q5D switches the IGBT gate voltage to 15 V to turn-on the IGBT or –8 V to turn-off the gate. The CSD877353Q5D power block is driven from the TPS51604 MOSFET gate driver.

The two protection functionalities implemented in this design are DESAT protection and UVLO. The first stage of DESAT protection is a DESAT fault detection section, which uses a high voltage diode logic and the TLV3201 comparator with a fast transient response. After detecting a DESAT fault, the protection circuit disables the drive stage and turns off the IGBT with a soft shutdown. The soft turn-off section does two functions: one is to discharge the gate capacitance until it reaches 2 V and then to strongly apply –8 V to the gate to keep the IGBT turned off.

The supply voltage to the primary side of the digital isolator should be the same as the MCU. The supply voltage on the secondary side of the digital isolator is 15 V and –8 V. The 0-V rail is the MCU's reference on the secondary side and is connected to the emitter of the IGBT. A 5-V LDO is used on the secondary side between the 15-V and –8-V rail to generate the –3-V rail. The 15-V and –8-V rail is given as an input from the TIDA-00199 gate drive power supply reference design for system evaluation. The reference design for the power topologies that can be used with this isolated gate driver design are:

- TIDA-00182: Reinforced Isolated IGBT Gate Drive Flyback Power Supply With 8 Outputs
- TIDA-00181: Isolated IGBT Gate-Drive Push-Pull Power Supply With 4 Outputs
- TIDA-00199: Wide-Input Isolated IGBT Gate-Drive Fly-Buck™ Power Supply for 3-Phase Inverters
- TIDA-00174: Isolated IGBT Gate-Drive Fly-Buck Power Supply With 4 Outputs
- TIDA-00195: Isolated IGBT Gate Driver Evaluation Platform for 3-Phase Inverter System

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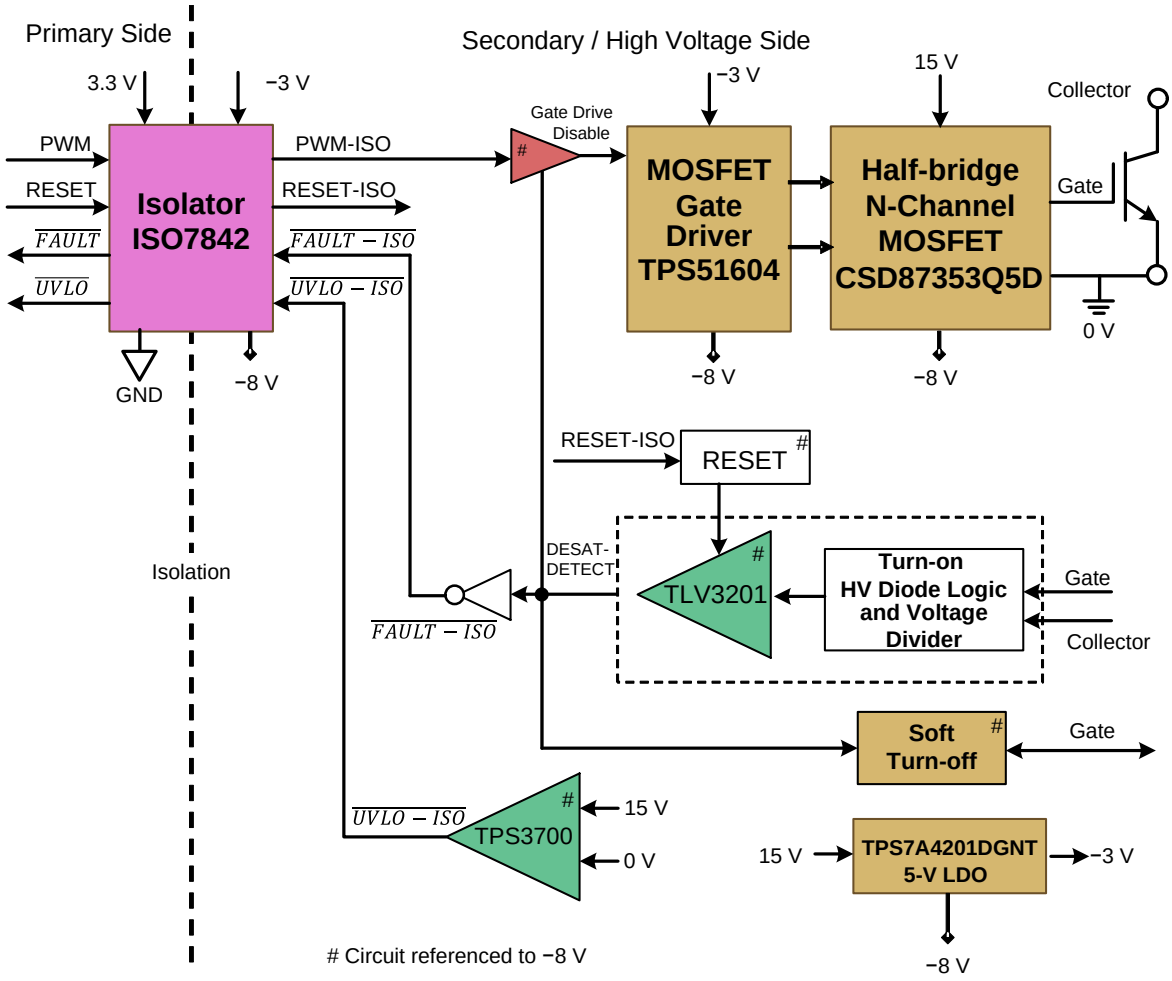

Figure 2. TIDA-00448 Block Diagram

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3.1 DESAT Detection and Soft Turn-Off

The desaturation of an IGBT indicates that a high fault current exists in the IGBT. This fault current is sensed by monitoring the V_{CE} drop during the on-state of the IGBT using a comparator with respect to a fixed voltage reference. As the current increases beyond the nominal current rating of the IGBT, the V_{CE} increases drastically. On the output characteristics of the IGBT, this is the transition from the saturation region to active region.

If the IGBT is turned off normally when carrying a high fault current, the V_{CE} overshoot can exceed the IGBT's voltage rating, resulting in its destruction. An overshoot is due to the interruption of a high fault current flowing through the stray inductance. Therefore, a soft turn-off is done by increasing the gate voltage discharge time during turn-off to reduce the di/dt after a DESAT fault condition.

3.2 Highlighted Products

Key features of the highlighted devices are taken from product datasheets.

3.2.1 ISO7842

The ISO7842 is a digital isolator with a 8000-V_{PK} isolation voltage. This device has reinforced isolation certifications according to VDE, CSA, and CQC. The isolator provides high electromagnetic immunity and low emissions at low power consumption while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. The ISO7842 has two forward and two reverse-direction channels. In case of an input power or signal loss, the device will output a default logic. For further details, see the "Device Functional Modes" section in the ISO7842 datasheet (SLLSEJ0). Used in conjunction with an isolated power supplies, this device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through an innovative chip design and layout techniques, electromagnetic compatibility of the ISO7842 has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO7842 is available in 16-pin SOIC wide-body (DW) and extra-wide body (DWW) packages.

3.2.2 TPS51604

The TPS51604 are FET drivers with integrated high-side boost-strap gate drive, optimized for high-frequency and 5-V FET applications. The TPS51604 drives the CSD87353Q5D NexFET Power Block, which has two N-Channel MOSFETs in a half-bridge configuration. The $\overline{SKIP}$ pin is pulled up to enable the gate drive from the TPS51604. The TPS51604 also supports two low-power modes. With the PWM input in tri-state, quiescent current is reduced to 130 µA with an immediate response. When $\overline{SKIP}$ is held at tri-state, the current is reduced to 8 µA (typically, 20 µs is required to resume switching). Paired with the appropriate TI controller, the drivers deliver an exceptionally high performance power supply system. The TPS51604 is packaged in a space saving, thermally enhanced 8-pin, 2×2-mm WSON package and operates from –40°C to 105°C.

3.2.3 CSD87353Q5D

The CSD87353Q5D NexFET power block is a two N-Channel MOSFETs in a half-bridges configuration, offering high current, high efficiency, and high frequency capability in a small 5×6-mm outline. The CSD87353Q5D is optimized for 5-V gate drive applications; this product offers a flexible solution capable of offering a high density solution when paired with any 5-V gate drive from an external controller or driver.

- V_{IN} up to 27 V and up to 40-A operation
- High frequency operation (up to 1.5 MHz)
- High density: SON 5×6-mm footprint
- Optimized for 5-V gate drives
- Low switching losses and ultra-low inductance package

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3.2.4 TLV3201

The TLV3201 is a single-channel comparators that offer the ultimate combination of high-speed (40 ns) and low-power consumption (40 µA), in extremely small packages with features such as rail-to-rail inputs, low offset voltage (1 mV), and large output drive current. The devices are also very easy to implement in a wide variety of applications where response time is critical. The TLV3201 is available in SOT23-5 and SC70-5 packages. All devices are specified for operation across the expanded industrial temperature range of –40°C to 125°C.

- Low propagation delay: 40 ns
- Low quiescent current: 40 µA per channel
- Input common-mode range extends 200 mV beyond either rail
- Low input offset voltage: 1 mV
- Push-pull outputs
- Supply range: 2.7 to 5.5 V

3.2.5 TPS3700

The TPS3700 wide-supply voltage window comparator operates over a 1.8-V to 18-V range. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for over- and undervoltage detection. The TPS3700 can be used as a window comparator or as two independent voltage monitors; the monitored voltage can be set with the use of external resistors. OUTA is driven low when the voltage at INA+ drops below ($V_{ITP} – V_{HYS}$) and goes high when the voltage returns above the respective threshold (V_{ITP}). OUTB is driven low when the voltage at INB– rises above V_{ITP} and goes high when the voltage drops below the respective threshold ($V_{ITP} – V_{HYS}$). Both comparators in the TPS3700 include built-in hysteresis for filtering to reject brief glitches, thereby ensuring stable output operation without false triggering. The TPS3700 is available in a SOT-6 and a 1.5×1.5-mm WSON-6 package and is specified over the junction temperature range of –40°C to 125°C.

3.2.6 TPS7A4201

The TPS7A42 is a very high voltage-tolerant linear regulator that offers the benefits of a thermally-enhanced package (MSOP-8), and is able to withstand continuous dc or transient input voltages of up to 28 V. The TPS7A42 is stable with any output capacitance greater than 4.7 µF and any input capacitance greater than 1 µF (over temperature and tolerance). Therefore, implementations of this device require minimal board space because of its miniaturized packaging (MSOP-8) and a potentially small output capacitor. In addition, the TPS7A42 offers an enable pin (EN) compatible with standard CMOS logic to enable a low-current shutdown mode. The TPS7A42 has an internal thermal shutdown and current limiting to protect the system during fault conditions. The MSOP-8 packages has an operating temperature range of T_J = –40°C to 125°C. In addition, the TPS7A42 is ideal for generating a low-voltage supply from intermediate voltage rails in telecom and industrial applications; not only can it supply a well-regulated voltage rail, but it can also withstand and maintain regulation during fast voltage transients. These features translate to simpler and more cost-effective electrical surge-protection circuitry for a wide range of applications.

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4 System Design Theory

4.1 Power Rails

The primary side of the isolator requires a bias voltage of 3.3/5 V to match the signal of the interfaced MCU. This voltage is supplied externally to the board on connector J1.

On the secondary side, the supply rail required to drive the IGBT are given externally. Header J2 has input for 15 V, 0 V, and –8 V. The secondary side has ICs that require a bias of 5 V. This is generated using a 5-V LDO between the 15-V rail and –8-V rail. The output of the LDO is at –3 V when measured from emitter of the IGBT. The IGBT emitter is connected to a 0-V rail. The power rail diagram is shown in Figure 3.

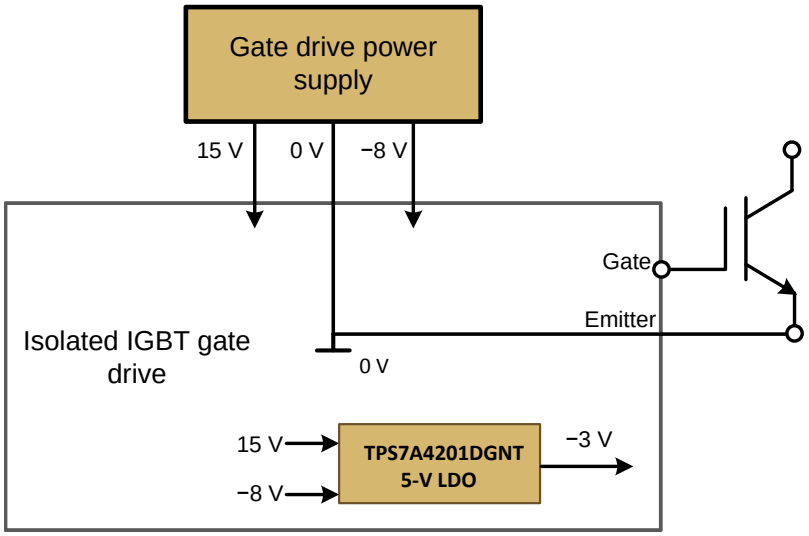

Figure 3. Power Rail Diagram for Secondary Side

The 5-V LDO is selected based on the load current, input voltage, power dissipation, and junction to ambient thermal resistance. The maximum current requirement is 50 mA and the input voltage is the difference of the 15-V and –8-V rail, thus 23 V. Power dissipation in the LDO is given as

$$P = \left(V_{IN} - V_{OUT}\right) \times I_L = (23 - 5) \times 50 \times 10^{-3} = 0.9\ W \quad (1)$$

An LDO rated up to 125°C is chosen. The maximum operating temperature should be 10 degrees less than 125°C to have a margin, (that is, 115°C) if the maximum ambient temperature is 55°C. The required junction to ambient thermal resistance is

$$\theta_{JA} = \frac{\left(T_J - T_A\right)}{P} = \frac{(115 - 55)}{0.9} = 66.66°C/W \quad (2)$$

This is the junction to the ambient thermal resistance that must be supported by the LDO package. The TPS7A42 in MSOP-8 package is chosen, as it is θ_{JA} of 66.7°C/W meets the design requirement.

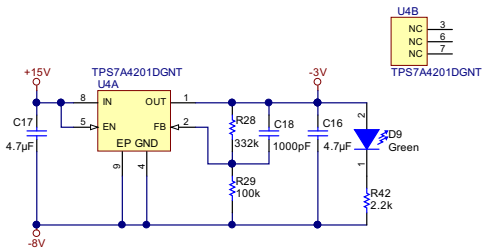

Figure 4. LDO Circuit

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4.2 Digital Isolator

The digital isolator is used for signal isolation between the low voltage MCU circuit (primary side) and the high voltage inverter circuit (secondary side). The isolator needs to support two input signals (PWM and RESET) and two output signals ($\overline{\text{FAULT}}$ and $\overline{\text{UVLO}}$). The isolator is chosen according to IEC61800-5-2 standards for reinforced isolation. The maximum voltage to the motor drive in which this gate driver is used is chosen to be 600 V and CAT III overvoltage rating. In this category, the isolation device requires a transient overvoltage (V_{IOTM}) of at least a 8000-V peak for reinforced isolation. The ISO7842 provides a 8000-V_{IOTM_peak},
2121-V_{IORM_peak}, and a very high CMTI of 50 kV/µs.

Figure 5 shows the circuit used. The signals have pulldown and pullup resistors, such that the signals are at the proper levels when powered up.

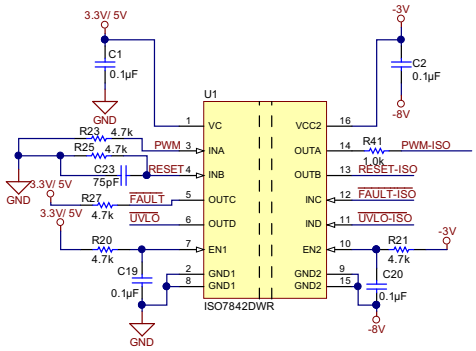

Figure 5. Digital Isolator Circuit

4.3 Drive Stage

Figure 6 shows the drive stage with a MOSFET power block to provide the sink and source currents and the MOSFET driver for the power block. The sink and source currents are limited by the gate resistor value. However, the value of gate resistor is system dependent and chosen to provide optimum performance of the system. The value of the gate resistor influences different aspects of the switching process such as:

- IGBT switching losses
- di/dt
- Cross conduction
- Reverse recovery losses of the diode
- Reduce parasitic miller voltage

Diode D1 is used to have different slew rates for turn-on and turn-off. The turn-on gate resistance is R_{g_on} = (R3 || R55) = 1 Ω, and turn-off gate resistance is R_{g_off} = (R3 || R5) || (R2 || R58) = 0.33 Ω, which are on the reference design. However, these may be changed according to system requirements. The IGBT also has an internal gate resistance ($R_{g\_internal}$) that limits the peak current; this is neglected to calculate the maximum possible peak current. The theoretical peak current at turn-on and turn-off are given as follows.

$$I_{peak\_on} = \frac{\Delta V_{GATE}}{R_{g\_on} + R_{g\_internal}} = \frac{23}{1} = 23\ A \quad (3)$$

$$I_{peak\_off} = \frac{\Delta V_{GATE}}{R_{g\_off} + R_{g\_internal}} = \frac{23}{0.3} = 69\ A \quad (4)$$

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Bulk capacitors are sized to supply the above switching currents and to the voltage ripple. The capacitance is given by

$$C = \frac{Q_g}{\Delta V} \tag{5}$$

Where Q_g is the gate capacitance of the IGBT and ΔV is the allowable voltage ripple of the bulk capacitor. The ripple is chosen to be 0.01 V; therefore, C = 10 µC/0.01 V = 100 µF. Part of the bulk capacitance is placed near the input connector J2, and the remaining is placed near the MOSFET power block. C11 and C12 are bulk capacitors on the 15-V rail, and C13 and C15 are bulk capacitors on the -8-V rail.

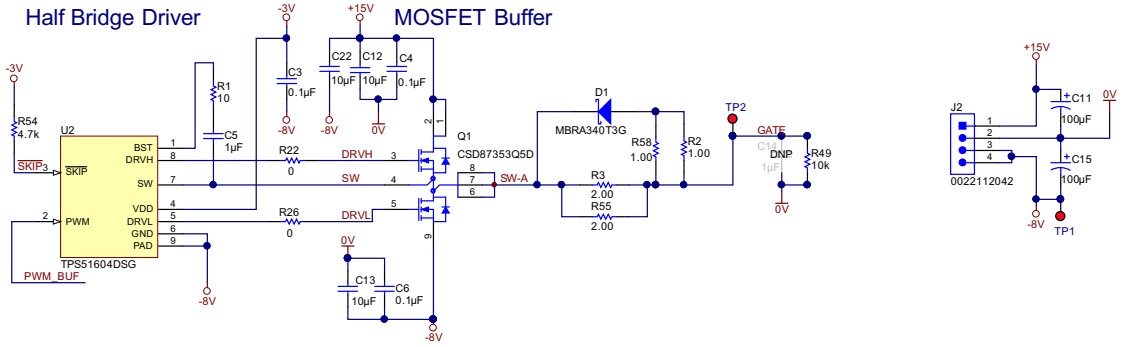

Figure 6. Drive Stage Circuit

4.3.1 Power Block Selection

TI has a wide variety of power blocks supporting from 15 to 40 A. Design flexibility to optimize for different peak current requirements is added by choosing a standard package. The power block requirements are a 5-V gate drive and a voltage rating of 30 V. A V_{DS} value of 30 V is selected to support the bipolar voltage swing of 23 V. In a SON5x5 package, the following power blocks are available, which fit the design requirements.

Table 2. Power Blocks in SON5x5 Package

PART NUMBER	ID, CONTINUOUS DRAIN CURRENT AT T_A = 25°C (A)
CSD87352Q5D	25
CSD87351Q5D	32
CSD87353Q5D	40

For further optimization in the current, the package can changed to a smaller SON3x3 footprint, which has the same pin configurations. Table 3 is a list of compatible power blocks in a SON3x3 package.

Table 3. Power Blocks in SON3x3 Package

PART NUMBER	ID, CONTINUOUS DRAIN CURRENT AT T_A = 25°C (A)
CSD87331Q3D	15
CSD87330Q3D	20

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4.3.2 Half-Bridge MOSFET Driver

The TPS51604 is used as the half-bridge MOSFET driver as shown in Figure 6. The TPS51604 uses a bootstrap power supply for the gate drive voltage for the top MOSFET of the power block. The bootstrap capacitor C5 is selected based on the charge required to turn on the top MOSFET and acceptable voltage ripple.

$$C5 = \frac{Q_g}{\Delta V} \quad (6)$$

Where Q_g is the gate capacitance of MOSFET power block; the CSD87353Q5D has a Q_g of 24 nC.

ΔV is the voltage ripple of the bootstrap capacitor, which is chosen to be 25 mV; then C5 = 24 nC/25 mV = 0.96 µF, so select C5 = 1 µF. The bootstrap resistor R1 limits the charging current and also controls the turn-on time of the MOSFET. The minimum recommended value in the CSD87353Q5D datasheet is 4.7 Ω; 10 Ω is selected for R1. The $\overline{SKIP}$ pin controls the state of the TPS51604, to switch between continuous conduction mode and discontinuous conduction mode or a low power state and is only relevant when the TPS51504 is used in a buck power supply. The $\overline{SKIP}$ pin is pulled high in the design to disable this behavior. To tri-state the output of the half-bridge, the voltage at the PWM input to the TPS51604 is put into a tri-state value.

4.3.3 Power Dissipation

In the process of turning the IGBT on and off, power is dissipated in the gate drive circuit, IGBT gate resistor, and any resistor in the gate drive. Only the power dissipation for charging and discharging of the gate capacitance is calculated, as this is the major component. The power dissipation is given by Equation 7:

$$P_{GATE} = Q_{GATE} \times F_{SW} \times \Delta V_{GATE} \quad (7)$$

where

- Q_{GATE} = total gate charge
- F_{SW} = Switching frequency
- ΔV_{GATE} = Gate driver output voltage swing

The gate driver needs to support Q_g up to 10 µC, and bipolar switching of 15 to –8 V. Therefore, ΔV_{GATE} is 23 V.

$$P_{GATE} = 10\ \mu C \times 16\ KHz \times 23\ V = 3.68\ W \quad (8)$$

A part of this power is dissipated in the external gate resistors. The external gate resistor and power supply are sized appropriately for this power dissipation.

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4.4 DESAT Protection

The implementation of the DESAT protection is divided into the following parts: the diode logic and potential divider, V_{CE} monitoring, gate drive disable, and the soft shutdown circuit. For the DESAT protection feature to function properly, all the circuit must work in tandem. The diode logic makes sure the DESAT monitoring happens only during the on-state of the IGBT. The diode logic interfaces with the collector pin, which is at high voltage. This is connected to the V_{CE} monitoring comparator. A comparator with fast response is selected and configured to latch after detection. After detection, the TPS51604 gate driver has to be turned off by tri-stating the PWM input. Subsequently, the gate is slowly discharged by the soft turn-off circuit.

4.4.1 HV Diode Logic and Potential Divider

Figure 7 shows the diode logic used, which comprises of D2 and D5. D2 is a high voltage diode, as the DC link voltage is dropped across the diode in the reverse bias region when the IGBT is turned-off. D2 is rated to 1200 V to be more than the DC link voltage of 800 V.

The circuit is analyzed for the steady state condition when IGBT is on and IGBT is off as shown in Table 4.

Table 4. HV Diode Logic and Potential Divider Circuit State

STATE	V_{GATE}	$V_{COLLECTOR}$	D2	D5	C8
IGBT on state	15 V	V_{CE_ON}	On	On	Charges
IGBT off state	–8 V	DC link voltage (1200 max)	Off	Off	Discharges

For IGBT to be on, the gate is driven to 15 V and the IGBT V_{CE} drops to a relatively small saturation voltage. D2 and D5 is on and this causes the capacitor C8 to charge. The voltage C8 charges to is designed by the combination of the resistors and diodes shown in Figure 7. Should the IGBT start to desaturate, meaning the V_{CE} voltage starts to increase, the voltage at TP5 also starts to increase and charges C8 further. There is a direct relation between the voltage across capacitor C8 and the V_{CE} voltage. This relation determined by the resistors R6, R8, R9, R11, and R12 and explained in the following sections.

When the IGBT is switched off, the gate voltage is at –8 V and capacitors D5 and D2 are off. Any voltage across C8 discharges through R12.

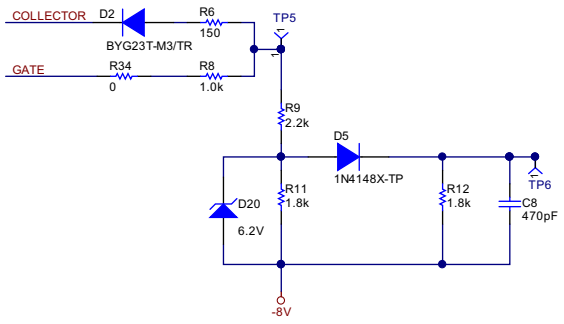

Figure 7. HV Diode Logic and Potential Divider Circuit

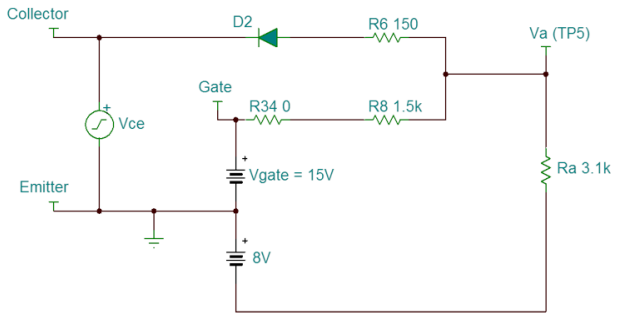

Figure 8. HV Diode Logic Circuit Used for Analysis

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Design Process and Equation

Figure 8 shows a simplified version of the HV Diode Logic Circuit where V_{CE} is the input and Va is output voltage across Ra, where Ra is the combination of R9, R11, and R12. Voltage at Va represents the V_{CE} voltage when the IGBT is on. The following analysis shows the method when choosing R6, R8, and Ra for proper functioning of the circuit as well as the method to split Ra to be used as a potential divider for voltage Va before giving as an input to the comparator.

Applying KCL to node TP5:

$$\frac{\left(Va - \left(V_{CE} + 8\right) - 0.7\right)}{R6} + \frac{\left(Va - \left(15 + 8\right)\right)}{R8} + \frac{Va}{Ra} = 0 \tag{9}$$

Where Ra = R9 + R11 || R12

Equation 9 is solved for Va:

$$Va = \left(\frac{V_{CE}}{R6} + \frac{8 + 0.7}{R6} + \frac{23}{R8}\right)\left(\frac{R8R6Ra}{R8R6 + R6Ra + R8Ra}\right) \tag{10}$$

$$Va = \frac{V_{CE}}{R6}\left(\frac{R8R6Ra}{R8R6 + R6Ra + R8Ra}\right) + \left(\frac{8 + 0.7}{R6} + \frac{23}{R8}\right)\left(\frac{R8R6Ra}{R8R6 + R6Ra + R8Ra}\right) \tag{11}$$

Compare with the line equation y = Mx + C, where y is Va and x is V_{CE}. The slope of the line M is

$$M = \frac{1}{R6}\left(\frac{R8R6Ra}{R8R6 + R6Ra + R8Ra}\right) \tag{12}$$

The potential divider should have good sensitivity where a change in the input V_{CE} causes an appreciable change in the output. For a potential divider, the slope cannot be more than one, so a slope less than one is chosen. Therefore, choose R8 >> R6 or R8Ra >> R8R6 + R6Ra.

The resistors are chosen less than 10 kΩ to reduce voltage drops caused by transient currents. Choose R6 = 150 Ω, R8 = 1.0 kΩ, Ra = 3.1kΩ.

Ra is obtained as two series resistors to form a potential divider. This potential divider limits voltage to comparator to a maximum of 5 V. The divider ratio is chosen as 1/3; that is, 3.1k value of Ra is obtained as series of 2.2 kΩ and 0.9 kΩ. The 0.9 kΩ required is obtained as two parallel 1.8 kΩ. This is done to insert D5 in the circuit between R11 and R12. This results in R12 controlling the discharge of C8.

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DC Transfer Graph

The DC transfer characteristic gives the relation between V_{CE} the x-axis variable and the voltage across C8 (Vcap), which is a y-axis variable. This relation is used to program the DESAT threshold voltage for a value of the V_{CE} on the x-axis and the corresponding Vcap voltage obtained on the y-axis. A reference voltage equal to this value is set at the inverting input by a Zener diode.

Spice simulation was done to obtain the DC transfer characteristics. This simulation calculates the V_{CE} threshold for the desaturation monitoring circuit for a chosen reference voltage in the DESAT monitoring circuit. The circuit diagram used for simulation is shown in Figure 9.

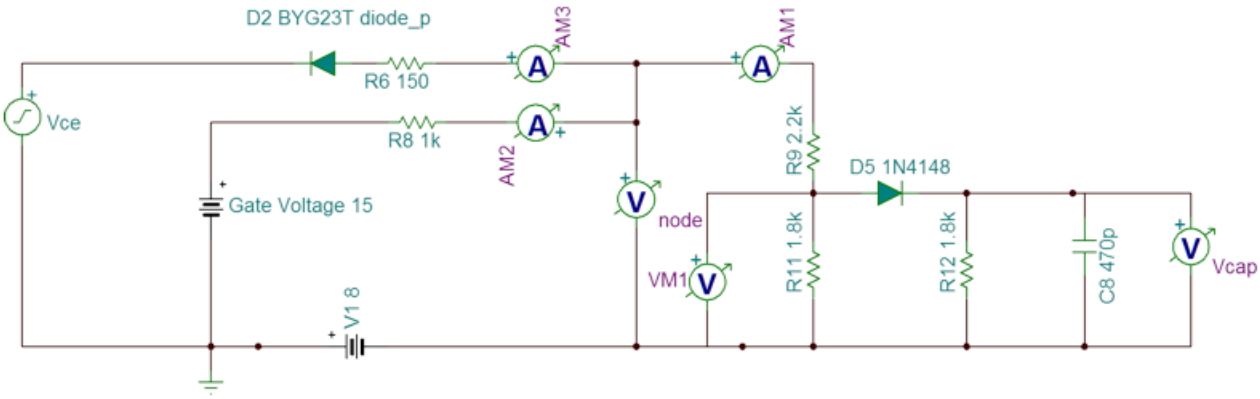

Figure 9. Simulation Circuit for HV Diode Logic and Potential Divider

The knee on the transfer characteristics when V_{CE} is 9 V is when the diode D2 becomes reverse biased. To increase the knee voltage, modify the resistors R11, R12, R8, and R9.

$$Vknee = 23 \times \frac{R11 \parallel R12}{R8 + R9 + R11 \parallel R12} \quad (13)$$

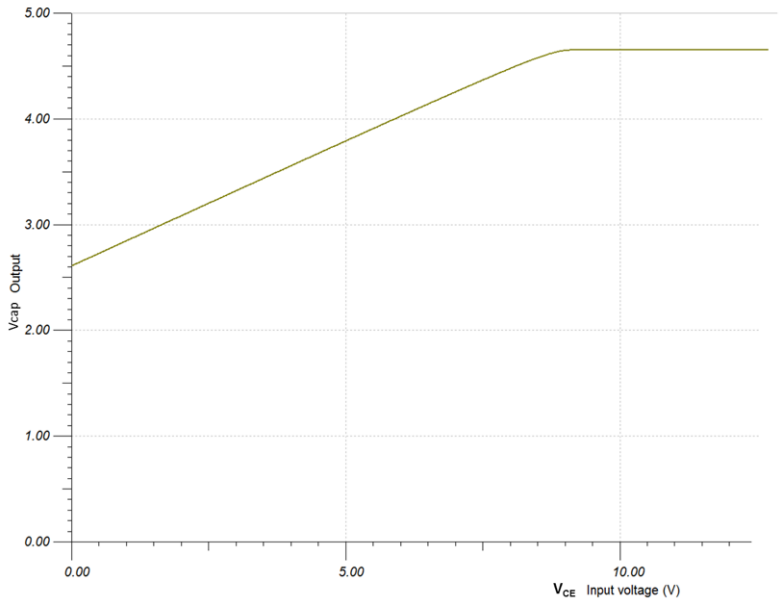

Figure 10. Transfer Characteristics (V_{CE} versus Vcap) for HV Diode Logic and Potential Divider

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Blanking Time

A blanking time for the DESAT monitoring circuit is required to prevent against false detection at turn-on event of the IGBT. The C8 capacitor in the circuit delays the input signal to the DESAT monitoring comparator. This delay is used as the blanking time, and is controlled by the charging time of the capacitor C8. The charging time is 5 × R_{EQ} × C, where R_{EQ} is the Thevenin resistance of the HV potential divider.

$$R_{EQ} = (R12 \parallel R11) \parallel (R9 + R6 \parallel R8) = 649.25\ \Omega \quad (14)$$

The choice of capacitor controls the blanking time. Choosing C8 = 470 pF, the blanking time is = 5 × 649.25 × 470p = 1.52 µs.

During the IGBT turn-on or off, transient voltages will appear across the potential divider. D20 protects the subsequent comparator TLV3201 from damage by the transient voltage. D20 shunts any negative voltage during the turn-on transient state, and prevents the voltage at the input to TLV3201 from exceeding 5.1 V during the turn-off transient state.

4.4.2 DESAT Monitoring by Comparator

Figure 11 shows the TLV3201 used for DESAT monitoring. The DESAT threshold voltage is set by D4 and connected to the inverting terminal. The value of Zener voltage can be selected based on the V_{CE} threshold for the monitoring circuit. The relation between the reference voltage and the V_{CE} threshold is discussed in Section 4.4.1. The output of the comparator is fed back to the non-inverting terminal through D6 and R14, which allows the circuit output to latch on DESAT detection.

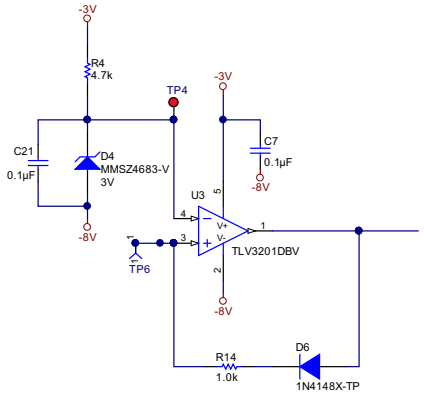

Figure 11. DESAT Monitoring Circuit

4.4.3 Gate Drive Disable

On detecting DESAT to turn-off the gate driver, the PWM input to the TPS51604DSG is tri-stated. This puts the power block into a high impedance state. This is done using the SN74LVC1G125, which is a digital signal buffer with an output enable pin to tri-state the output. Figure 12 shows the circuit. The PWM signal from the isolator is routed through the SN74LVC1G125 to the TPS51604DSG. The DESAT signal is connected to the output enable pin. When DESAT-DETECT signal is active, PWM_BUF signal is tri-stated. A low-pass filter comprising of R60 and C41 is used for noise rejection.

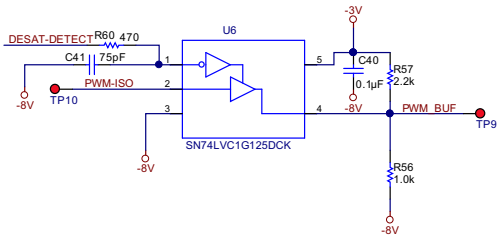

Figure 12. Gate Drive Disable Circuit

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4.4.4 Soft Turn-off

After the gate driver has been tri-stated, the IGBT is still on with the gate at 15 V. This is then discharged by the soft turn-off circuit. There is a required time that needs to be spent in soft run-off to reduce the V_{CE} overshoot. However, there is also a limit on the maximum time allowed for soft turn-off. This is given in datasheet of the IGBT as the short circuit withstanding time. The typical value is between 5 to 10 µs.

Figure 13 shows the soft turn of circuit. There are two parts to the soft turn-off circuit: the first part comprises of Zener diode D18 and resistor R5 for the capacitor discharge, and the second part is the clamp circuit comprised of Q8 and Q7.

After the DESAT-DETECT signal goes high, Q9 turns-on and causes Q2 to turn on, which engages the Zener and resistor to discharge the gate. Once the gate voltage reduces to 2 V, the clamp circuit (Q8 and Q7) is activated. Q8 is used as a comparator by comparing the gate voltage with the base emitter saturation voltage (V_{BE_sat}) of 0.85 V.

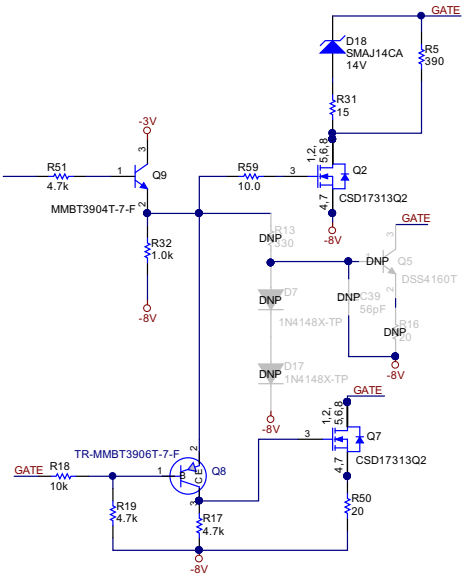

Figure 13. Soft Turn-off Circuit

Design Processes

The gate waveform when the soft turn off is activated is shown in Figure 14. At = 0, the soft turn-off starts, and V1 is 23 V with regards to the –8-V rail. The voltage V2 is near the IGBT gate threshold voltage. This voltage is set by the Zener voltage of the diode D18. For CM450DX-24S, the threshold voltage is 6 V. The Zener is referenced to the –8-V rail. The Zener voltage chosen is 6 V + 8 V = 14 V.

The time taken to transition to V2 is short and neglected. T1 is the transition time from V2 to V3. T1 is used as an indirect parameter to control the soft turn-off time. The IGBT turn-off completes near the V2 region, and the actual turn-off time is much smaller than T1. T1 is programmed by the value of R5 and is given by

$$R5 = \frac{T1}{C_g \times \mathrm{Log_e}\left(\frac{V2 - V4}{V3 - V4}\right)} \tag{15}$$

Where T1 is the required time, and C_g is the gate capacitance taken from the graph of gate charge characteristics (gate-emitter voltage versus Q_g) found in the datasheet of IGBT. For CM450DX-24S, C_g = 29.54 nF. V2 is at 6 V, V3 is chosen as 2 V, and V4 is the final voltage.

$$R5 = \frac{4.0\ \mu s}{29.54\ nF \times \mathrm{Log_e}\left(\frac{6 - (-8)}{2 - (-8)}\right)} = 402.4\ \Omega \tag{16}$$

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V3 is the voltage at which the clamp activates when the base emitter voltage of Q8 exceeds the 0.85 threshold voltage (in other words, the base voltage (V_{BB}) drops below the threshold voltage V_t = (5 – 0.85 – 0.85) = 3.3 V. R18 and R19 in Figure 13 set the voltage at which the IGBT gate gets clamped. Select R18 = 10 kΩ then R19 is given by.

$$R19 = R18 \times \frac{V_t}{V3 - V4 - V_t}$$

$$R19 = 10k \times \frac{3.3}{2 - (-8) - 3.3} = 4.92\ k\Omega \quad (17)$$

Select R19 = 4.7 kΩ

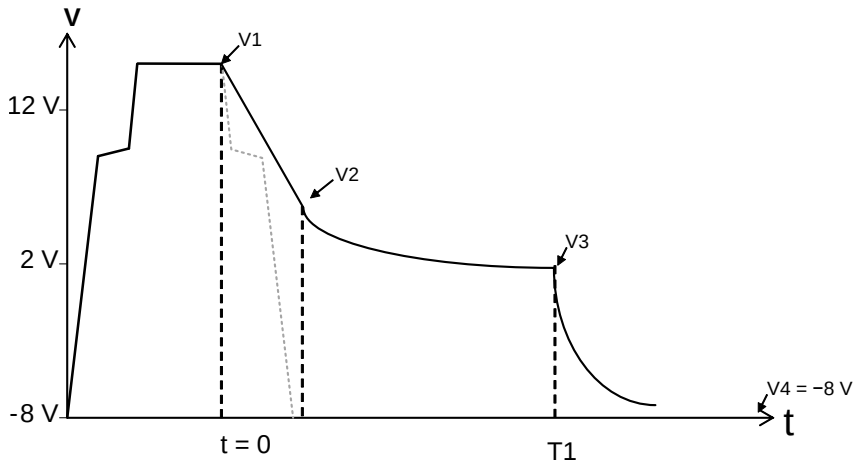

Figure 14. IGBT Gate Waveform During Soft Turn-off

Alternatively the soft turn can be done using a constant current sink circuit. This implemented by R13, D7, D17, Q5, and R16; however, the provision is not used for the test in Section 6.

4.4.5 RESET Circuit

After the motor controller has responded to the $\overline{\text{FAULT}}$ signal, it may re-apply the PWM after resetting the gate driver. The sequence needed for resetting are:

1. MCU must respond to the gate driver by turning-off the PWM.
2. Have the MCU assert RESET when the MCU is ready to start again.
3. The PWM can then be started.

The circuit to implement the RESET feature is given in Figure 15. Transistor Q6 is used to pull down the non-inverting terminal of DESAT monitoring comparator to zero. This clears the output of the comparator that was latched. Also, transistor Q3 momentarily gives a low signal at the $\overline{\text{SKIP}}$ input of the TPS51604 for RESET.

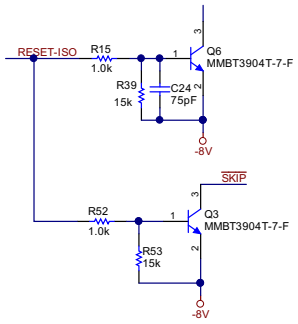

Figure 15. RESET Circuit

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4.5 UVLO

The IGBT gate is driven from the 15-V rail to turn on the IGBT. The 15-V rail should not drop below the minimum gate voltage to properly turn on the IGBT. Operating the IGBT with a lesser gate voltage causes excessive power dissipation in the IGBT, leading to failure. Therefore, it is required to detect when the 15-V rail drops and disable the gate output.

Figure 16 shows the UVLO circuit using the TPS3700. The TPS3700 has two internal comparators. The block diagram for the TPS3700 is shown in Figure 17. The non-inverting comparator monitors the 15-V rail with regards to the –8-V rail and detects if it drops. The inverting comparator monitors the 0-V rail to check if it increases, thereby reducing the voltage difference between the 15-V and 0-V rails. The voltage difference between the 15-V and 0-V rails is required to be monitored on the board. To do this, UVLO is detected in case the 15-V rail drops by 1.5 V or the 0-V rail increases by 1.5 V. The OR logic is implemented by connecting the two open drain outputs of the TPS3700. The worst case is when both situations happen, where the voltage drops 3 V. Diode D8 pulls the signal PWM-ISO low when the undervoltage signal is active, which disables the gate driver.

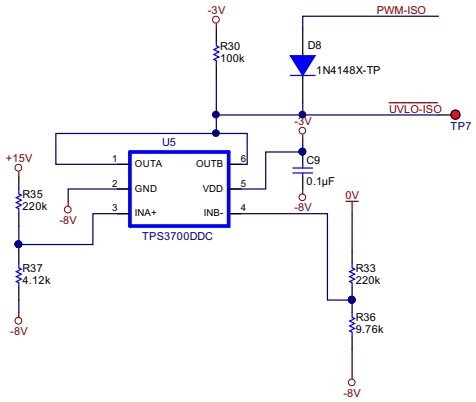

Figure 16. UVLO Circuit

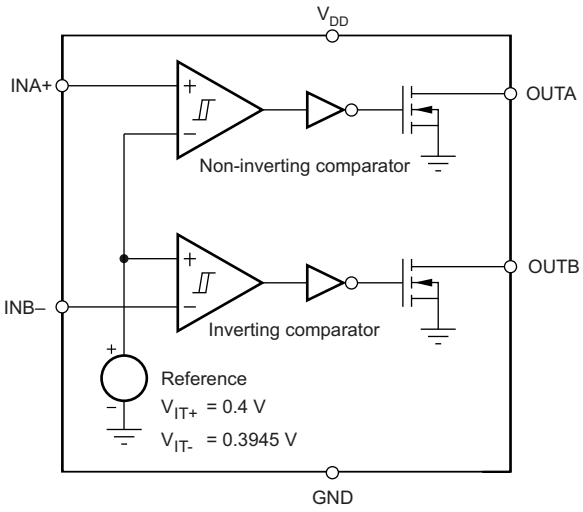

Figure 17. TPS3700 Block Diagram

4.5.1 15-V Rail

The INA+ terminal of the TPS3700 detects when the 15-V rail drops by 1.5 V. The 15-V rail is at 23 V with regards to –8 V (23 V transitions to 21.5 V). Use the lower threshold value of the TPS3700 for this negative going signal:

$$R37 = \frac{\left(V_{IT-} \times R35\right)}{V_{MON} - V_{IT-}} \tag{18}$$

Select R35 = 220 kΩ, V_{MON} = 21.5 V, V_{IT}– = 0.3945.

$$R37 = \frac{\left(0.3945 \times 220\ k\Omega\right)}{21.5 - 0.3945} = 4.1122\ k\Omega \tag{19}$$

Select R37 = 4.12 kΩ at 1%.

V_{MON} is recalculated as:

$$V_{MON} = \frac{\left(R35 \times V_{IT-}\right)}{R37} = \frac{\left(220 \times 0.3945\right)}{4.12} + 0.4 = 21.4655\ V \tag{20}$$

Therefore, the effectively or selection error is 21.5 – 21.4655 = 0.0345 V

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4.5.2 –8-V Rail

The INB– terminal of the TPS3700 detects when the 0-V rail increases by 1.5 V. The 0-V rail is at 8 V with regards to the –8-V rail (8 V transitions to 9.5 V). V_{MON} = 9.5 V. Use the upper threshold value of the TPS3700 for the positive going signal:

$$R36 = \frac{\left(V_{IT+} \times R35\right)}{V_{MON} - V_{IT+}} \quad (21)$$

Select R33 = 220 kΩ, V_{MON} = 9.5 V, V_{IT+} = 0.4 V.

$$R36 = \frac{\left(0.4 \times 220\ k\Omega\right)}{9.5 - 0.4} = 9.6703\ k\Omega \quad (22)$$

Select R36 = 9.76 kΩ at 1%.

V_{MON} is recalculated as:

$$V_{MON} = \frac{\left(R36 \times V_{IT+}\right)}{R36} = \frac{\left(220 \times 0.4\right)}{9.76} + 0.4 = 9.4164\ V \quad (23)$$

Effectively or selection error is 9.5 – 9.4164 = 0.0836 V.

4.6 Connectors

Figure 18 shows the connectors for external interface J1 is on the primary side of the isolator and J2 is on the secondary side. The 15-V and –8-V power rail on J2 has bulk capacitors.

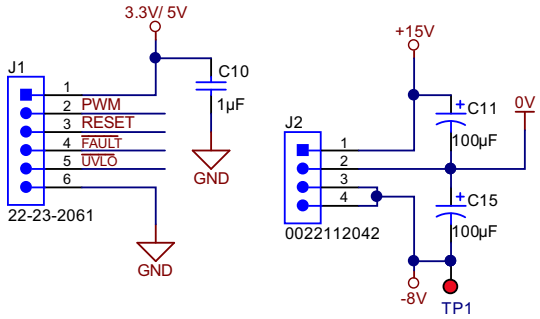

Figure 18. Board Connectors

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5 Getting Started: Hardware

Figure 19 and Figure 20 show the board images.

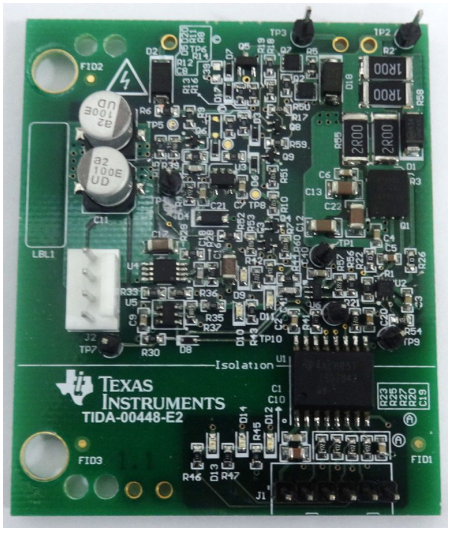

Figure 19. Isolated IGBT Gate Driver Top Side

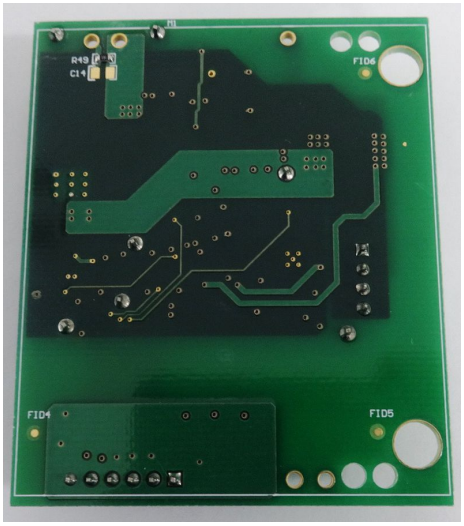

Figure 20. Isolated IGBT Gate Driver Bottom Side

Figure 21 shows the board interface and board sections.

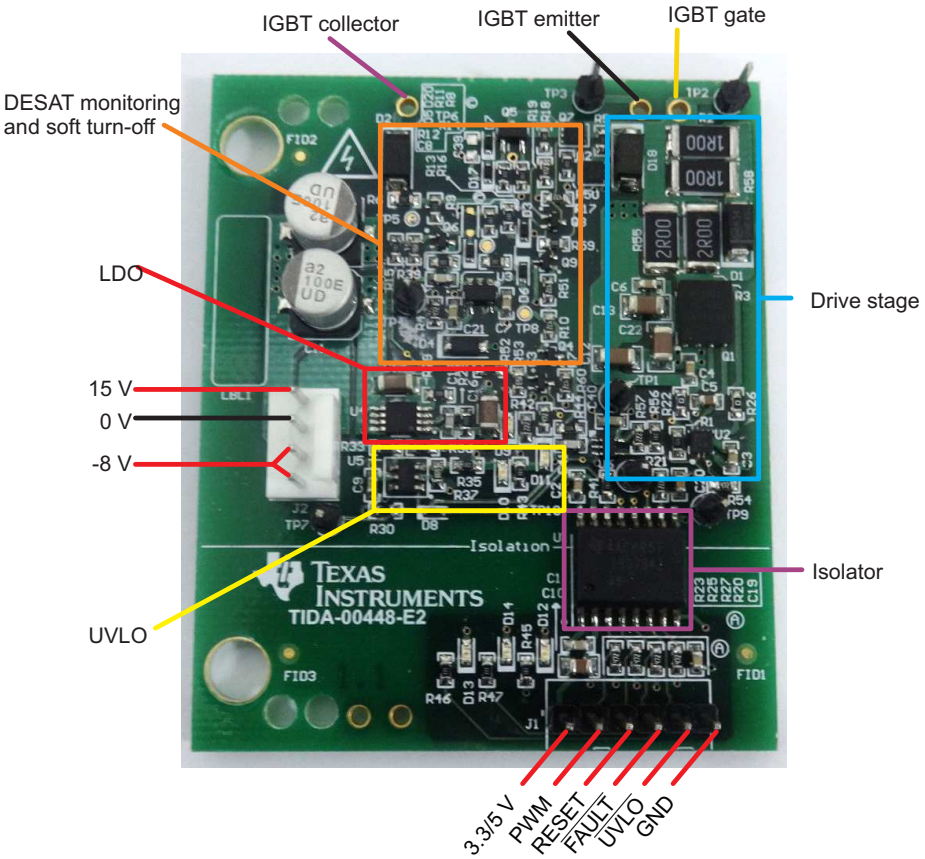

Figure 21. Isolated IGBT Gate Driver Board Connections

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Figure 22 shows the Isolated IGBT Gate Driver mounted on the CM450DX-24S IGBT module.

Figure 22. Isolated IGBT Gate Driver Mounted on IGBT Module

Figure 23 shows the capacitor banks used for the 800-V DC link voltage mentioned in Section 6.

Figure 23. DC Link Capacitor Bank

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6 Test Data

6.1 Propagation Delay of Drive Circuit

The propagation delay test for the driver is done in two parts. The first part is the PWM buffer propagation delay from the PWM-ISO signal after the digital isolator to the gate signal. The second part is the overall propagation delay from the input PWM signal to the gate. The propagation delay of the digital isolator is inferred from the difference of these result. This is illustrated in Figure 24.

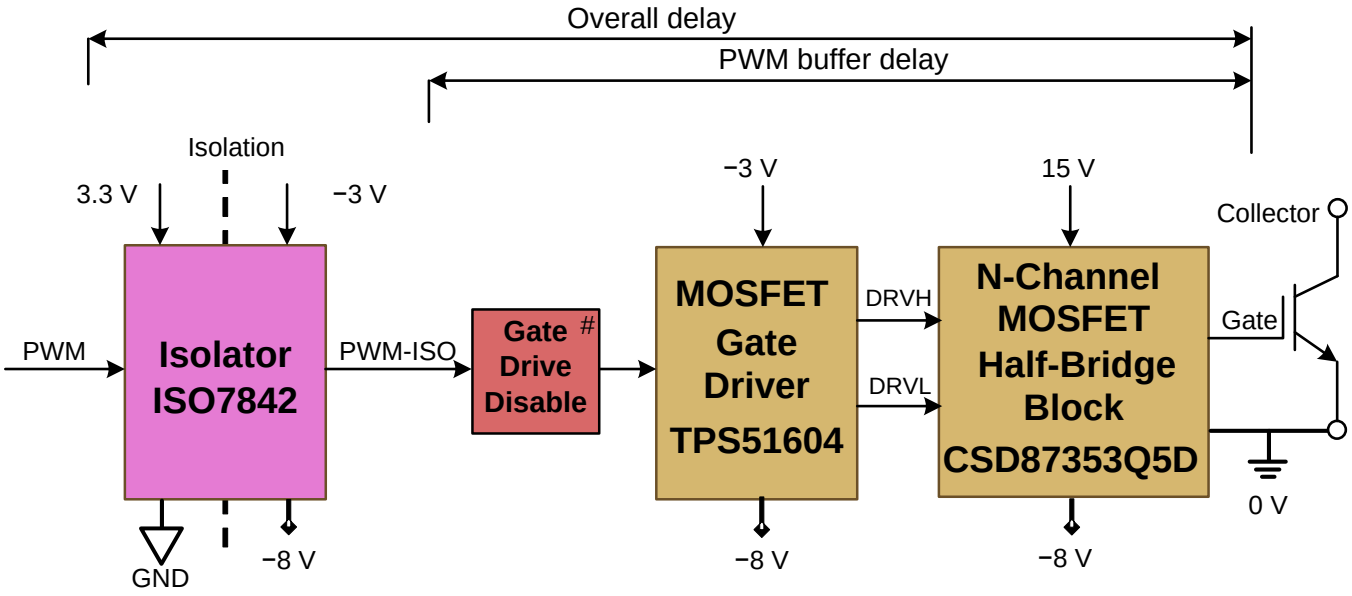

Figure 24. Propagation Delay Measurement Points

Test Condition

Figure 25 shows the test circuit used for the propagation delay. The IGBT module is the CM450DX-24S with an 800-V DC-link voltage across the half H-bridge. The Isolated IGBT Gate Driver drives the bottom IGBT and is powered from the TIDA-00199. The gate of the top IGBT is kept turned-off with a –8-V from isolated power supply.

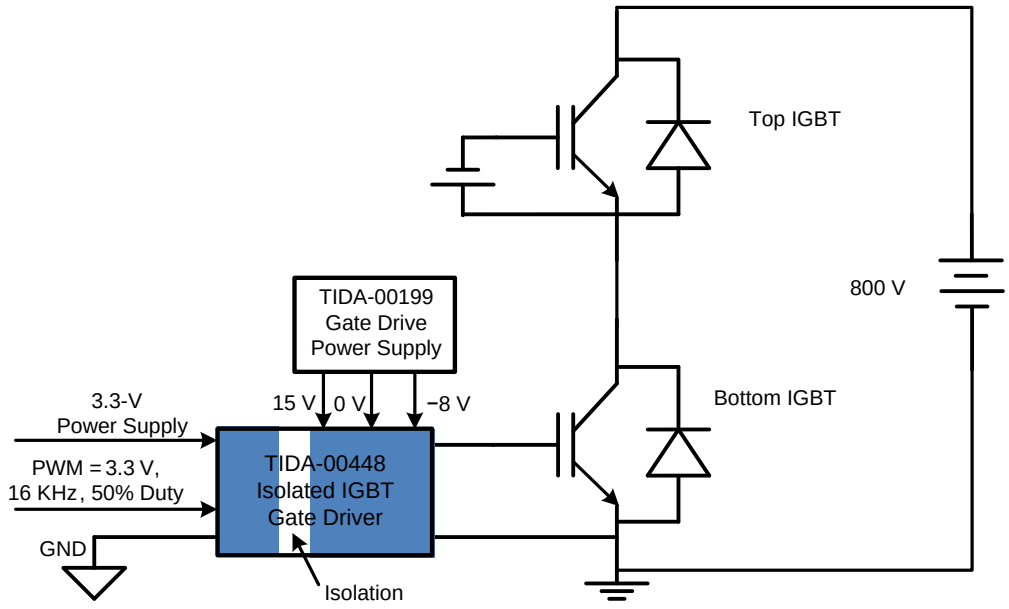

Figure 25. Propagation Delay Test Diagram

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6.1.1 PWM Buffer Propagation Delay

The propagation delay from PWM-ISO to the TPS51604 output for the rising edge of PWM are presented in Figure 26 to Figure 28.

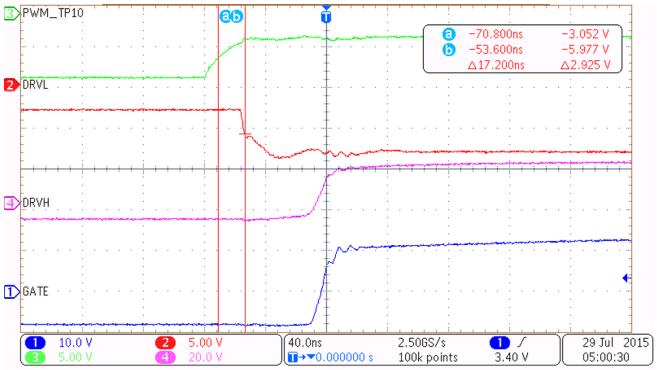

Figure 26. PWM-ISO to DRVL (Rising Edge)

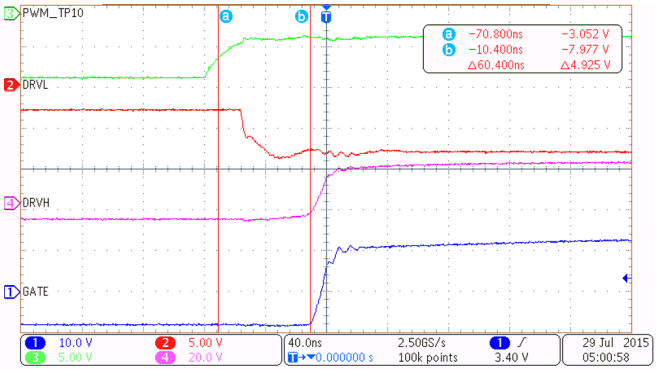

Figure 27. PWM-ISO to DRVH (Rising Edge)

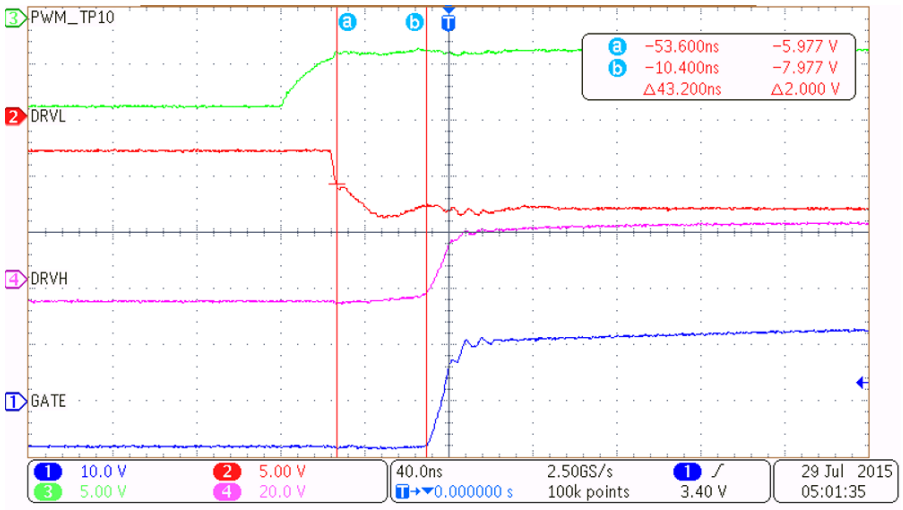

Figure 28. Dead Time Between DRVL and DRVH (Rising Edge)

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Propagation delay from PWM-ISO to TPS51604 output for falling edge of PWM are presented in Figure 29 to Figure 31.

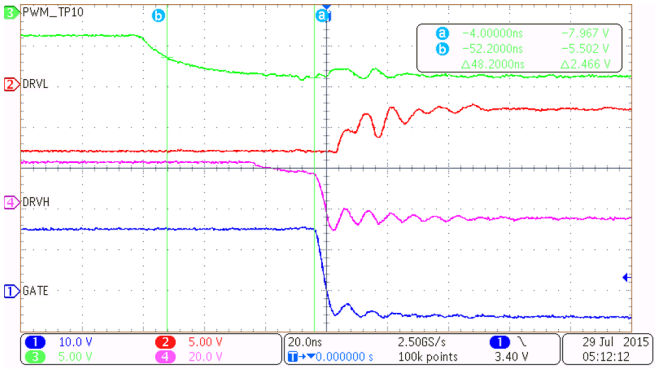

Figure 29. PWM-ISO to DRVH (Falling Edge)

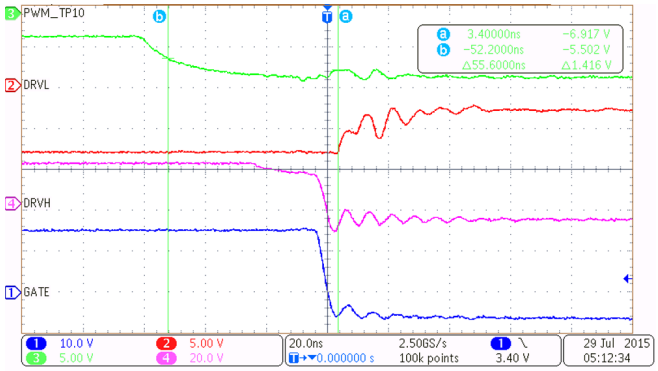

Figure 30. PWM-ISO to DRVL (Rising Edge)

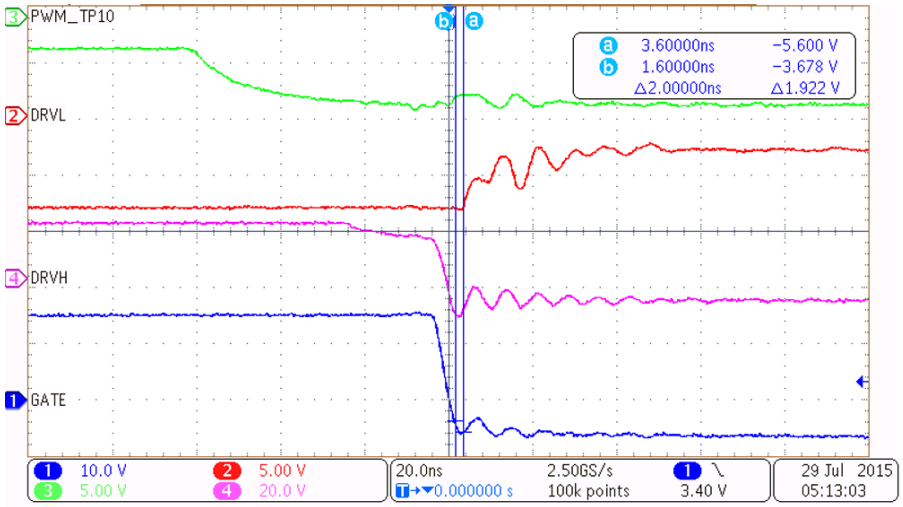

Figure 31. Dead Time Between DRVH and DRVL (Falling Edge)

Table 5. PWM Buffer Propagation Delay Results

PROPAGATION MEASUREMENT	TIME
Propagation delay PWM-ISO to DRVL (Rising edge)	17.2 ns
Propagation delay PWM-ISO to DRVH (Rising edge)	60 ns
Dead time between DRVL to DRVH(Rising edge)	43.2 ns
Propagation delay PWM-ISO to DRVH (Falling edge)	48.2 ns
Propagation delay PWM-ISO to DRVL (Falling edge)	55.60 ns
Dead time between DRVL to DRVH (Falling edge)	2 ns

The PWM buffer propagation delays are observed be slightly greater than the TPS51604 datasheet as expected.

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6.1.2 Overall Propagation Delay

NOTE: The oscilloscope channels have to be isolated for this test, as signal on CH1 and CH3 are measured with different references. CH1: Gate signal is measured referenced to 0 V, CH3: PWM input is measured referenced to GND.

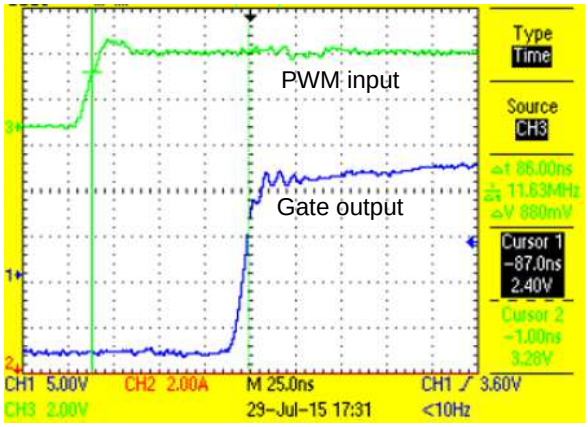

Figure 32. Overall Propagation Delay (Rising Edge)

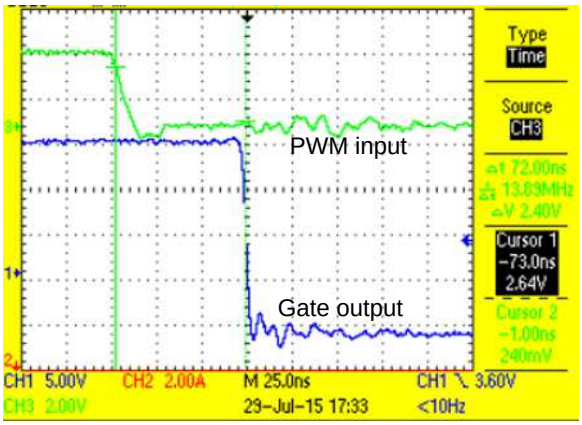

Figure 33. Overall Propagation Delay (Falling Edge)

Table 6. Overall Propagation Delay Results

PROPAGATION MEASUREMENT	TIME
Propagation delay (Rising edge)	86 ns
Propagation delay (Falling edge)	72 ns

The overall propagation delay is observed to be slightly greater than the sum of the propagation delays from the TPS51604 and ISO7842 digital isolator datasheets.

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6.2 Min and Max Gate Pulse Duration at 16 kHz

The test circuit for the min and max gate pulse duration is shown in Figure 34 and Figure 35.

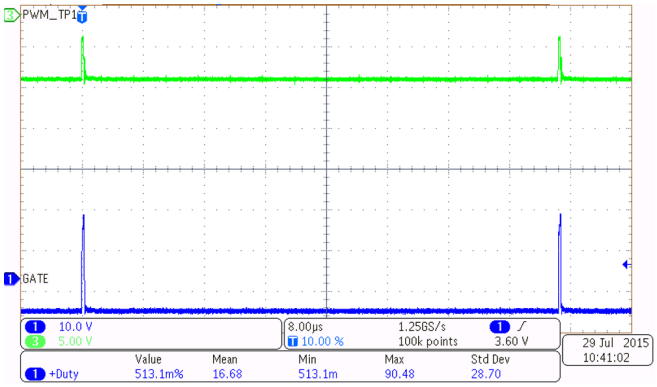

Figure 34. Min Gate Pulse

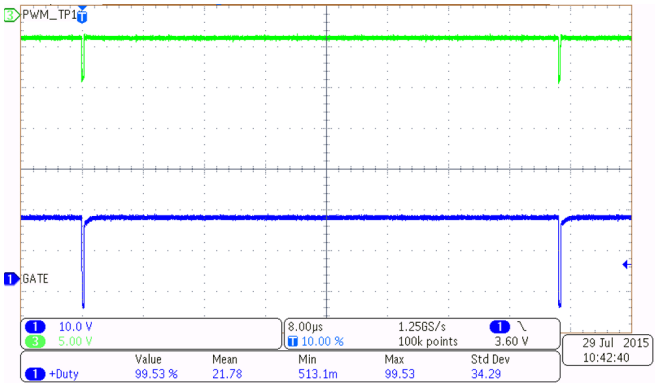

Figure 35. Max Gate Pulse

Table 7. Min and Max Gate Pulse Results

MEASURED PARAMETER	VALUE
Min gate pulse on period	324.8 ns
Min duty at F = 16 kHz	0.51%
Max gate pulse on time	62.23 µs
Max duty at F = 16 kHz	99.53%

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6.3 Maximum Gate Sink/Source Currents

The max source and sink current test is done using the test circuit shown in Figure 36. A capacitive load emulates an IGBT with a high gate capacitance. The gate resistors are modified for R_{g_on} = 0.5 Ω and R_{g_off} = 0.166 Ω.

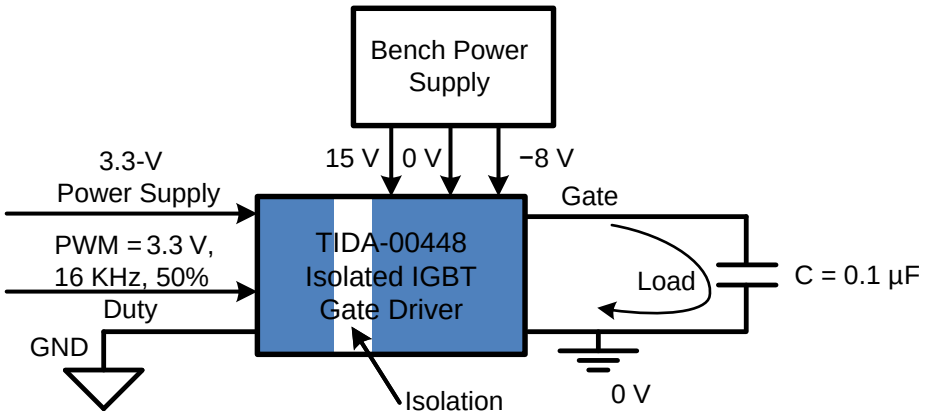

Figure 36. Test Circuit for Maximum Gate Sink/Source Currents

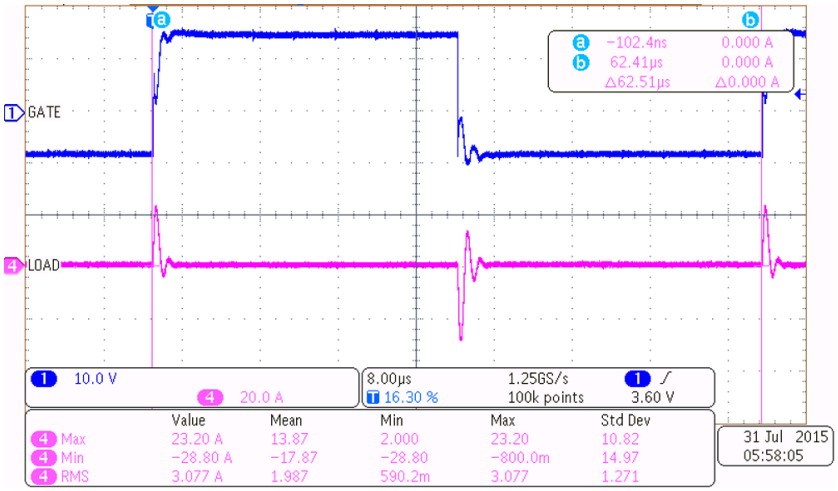

Figure 37. Maximum Gate Sink and Source Currents

Table 8. Maximum Gate Sink and Source Currents Results

MEASURED PARAMETER	VALUE
Max source current	23.2 A
Max sink current	28.8 A

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6.4 Miller-Induced Voltage

The Miller-induced voltage on the bottom IGBT gate is measured using the test circuit shown in Figure 38. This is done with two Isolated IGBT Gate Driver boards, one connected to the top IGBT and one to the bottom IGBT. Each board is powered from individual isolated outputs from the TIDA-00199. The bottom IGBT is kept off while the top IGBT gate is pulsed. The Miller-induced voltage is a function of circuit conditions like the IGBT module capacitance and dv/dt of the V_{CE} across the IGBT. However, the gate drive has to make sure the gate voltage does not cross the turn-on threshold of the IGBT. The Isolated IGBT Gate Driver does this by turning off the IGBT with a negative voltage of –8 V.

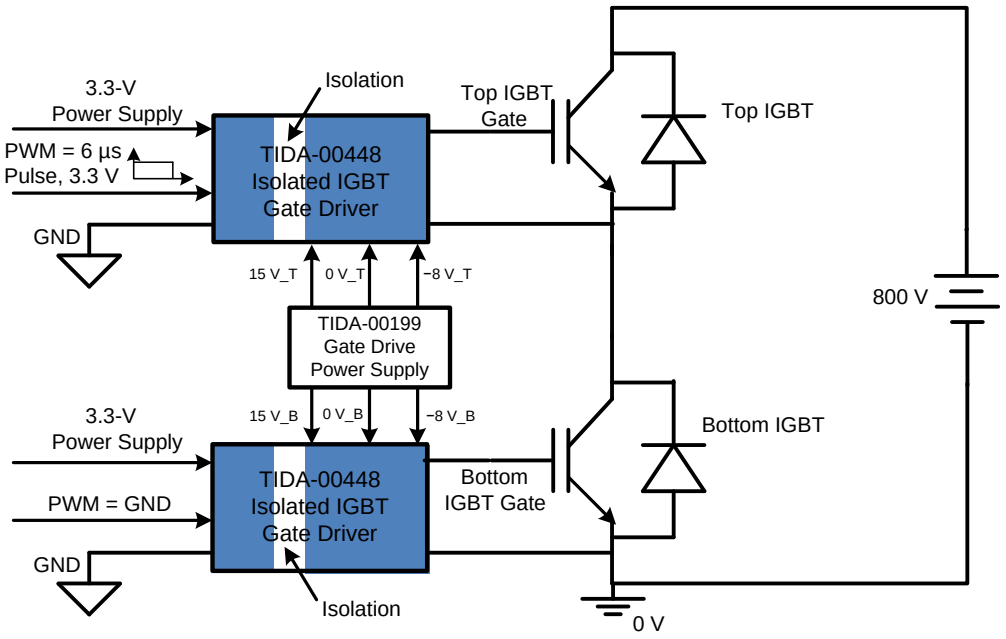

Figure 38. Test Circuit to Measure Miller-Induced Voltage

Figure 39 shows a dV/dt of 10 kV/µs across the bottom IGBT cause a Miller-induced voltage of 1.4 V.

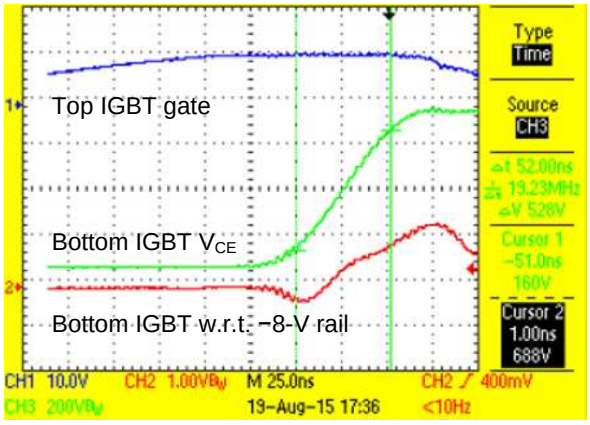

Figure 39. dV/dt of 10 kV/µs Across Bottom IGBT

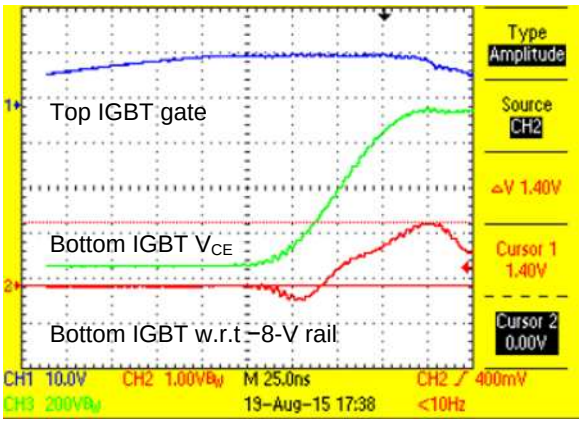

Figure 40. Miller Capacitance Induced Voltage

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6.5 Undervoltage Protection

The UVLO is tested using a bench power supply to power the Isolated IGBT Gate Driver. The 15-V rail is varied. Figure 41 shows when the 15-V rail is slowly increased. When the UVLO signal goes high, the PWM-ISO signal on the secondary side of the digital isolator is pulled down when the UVLO signal is active. Figure 42 is the graph when the 15-V rail is slowly decreased. The UVLO signal goes low to indicate the UVLO is active, which also pulls down PWM-ISO to disable the gate signal.

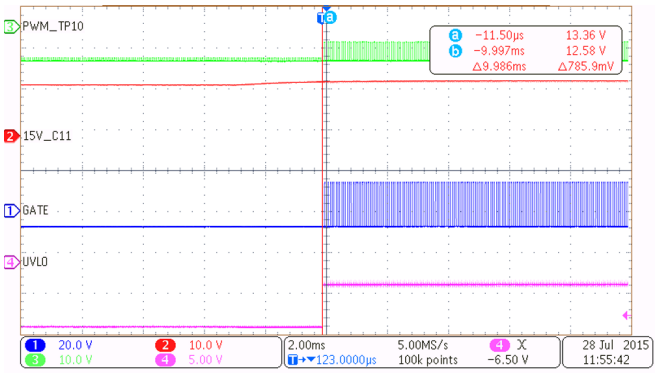

Figure 41. Voltage Rising on 15-V Rail

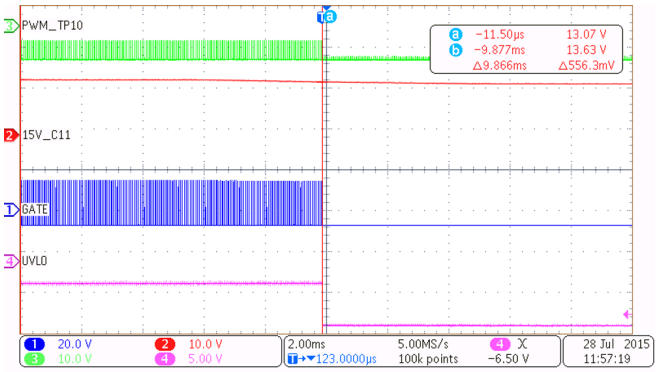

Figure 42. Voltage Falling on 15-V Rail

Table 9. UVLO Test Results

MEASURED PARAMETER	VALUE
Voltage at which 15-V rail come out of UVLO when 15-V rail is rising	> 13.36 V
Voltage at which 15-V rail enters UVLO when 15-V rail is falling	< 13.07 V

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6.6 DESAT Protection Test

To test the DESAT detection, a short circuit test is done, where a high current flows due to a shoot-through from the top IGBT to the bottom IGBT. This is accomplished by keeping the top IGBT on using 15 V from the TIDA-00199 power supply and turning on the bottom IGBT using the Isolated IGBT Gate Driver (see Figure 43). The bottom IGBT is driven by a single-shot pulse with an on-time limited to 6 µs for safety.

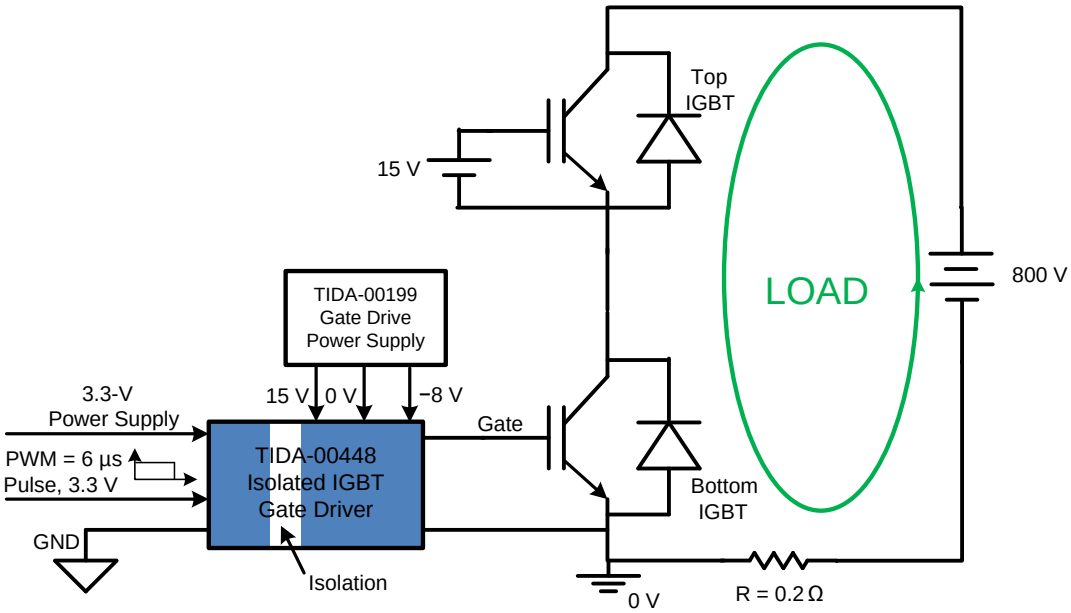

Figure 43. Test Circuit for Validating DESAT Protection

During the short circuit test, the gate voltage, the voltage across C8, V_{CE} of the bottom IGBT, and the load current (short circuit current) are captured. Figure 44 shows the normal operation.

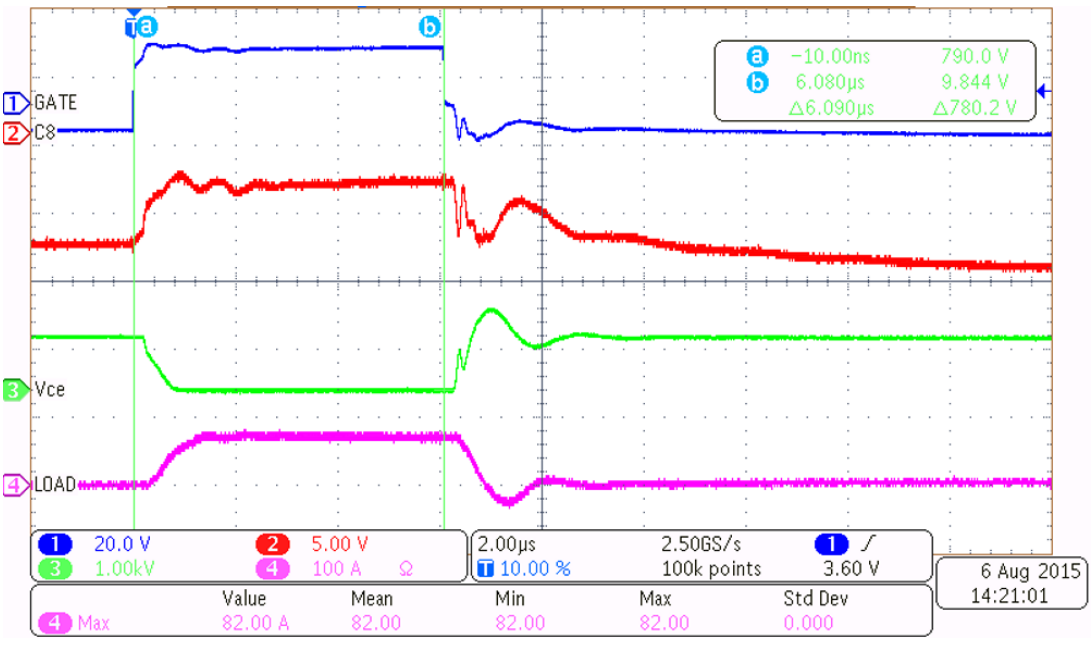

Figure 44. Normal Operation

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6.6.1 DESAT Detection, V_{CE} Threshold = 4.18 V, Reference Voltage = 3.6 V

Figure 45 to Figure 48 show the DESAT detection and soft turn-off operation when the V_{CE} threshold is 4.18 V. This is set by using a 3.6-V Zener diode to generate the reference voltage of the DESAT monitoring circuit (D4 = 3.6 V).

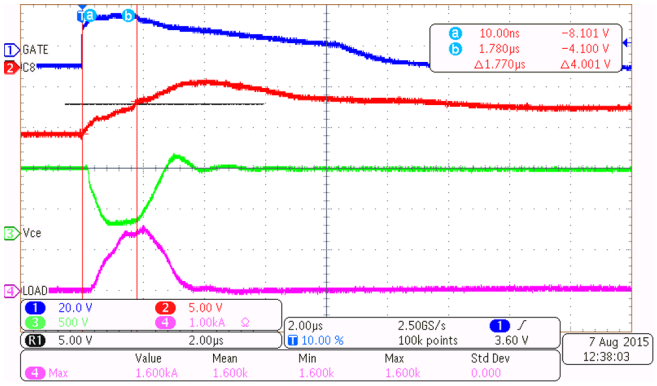

Figure 45. Fault Detection Time

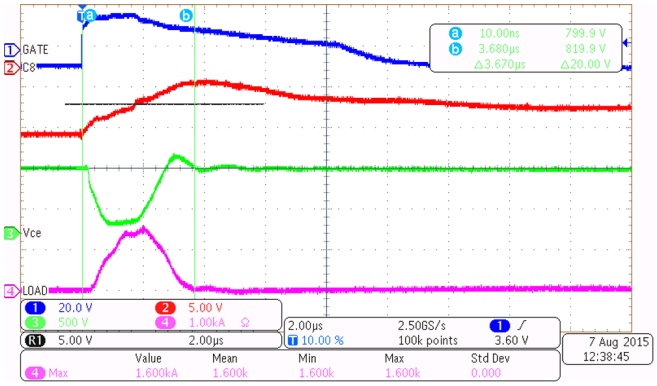

Figure 46. Overall Short Circuit Time

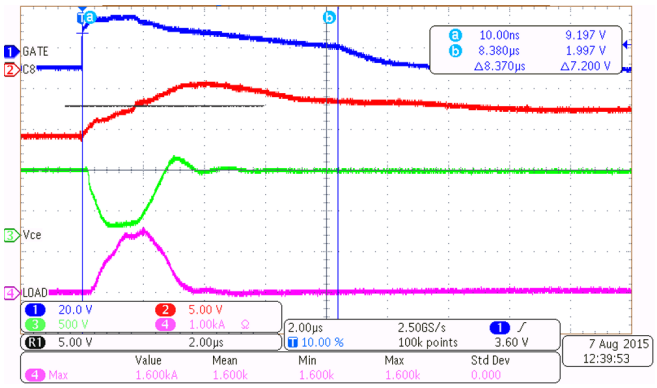

Figure 47. Activating Clamp When Gate Reaches 2 V

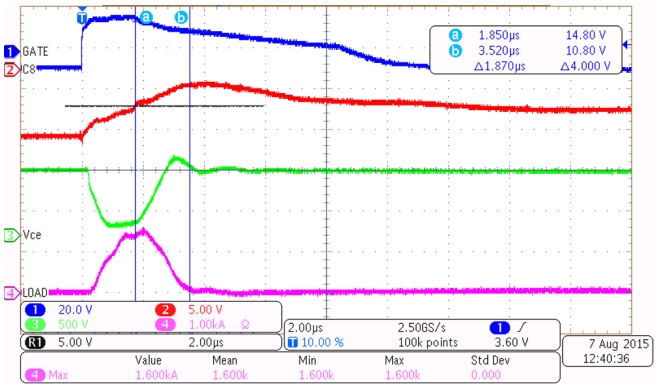

Figure 48. Soft Turn-off Time

The time taken to detect the fault or blanking time is 1.7 µs. The DESAT monitoring circuit latches; this can be inferred by the voltage across C8, which remains high after detection. The gate voltage drops slowly due to the soft turn-off. The soft turn-off time is 1.87 µs. In Figure 47, at 8.37 µs the gate waveform has a knee and discharges faster due to activating the clamp circuit to hold the gate at –8 V.

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6.6.2 DESAT, V_{CE} Threshold = 1.64 V, Reference Voltage = 3 V

Figure 49 shows the waveform from DESAT detection and soft turn off test with a V_{CE} threshold of 1.64 V. This is set by using 3.6-V Zener diode for D4 as reference voltage of the DESAT monitoring circuit.

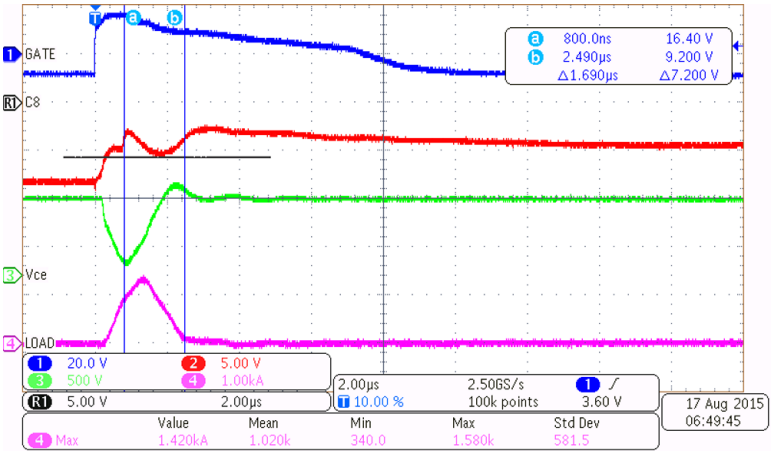

Figure 49. Soft Turn-off V_{CE} = 1.64 V

6.6.3 Configurable Soft Turn-off

The soft turn-off time is controlled by the gate discharge time. This can be configured by the values of resistors R5 and R31 in the soft turn-off circuit.

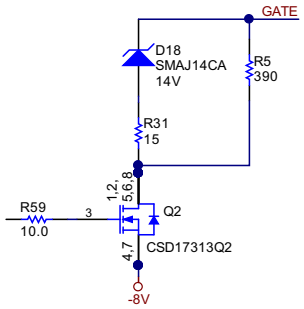

Figure 50. Soft Turn Configured Using R5 and R31

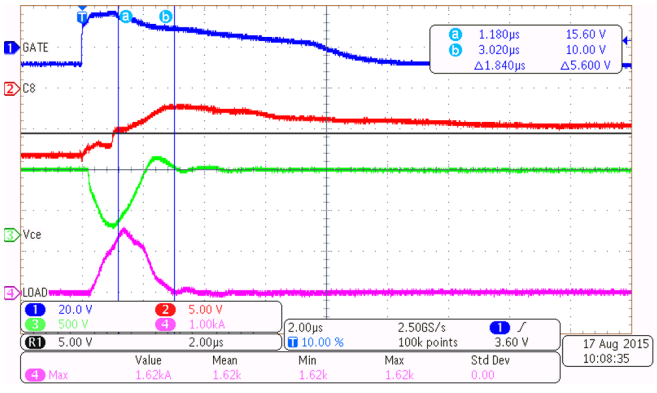

Figure 51. R5 = 680 Ω and R31 = 20 Ω

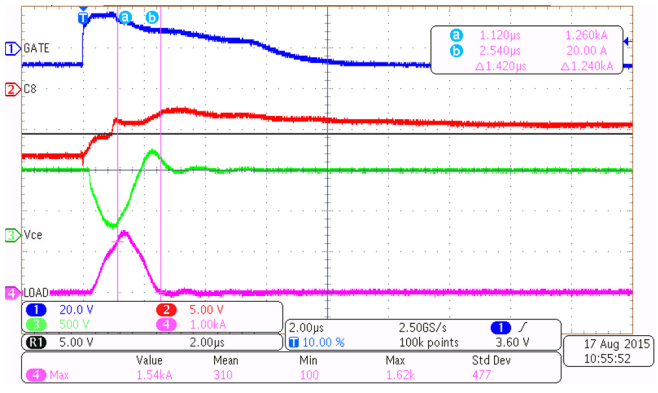

Figure 52. R5 = 390 Ω and R31 = 15 Ω

The soft turn-off time with R5 = 680 Ω and R31 = 20 Ω is 1.84 µs, and the gate turn-off time with R5 = 390 Ω and R31 = 15 Ω is 1.42 µs. Also, the amount of V_{CE} overshoots is smaller for a longer soft turn-off time.

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6.6.4 Fault Signal Delay

Figure 53 shows the time when the PWM signal is applied at the input of the digital isolator and the time when the DESAT condition is detected and reported at the $\overline{\text{FAULT}}$ signal at the input of digital isolator. The time taken is 2.02 µs. The DESAT fault is generated with the V_{CE} threshold at 4.18 V.

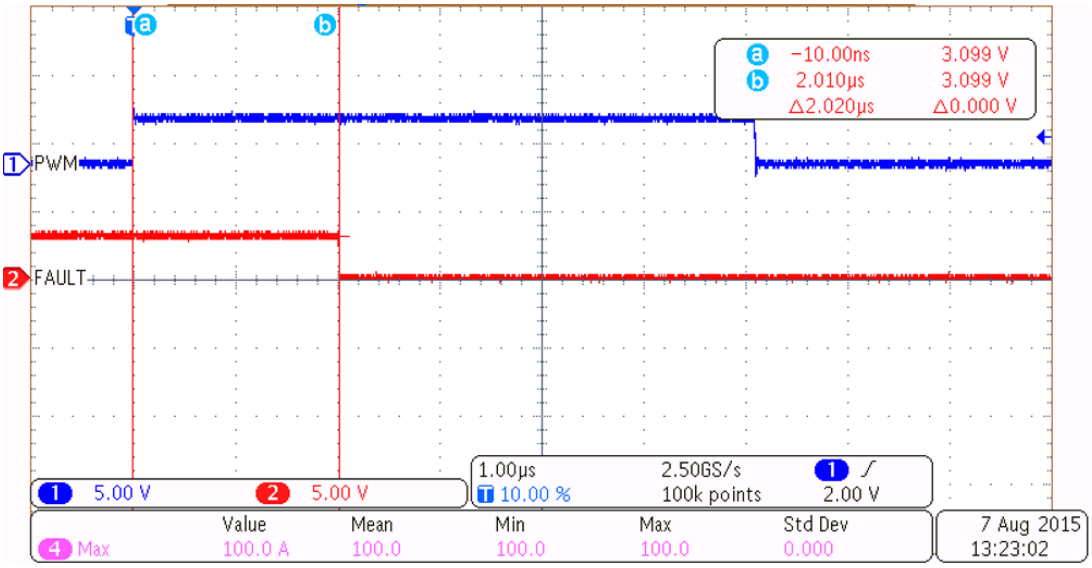

Figure 53. Propagation Delay From PWM Rising Edge to Fault Signal

6.6.5 RESET Signal Propagation Delay

Figure 54 shows the time when the RESET signal is applied at the input of the digital isolator and the time when the fault is cleared and reported at the $\overline{\text{FAULT}}$ signal at the input of digital isolator. The time taken is 1.28 µs.

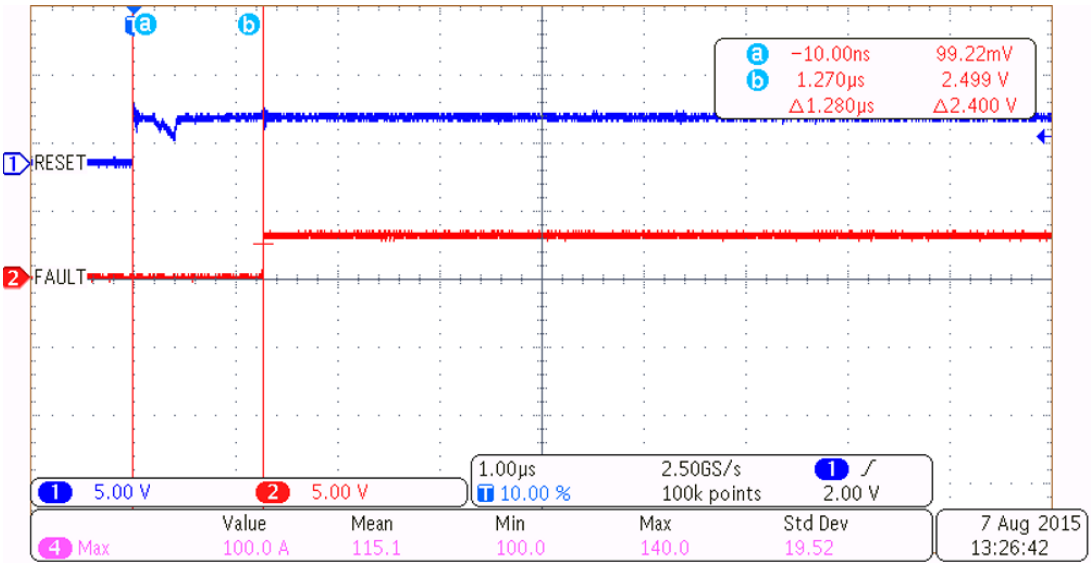

Figure 54. Propagation Delay From RESET Signal to FAULT Clear

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7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00448.

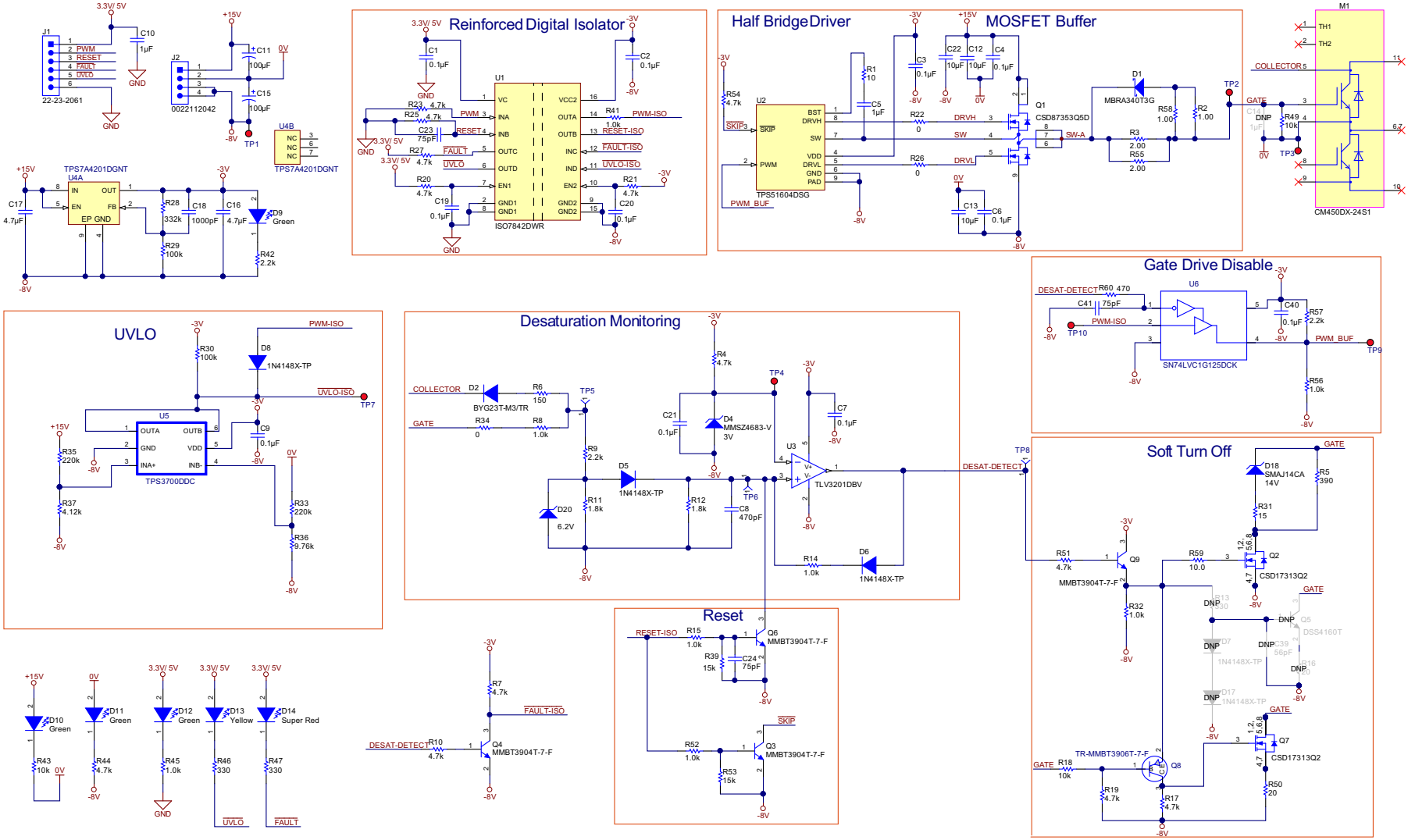

Figure 55. TIDA-00448 Schematic

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7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00448.

7.3 PCB Layout Guidelines

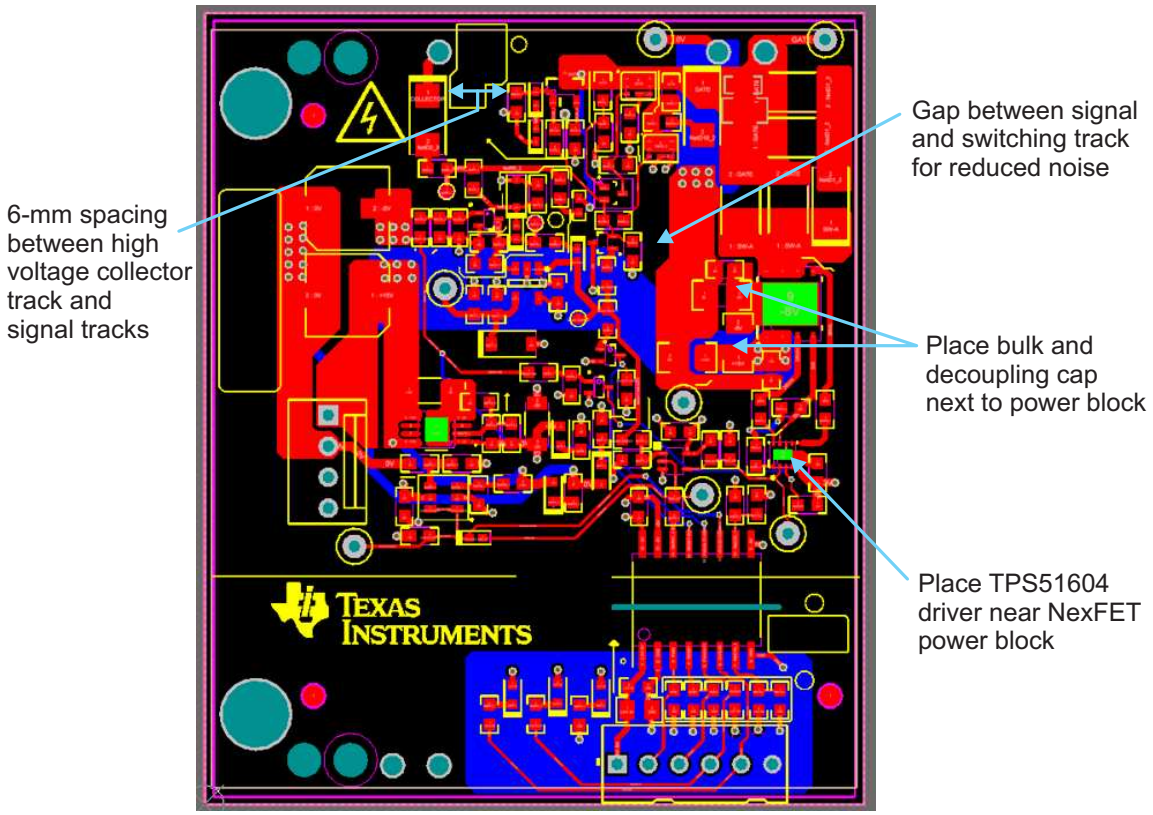

Figure 56. Layout Guidelines

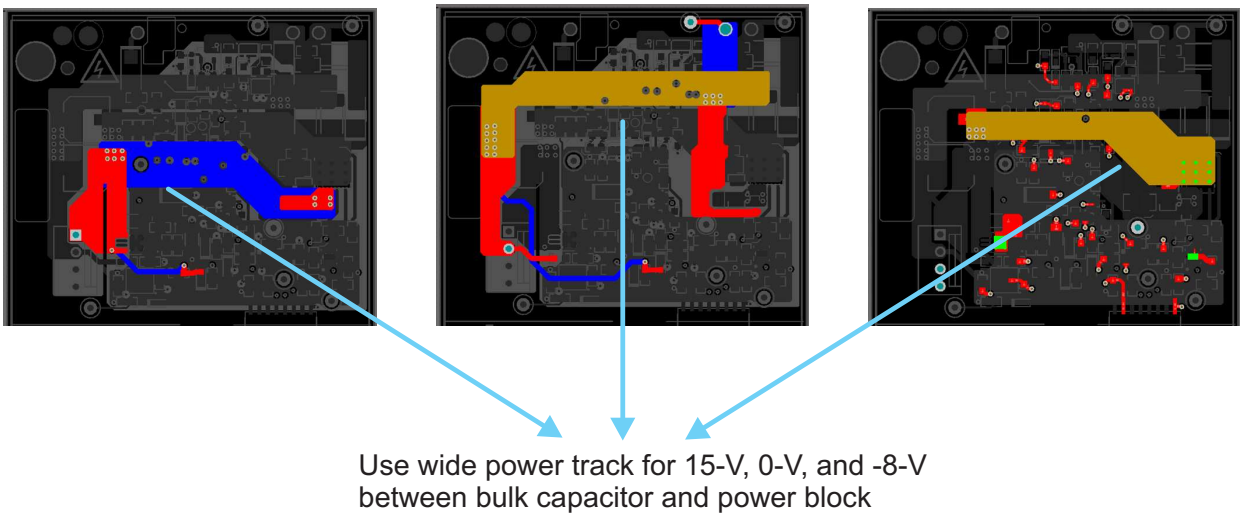

Figure 57. Layout Guidelines for Power Tracks

7.3.1 Layer Plots

To download the layer plots, see the design files at TIDA-00448.

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7.4 Gerber Files

To download the Gerber files, see the design files at TIDA-00448.

7.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00448.

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8 References

1. Texas Instruments, *Reinforced Isolated IGBT Gate-Drive Flyback Power Supply with Eight Outputs*, TIDA-00182 Design Guide (TIDU411)
2. Texas Instruments, *Isolated IGBT Gate-Drive Push-Pull Power Supply with 4 Outputs*, TIDA-00181 Design Guide (TIDU355)
3. Texas Instruments, *Wide-Input Isolated IGBT Gate-Drive Fly-Buck™ Power Supply for Three-Phase Inverters*, TIDA-00199 Design Guide (TIDU670)
4. Texas Instruments, *Isolated IGBT Gate-Drive Fly-Buck™ Power Supply with 4 Outputs*, TIDA-00174 Design Guide (TIDU478)
5. Texas Instruments, *Isolated IGBT Gate Driver Evaluation Platform for 3-Phase Inverter System*, TIDA-00195 Design Guide (TIDUA15)

9 Terminology

CMTI— Common Mode Transient Immunity

DESAT— Desaturation

IGBT— Insulated Gate Bipolar Transistor

PWM— Pulse Width Modulation

MCU— Microcontroller Unit

FETs, MOSFETs—Metal Oxide Semiconductor Field Effect Transistor

10 About the Author

NELSON ALEXANDER is a systems engineer at Texas Instruments where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Nelson has been with TI since 2011 and has been involved in designing products related to smart grid and embedded systems based on microcontrollers. Nelson earned his bachelor of technology in electrical engineering at MSRIT, Bangalore.

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Revision History

Changes from Original (September 2015) to A Revision	Page
• Changed from preview page	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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