Test Data
For PMP10652
06/1/2015

Contents

1. Design Specifications

Vin Minimum	**4.8VDC**
Vin Maximum	**30 VDC(OVP at 20V)**
Vout1	**3.3 VDC_Slave**
Iout 1	**0.5A**
Vout2	**1.2VDC_Slave**
Iout 2	**4A**
Vout3	**3.3VDC_Master**
Iout 3	**0.500A**
Vout4	**1.2VDC_Master**
Iout4	**4A**
Vout5	**1.8V_PLLDVDD**
Iout5	**0.6A**
Vout6	**1.5V_AVDD**
Iout6	**0.6A**
Vout7	**5V_CAN**
Iout7	**140mA**
Vout8,9,10	**Linear Reg for noise sensitive supply**
Approximate Switching Frequency	**2.1MHz Approx(all the DC/DC converters)**
ISO Pulse test	**TVS diode used for protection**
EMI	**CISPR25 Class 3 (Class 5 upto 30MHz domain)**
Protection	**Input Overvoltage, Reverse polarity , Short Circuit protections at Outputs, Load Dump protection**

2. Circuit Description and PCB details

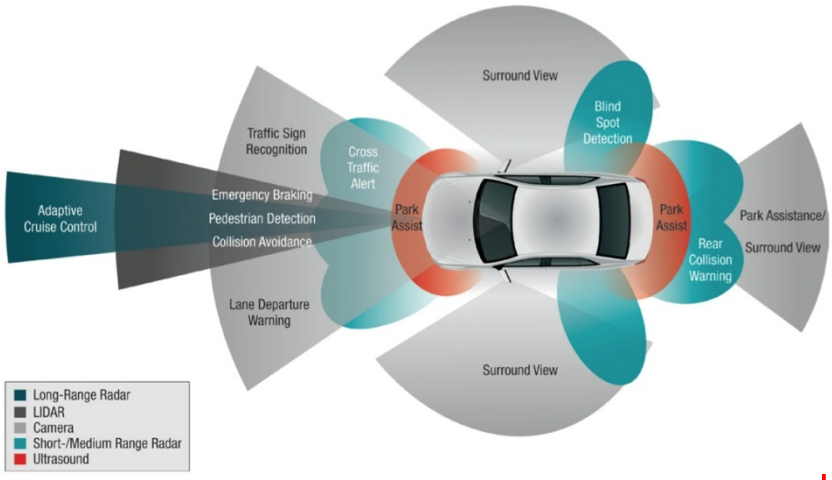
PMP10652 is a System optimized (CISPR 25 Class 3) 30W design for Surround View ADAS system.

The design has various protections such as Load dump through TVS (ISO pulse testing), Reverse Voltage (Innovative Smart diode with very low Iq), Battery Disconnect Switch with OVP protection (PFET) and is EMI optimized to meet Conductive EMI limits of CISPR25 Class3 (overall) and Class5 upto 30MHz Range .

Input voltage range is between 4.5V to 30V with OVP at 20V and hence will operate in Cold Cranking conditions.

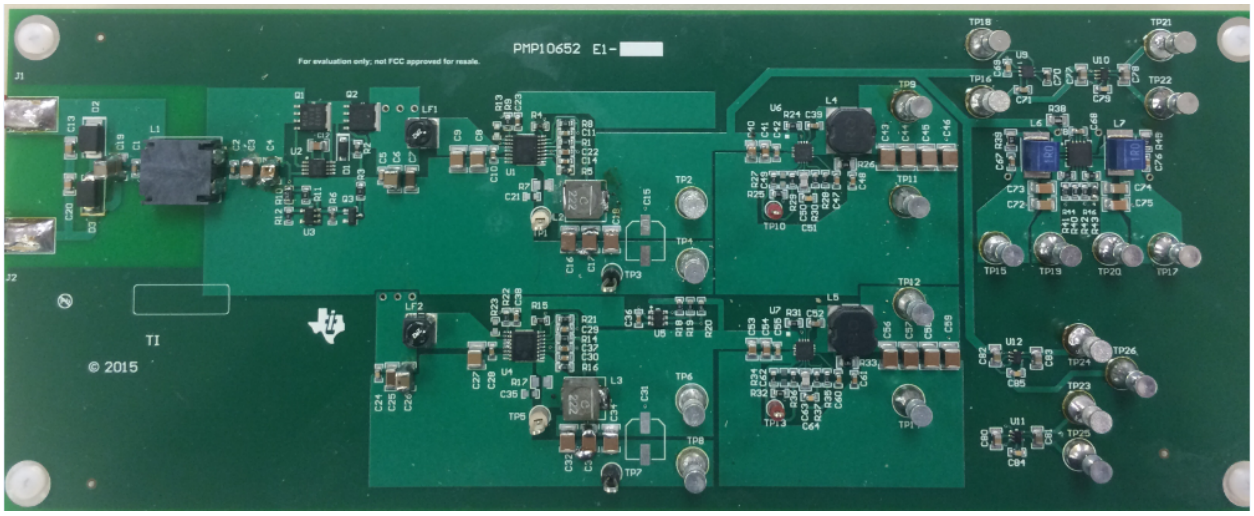
LM74610 is used for Battery reverse protection which utilizes a charge pump to drive an N-channel FET to provide a resistive path for the bypass current to flow. LM53603Q1 is used as front end DC/DC Buck converter which is 2.2MHz switching, Synchronous rectified Wide Vin Buck Converter which can take transient upto 42V .TPS57114Q1 is used to provide power to the cores and it is a high current 2,2MHz switching buck converter. LM26420 is a dual 2.2MHz switching buck converter which is used for generating other required supplies.

LM3880 sequencer is used for all the power up and power down sequencing requirements.

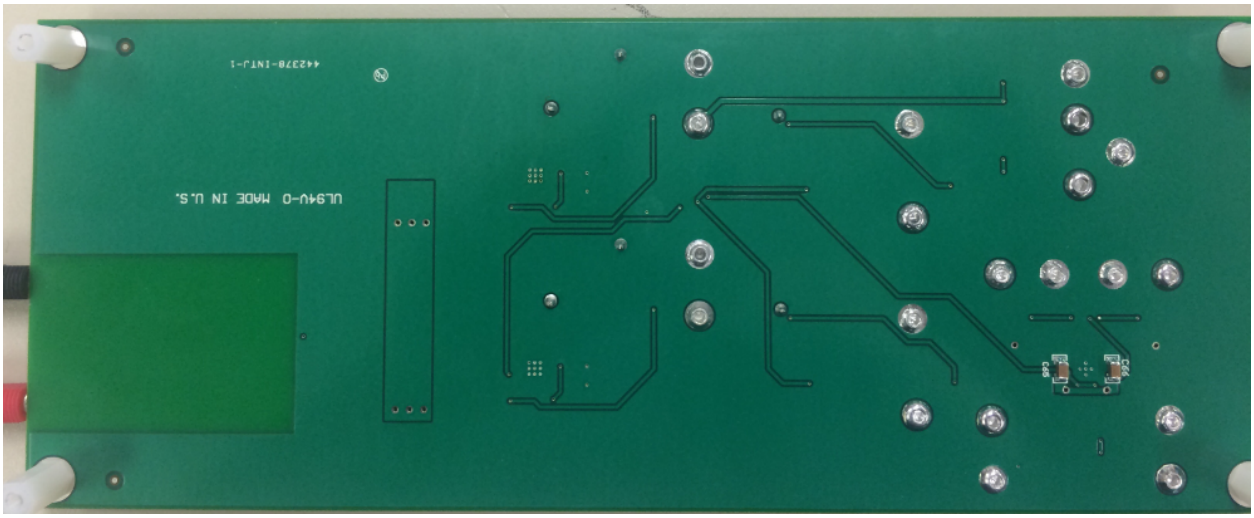


The Board dimension of PMP9487 PCB is 2500mil * 8000mil. Four layer PCB was used for the design.

3. PMP10652 Board Photos



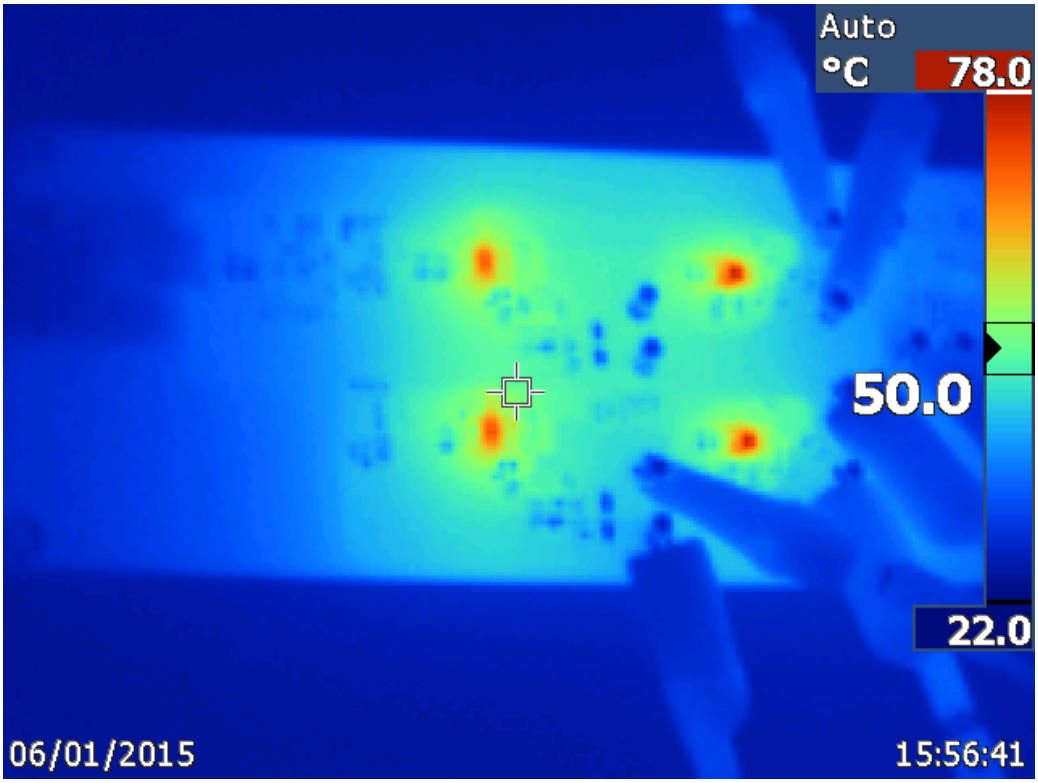
Board Photo (Top)

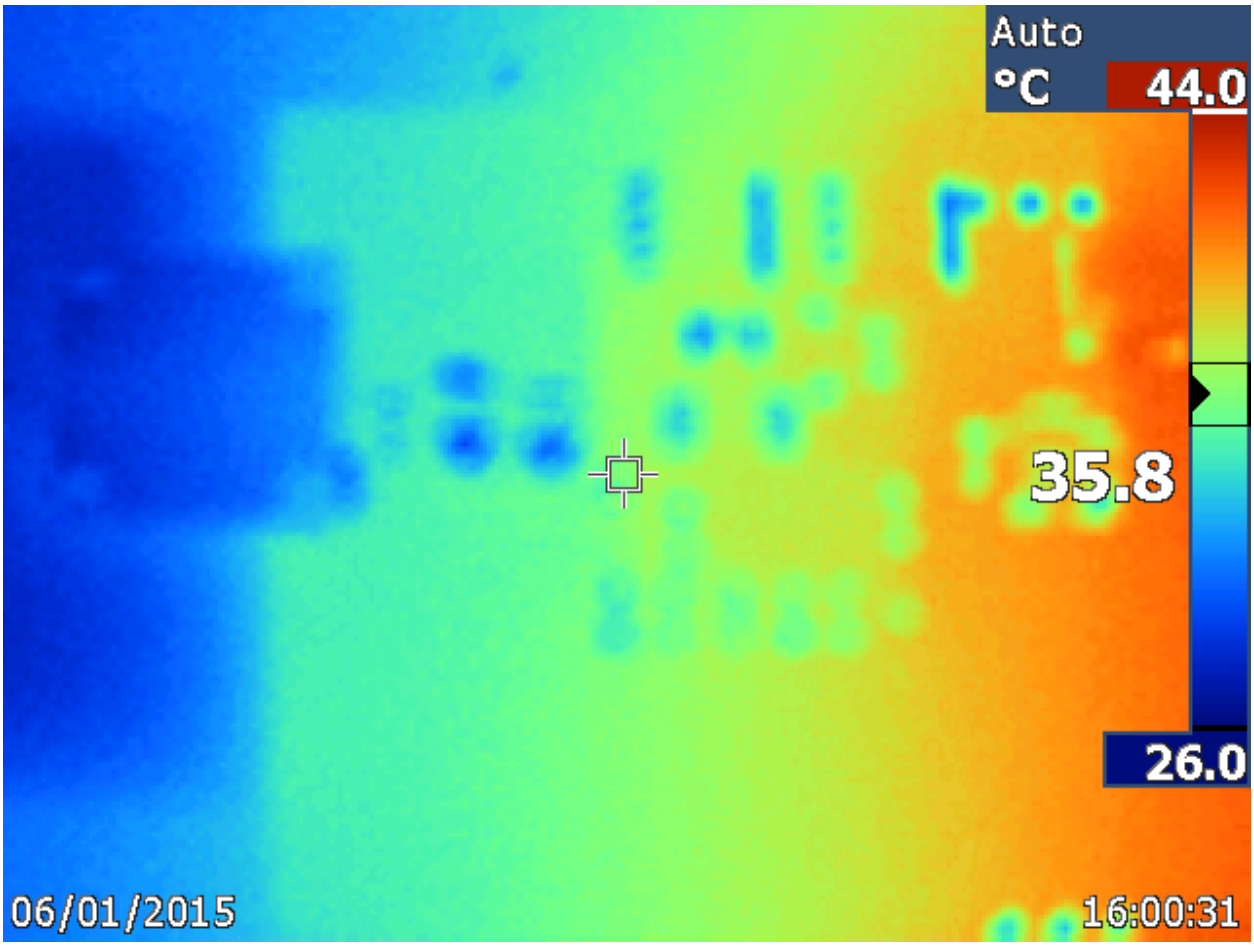


Board Photo (Bottom)

4. Thermal Data

IR thermal image taken at steady state with 12Vin and all the outputs at full load (no airflow)

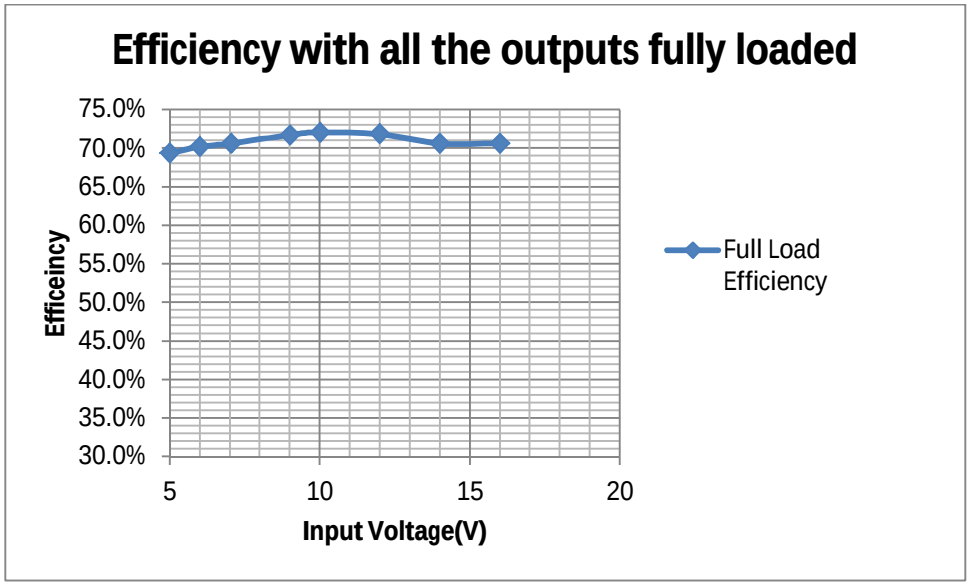




IR thermal image taken at steady state with 12Vin and Zoomed on protection FETs

5. Efficiency

5.1 Efficiency Chart – Input Voltage Vs Efficiency with all output fully Loaded



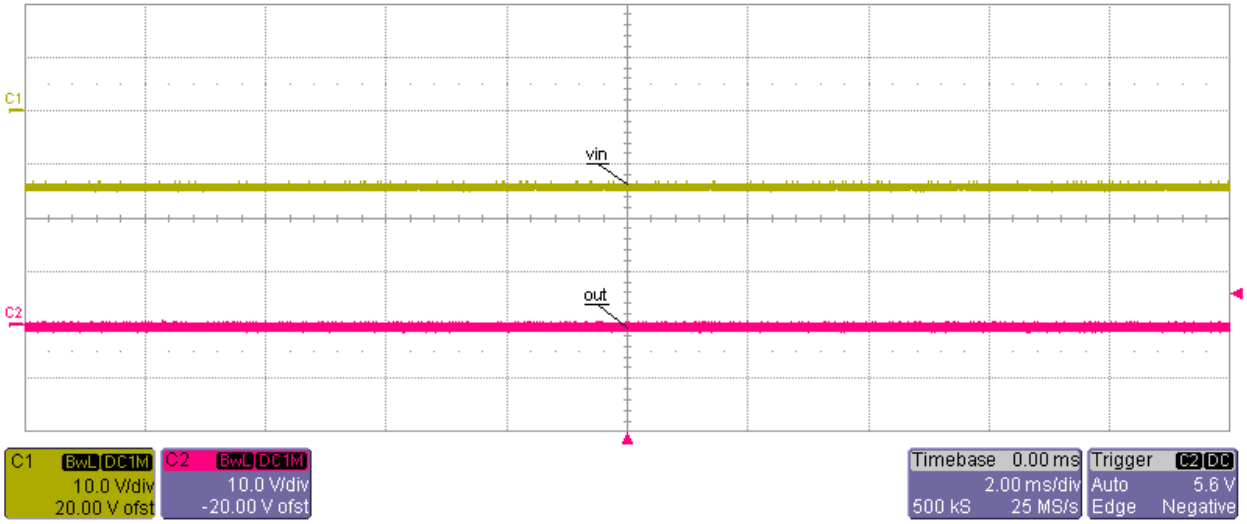
5.3 Efficiency Data

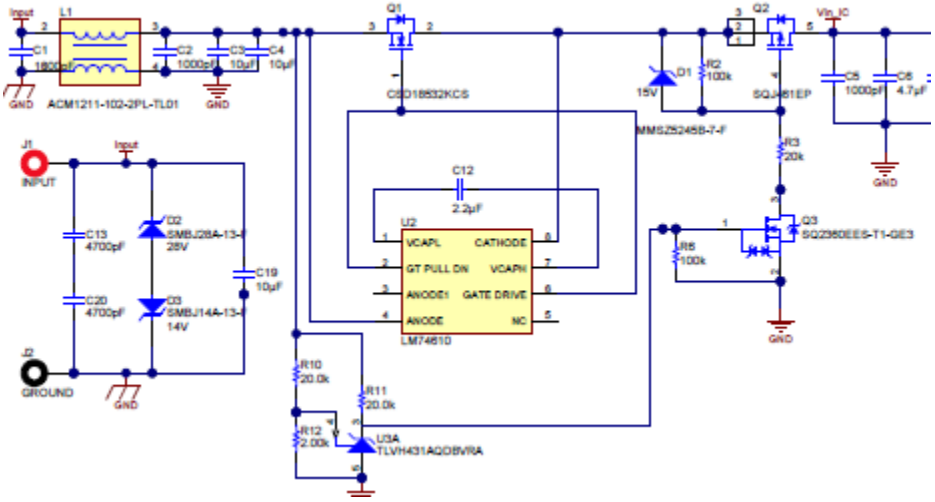
Efficiency of total System Vs Input Voltage

Vin (V)	Iin (A)	Vout 1 (V)	Iout 1(A)	Vout 2 (V)	Iout 2(A)	Vout 3 (V)	Iout 3(A)	Vout 4 (V)	Iout 4(A)	Vout 5 (V)	Iout 5(A)	Pin (W)	Pout (W)	Efficiency (%)
5	4.3	3.338	1	1.2	4	1.2	4	1.8	0.6	1.5	0.6	21.5	14.918	69.4%
6	3.54	3.338	1	1.2	4	1.2	4	1.8	0.6	1.5	0.6	21.24	14.918	70.2%
7.04	3	3.338	1	1.2	4	1.2	4	1.8	0.6	1.5	0.6	21.12	14.918	70.6%
9	2.31	3.338	1	1.2	4	1.2	4	1.8	0.6	1.5	0.6	20.79	14.918	71.8%
10	2.07	3.338	1	1.2	4	1.2	4	1.8	0.6	1.5	0.6	20.7	14.918	72.1%
12	1.73	3.338	1	1.2	4	1.2	4	1.8	0.6	1.5	0.6	20.76	14.918	71.9%
14	1.508	3.338	1	1.2	4	1.2	4	1.8	0.6	1.5	0.6	21.112	14.918	70.7%
16	1.32	3.338	1	1.2	4	1.2	4	1.8	0.6	1.5	0.6	21.12	14.918	70.6%

6. Waveforms

6.1 Reverse Protection –Smart diode

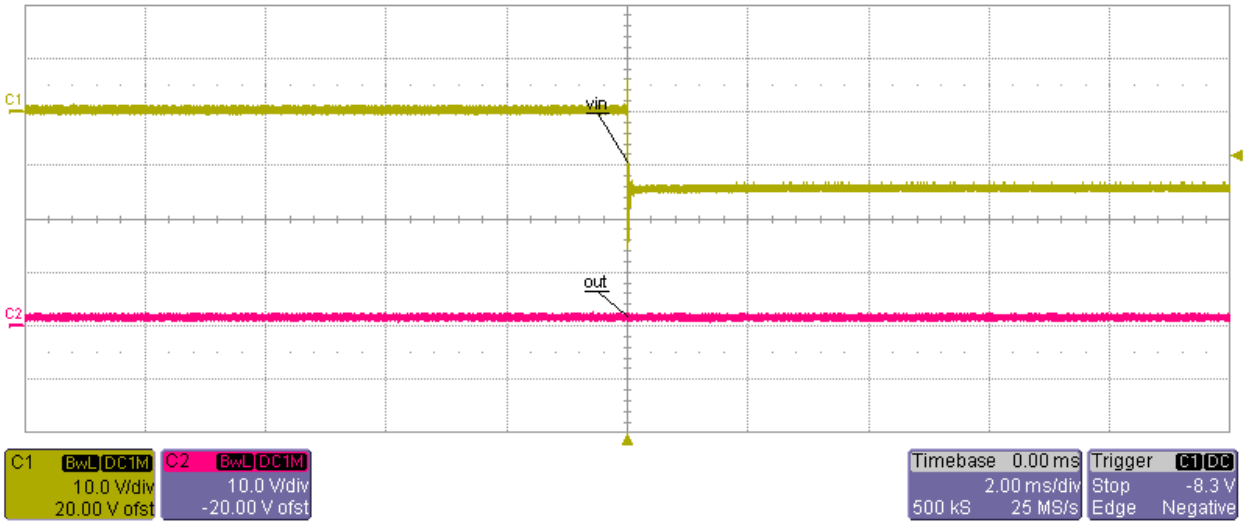




C1- Input

C2- Vin_IC

Continuous Reverse Voltage at Input

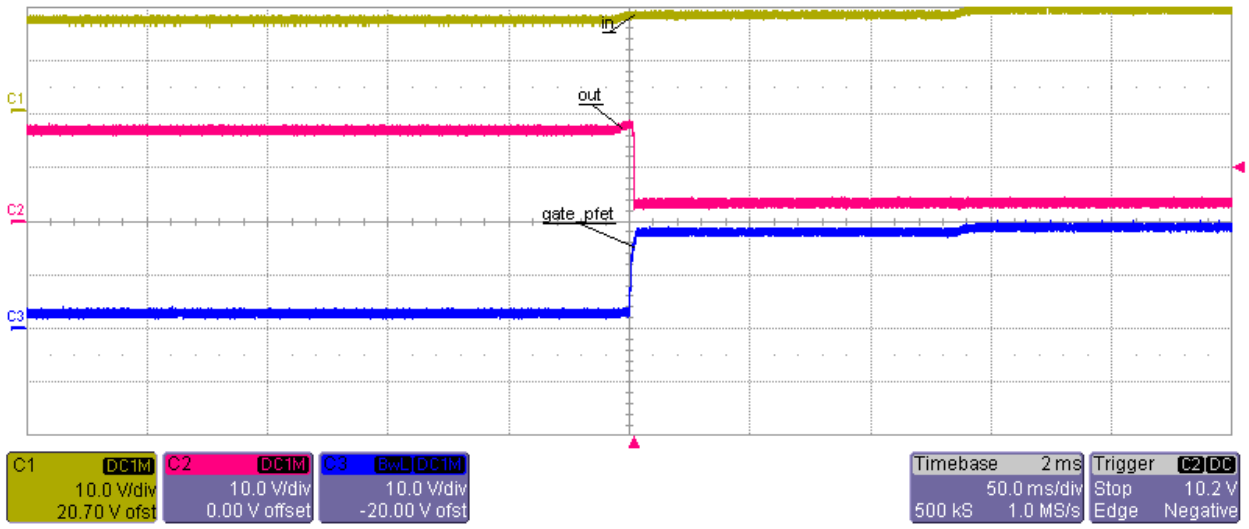


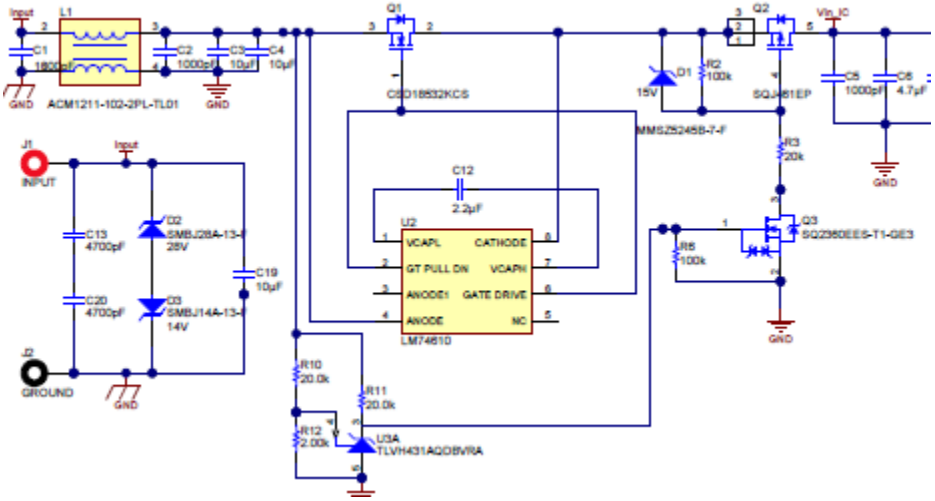
C1- Input

C2- Vin_IC

Transition to Reverse Voltage at Input

6.2 Input Overvoltage Protection – PFET Fault switch



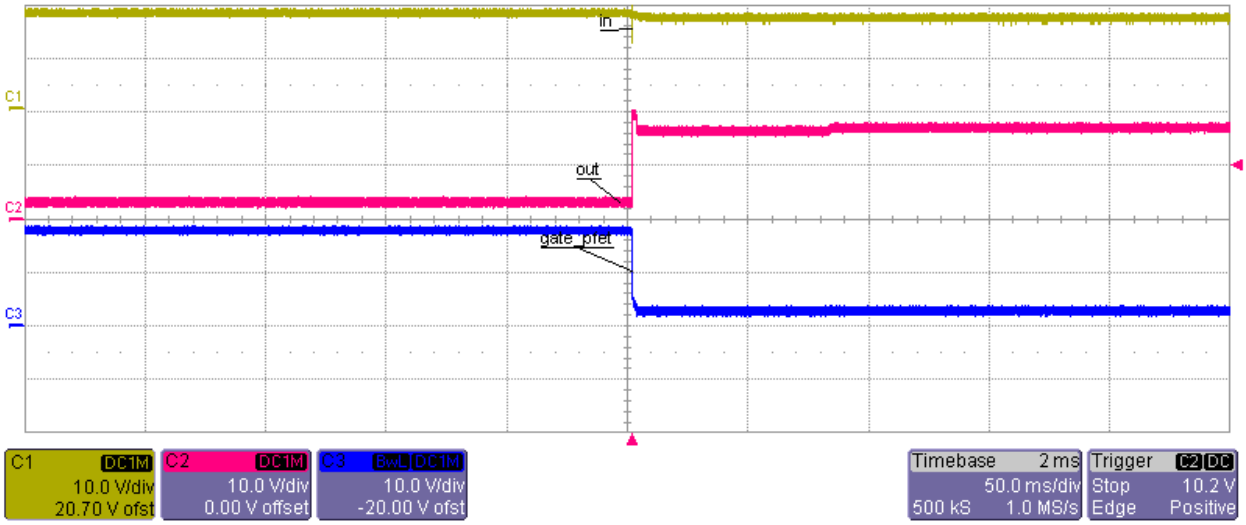


C1- Input

C2- Vin_IC

C3-Q2 PFET's gate

Transition to Overvoltage condition .



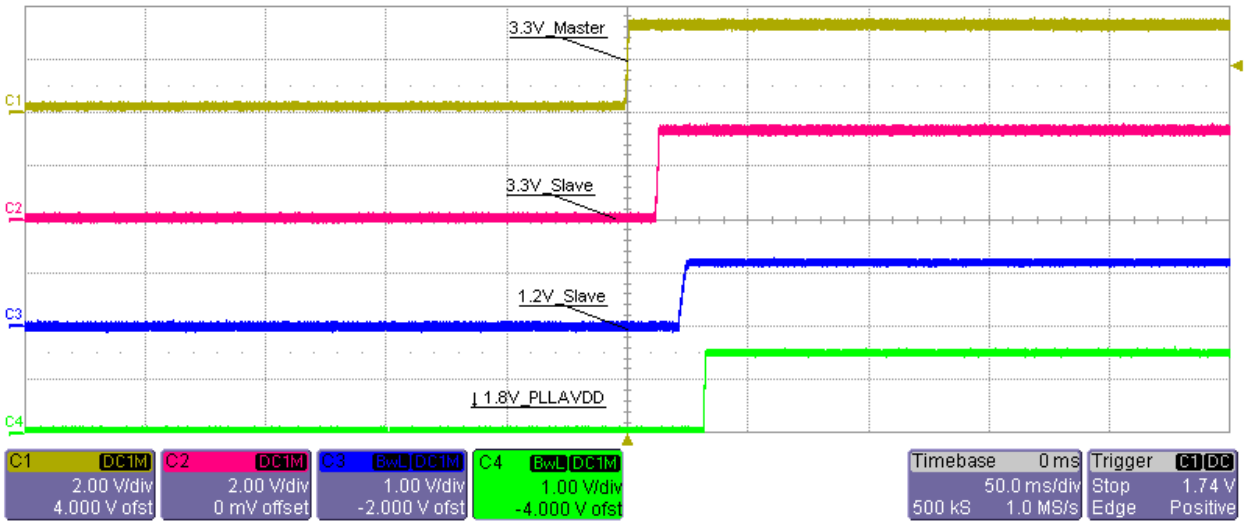
C1- Input

C2- Vin_IC

C3-Q2 PFET's gate

Transition From Overvoltage to normal condition

6.3 Power Up and Power Down sequencing – LM3880



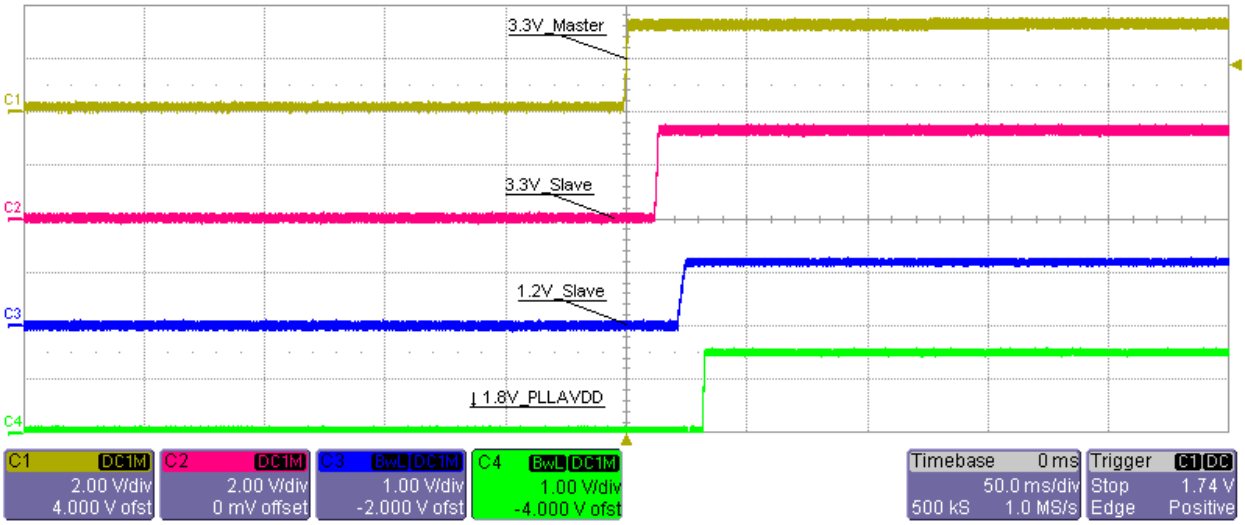
C1- 3.3V_Master

C2- 3.3V_Slave

C3-1.2V_Slave

C4-1.8V_PLLDVDD

No Load Power up sequencing at 12 Vin as per Controller's requirements



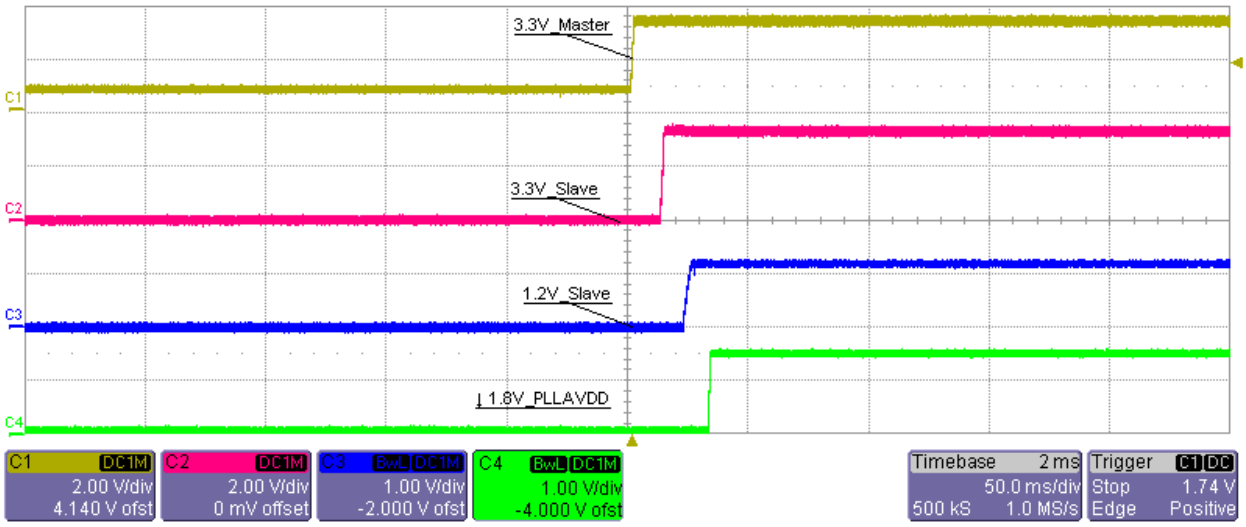
C1- 3.3V_Master

C2- 3.3V_Slave

C3-1.2V_Slave

C4-1.8V_PLLDVDD

No Load Power up sequencing at 4.5 Vin as per Controller's requirements



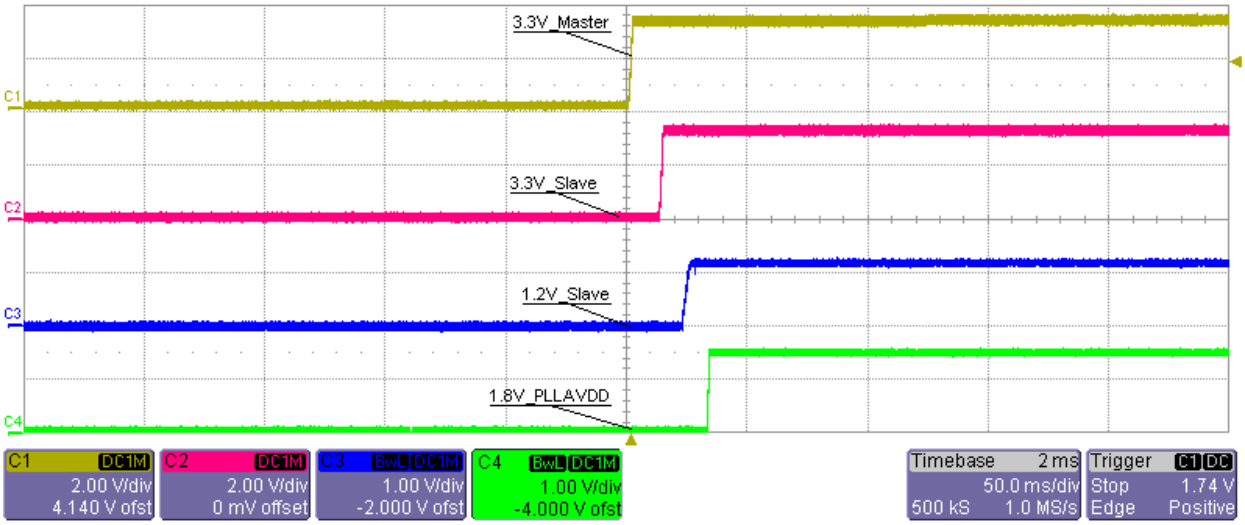
C1- 3.3V_Master

C2- 3.3V_Slave

C3-1.2V_Slave

C4-1.8V_PLLDVDD

Full Load Power up sequencing at 12 Vin as per Controller's requirements



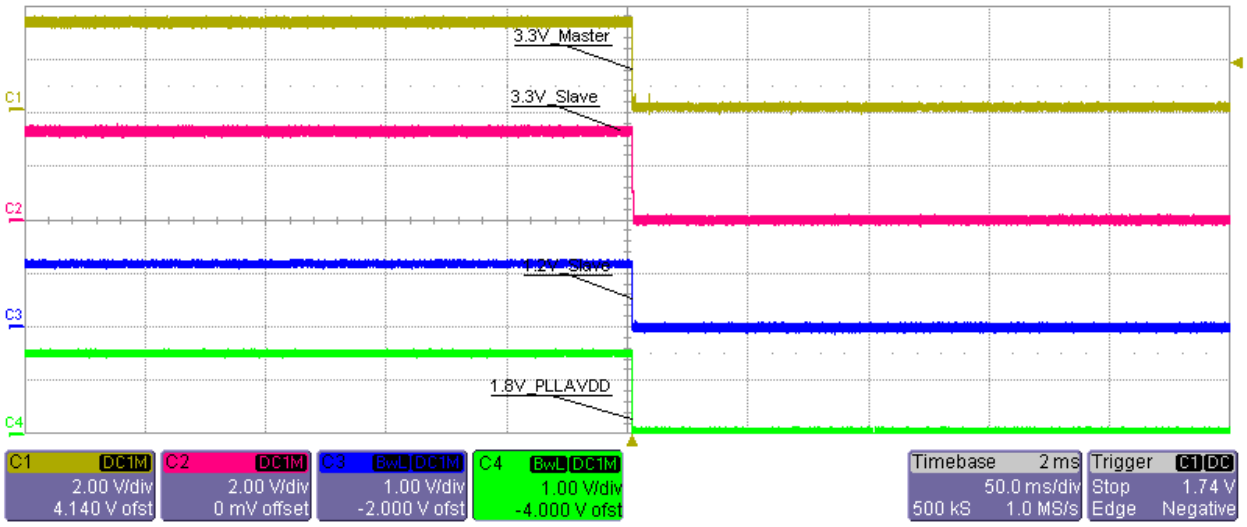
C1- 3.3V_Master

C2- 3.3V_Slave

C3-1.2V_Slave

C4-1.8V_PLLDVDD

Full Load Power up sequencing at 4.5 Vin as per Controller's requirements



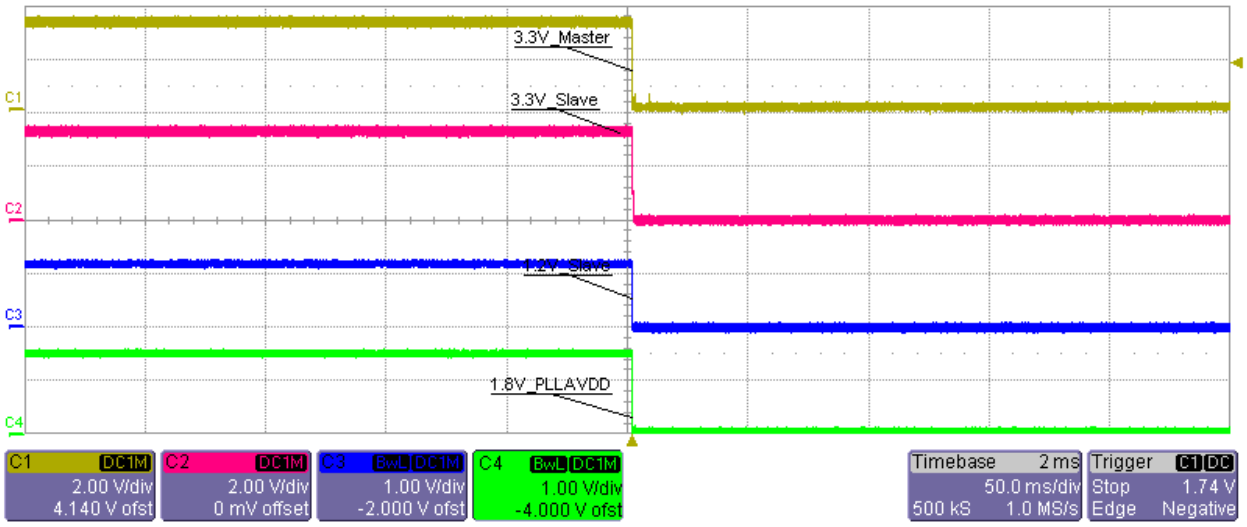
C1- 3.3V_Master

C2- 3.3V_Slave

C3-1.2V_Slave

C4-1.8V_PLLDVDD

Full Load Power down sequencing at 12 Vin as per Controller's requirements



C1- 3.3V_Master

C2- 3.3V_Slave

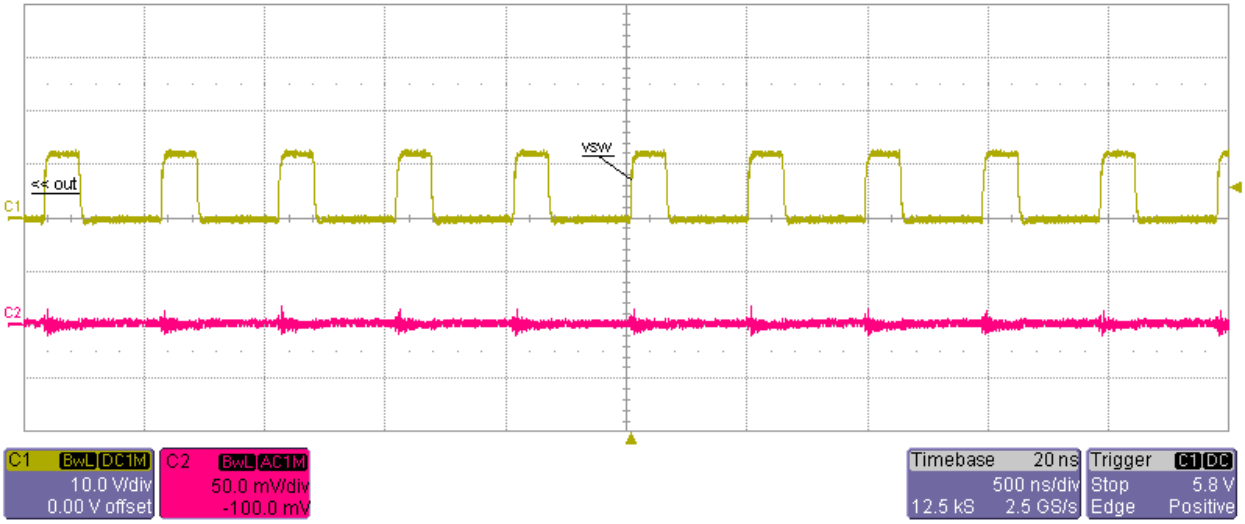
C3-1.2V_Slave

C4-1.8V_PLLDVDD

Full Load Power down sequencing at 4.5 Vin as per Controller's requirements

6.4 Output Voltage Ripple and Switch Node Voltage

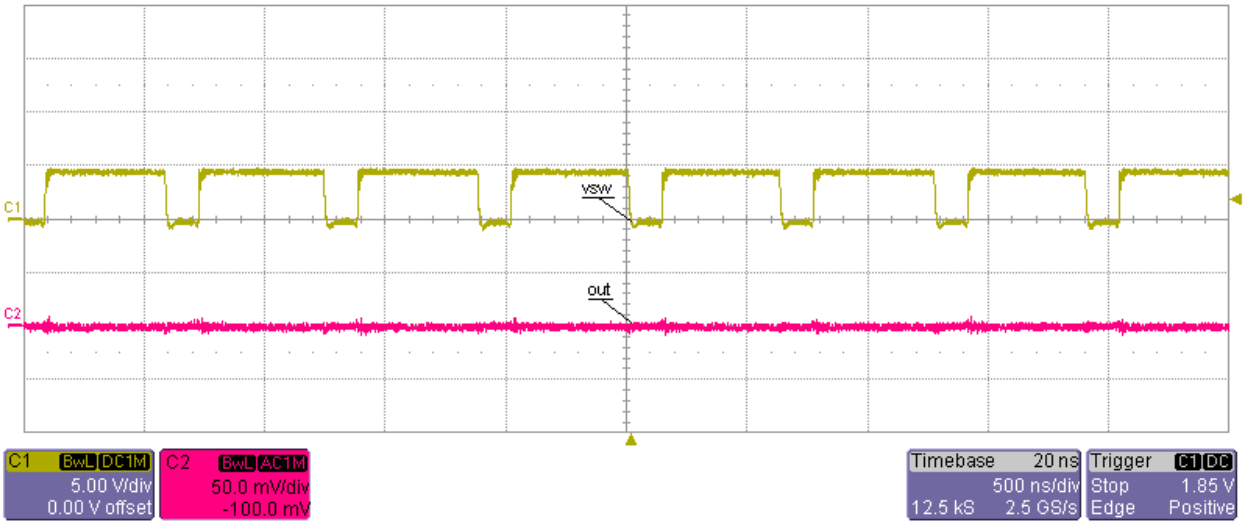
6.4.1 LM53603Q1 output -3.3Vout



Switch Node Voltage and Output Voltage Ripple at 12 Vin and Full Load on all the outputs (Vripple < 50mVp-p)

Ch2-Vout1 (AC Coupled)

Ch1-Switching Waveform

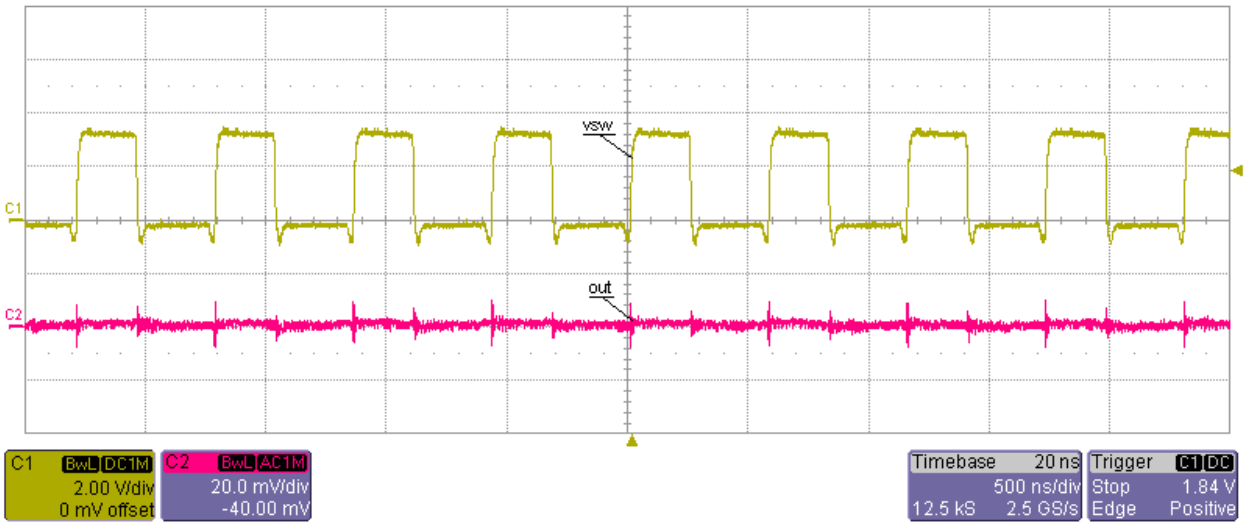


Switch Node Voltage and Output Voltage Ripple at 4.5 Vin and Full Load on all the outputs (Vripple < 50mVp-p)

Ch2-Vout1 (AC Coupled)

Ch1-Switching Waveform

6.4.2 TPS57114Q1 output – 1.2V

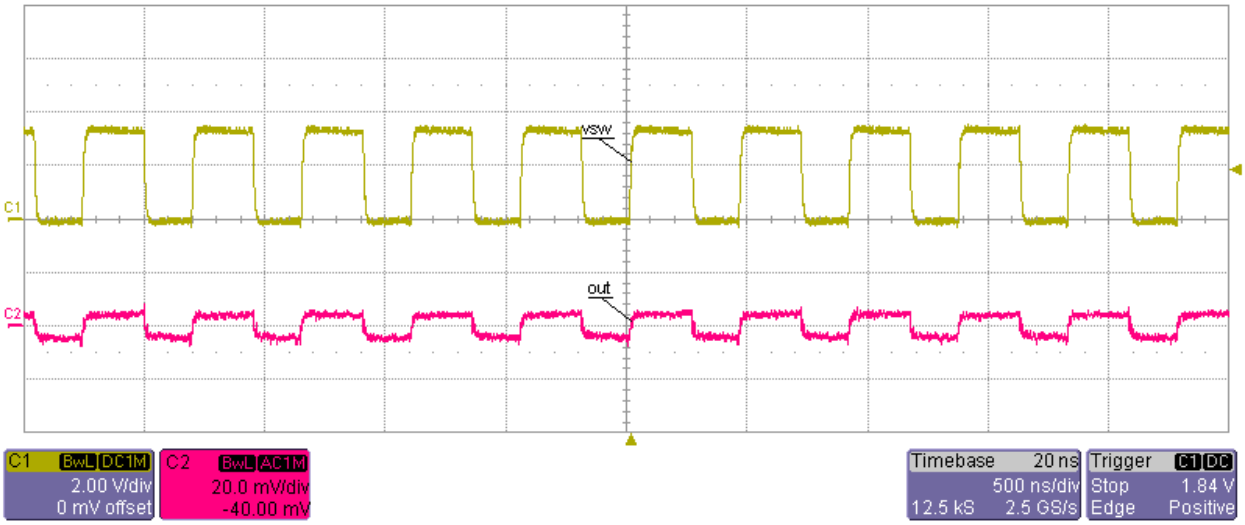


Switch Node Voltage and Output Voltage Ripple at 12 Vin and Full Load on all the outputs (Vripple < 50mVp-p)

Ch2-Vout2 (AC Coupled)

Ch1-Switching Waveform

6.4.3 LM26420Q1 Dual output – 1.8V and 1.5V

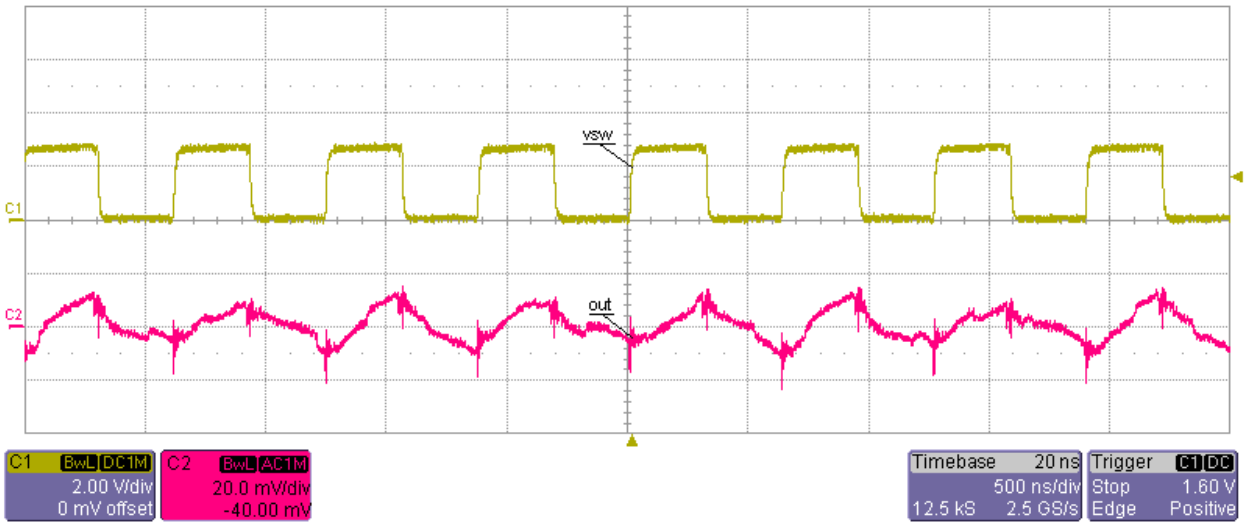


Switch Node Voltage and Output Voltage Ripple at 12 Vin and Full Load on all the outputs (Vripple < 50mVp-p)

Ch2-Vout5 (AC Coupled)

Ch1-Switching Waveform

6.4.4 TPS60150 Charge Pump output -5V



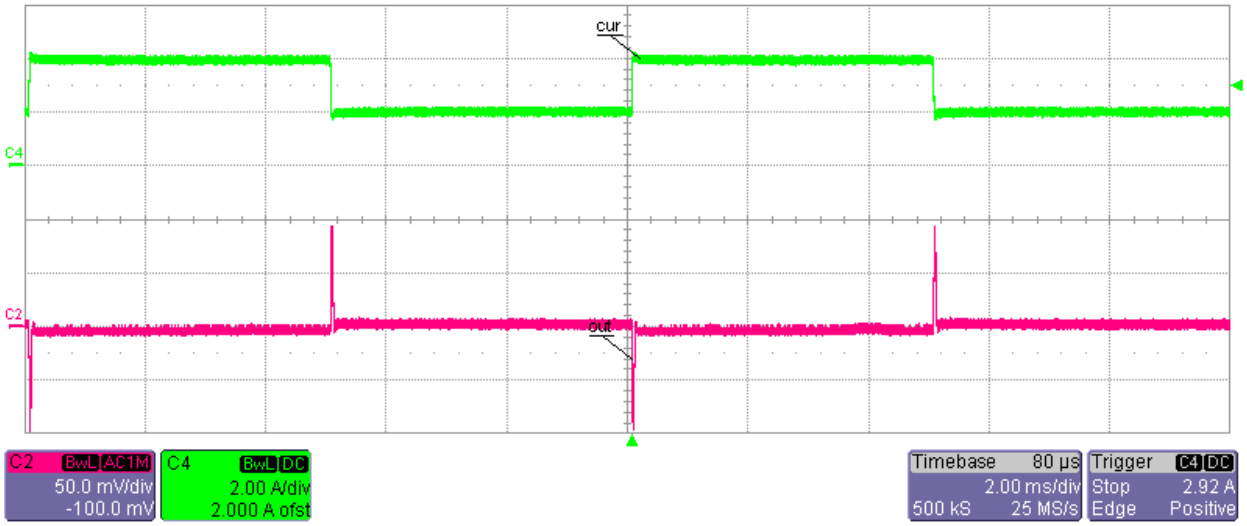
Switch Node Voltage and Output Voltage Ripple at 12 Vin and Full Load on all the outputs (Vripple < 50mVp-p)

Ch2-Vout7 (AC Coupled)

Ch1-Switching Waveform

6.5 Load Transient Response

6.5.1 TPS57114Q1 outputs

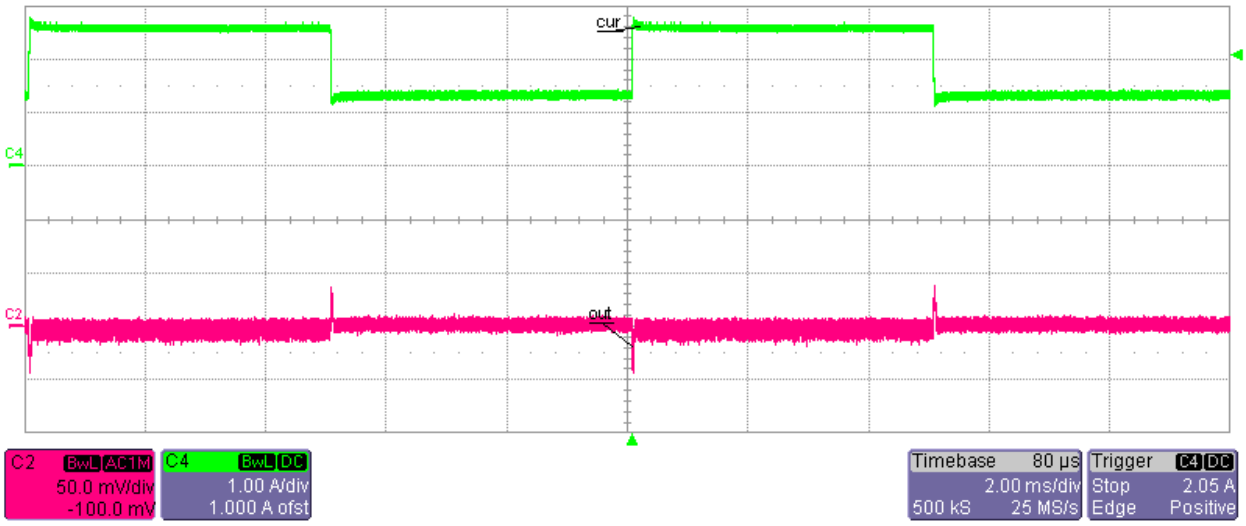


Load Transient Response at 12 Vin and 50%-to-100% Load Step on 1.2 V Output Vout2 (Full Load were connected to all other outputs)

Ch2 – Vout2 (AC coupled)

Ch4- Iout 2

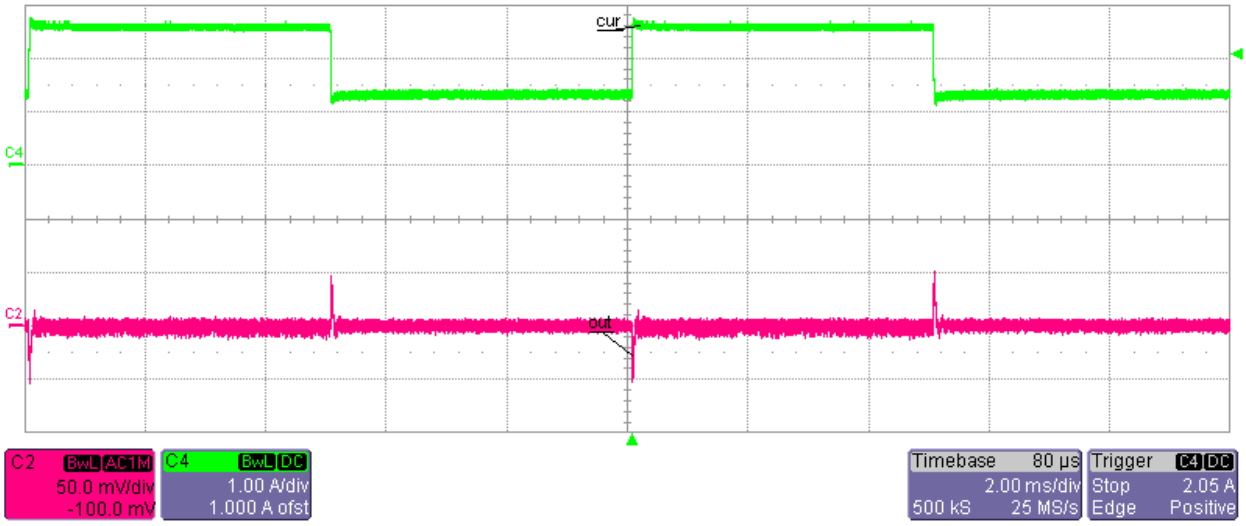
6.5.2 LM53603 outputs



Load Transient Response at 12 Vin and 50%-to-100% Load Step on 3.3 V Output Vout1 (Full Load were connected to all other outputs)

Ch2 – Vout1 (AC coupled)

Ch4- Iout 1

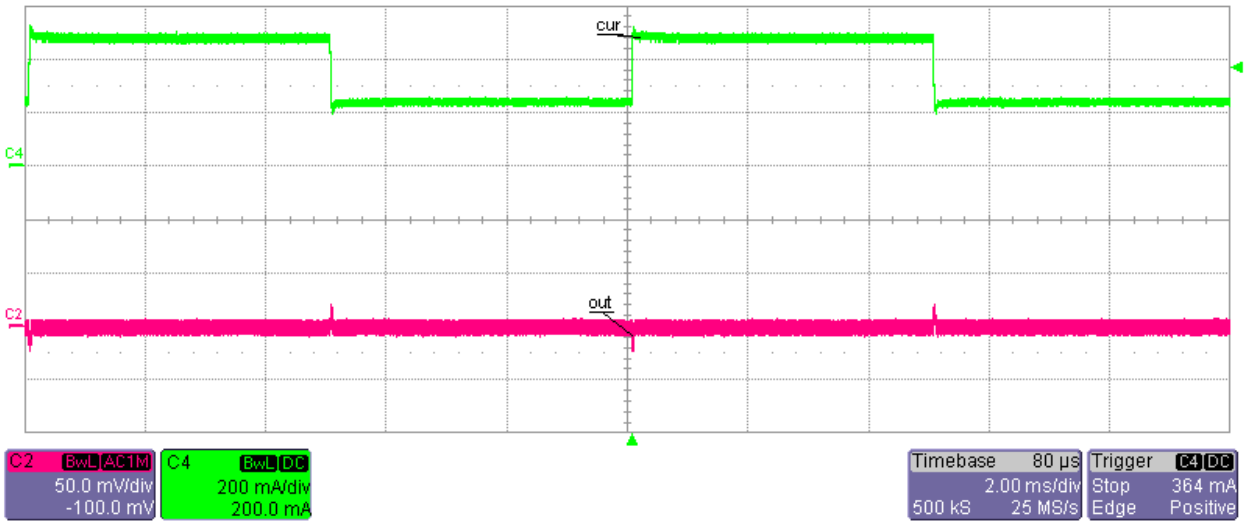


Load Transient Response at 4.5 Vin and 50%-to-100% Load Step on 3.3 V Output Vout1 (Full Load were connected to all other outputs)

Ch2 – Vout1 (AC coupled)

Ch4- Iout 1

6.5.3 LM26420 Output

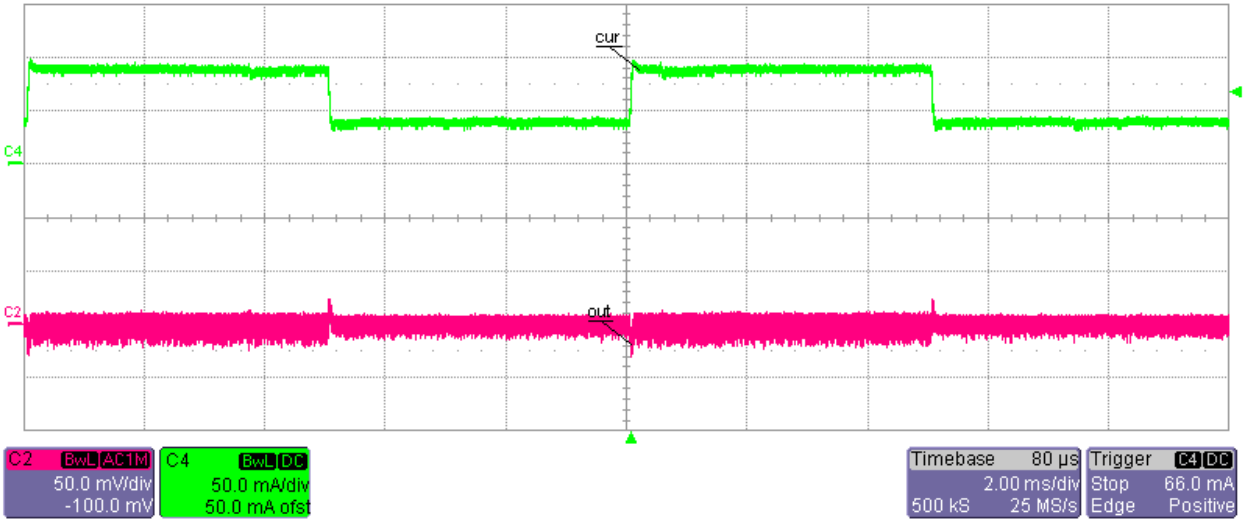


Load Transient Response at 12 Vin and 50%-to-100% Load Step on 1.8 V Output Vout5 (Full Load were connected to all other outputs)

Ch2 – Vout5 (AC coupled)

Ch4- Iout 5

6.5.4 TPS60150 – 5V



Load Transient Response at 12 Vin and 50%-to-100% Load Step on 5 V Output Vout5 (Full Load were connected to all other outputs)

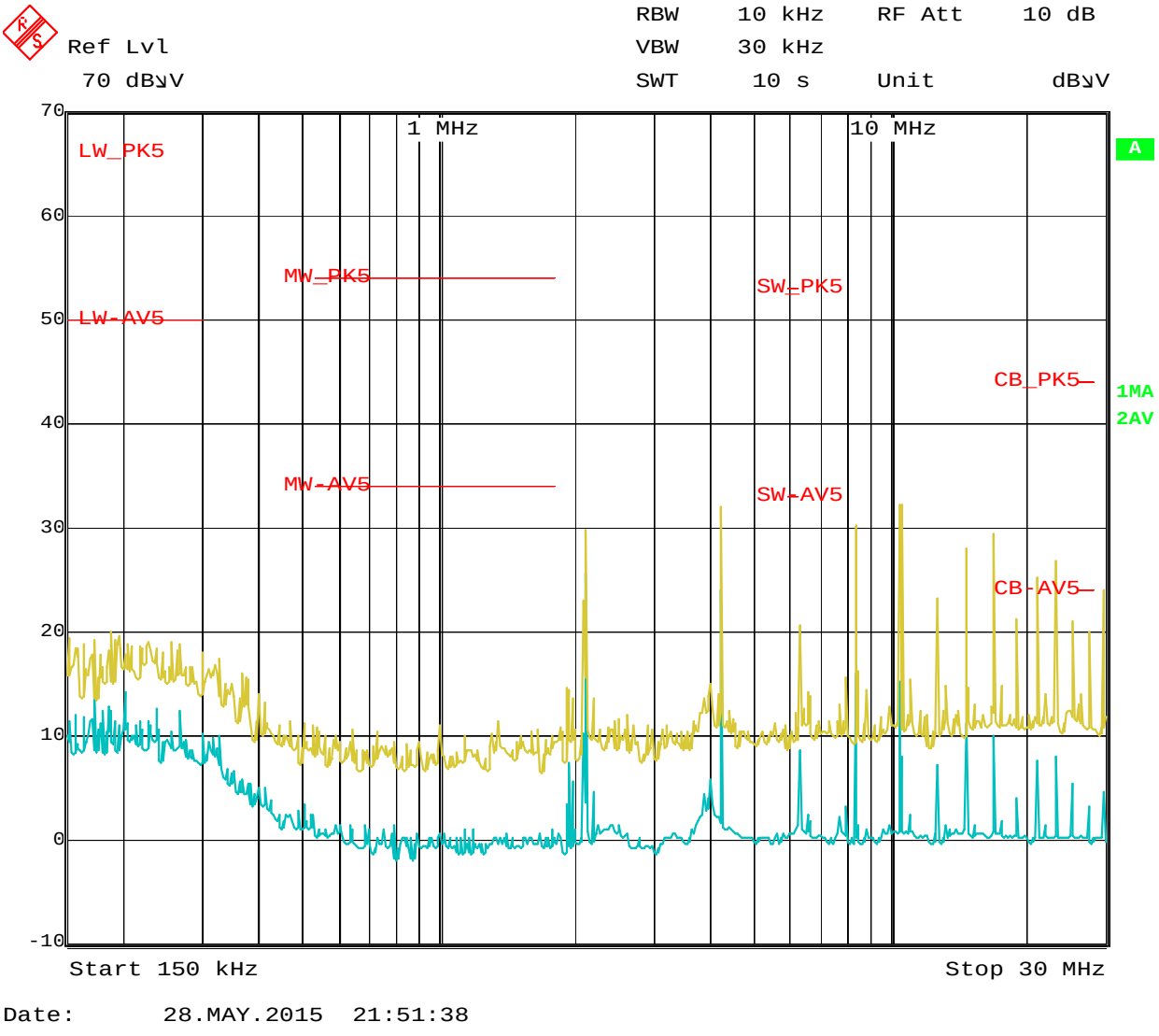
Ch2 – Vout7 (AC coupled)

Ch4- Iout 7

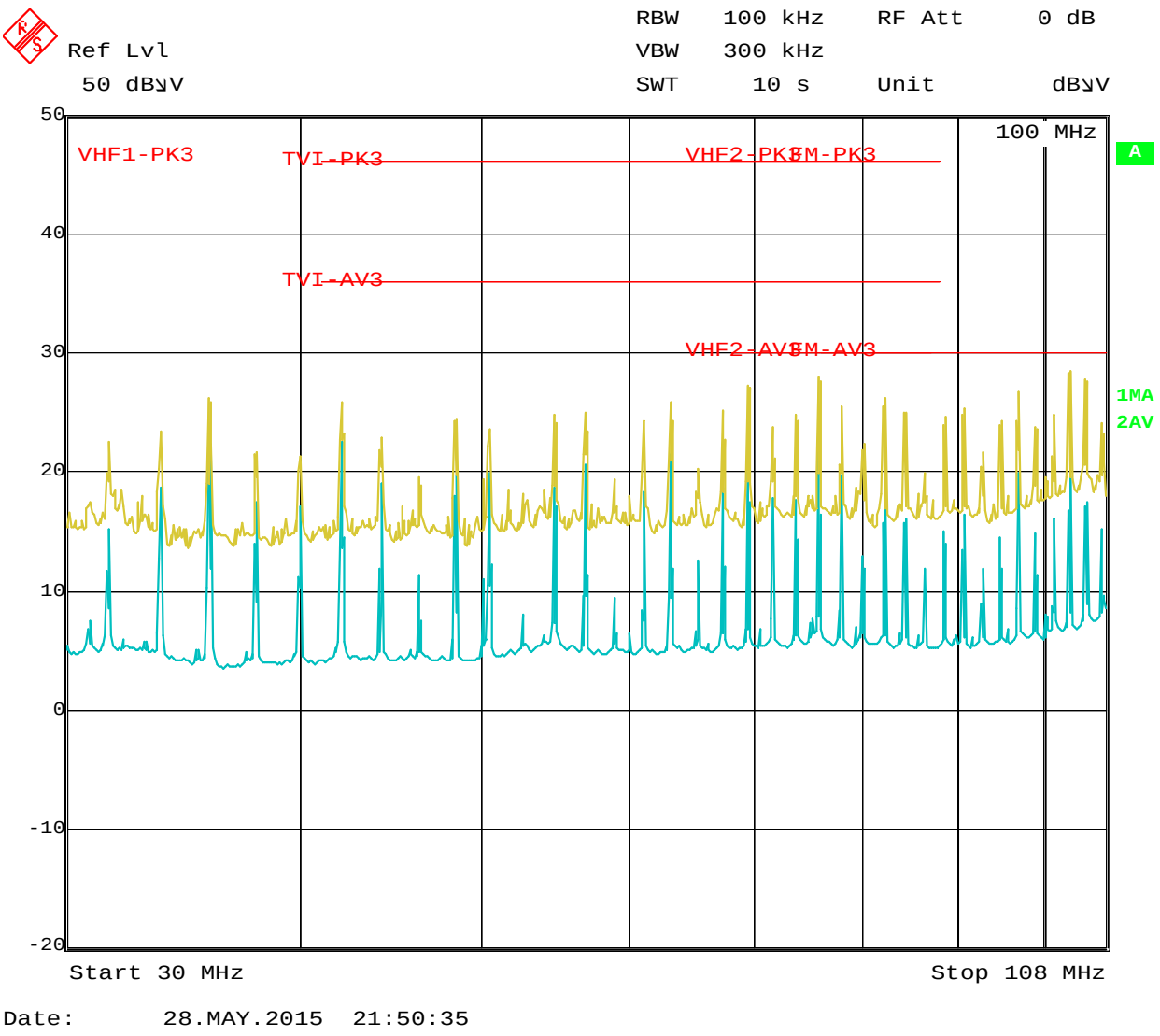
7 . Conducted Emissions

The conducted emissions is tested followed the of CISPR 25 standards. The frequency band examined spans from 150 kHz to 108 MHz covering the AM, FM radio bands, VHF band, and TV band specified in the CISPR 25.

The test results are shown in below two Figures. The first Figure show the test result using peak detector and Average detector measurement respectively up to 30MHz , and the last Figure show the test result using average detector and Peak Detector measurement from 30MHz to 108MHz. The limit lines shown in red are the Class 5 limits(up to 30MHz) and Class 3 limits (30MHz to 108MHz) for conducted disturbances specified in the CISPR 25; the yellow(Peak Detector measurement) and blue(Average detector measurement) traces is the test result. It can be seen that the power supply operates quietly and the noise is below the Class 3 limits overall.



Test result – Upto 30MHz Conducted Emission –Peak and Average Detection



Test result –30MHz to 108MHz Conducted Emission –Peak and Average Detection

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