TI Designs

Ethernet POWERLINK Development Platform Reference Design

Design Overview

The TIDEP0028 Ethernet POWERLINK development platform combines the AM335x Sitara™ processor family from Texas Instruments (TI) and the POWERLINK open media access control (MAC) layer into a single system-on-chip (SoC) solution. Targeted for Ethernet POWERLINK slave communications, the TIDEP0028 design allows designers to implement the real-time POWERLINK communication standard for a broad range of industrial automation equipment.
The design is based on the TMDSICE3359 Industrial Communications Engine (ICE).

Design Resources

TIDEP0028	Tool Folder Containing Design Files
AM3359	Product Folder
TMDSICE3359	Product Folder
OtherEVMs/TI Designs	Tools Folder

TI E2E™ Community

ASK Our E2E Experts
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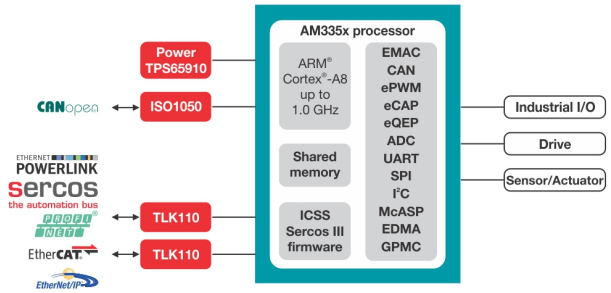
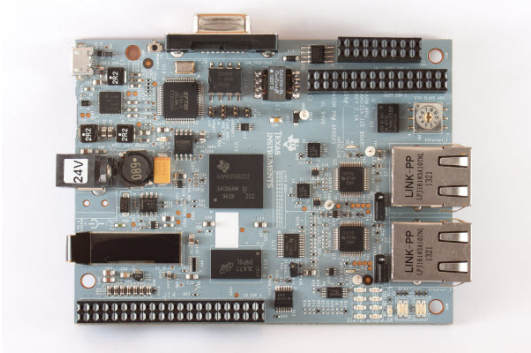
Design Features

- Combines Half-Duplex Operation With POWERLINK's Strict Communication Scheme to Provide Extreme Low Latency and Fully-Predictable Network Infrastructure
- Uses the Low-Power Sitara AM335x Processor
- Development Board is Orderable and Includes Hardware, User Guides, StarterWare™ software from TI, and Application Stacks

Featured Applications

- Motor Drives
- Programmable Logic Controllers
- Digital and Analog I/O Module
- Human Machine Interface (HMI)
- Motion Control





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1 System Description

The traditional, centralized I/O systems are inadequate for building large machines. Running high-speed I/O lines over long distances increases the cabling requirements and errors due to signal noise with higher frequencies. The use of Industrial Ethernet solves many of these problems by providing a system-on-chip (SoC) accelerated methodology to manage I/Os, sensors, and actuators for high-frequency applications such as motion control. The SoC provides a protocol for real-time, deterministic, jitter-free Ethernet communications, as well as reliable deterministic synchronization capabilities over large distances.

POWERLINK is a real-time Ethernet fieldbus system based on the Ethernet standard IEEE 802.3. POWERLINK was initially developed by B&R and introduced in 2001. Since 2003, further development is driven by the Ethernet POWERLINK Standardization Group (EPSG), an independent user organization. The EPSG cooperates with other relevant standardization and user organizations such as CAN in Automation (CiA) or the International Electrotechnical Commission (IEC). Free open-source versions of POWERLINK have been available since 2008.

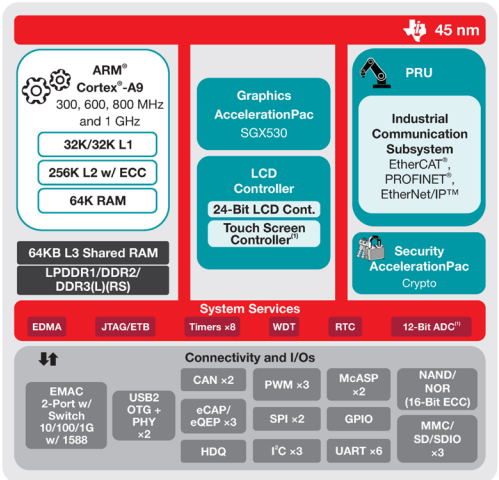
POWERLINK supports Ethernet standard features such as cross-traffic, hot-plugging, and different types of network configurations such as star, ring, and mixed topologies. The communication profile of Ethernet POWERLINK is based on CANopen. Process data object (PDO) for process variables and service data objects (SDO) for configuration and remote objects are re-used. For safety applications, POWERLINK can be used with the openSAFETY stack, which is also available as open source.

The TIDEP0028 design provides an example of how POWERLINK is implemented on the Sitara platform.

1.1 Powerlink Solution With Sitara

The Sitara AM335x processors are low power with an ARM® Cortex®-A8 from TI and a broad range of integrated industrial peripherals (see Figure 1). The ARM Cortex-A8 supports clock frequency ranges from 300 MHz for simple I/O applications up to 1 GHz for complex control applications that require more CPU performance.

The AM335x device family contains an instance of TI's Programmable Real-Time Unit within the Industrial Communication Subsystem (PRU-ICSS). The PRU-ICSS has two dedicated processing cores (Programmable Real-time Units or PRUs) and industrial communication interfaces such as universal asynchronous receiver/transmitters (UARTs), media independent interfaces (MIIs), and management data input/outputs (MDIOs). The two PRU-MII interfaces connect directly to two Ethernet PHY devices and their ports on the board. Now software can be used to implement any kind of Ethernet MAC implementation to serve different industrial protocol implementations.



* 800 MHz / 1 GHz only available on 15×15 package. 13×13 supports up to 600 MHz.
(1) Use of TSC will limit available ADC channels.

Figure 2: AM335x SoC block diagram

Figure 1. AM335x SoC Block Diagram

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1.2 TI openMAC

Texas Instruments implemented the openMAC module for POWERLINK, which is a standard Ethernet MAC with extensions for POWERLINK, such as auto-reply and time-triggered send functions. By using the openMAC module on a PRU-ICSS and running a POWERLINK stack on an ARM host inside the AM335x processor, the user can implement an integrated POWERLINK Controlled Node (CN) or Managing Node (MN).

The main features of the TI openMAC implementation are:

- Compliance to openMAC specification
- Two MII interfaces with 100-Mbps full-duplex and half-duplex support
- Three-port hub implementation
- 16 Rx filters
- Ability to filter up to first 31 bytes of an Rx packet
- Auto-response feature
- Time stamping of Tx and Rx packets, interrupt request (IRQ) generation to host processor
- Operating system (OS) independent driver and Hardware Abstraction Layer (HAL) code

Figure 2 shows an example usage scenario for openMAC. The openMAC module implements the lower layer of an Ethernet hub that is capable of use with a POWERLINK stack. Customers can then implement POWERLINK MN or CN solutions on top.

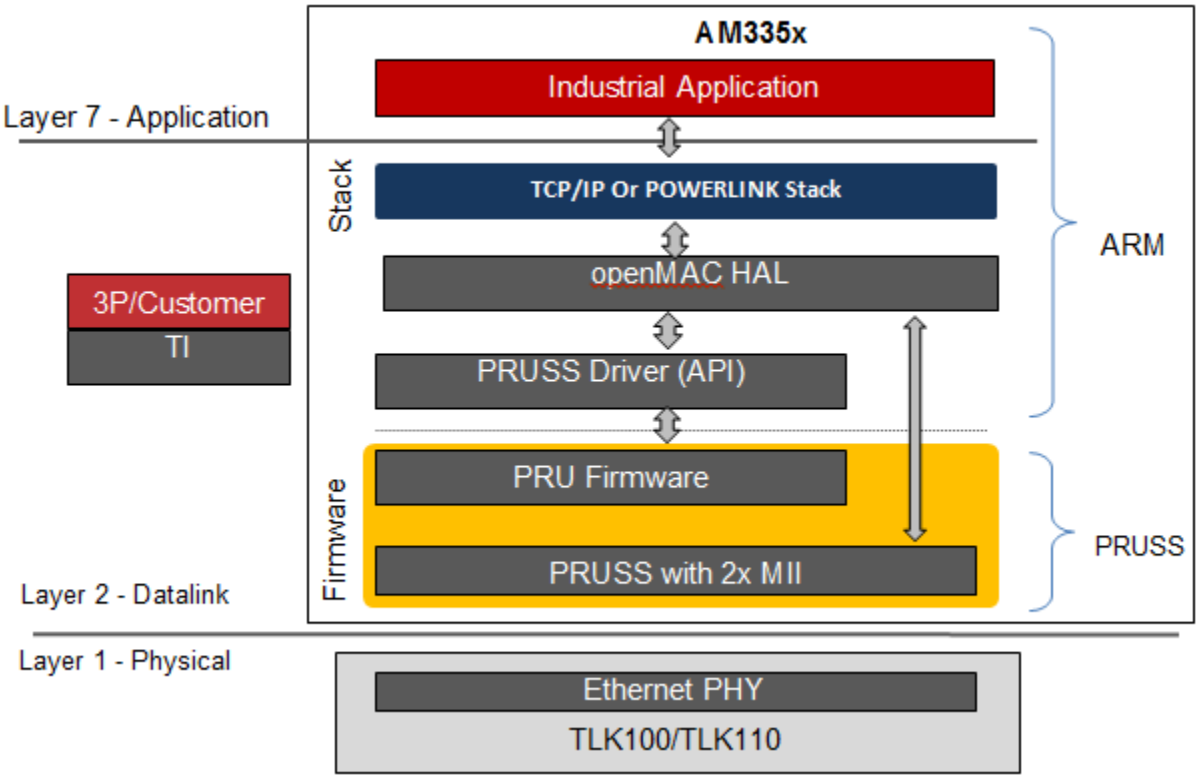

Figure 2. Example openMAC Usage

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1.3 3rd Party Support from Port

A third-party protocol stack is available from port GmbH, which is located in Halle, Germany. Port uses its own POWERLINK stack and tools that support customers in creating the required device description files and application code. The solution consists of port software running on TI development boards and the solution was officially certified by the EPSG. Port has created a driver to interface with TI POWERLINK PRU firmware and offers features for POWERLINK products according to Table 1.

Table 1. Stack Features

FEATURE	SUPPORT
Controlled node functionality	Yes
Managing node functionality	–
Isochronous controlled node	Yes
Async-only controlled node	Yes
PDO producer	Yes
PDO consumer	Yes
Number of supported transmit-PDOs	1
Number of supported receive-PDOs	1–254
Dynamic PDO mapping	Yes
Static PDO mapping	Yes
IP support	Yes
SDO-server	Yes
SDO-client	Yes
SDO over UDP	Yes
SDO over ADnd	Yes
SDO over PDO	–
SDO expedited transfer	Yes
SDO segmented transfer	Yes
Number of supported lines	1
Multiplexing	Yes
Usage of nonvolatile memory	Yes
CN NMT state machine	Yes
Object dictionary	Yes
Extended data types	Yes
Usage of CANopen profiles	Yes
CA-401 framework support	Yes
Frame autoreply support	Yes

TIDEP0028 is supported by Port's POWERLINK Design Tool to manage complex object dictionaries.

The POWERLINK Design Tool:

- Manages the object dictionary (dynamically or statically)
- Configures the POWERLINK stack accordingly
- Creates the .XDD device description file
- Creates the application stubs for the customer's application
- Provides a documentation of the object dictionary
- Provides an automatic, error-free, and reproducible measure to create the configuration

The design tool expands the POWERLINK offering from a simple protocol stack offering to a POWERLINK solution chain.

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2 Block Diagram

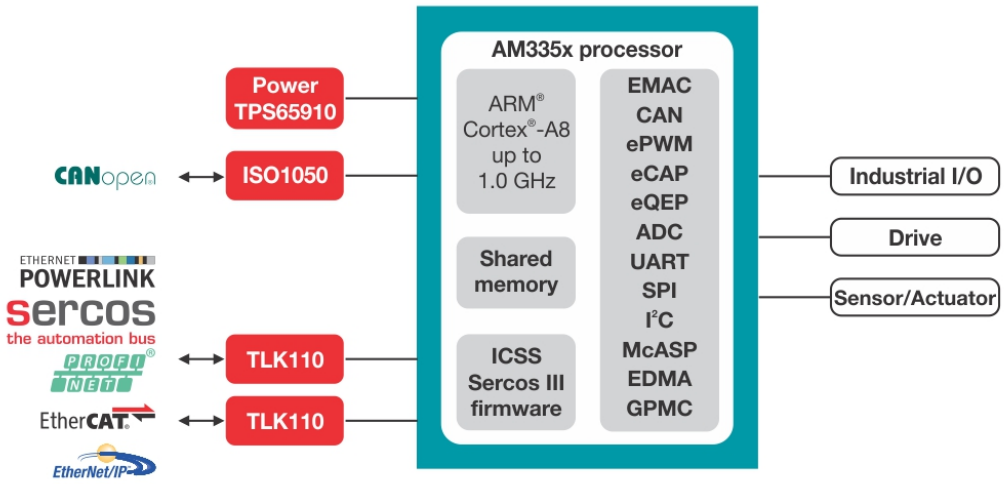

Figure 3. TMDSICE3359 Industrial Communication Engine (ICE) Board System Block Diagram

2.1 Highlighted Products

The Industrial Communication Engine is based on a Sitara AM3359 device. The ICE uses many of the SoC peripherals such as a serial peripheral interface (SPI), I^2C, UARTs, and general purpose input/output (GPIO) pins to drive light-emitting diodes (LEDs), a display, and other components such as the TLK110 Ethernet PHY devices on the board. For Ethernet connectivity, the ICE supports two Ethernet ports that are connected to PRU-MIIs. ICE boards are equipped with SPI- and NOR-based flash memory as well as an SD card interface for permanent storage.

Port provides an evaluation software package that the user can directly apply on the board. The supplied binary application program must be copied onto a microSD card. After inserting the microSD card, the board can boot from the card and run the POWERLINK CN implementation. Now the user may import the associated device description file into a programmable logic controller (PLC) system with POWERLINK master (MN) functionality. Data transfers between MN and CN can be implemented by using the defined input and output data fields. The CN output data is associated in the example application with eight LEDs on the board. Data sent from the MN is directly visualized on the board.

The example application based on TI's openMAC module and port's POWERLINK CN stack currently supports features according to Table 2.

Table 2. ICE Features

FEATURE	DESCRIPTION
POWERLINK cycle time	200 µs to 10000 µs
Multiplexing	Yes
Async MTU size	300 to 1500 bytes
Basic Ethernet mode	Yes
SDO	Using ASnd and UDP
Conformance	POWERLINK conformance test version 1.1.0
Ports	Two external Ethernet ports, internal hub

Further software development can be done using the Industrial Automation Software Development Kit (IA-SDK), which combines the TI SYS/BIOS™ real-time operating system (RTOS) and example projects using industrial Ethernet protocols.

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2.1.1 AM3359

Up to 800-MHz Sitara™ARM® Cortex®-A8 32-bit reduced instruction set computer (RISC) processor

- ARM® NEON™ single instruction/multiple data (SIMD) coprocessor
- 32KB of L1 instruction and 32KB of data cache with single-error detection (parity)
- 256KB of L2 cache with error correcting code (ECC)
- 176KB of on-chip boot ROM
- 64KB of dedicated RAM
- Emulation and Debug − JTAG
- Interrupt controller (up to 128 interrupt requests)

Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)

- Supports protocols such as EtherCAT®, PROFIBUS, PROFINET, EtherNet/IP™, and more
- Two Programmable Real-Time Units (PRUs)
- 32-bit load/store RISC processor capable of running at 200 MHz
- 8KB of instruction RAM with single-error detection (parity)
- 8KB of data RAM with single-error detection (parity)
- Single-cycle 32-bit multiplier with 64-bit accumulator
- Enhanced GPIO module provides shift-in and shift-out support and parallel latch on the external signal
- 12KB of shared RAM with single-error detection (parity)
- Three 120-byte register banks accessible by each PRU
- Interrupt controller INTC) module (for handling system input events
- Local interconnect bus for connecting internal and external masters to the resources inside the PRU-ICSS
- Peripherals inside the PRU-ICSS:
  - One UART port with flow control pins, supports up to 12 Mbps
  - One enhanced capture (eCAP) module
  - Two MII Ethernet ports that support industrial Ethernet, such as EtherCAT
  - One MDIO port

On-chip memory (shared L3 RAM)

- 64KB of general-purpose on-chip memory controller (OCMC) RAM
- Accessible to all masters

External memory interfaces (EMIF)

- mDDR(LPDDR), DDR2, DDR3, and DDR3L controller:
  - mDDR: 200-MHz clock (400-MHz data rate)
  - DDR2: 266-MHz clock (532-MHz data rate)
  - DDR3: 400-MHz clock (800-MHz data rate)
  - DDR3L: 400-MHz clock (800-MHz data rate)
  - 16-bit data bus
  - 1GB of total addressable space
  - Supports one x16 or two x8 memory device configurations
- General-purpose memory controller (GPMC)
  - Flexible 8-bit and 16-bit asynchronous memory interface with up to seven chip selects (NAND, NOR, Muxed-NOR, SRAM)
  - Uses BCH code to support 4-, 8-, or 16-bit ECC
  - Uses hamming code to support 1-bit ECC

See the AM335x data sheet for a complete list of features (SPRS717).

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2.1.2 TMDSICE3359 Industrial Communication Engine EVM

Hardware specification

- AM3359 ARM Cortex-A8
- DDR3, NOR Flash, and SPI Flash
- Organic light-emitting diode (OLED) display
- TPS65910 power management
- 24-V power supply
- USB cable for JTAG interface and serial console

Software and tools

- SYS/BIOS Real-time OS
- TI's StarterWare™ software
- TI's Code Composer Studio™ integrated development environment (IDE)
- Application stack for industrial communication protocols
- Sample industrial applications

Connectivity

- PROFIBUS interface
- CANOpen
- EtherNet/IP
- PROFINET
- Sercos III
- Digital inputs and outputs (I/O)
- SPI
- UART
- JTAG

See the TMDSICE3359 website for a complete list of features and design resources: www.ti.com/tool/tmdsice3359.

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3 Test Setup

The Ethernet POWERLINK solution for the Sitara AM335x processor has been validated with openCONFORMANCE, the POWERLINK conformance tool by the EPSG.

4 Test Data

ETHERNET POWERLINK Standardization Group

Certificate

Ethernet POWERLINK Standardization Group grants to

Texas Instruments Deutschland GmbH
Haggertystr. 1
85356 Freising
Germany

Certificate No. 10000123

Certified Product Name	AM3359 Industrial Communications Engine
VendorID	0x34
Device Type	CN
HW Revision	1.0A
SW/FW Revision	R-251
XDD File name / Date	00000034_ICE_port_epl_am335x.xdd
Test date	2014-06-04
Test Report Number	04062014_034_CN_1
Expiry date of Certificate	2017-06-03

This declaration of conformity is valid for the entire product family using the identical fieldbus communication interface technology as in the tested product.
This certificate confirms that the product has successfully passed the POWERLINK certification tests conducted at an authorized test laboratory. Further this certification authorizes the product vendor to use the official POWERLINK »Certified Product« label as shown below for the POWERLINK compliant products as listed above.

The tests were executed in accordance with the following document: DS301 V1.1.0

ETHERNET POWERLINK certified product

Issuing date: Fredersdorf, 2014-06-16

Stefan Schönegger
General Manager

Heide Rennemann-Ihlenburg
POWERLINK-Office of EPSG

Figure 4. EPSG Certificate

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5 Design Files

5.1 Schematics

To download the schematics, see the design files at.TIDEP0028.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDEP0028.

5.3 PCB Layout

To download the PCB layout, see the design files at TIDEP0028.

5.4 Software Files

To download the software files, see the design files at TIDEP0028.

6 References

1. Ethernet-POWERLINK.org, *ETHERNET POWERLINK Standardization Group*, http://www.ethernet-powerlink.org/
2. port GmbH, *Applications*, http://www.port.de/en/products/applications/

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