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TI Designs: PMP9773 Reference Guide

USB Power Supply Using TPS61088 to Support Quick Charge 2.0

TI Designs

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Circuit Description

This Reference-Design is to power the USB port that aims to support Quick Charge 2.0 from Lithium-ion battery or a voltage supply between 2.7 V and 4.4 V. The Reference-Design includes a boost converter TPS61088 to boost the input voltage up to 12 V, a 12-V E-fuse TPS2592AA with 2-A to 3.7-A adjustable current limit for short circuit protection and a QC2.0 interface IC CHY100 to adjust output voltage according to the Quick Charge 2.0 standard. This Reference-Design can support 5V&3A, 9V&2A and 12V&1.5A output power.

Design Resources

Design Page	All Design files
TPS61088	Datasheet
TPS2592AA	Datasheet

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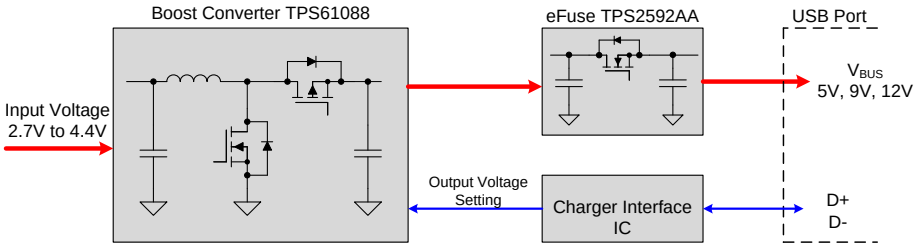

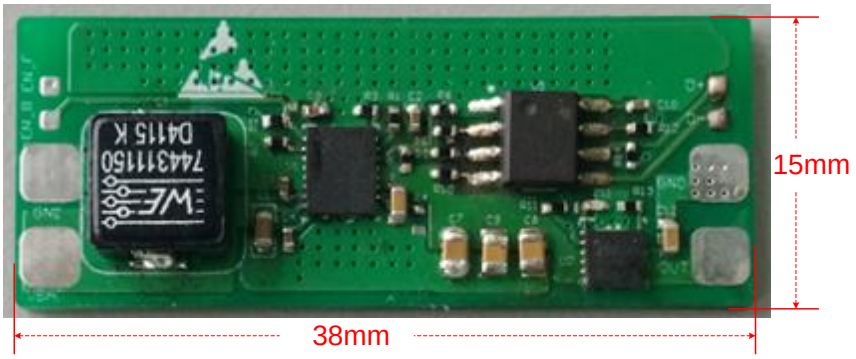

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1 Introduction

The Reference-Design (RD) builds a power circuit for USB port that supports Quick Charge 2.0 (QC2.0) class A. The input and output capability of this design is shown in Table 1 . By using a charger interface IC, the output voltage V_{BUS} can be one of the three voltages, 5V, 9V or 12V, based on the signal on D+ and D- pin of the USB port. The maximum output power of the RD is 18W.

Table 1 Performance Specification Summary

specification	Test Condition	Min	typical	Max	Unit
Input Voltage		2.7		4.4	V
Output Voltage	Output Current lower than the maximum value		5.0		V
			9.0		V
			12.0		V
Output Current	V_{BUS} = 5V	0		3	A
	V_{BUS} = 9V	0		2	A
	V_{BUS} = 12V	0		1.5	A

The following chapters describe the operation principle, schematic, PCB layout, output characteristics and thermal performance of the RD.

2 Design Description

The RD's block diagram is shown in Figure 1. The primary input power is Lithium-ion battery, the voltage of which is from 3 V to 4.35 V. According the QC2.0 standard class A, the voltage for the USB power output is 5 V, 9 V or 12 V. So the TPS61088 is used to boost the low input voltage to the target voltage.

The TPS2592AA is a 12-V e-Fuse with adjustable 2-A to 3.7-A current limit. It is to protest the battery and the TPS61088 in case of short circuit happening in the USB output port.

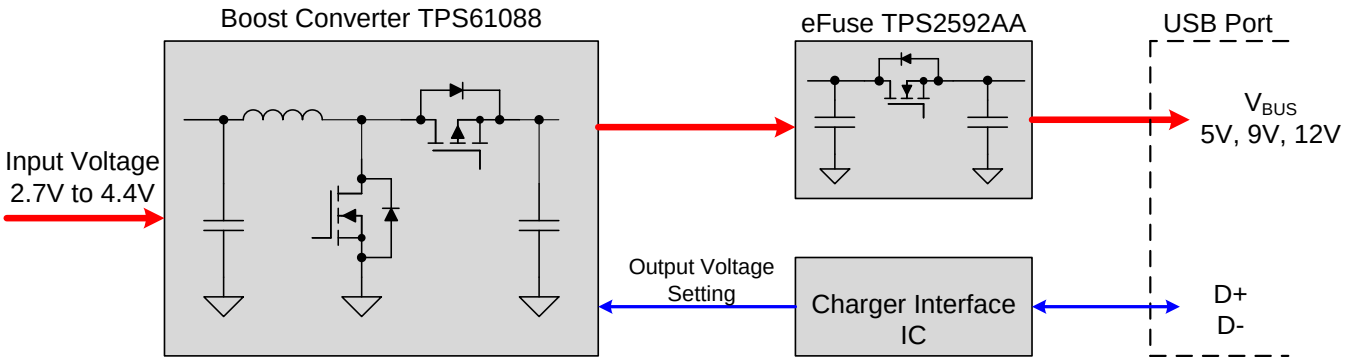


Figure 1: Block Diagram of the Reference-Design

The Charger interface IC communicates with the portable device being charged to identify if the portable device supports QC2.0. If yes, it changes the boost converter's output voltage by changing the feedback resistor according to the requirement of the portable device. If not, the boost converter keeps the default output voltage of 5 V.

2.1 Boost Converter Solution

The schematic of the boost converter solution based on the TPS61088 is shown in Figure 2. The detail operating principle, pin functions and electrical characteristics of the TPS61088 are described in its datasheet (SLVSCM8A).

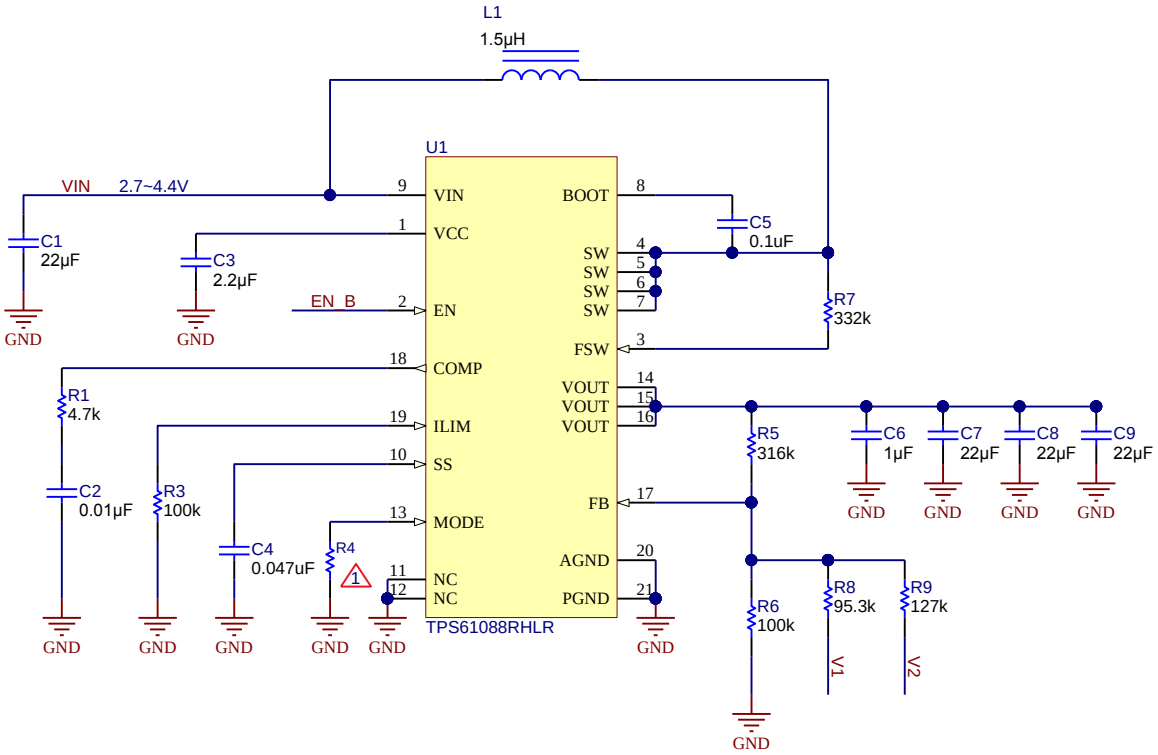


Figure 2 TPS61088 Boost Converter Schematic

2.1.1 Frequency, Inductor and capacitor selection

The switching frequency of a boost converter impacts its inductor value, input and output capacitor value and the efficiency. High frequency benefits small inductor and capacitor value, and also small solution size, but is adverse to efficiency; while low frequency benefits high efficiency but causes large solution size. The switching frequency of the TPS61088 is set by a resistor between its SW pin and FSW pin. The frequency at this design is set to approximate 500 KHz.

The average input current of a boost converter is defined by equation (1), where η is the efficiency and V_{OUT} is the output voltage of the boost converter (the output voltage of the RD is represented by V_{BUS}). Given V_{IN}=3V, η=0.9, V_{OUT}=9V, I_{OUT}=2A, the average input current I_{AVE}=6.7A.

$$I_{AVE} = \frac{V_{VOUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \quad (1)$$

The inductor value is determined by the current ripple, normally 20% to 40% of the average input current. Then inductor value can be calculated by equation (2), where I_{PP} is the peak to peak current ripple, f_s is 500 KHz.

$$L = \frac{1}{I_{PP} \cdot \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}\right) \cdot f_s} \quad (2)$$

A 1.5-μH inductor is selected in the RD considering the efficiency of the RD and package of the inductor.

Low-ESR ceramic capacitor is used for this high switching frequency boost converter. So the output voltage ripple is primarily determined by the equation (3), in which C_{OUT} is the effective capacitance.

$$V_{RIP} = \frac{(V_{BST} - V_{IN}) \cdot I_{OUT}}{C_{OUT} \cdot V_{BST} \cdot f_s} \quad (3)$$

Three 22-µF,0805 package capacitors in parallel are used in the RD. The effective capacitance of ceramic capacitor is largely impacted by its bias voltage. The total effective capacitance and output ripple at V_{IN}=3.6V based on equation (3) are shown in Table 2.

Table 2 PMP9775 Output Effective Capacitance and Ripple

V_{OUT}	5 V	9 V	12 V
Effective Cap.	33 µF	16.5 µF	13.2 µF
V_{RIP}	51 mV	145 mV	159 mV

2.1.2 Compensation Capacitor and Resistor

The converter must be stable under 5 V, 9 V and 12 V with the same compensation capacitor and resistor, which are C2 and R1 in Figure 2. The C2 and R1 are designed based on 5-V output condition, because the right hand panel zero of the boost converter is smallest at 5-V condition. Refer to the TPS61088 datasheet for the detail about the small signal model.

In real board, the stability and phase margin of the converter can be estimated using the load transient waveform, as described in the page 5, 6 of the application-note “Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor” (SLVA289).

2.1.3 Output Voltage Setting

The output voltage of the boost converter is set by the interface IC through changing the TPS61088 feedback resistor. As shown in Figure 2, when R8 and R9 are opened, the V_{VOUT} can be calculated by equation (4). The RD output V_{BUS} is approximately equal to V_{OUT} when the e-fuse is enabled.

$$V_{OUT} = \frac{R5 + R6}{R6} \cdot V_{REF} \approx 5V \quad (4)$$

When R8 is shorted to GND and R9 keeps opened, the output voltage can be calculated by equation (5)

$$V_{OUT} = \frac{R5 \cdot (R6 + R8) + R6 \cdot R8}{R6 \cdot R8} \cdot V_{REF} \approx 9V \quad (5)$$

When R8 and R9 are both shorted to GND, the output voltage can be calculated by the equation (6)

$$V_{OUT} = \frac{R5 \cdot (R6 \cdot R8 + R8 \cdot R9 + R6 \cdot R9) + R6 \cdot R8 \cdot R9}{R6 \cdot R8 \cdot R9} \cdot V_{REF} \approx 12V \quad (6)$$

2.2 E-fuse and Interface

The external components for the E-fuse TPS2592AA and the interface control IC CHY100 are easy to design following the suggestion in their datasheets.

3 A method to Enter QC2.0

According the description in the CHY100 datasheet, the processes to enter QC2.0 are:

- Apply a voltage between 0.325 V and 2 V to D+ for at least 1.25 seconds
- Discharge the D- voltage below 0.325 V for at least 1ms while keep the D+ voltage above 0.325 V
- Apply the voltage levels in Table 3 to set the output voltage. (must keep the D+ voltage above 0.325 V)

Table 3 Quick Charge 2.0 Lookup Table

D+	D-	Output Voltage
0.325 V – 2 V	0.325 V – 2 V	12 V
>2 V	0.325 V – 2 V	9 V
0.325 V – 2 V	GND	5 V(default)

Figure 3(a) shows an interface-circuit that can help the RD to enter QC2.0 for evaluation. Following lists the steps to connect the interface-circuit to the reference-design and the D+/D- voltage, and the V_{BUS} voltage in each step is shown in Figure 3(b):

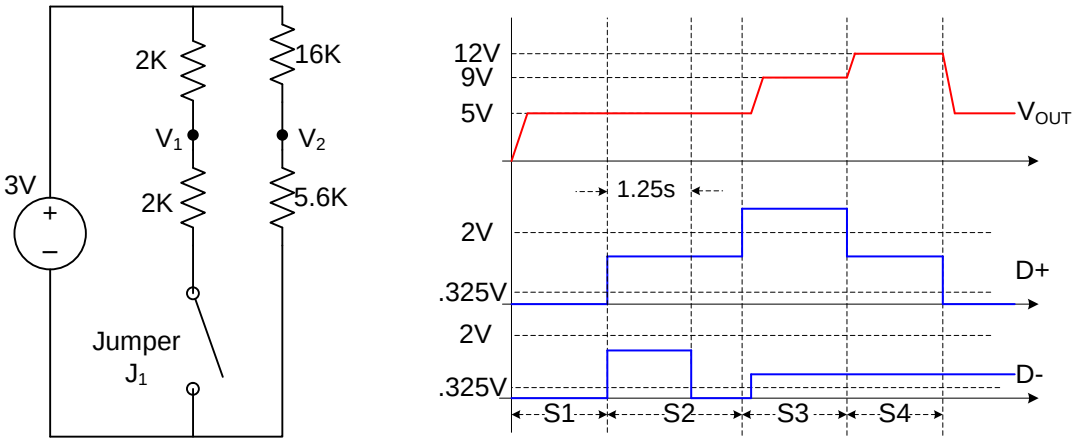
S1 Connect a power-supply between 2.7 V and 4.4 V to the RD, and connect a 3V power-supply to the interface-circuit (the V_{BUS} ramps up to approx. 5V after this step).

S2 Close the Jumper J_1, connect V1 to the D+ pin and keep the D- floating, then wait at least 2 seconds. Two actions happen during this 2 seconds:
- The D+ and D- voltage equal to 1.5V for 1.25 seconds. (because the D+ and D- pins connect together inside the CHY100)
- Then the D+ keeps at 1.5V and the D- voltage decrease to zero. (because the D+ and D- pins disconnect and a resistor inside the CHY100 discharges the D-)

S3 Open the J_1, and then connect the D- to V_2. The V_{BUS} jumps to 9V. (because the D+ voltage is above 3V and the D- voltage is between 2V and 0.325V)

S4 While keep the D- connection with V_2, close the Jumper J_1. The V_{BUS} jumps to 12V. (because the D+ and D- voltage are between 2V and 0.325V)

S5 Disconnect the D+ with V_1. V_{BUS} jumps to 5V (Because the RD quits the QC2.0 and V_{BUS} goes to the default value 5V. start from S1 when needing to enter QC2.0 again)



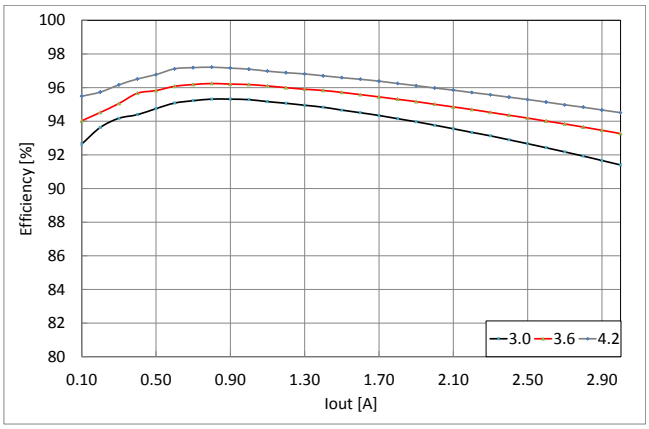
(a)QC2.0 Interface-Circuit (b) D+/D- and V_{BUS} Waveform

Figure 3 An Interface-Circuit to Enter Quick Charge 2.0

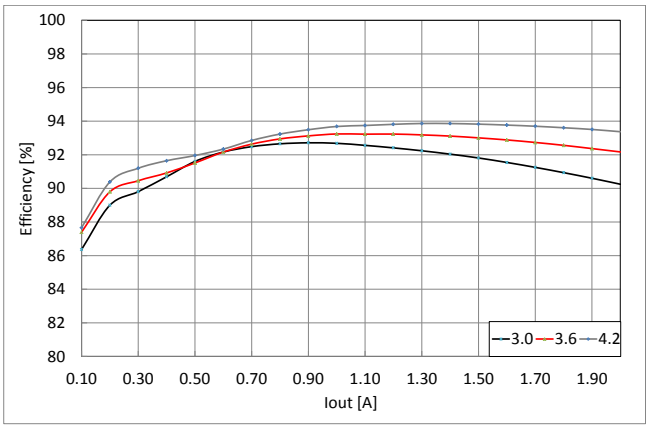
4 Test Result

4.1 Efficiency

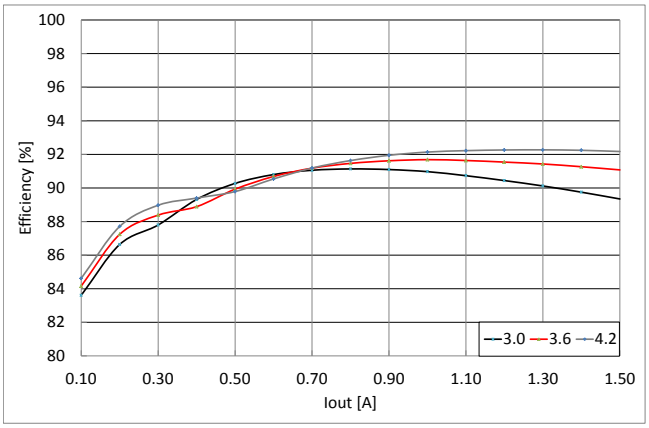
Figure 4 shows the efficiency of the RD at V_{BUS} = 5 V, 9 V and 12 V from 0.1A to full load (Refer the TPS61088 datasheet for more efficiency data of the TPS61088). The efficiency does not just depend on the IC, but also depends on the inductor and the PCB layout. A small DCR inductor and PCB power tracks with small resistance can help to improve the efficiency.



(a) V_{BUS}=5V



(b) V_{BUS}=9V

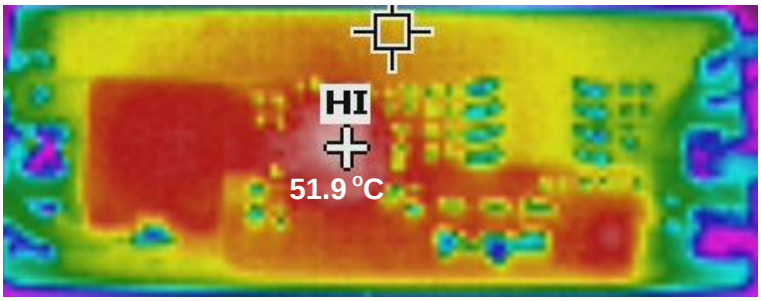


(c) V_{BUS}=12V

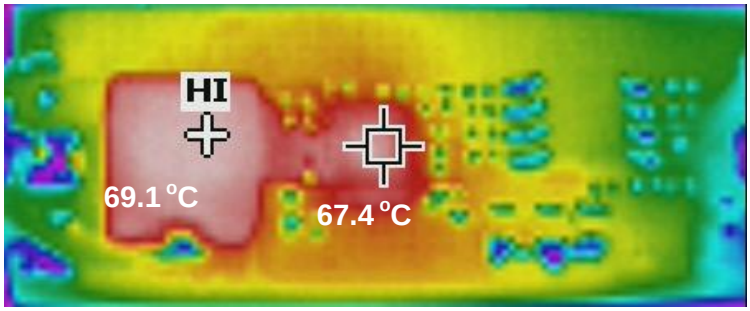
Figure 4 Efficiency of the Reference Design

4.2 Thermal Performance

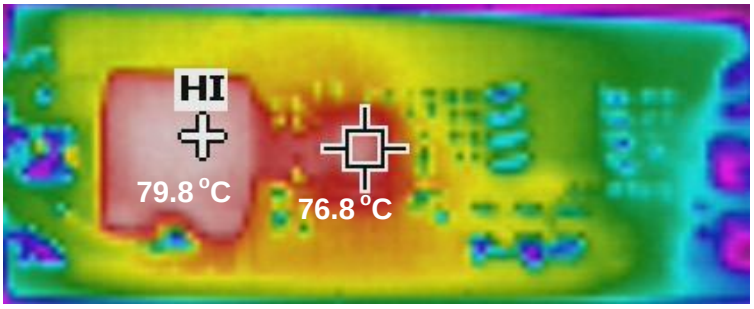
Figure 5 shows the thermal performance at full output power condition when V_{IN}=3.6V. The ambient temperature T_A is 23ºC and highest temperature point is at the inductor or TPS61088. The worst case happens at V_{BUS}=12V because of lowest efficiency.



(a) V_{BUS}=5V, I_{OUT}=3A



(b) V_{BUS}=9V, I_{OUT}=2A



(c) V_{BUS}=12V, I_{OUT}=1.5A

Figure 5 Thermal Performance at V_{IN}=3.6V

Table 4 summarize the temperature-rise at V_{BUS}=9V and T_A=23ºC.

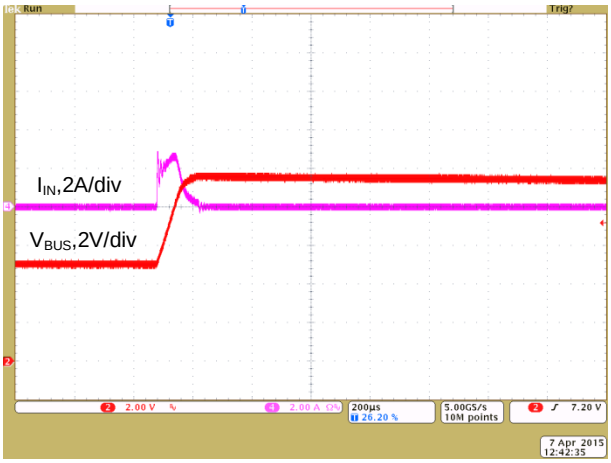
Table 4 Temperature-Rise at V_{BUS}=9V

Different Input Voltage Conditions			
	V_{IN}=3V	V_{IN}=3.3V	V_{IN}=3.6V
I_{OUT}=2A	59.6°C	51.8°C	46.1°C
Different Output Current Conditions			
	I_{OUT}=1A	I_{OUT}=1.5A	I_{OUT}=2A
V_{IN}=3.6V	24.2°C	33.5°C	46.1°C

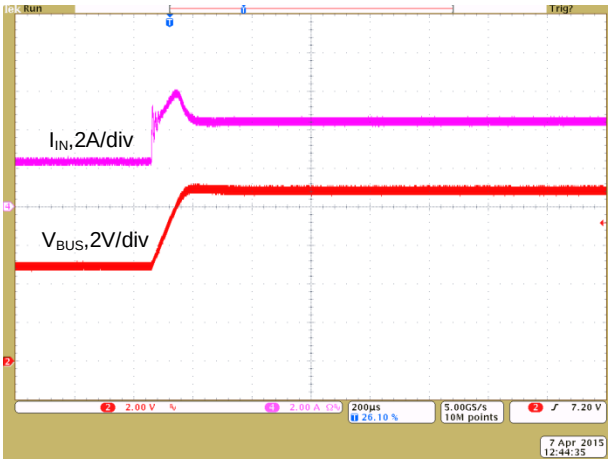
4.3 V_{BUS} Voltage Transition

The voltage's rising up waveforms from 5V to 9V, 9V to 12V and 5V to 12V are shown in Figure 6, Figure 7, and Figure 8 respectively. The waveforms are measured by changing the D+ and D- voltage level.

There is output voltage overshoot at no load condition. The worst case is 5V to 12V, at which the output voltage could reach 13.2V for a short period. It is caused by the fast transition of V_{BUS} and the power save mode enabled. Make sure the device powered by the circuit can tolerate the voltage overshoot, or apply some load during the transition, or disable the power save mode of the TPS61088 by shorting its MODE pin to ground.

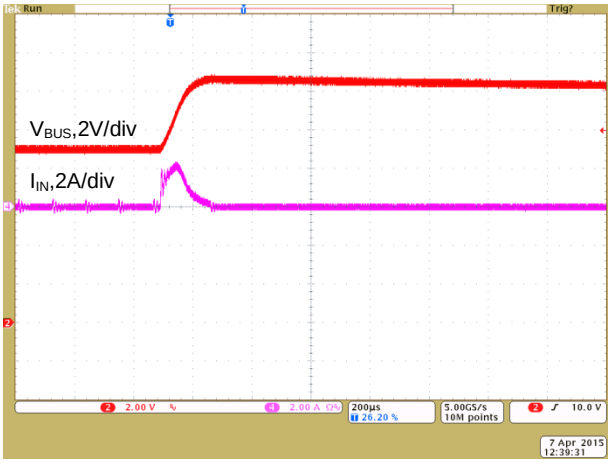


(a) I_{OUT} = 0A

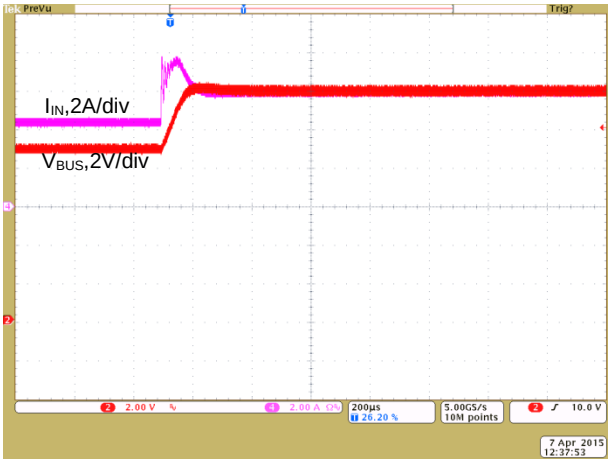


(b) I_{OUT} = 1.5A

Figure 6 V_{BUS} Transits from 5V to 9V at V_{IN}=3.6V

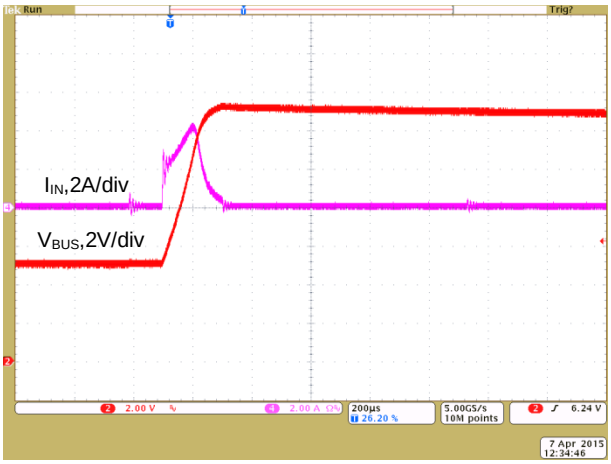


(a) I_{OUT} = 0A

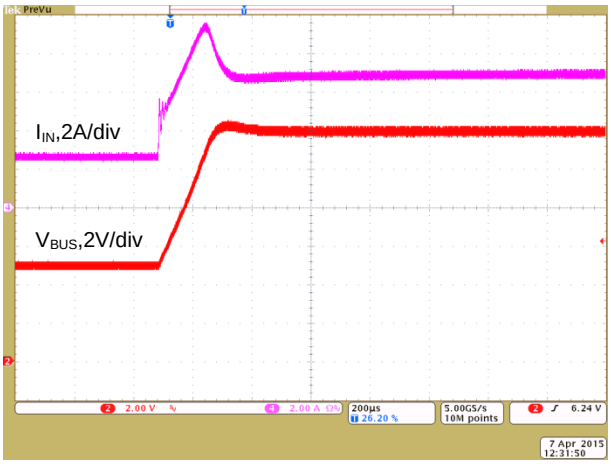


(b) I_{OUT} = 1.5A

Figure 7 V_{BUS} Transits from 9V to 12V at V_{IN}=3.6V



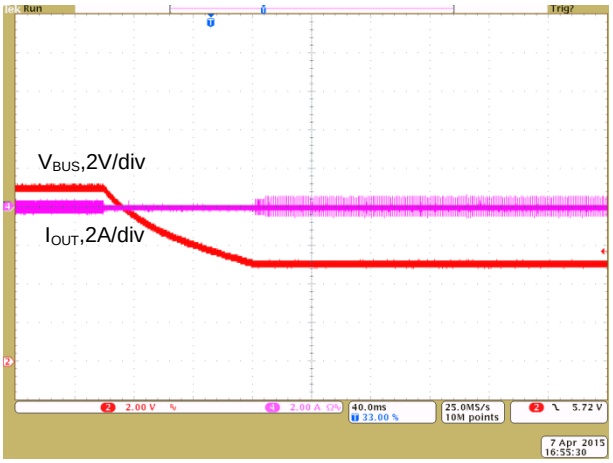
(a) I_{OUT} = 0A



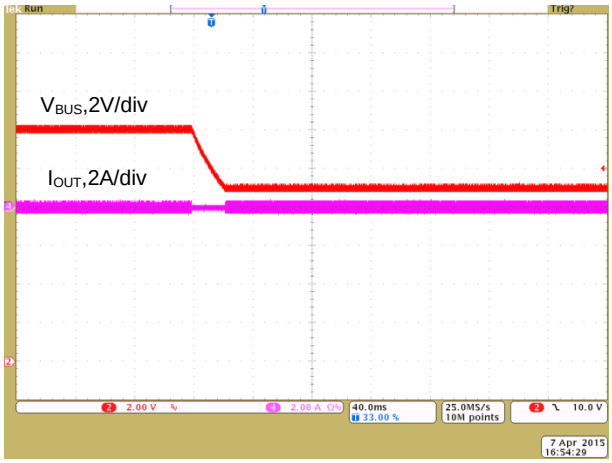
(b) I_{OUT} = 1.5A

Figure 8 V_{BUS} Transits from 5V to 12V at V_{IN}=3.6V

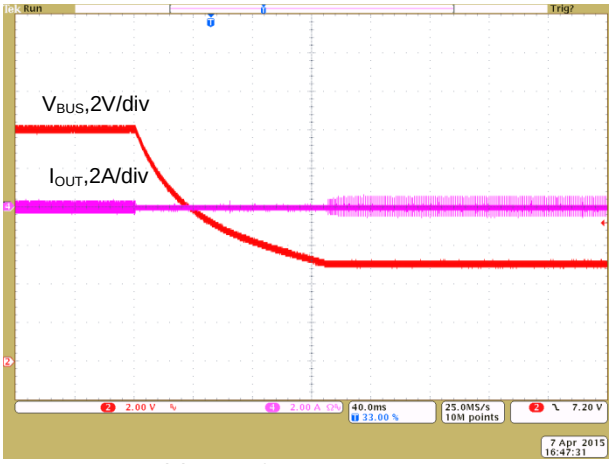
The falling-time from 9 V to 5 V, 12 V to 9 V and 12 V to 5 V at no load condition are shown in Figure 9, the longest falling-time happens at 12-V to 5-V transition which lasts about 120 ms.



(a) V_{BUS} from 9 V to 5 V



(b) V_{BUS} from 12 V to 9 V

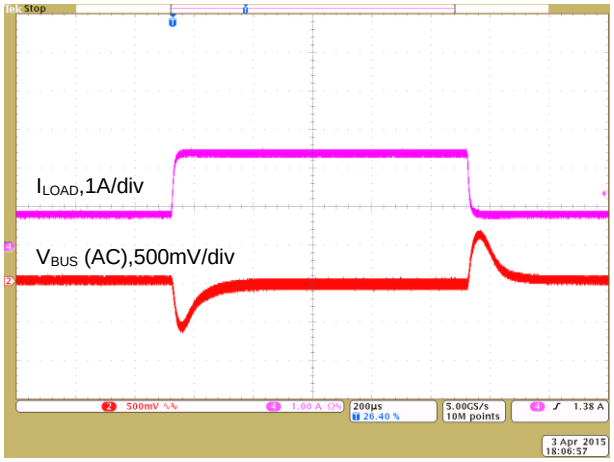


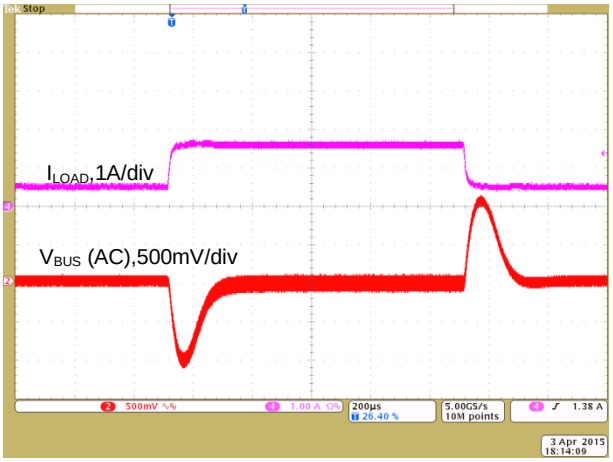
(c) V_{BUS} from 12 V to 5 V

Figure 9 Falling-Time at VIN=3.6V&I_{OUT}=0A

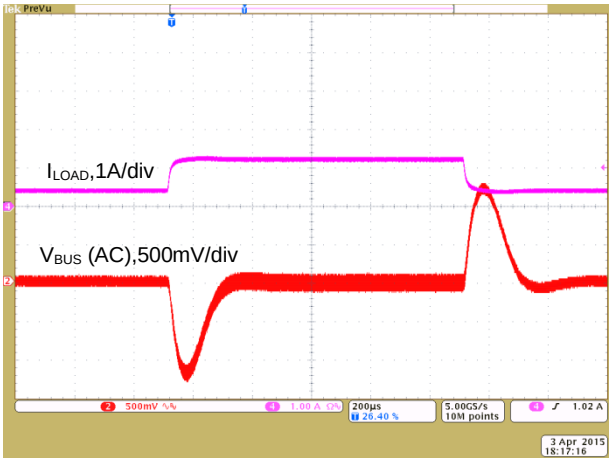
4.4 Load Transient

The load transient waveform at 5-V, 9-V and 12-V output voltage are shown in Figure 10 (a), (b) and (c) respectively. The test condition is 25% to 75% to 25% of full load with current slew rate of 0.5A/µs. The load transient waveforms indicate that the designed circuit is stable at the three output voltage condition with enough phase margins.





(a) V_{BUS}=5V I_{OUT}=0.75~2.25A (b) V_{BUS}=9V I_{OUT}=0. 5~1.5A



(c) V_{BUS}=12V I_{OUT}=0.38~1.13A

Figure 10 Load Transient Waveform

The overshoot and undershoot of the load transient are summarized in Table 5. More output capacitors can help to reduce the overshoot and undershoot but result in high cost.

Table 5 Over/undershoot of Load Transient

V_{BUS}	5 V	9 V	12 V
Overshoot	550 mV	1 V	1.2 V
undershoot	650 mV	1 V	1.2 V

4.5 Short Circuit Protection

The short circuit protection waveform is shown in Figure 11, where V_{BST} is the output voltage of the boost converter. When the V_{BUS} is short to ground, the E-fuse protects the TPS61088 from damage during the short circuit. The output voltage recovers when the short circuit is removed.

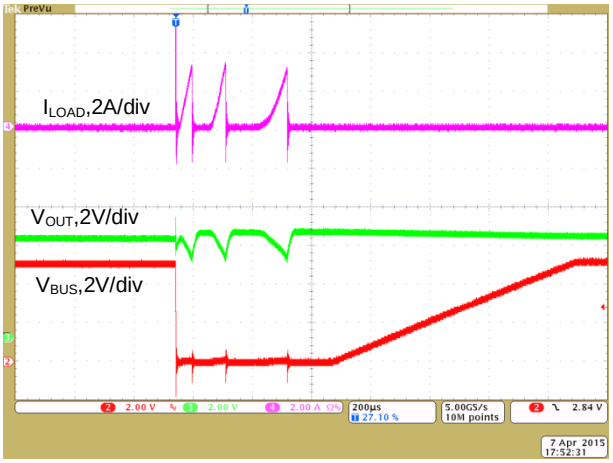


Figure 11 Short Circuit Protection

4.6 Mobile phone Charging

The setup to charge a mobile phone that supports Quick Charger 2.0 is shown in Figure 12. A cable with a micro-B type male connector is used to link the mobile phone (Samsung Note 4) and the RD. A current probe and a voltage probe are to measure the output current and voltage respectively. The EN pins of the TPS61088 and the TPS2592AA are connected together.

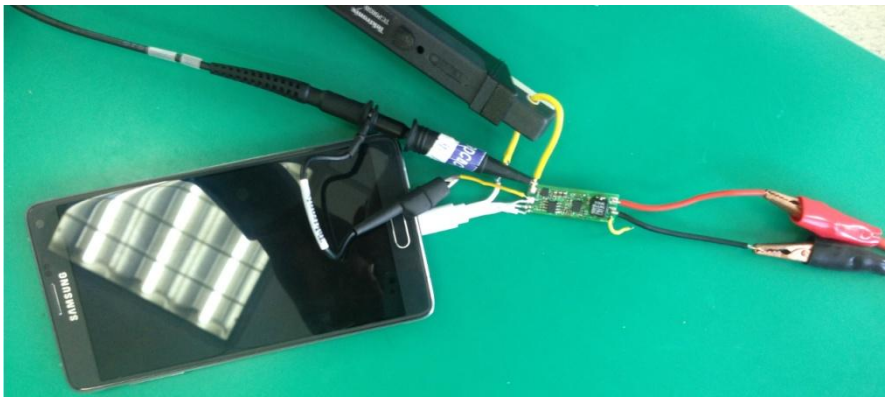


Figure 12 Setup to Charge a Mobile Phone

Figure 13 shows the waveforms of output voltage and current after enabling the RD:

- Firstly, the circuit ramps up to 5V;
- Then, the V_{BUS} keeps at 5V for approx. 1.6s. The mobile phone needs this period to enter QC2.0
- And then the V_{BUS} jumps to 9V. No overshoot happens at V_{BUS}. The load current is not constant because the phone is active.
- Finally the phone is inactive (screen turns off), the charge-power keeps at 9V&1.5A.

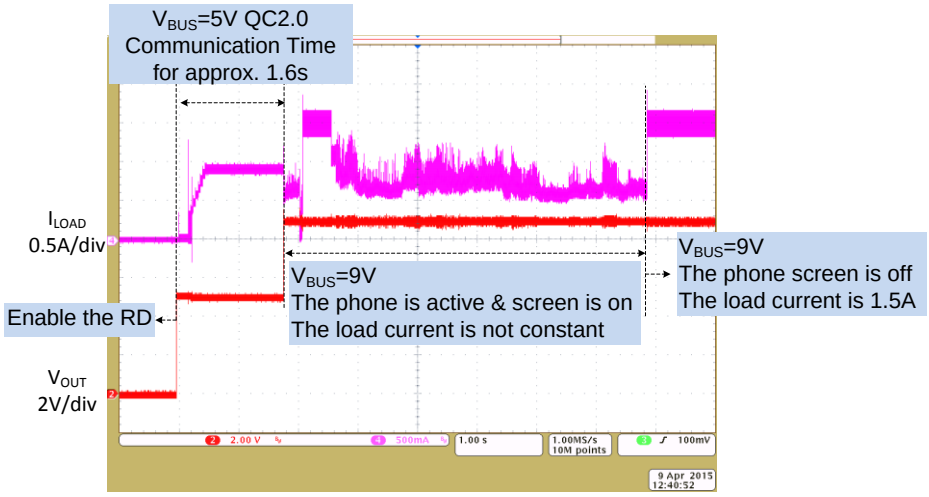


Figure 13 Waveform of Charging a Mobile Phone

5 Schematic, Bill of Materials and PCB Layout

5.1 Schematic

Figure 14 shows the schematic of the RD.

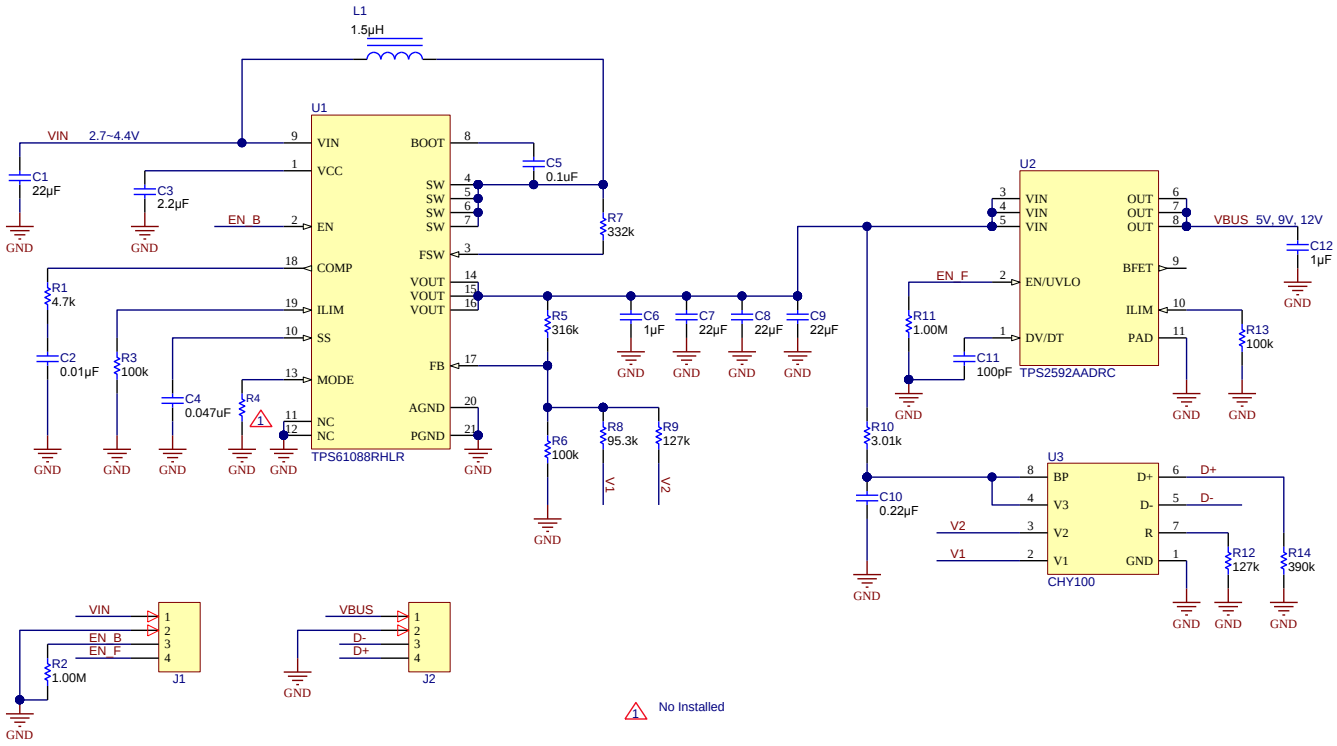


Figure 14 PMP9773 Schematic

5.2 Bill of Materials

The bill of materials in the reference design is shown in Table 6

Table 6 PMP9773 Bill of Material

Designator	Quantity	Value	Description	Package	Part Number	Manufacturer
C1	1	22uF	CAP, CERM, 22 µF, 10 V, +/- 20%, X5R, 0603	0603	GRM188R61A226ME15D	MuRata
C2	1	0.01uF	CAP, CERM, 0.01 µF, 50 V, +/- 10%, X7R, 0402	0402	GRM155R71H103KA88D	MuRata
C3	1	2.2uF	CAP, CERM, 2.2 µF, 25 V, +/- 10%, X5R, 0402	0402	GRM155R61E225KE11D	MuRata
C4	1	0.047uF	CAP, CERM, 0.047uF, 10V, +/- 10%, X5R, 0402	0402	GRM155R61A473KA01D	MuRata
C5	1	0.1uF	CAP, CERM, 0.1uF, 16V, +/-10%, X5R, 0402	0402	GRM155R61C104KA88D	MuRata
C6, C12	2	1uF	CAP, CERM, 1 µF, 25 V, +/- 10%, X5R, 0603	0603	GRM188R61E105KA12D	MuRata
C7, C8, C9	3	22uF	CAP, CERM, 22 µF, 25 V, +/- 20%, X5R, 0805	0805	GRM21BR61E226ME44	MuRata
C10	1	0.22uF	CAP, CERM, 0.22 µF, 10 V, +/- 10%, X5R, 0402	0402	GRM155R61A224KE19D	MuRata
C11	1	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	GRM1535C1H101JDD5D	MuRata
L1	1	1.5uH	Inductor, Shielded Drum Core, Superflux, 1.5 µH, 11 A, 0.0078 ohm, SMD	WE-HC4	744311150	Wurth Elektronik eiSos
R1	1	4.7k	RES, 4.7 k, 5%, 0.063 W, 0402	0402	CRCW04024K70JNED	Vishay-Dale
R2, R11	2	1.00Meg	RES, 1.00 M, 1%, 0.063 W, 0402	0402	CRCW04021M00FKED	Vishay-Dale
R3, R13	2	100k	RES, 100k ohm, 1%, 0.063W, 0402	0402	CRCW0402100KFKED	Vishay-Dale
R5	1	316k	RES, 316 k, 1%, 0.063 W, 0402	0402	CRCW0402316KFKED	Vishay-Dale
R6	1	100k	RES, 100 k, 1%, 0.063 W, 0402	0402	CRCW0402100KFKED	Vishay-Dale
R7	1	332k	RES, 332 k, 1%, 0.063 W, 0402	0402	CRCW0402332KFKED	Vishay-Dale
R8	1	95.3k	RES, 95.3 k, 1%, 0.063 W, 0402	0402	CRCW040295K3FKED	Vishay-Dale
R9, R12	2	127k	RES, 127 k, 1%, 0.063 W, 0402	0402	CRCW0402127KFKED	Vishay-Dale
R10	1	3.01k	RES, 3.01 k, 1%, 0.063 W, 0402	0402	CRCW04023K01FKED	Vishay-Dale
R14	1	390k	RES, 390 k, 5%, 0.063 W, 0402	0402	CRCW0402390KJNED	Vishay-Dale
U1	1		13.2-V Output, Synchronous Boost Converter with 10-A Switch, RHL0020A	RHL0020A	TPS61088RHLR	Texas Instruments
U2	1		12V eFuse with Integrated Blocking FET Driver, Auto Retry, DRC0010J	DRC0010J	TPS2592AADRC	Texas Instruments
U3	1				CHY100	Power Integrations

5.3 PCB Layout

Figure 15 and Figure 16 show the layout of the reference design. The bulk output capacitor is far away from the TPS61088, so a small package output capacitor C6 is placed near the IC and connected with short track to reduce the voltage spike at SW pin. The copper for the thermal pad of the TPS61088 should be as large as possible to reduce the temperature-rise caused by the power loss.

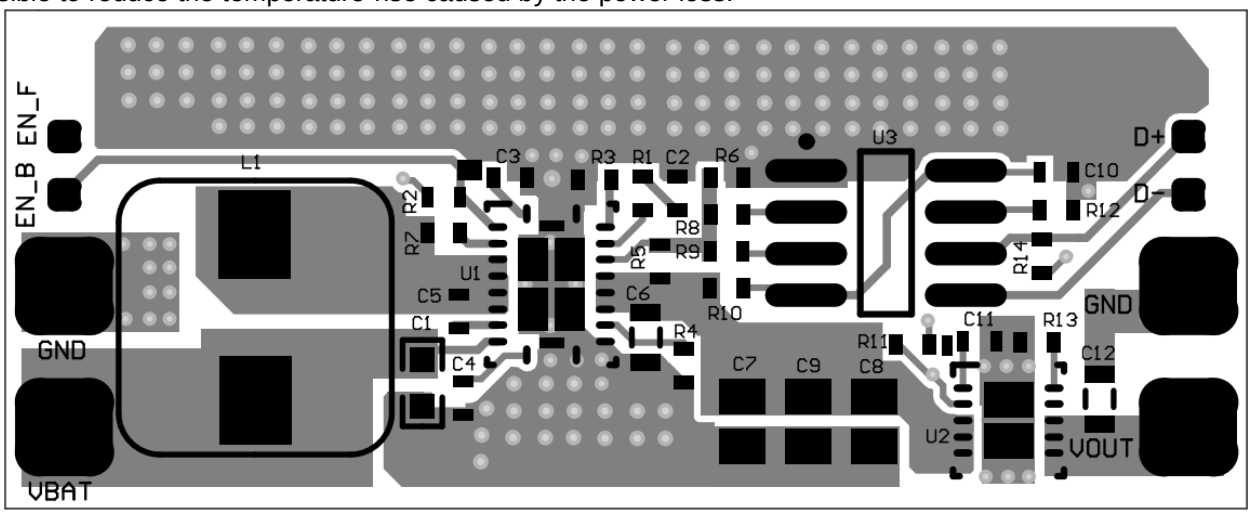


Figure 15 PMP9773 Top Overlay, Top Layer and Top Paste

Figure 16 PMP9773 Bottom Overlay and Bottom Layer

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