TI Designs: TIDA-00204
EMI/EMC-Compliant Industrial Temp Dual-Port Gigabit Ethernet Reference Design

Description

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Resources

TIDA-00204	Design Folder
DP83867IR	Product Folder
LM46002	Product Folder
AM3359	Product Folder
TPS65910A3	Product Folder
TPS51200	Product Folder
LMZ10501	Product Folder
TPS720	Product Folder
TPS737	Product Folder
TPD4E05U06	Product Folder
TPS717	Product Folder
TPD4S012	Product Folder
CDCE913	Product Folder

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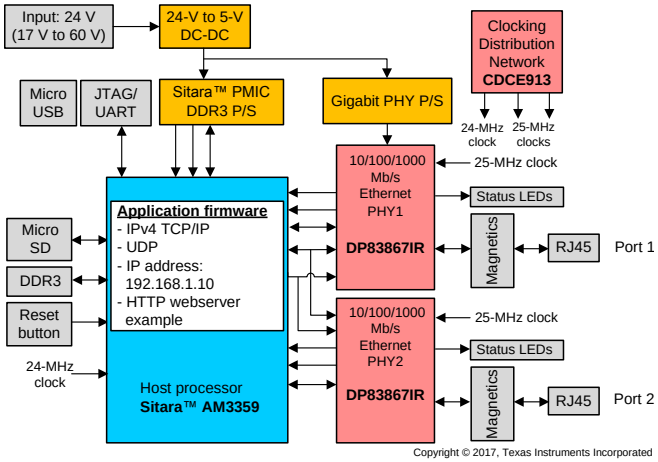
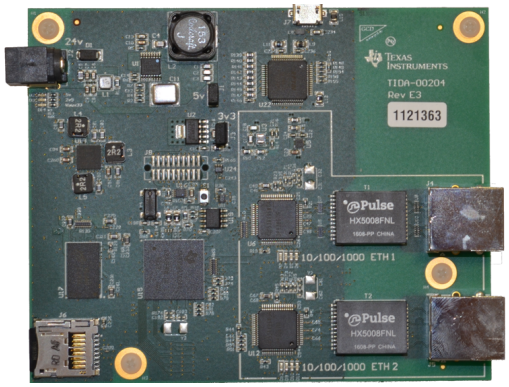
Features

- EMI- and EMC-Compliant Design With Wide Input Voltage Range (17 to 60 V) Using Two DP83867IR Gigabit Ethernet PHYs and AM3359 Sitara™ Processor to Work in Harsh Industrial Environments
- Exceeds CISPR 11 / EN55011 Class A Radiated Emission Requirement by > 4.3 dB
- Exceeds IEC61800-3 EMC Immunity Requirements:
  - ±6-kV ESD CD per IEC 61000-4-2
  - ±4-kV EFT per IEC 61000-4-4
  - ±2-kV Surge per IEC 61000-4-5
- Sitara AM3359 Firmware, Including UDP and TCP/IP Stack and HTTP Web Server Examples, Boots From Onboard SD-Card Allowing Easy Standalone Operation
- Access to DP83867IR Registers Through USB Virtual COM Port Allows for Custom Specific PHY Configurations Such as RGMII Delay Mode
- Reduces Jitter and Phase Shift From Clocks by Using Clock Synthesizer to Generate System Clocks

Applications

- Industrial Drives
- Factory Automation and Control
- Industrial Networks
- Test and Measurement





1 System Description

This TI design supports dual-port Gigabit Ethernet communication through twisted pair copper cable as defined in IEEE 802.3ab. It is designed to be evaluated for harsh industrial environment with regards to standard compliance to CISPR 11 / EN55011 Class A radiated immunity requirements and EMC immunity requirements for ESD according to 61000-4-2, fast transient burst (EFT) according to IEC61000-4-4, and surge according to IEC61000-4-5.

The design implements dual-port Gigabit Ethernet using two DP83867IR Gigabit Ethernet PHYs, which are connected through the Reduced Gigabit Media Independent Interface (RGMII) to AM3359 Sitara processor with integrated Ethernet MAC and Switch. It offers a wide input voltage range from 17 to 60 V with nominal 24-V input voltage and meets industrial requirements for EMI and EMC.

For easy standalone operation, the host processor is configured to boot the pre-installed application firmware from an onboard SD-Card. The application firmware implements a driver for the DP83867IR, UDP and TCP/IP stack, and HTTP web server examples, based on TI's SYS/BIOS Industrial SDK and TI's Networking Development Kit NDK. A USB virtual COM port offers optional user access to read or write to DP83867IR registers for custom configurations like RGMII Delay Mode, if required. A JTAG interface on the AM3359 provides the option for custom software development, test, and debug.

Therefore, this design allows for performance evaluation of two DP83867IR Gigabit Ethernet PHYs and AM3359 Sitara processor with integrated Ethernet MAC and Switch.

1.1 Key System Specifications

This design allows for performance evaluation of two DP83867IR Gigabit Ethernet PHYs and AM3359 Sitara™ processors with an integrated Ethernet MAC and Switch. It meets industrial requirements for EMI and EMC, supports industrial temperature grade, and offers a wide input voltage range with a default of 24 V.

To allow for easy standalone operation, the AM3359 Sitara boots the application firmware from SD-Card. The application firmware implements the driver for the DP83867IR, UDP and TCP/IP stack, and HTTP web server examples and is based on TI's SYS/BIOS Industrial SDK. An additional option is provided to access the DP83867IR Gigabit Ethernet PHY registers through USB virtual COM port. A JTAG interface option is also provided to allow for custom software development with that board.

Table 1. TIDA-00204 Hardware Specification

FUNCTION	INFO	SPECIFICATION	COMMENT
Gigabit Ethernet IEEE 802.3ab	Number of ports	2	—
	MDI	1000BASE-T (copper)	—
	MAC interface	RGMII	—
	EMAC and switch	Y	Integrated with Sitara AM3359
	Status LED	Y	—
	IEEE 1588v2	Y	Hardware enabled but not tested
	Separate transformer and RJ45 jack	Y	Option to place protection diodes on either side of the magnetics, used for test purpose
	SMI	Y (2.5 MHz)	—
	Configurable PHY address (SMI)	Y	Through strap resistors
DP83867IR	Low power	565 mW	—
	Integrated termination resistors	Y	—
	RGMII Delay Mode on RX/TX	Programmable	—
	Clock	25 MHz (< 50 ppm)	—

Table 1. TIDA-00204 Hardware Specification (continued)

FUNCTION	INFO	SPECIFICATION	COMMENT
Power	Input voltage	24 V (17 to 60 V)	—
	Output voltage	5 V	Intermediate voltage
	Output current	850 mA (nominal), 1.2 A (maximum)	—
	Indicator LED	Y	For 5 V, 3.3 V and 2.5 V
	Point of load for all ICs	Y	PMIC for AM3359, 3.3 V (I/O), 2.5 V and 1.1 V for PHYs
Standalone operation	Boot from SD-Card interface	Y	—
USB virtual COM port	Access to PHY registers	Y	Read and write operation to both registers of PHY supported
JTAG	JTAG header	Y	—
Temperature range	Industrial	–40°C to 85°C	Selected devices support industrial temperature range
EMI	CISPR 11 / EN55011	Class A radiated emissions	—
EMC	IEC61800-3	IEC61000-4-2 ±4-kV ESD CD, Criterion B	Shielded Ethernet cable
		IEC61000-4-4 ±2-kV EFT, Criterion B	Shielded Ethernet cable
		IEC61000-4-5 ±1-kV Surge, Criterion B	Shielded Ethernet cable, min 20 m

Table 2. TIDA-00204 Firmware Specification (AM3359)

FUNCTION	INFO	SPECIFICATION	COMMENT
Boot loader	Boot application firmware from SD-Card	Y	—
DDR3 memory	Driver for DDR3	Y	—
USB virtual COM port	Driver for UART	Y	—
PHY	Driver for DP83867IR	Y	—
RTOS	TI SYS/BIOS	Y	—
UDP and TCP/IP	IPv4 protocol support	Y	Based on TI's AM335x industrial SDK and NDK
	Fixed IP	192.168.1.10	—
HTTP	Web server example	Y	Based on TI's AM335x industrial SDK and NDK

2 System Overview

2.1 Block Diagram

Figure 1 shows the system block diagram. The major building blocks are the DP83867IR Gigabit Ethernet PHY, the AM3359 Sitara Host Processor, and the power supplies.

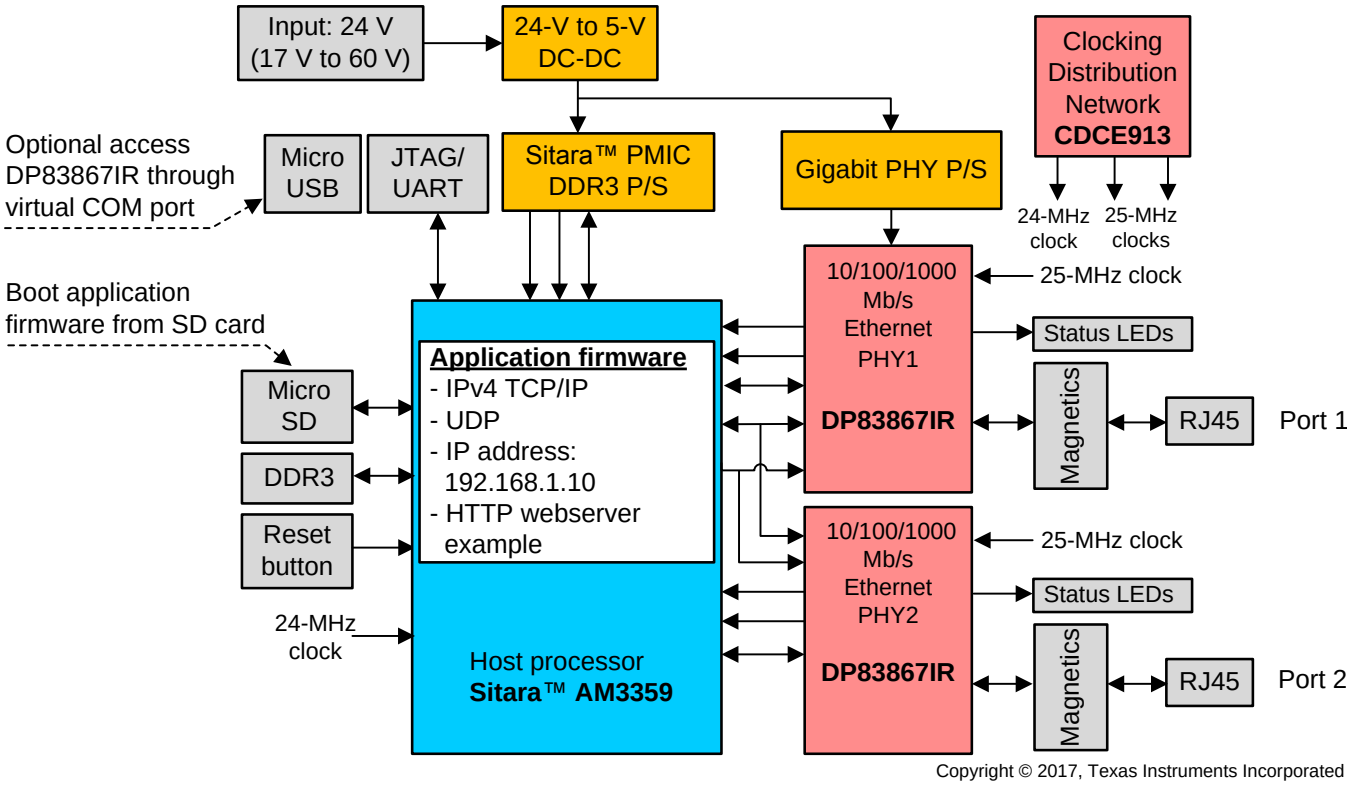


Figure 1. System Block Diagram of TIDA-00204

2.2 Design Considerations

2.2.1 Gigabit Ethernet Overview

Ethernet has heavily expanded usage over the years. Ethernet became an attractive option for industrial networking applications. The opportunity to use open protocols (such as TCP/IP over Ethernet networks) help replace proprietary communications in industrial control and factory automation applications. When using Ethernet, there are several speeds available today: 10 Mb/s, 100 Mb/s (Fast Ethernet), 1000 Mb/s (Gigabit Ethernet), and 10 Gb/s (10-Gigabit Ethernet).

Gigabit Ethernet uses the extended Ethernet MAC layer interface, connected through a Gigabit Media Independent Interface (GMII) layer to physical layer entities (PHY sublayers) such as 1000BASE-LX, 1000BASE-SX, 1000BASE-CX, and 1000BASE-T. The topology for a 1000-Mb/s full-duplex operation is comparable to the 100BASE-T full-duplex mode, and the minimum packet transmission time has been reduced by a factor of ten. The resulting achievable topologies for the half-duplex 1000-Mb/s CSMA/CD MAC are similar to those found in half duplex 100BASE-T.

Table 3. Gigabit Ethernet Standards

IEEE STANDARD	NAME	MEDIUM
IEEE 802.3ab	1000BASE-T	Twisted-pair copper cable
IEEE 802.3z	1000BASE-SX	Fiber optic cable
	1000BASE-LX	Fiber optic cable
	1000BASE-CX	Twinax

As previously mentioned, this TI Design uses twisted-pair copper cables as defined IEEE 802.3ab.

2.2.2 Gigabit Ethernet PHY Interfaces

2.2.2.1 Medium Dependent Interface: PHY Layer 1000BASE-T

The 1000BASE-T Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and baseband medium specifications are intended for users who want a 1000-Mb/s performance over balanced twisted-pair cabling systems.

The 1000BASE-T PHY supports full-duplex baseband transmission through four pairs of minimum CAT5 balanced cables. The 1000 Mb/s is achieved by transmitting through four wires pairs, each at 250 Mb/s. Using hybrids and cancellers enable full duplex transmission by allowing symbols to be transmitted and received on the same wire pairs at the same time. Baseband signaling with a modulation rate of 125 MBd is used on each of the wire pairs. The transmitted symbols are selected from a four-dimensional five-level symbol constellation (4D-PAM5). In the absence of data, idle symbols are transmitted.

The IEEE 802.3 specifies specify that a PHY with a MDI that is not a power interface (PI) should provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical isolation shall withstand at least one of the following electrical strength tests:

- 1500 V_{RMS} at 50 to 60 Hz for 60 s
- 2250-V DC for 60 s
- A sequence of ten 2400-V impulses of alternating polarity, applied at intervals of not less than 1 s

To meet this requirement transformers are typically used for isolation. The typical transformer configuration for 1000BASE-T can be seen in Figure 2 for a one differential pair.

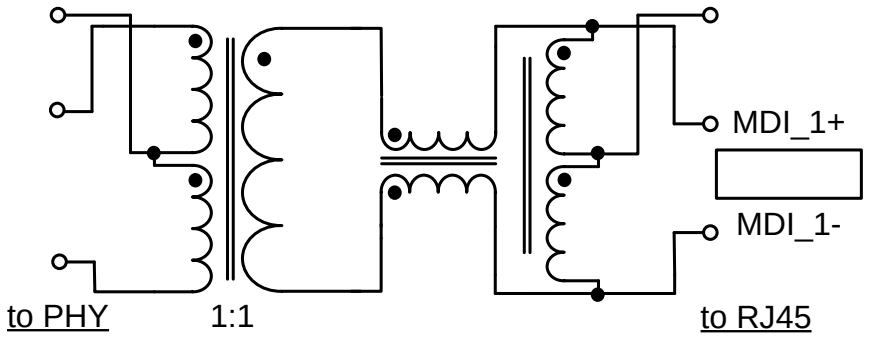


Figure 2. Gigabit Ethernet Transformer (One out of Four Pairs)

Depending on the PHY device, parallel termination might be needed for each of the MDI differential signal pair. The termination impedance is typically 100 Ω differentially. Newer devices like the DP83867IR include integrated termination so no external termination resistors are required.

2.2.2.2 Medium Independent Interface: MAC Layer Interface

For the MAC layer interface to the Gigabit PHY, there are three different options defined in the IEEE 802.3ab standard: The standard Media Independent Interface (MII), the GMII, SGMII, or the RGMII.

2.2.2.2.1 GMII

The purpose of GMII is to make various physical media transparent to the MAC layer. The GMII accepts either GMII or MII data, control, and status signals and routes them either to the 1000BASE-T, 100BASE-TX, or 10BASE-T modules, respectively.

The GMII provides full-duplex operation and is an 8-bit wide transmit and receive data path interface clocked at 125 MHz defining speeds up to 1000 Mb/s. GMII is backwards compatible with the MII specification, thereby supporting 10 (2.5 MHz) and 100 (25 MHz) Mb/s speeds. Data and delimiters are synchronous to clock references. It also provides a simple management interface.

The transmit signals are GTX_CLK, TX_CLK, TX_D[7:0], TX_EN, and TX_ER. The GTX_CLK signal is supplied to the PHY when it is operating in Gigabit mode. When this is done, the TX_D, TX_EN, and TX_ER are synchronized to the GTX_CLK signal. For a 10/100-Mb operation, the TX_CLK is supplied to the MAC, and the TX_CLK signal is used to synchronize the signals (TX_D, TX_EN, and TX_ER). The receiver signals are RX_CLK, RX_D[7:0], RX_DV, RX_ER, COL, and CS. The GMII uses in total a maximum of 25 pins.

2.2.2.2.2 RGMII

The RGMII is designed to reduce the number of pins required to interconnect the MAC and PHY (12 pins for RGMII relative to 24 pins for GMII). With this optimization, the RGMII consists of 12 signals: 6 signals for receive, which are RX_CTL, RX_CLK, RX_D[3:0], and 6 for transmit, which are TX_CTL, TX_CLK,TX_D[3:0]. To accomplish this, the data paths and all associated control signals are reduced and are multiplexed. Both rising and trailing edges of the clock are used. The TX_CTL and RX_CTL signal carries data valid (*DV*) on the rising edge and *DV XOR ERROR* on the falling edge, for CTL signals there is no change between 10/100Mb/s or 1000Mb/s operation.

For a Gigabit operation, the GTX_CLK and RX_CLK clocks are 125 MHz, and for 10- and 100-Mb/s operation, the clock frequencies are 2.5 MHz and 25 MHz, respectively.

2.2.2.2.3 SGMII

The SGMII differs from the GMII and RGMII by having a higher clock frequency and the 8b/10b (SerDes) coded interface. It uses differential pairs at a 625-MHz clock frequency double data rate (DDR) for TX and RX data and for TX and RX clock. The transmit and receive path uses one differential pair for data and in some cases one for clock. TX and RX clocks must be generated on device output but are optional on device input. With revision 1.8 of the SGMII standard, clock recovery can be used, removing the need for the clock signal. This means that the SGMII can be a 4- to 8-pin solution.

2.2.2.3 Serial Management Interface

The serial management interface (SMI) consists of a Management Data Clock (MDC) and a Management Data Input/Output (MDIO) signal. It provides access to the PHY's internal register space for status information and configuration. The MDC and MDIO signals can be shared amongst several PHYs due to the serial communication protocol, where an address is used to identify the corresponding PHY slave. The MDIO has a standard set of registers from 0 to 31 each containing 16 bits. In IEEE 802ah clause 45, an extended register set was defined for extra functionality of the PHYs. The SMI is initially specified at a 2.5-MHz clock.

2.2.3 IEEE 1588v2

Precise time information is important, especially for distributed systems like in factory automation. The IEEE 1588v2 is an IEEE standard for precision clock synchronization protocol for networked measurement and control systems. The protocol is used to synchronize the time and clock frequency. It defines a way to provide sub-microsecond precision synchronization.

To define this synchronization, the start of package detection is needed. Depending on which application layer this detection happens, the timing error varies. The lower the layer, the smaller the error.

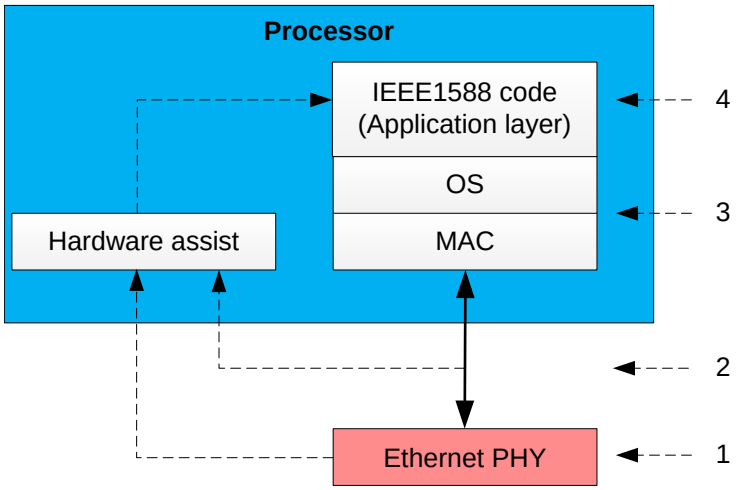


Figure 3. Options 1 to 4 for Time Stamp versus Layer

The closer to the PHY the time stamp is set the better the time reference. The time stamp consists of two signals the Ingress (RX) and Egress (TX) time stamp. Depending on when the time stamp is done, the delay can vary from nanoseconds to microseconds.

2.3 System Design Theory

2.3.1 Circuit Design and Component Selection

2.3.1.1 DP83867IR 10/100/1000-Mb/s Gigabit Ethernet PHY

The DP83867IR was selected due to following features:

- IEEE 802.3ab 1000BASE-T compliant
- Operating temperature range –40°C to 85°C
- 8-kV IEC 61000-4-2 ESD protection (direct contact)
- RGMII with software (register) programmable and hardware configurable (strap resistors) clock skew
- Integrated termination resistors
- Low power: 565 mW
- SOF detect for IEEE 1588 time stamp

In addition to the above features, the DP83867IR also offers the following features:

- Low deterministic TX and RX latency
- Wake on LAN (WoL)
- Synchronized clock output to synchronize multiple PHYs using one crystal (or clock)

2.3.1.1.1 DP83867IR Gigabit Ethernet PHY Configuration

When configuring the DP83867IR, this can be done using either a SMI or a strap configuration through the four-level strap pins. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the four-level strap pin input and the supply to select one of the possible selected modes. The device should feature four-level strap pins, each supporting at least four selectable options, as shown in Figure 4 and Table 4. Strap resistors with 1% tolerance are recommended.

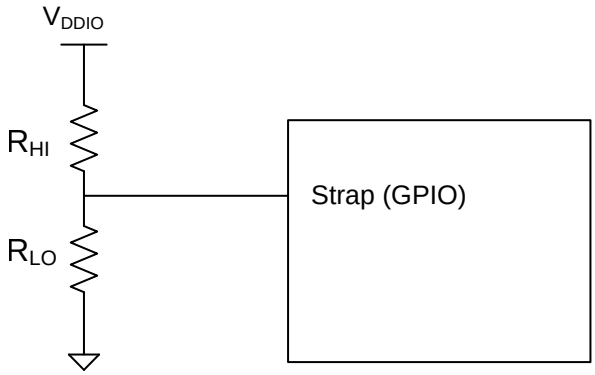


Figure 4. Strap Circuit

Table 4. Four-Level Strap Resistor Ratios

MODE	RESISTOR R_{HI} (kΩ)	RESISTOR R_{LO} (kΩ)
1	OPEN	OPEN
2	11	2.49
3	6.04	2.49
4	2.49	OPEN

Because this design employs two DP83867IR, the SMI will have two DP83867IR slaves addresses. This means that the SMI address of the two DP83867IR have to differ to ensure a valid communication. To set the DP83867IR SMI address a strap configuration option can be used on one DP83867IR to change the default address from 0x00. In this design, it was chosen to use the pin RX_D4 to set the SMI address, as this pin is not used for the RGMII.

A strap configuration option was chosen so the RGMII is always enabled to ensure the RGMII is enabled when as the RX_D6 pin is used as input pin on the AM3359 Sitara processor.

As the clock out option of the device is not used by default, RX_D7 strap configuration option was done to disable the clock out of the device. This feature is default on if this strap on is not done and if it needs to be disabled without strap configuration. It would have to be done using the SMI.

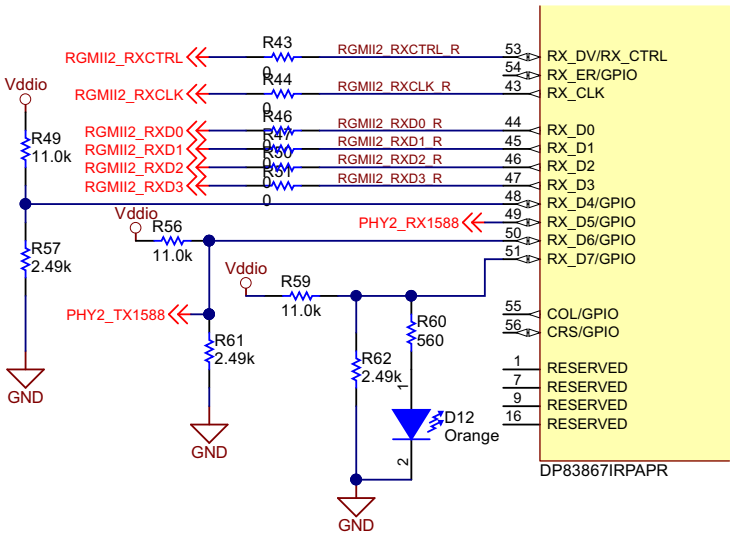


Figure 5. Schematic for DP83867IR Strap Configuration on ETH2

Table 5. DP83867IR Strap on Resistor Chosen

DP83687IR PIN NAME	CONFIGURATION	MODE
RX_D4	Strap resistors	2 (PHY_ADD4 = 1, only ETH2)
RX_D6	Strap resistors	2 (RGMII enable)
RX_D7	Strap resistors	2 (Clock out disable)

When using the strap configuration on a specific pin, ensure that the additional function mapped to this pin is applicable. For example, due to this the TX_D0 to TX_D3 and RX_D0 to RX_D3 pins, which are used by the RGMII, have not been used for strap configuration. This is because this strap resistor configuration would have needed to be compensated with trace matching from the other RGMII pins used. Another example is the LED indicator pins: When used with both LED functionality and strap configuration, take caution on how to connect the LED with regards to the strap resistors. An example for strap mode 0 and strap mode 4 with indicator LED is shown in Figure 6.

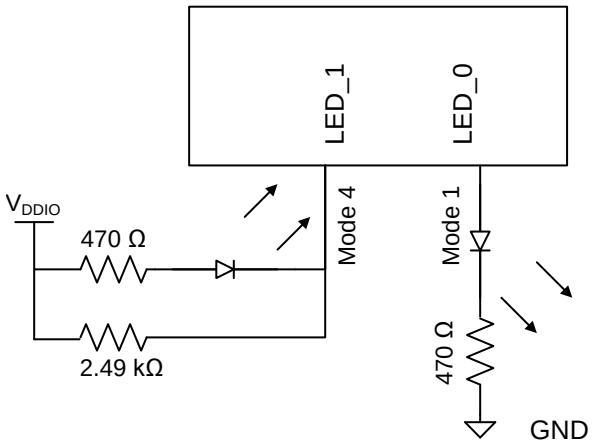


Figure 6. Example Strap Connections With Indicator LEDs for Mode 1 and Mode 4

2.3.1.1.2 MAC Layer Interface

The MAC interface of this design was chosen according to minimum number of pins at lowest possible clock frequency. See Table 6 of the pin definitions.

Table 6. MAC Interface Option Pinout for the Different Standards

DECISION CRITERION	GMII	RGMII	SGMII
Number of MAC interface signals	25	12	4 or 6
Clock frequency	125 MHz	125 MHz	625 MHz

With those considerations, the choice was to use the RGMII as it is running at a lower frequency than the SGMII. Therefore, the RGMII allows for easier PCB routing of the signals, and the number of signals is acceptable.

The RGMII signals are not differential but single-ended, and they are referenced to a clock signal of 125 MHz. It is crucial that length matching is done properly for all signals to avoid skew due to different propagation delay between the clock and the data signals.

For this design, the following rules were followed on the RGMII signals.

Table 7. DP83867 RGMII Design Rules on TIDA-00204 PCB

RULES	DISTANCE
RGMII TX length matching	0.254 mm
RGMII RX length matching	0.254 mm
RGMII data-to-data distance separation	0.762 mm
RGMII clock-to-data distance separation	1.27 mm
RGMII clock-to-clock distance separation	1.27 mm
RGMII TX length matching	0.254 mm
RGMII RX length matching	0.254 mm
Max total trace length	63.5 mm

These rules are referenced from *High-Speed Interface Layout Guidelines* (SPRAAR7).

Additional considerations are to place each PHYs RGMII TX and RX on the same layer and add series termination resistors close to the corresponding output pins. Because the DP83867IR has an integrated 50-Ω series impedance, a 0-Ω series termination has been placed at the DP83867 RGMII RX output pins. This was a test and debug option and the termination resistor (array) can be removed in a production design.

A 22-Ω series termination resistor was placed close to the RGMII1 and RGMII2 TX pins of the AM3359 Sitara.

2.3.1.1.3 Interface From PHY to RJ-45

The transformer used in the MDI connection provides DC isolation between local circuitry and the network cable. The center tap of the isolated winding has a "Bob Smith" termination through a 75-Ω and a 1000-pF capacitor-to-chassis ground. The termination capacitor should be voltage rated to at least 2 kV. The Bob Smith termination reduces noise resulting from common mode current flows.

NOTE: A TVS diode has been placed each between the DP83867IR and the transformer and the transformer and the RJ45 jack. This was a test and debug option only and the position between the DP83876IR and the magnetics showed slightly better results in EMC and EMI, as shown in Figure 7.

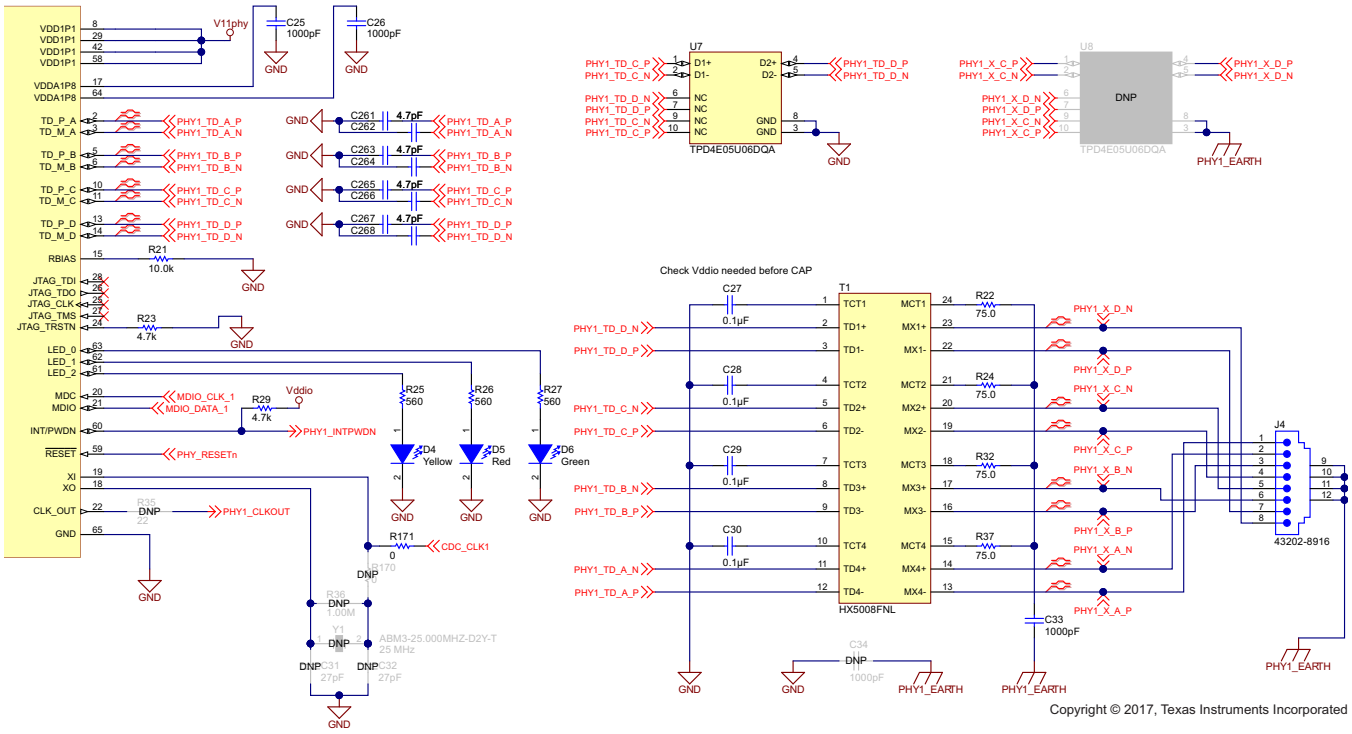


Figure 7. Schematic of Media Dependent Interface of ETH1

The trace length that needs to be considered is from RJ45 to magnetic and from magnetic to DP8867IR, for these signals they are differential pairs. This means that the signals needs to be routed differentially as long as possible without making the traces longer than necessary. To ensure data integrity, the trace's difference should be below 10 mil (0.254 mm).

Table 8. Differential Signal Trace Length From PHY to Magnetic and Magnetic to RJ45 Jack

MEDIA DEPENDENT INTERFACE	RJ45 TO MAGNETIC (mm)	MAGNETIC TO DP8867IR (mm)
PHY1 Differential pair A (N,P)	13.0123 (N), 13.0708 (P)	10.0302 (N), 10.0302 (P)
PHY1 Differential pair B (N,P)	13.1709 (N), 13.3115 (P)	10.0223 (N), 10.0223 (P)
PHY1 Differential pair C (N,P)	13.1321 (N), 13.0146 (P)	10.0175 (N), 10.0082 (P)
PHY1 Differential pair D (N,P)	13.0804 (N), 13.0003 (P)	10.0163 (N), 10.0163 (P)
PHY2 Differential pair A (N,P)	12.9469 (N), 13.0056 (P)	13.3910 (N), 13.4938 (P)
PHY2 Differential pair B (N,P)	12.9398 (N), 13.0815 (P)	13.1988 (N), 13.1047 (P)
PHY2 Differential pair C (N,P)	13.0899 (N), 13.0409 (P)	13.0679 (N), 13.1622 (P)
PHY2 Differential pair D (N,P)	13.1864 (N), 13.1063 (P)	13.3252 (N), 13.2272 (P)

To ensure no unnecessary stubs, all traces are routed on the top layer. The only exception is the pins D2_P and D2_N. Due to the RJ45 jack pin assignment without integrated transformer, this differential pair changed the layer to minimize the overall differential trace length of the four pairs.

Table 9. RJ45 Connector Pinout

PIN	SIGNAL	PIN	SIGNAL
1	D1_P	5	D3_N
2	D1_N	6	D2_N
3	D2_P	7	D4_P
4	D3_P	8	D4_N

2.3.1.1.4 DP83867IR Input Clock Selection

For the input clock, either a crystal or an external clock source can be used. For both cases, the clock needs to be 25 MHz with a tolerance of less than ±50 ppm. For more details, refer to the DP83867IR data sheet, Sections 8.2.1.2 and 8.2.1.3[1]. For this design, a 25-MHz crystal was chosen (see Section 2.3.1.4 for more details).

The DP83867IR has a clock out pin CLK_OUT too. This allows to route the 25-MHz clock from one DP83867IR PHY to the second DP83867IR PHY and eliminates the need for a crystal at the second PHY, reducing costs. The TIDA-00204 design has been prepared for this configuration by adding series 0-Ω resistors.

The preferred option, as realized with revision E3 of this design, is to have all system clocks in the design synced to a single reference clock. This consolidation helps to reduce jitter between the individual clocks on the board. This option is a key feature for system performance between the PHY and the MAC layer communication, especially in real-time Ethernet systems. See Section 2.3.1.4.2 for more details.

The CDCE913 programmable 1-PLL VCXO clock synthesizer is used to generate the two 25-MHz clocks for the DP83867IR.

2.3.1.1.5 Power and Ground Pins

For each of the three power rails on the DP83867IR, decoupling capacitors are recommended as follows. A 1-nF capacitor is recommended be placed close to each supply pin of the DP83867IR. A 10-nF and a 10-µF capacitor are recommended per supply rail.

2.3.1.1.6 PHY RESET

The DP83867IR PHYs are automatically reset after power-up, through signal SYS_RESETn. Additionally, the DP83867IR hardware reset signal PHY_RESETn can be issued by the Sitara AM3359 GPIO pin with the signal GPIO_PHY_RESETn, which offers a software option to reset the PHYs if needed.

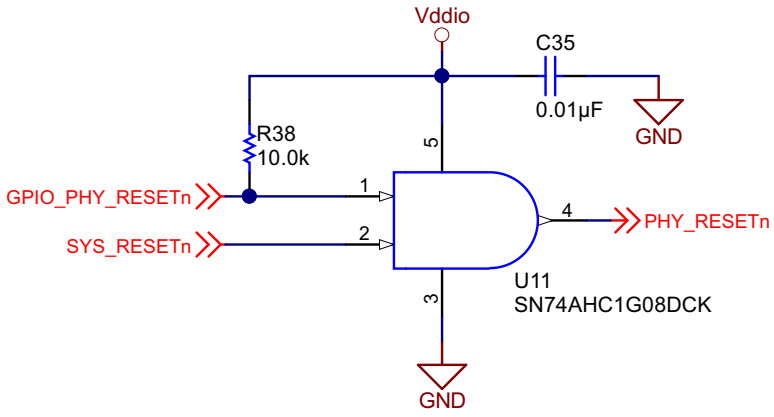


Figure 8. PHY Reset Option During Power Up (SYS_RESETn) and Software Reset (GPIO_PHY_RESETn)

2.3.1.1.7 Not Connected Pins on DP83867

Table 10. DP83867IR Not Connected Pins

PINS	REASON
TXD4:7	Internal pull-down
TX_ER	Internal pull-down
TX_CLK	Output
COL	Internal pull-down
CRS	Internal pull-down
Reserved	Reserved
JTAG (TDI, TMS, TCLK)	Internal pull-up
JTAG (TDO)	Output

2.3.1.2 Host Processor

The Sitara AM3359 was chosen as it has a 2-Gb Ethernet MAC with switch layer supporting RGMII to both DP83867IRs. The MAC switch layer inside the AM3359 is supporting several features of passing messages from one PHY to the other without the use of the core. To achieve deterministic and very low transmit and receive latency, the ICSS/PRU subsystem can be used to capture the start of frame for IEEE 1588 time stamp. The TIDA-00204 hardware is provisioned for this feature but not tested.

2.3.1.2.1 AM3359 Boot Mode Configuration

The AM3359 internal ROM code selects the corresponding peripheral based on the level of the SYSBOOT configuration at power on reset of the device. For the full details of this boot procedure, read Sections 26.1.5 to 26.1.8 of the Technical Reference Manual of the AM335x Sitara processors.

For easy standalone operation, the AM3359 has been configured to boot from MMC1/SD-Card. This configuration requires the SYSBOOT[15:0] pins to be "0100 0000 0001 1100". This is achieved by setting the corresponding pull-up and pull-down resistors as per the schematics in Figure 9.

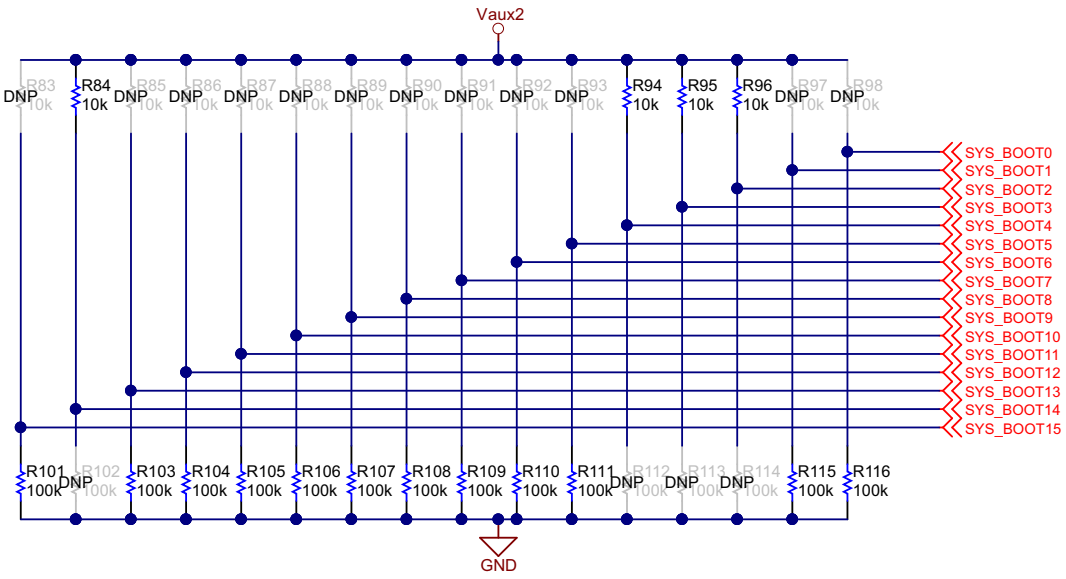


Figure 9. AM3359 SYSBOOT Pin Configuration for MMC1/SD-Card Boot Mode

2.3.1.2.2 AM3359 GPIO Pin Assignment

When using the Sitara before starting the design, ensure that the peripherals functions required for the design can be assigned to the specific GPIO pins without a mux conflict. For this purpose, there is a pin mux tool utility for TI processors called PINMUXTOOL-V3. The tool can be downloaded from the TI website (www.ti.com). There are specific versions pending the device, part, and package. This tool is a huge help for AM3359 pin assignment.

This design uses the following peripherals: EMAC with RGMII1 and RGMII2, UART, MMC0 and MMC1, MDIO, SDRAM/DDR3, I^2C, and ECAP.

The pin mux tool was used to find the optimum pin assignment for the different peripherals used in the TIDA-00204 reference design.

Table 11. AM3359 Pin Assignment

SIGNAL	PINS (GPIO MODE)	AMOUNT OF PINS
RGMII1	J16-J18, K15-K18, L15-L18, M16 (Mode 2)	12
RGMII2	R13-14, V14-V17, U14-U16, T14-T16 (Mode 2)	12
UART	G15-G16(Mode 3)	2
MMC	U9, V9 (Mode 2), U7, V7, R8, T8 (Mode 1)	6
MDIO	M17-M18 (Mode 0)	2
JTAG	Fixed pins not available with mux	8 to 11
SDRAM (DDR3)	Fixed pins not available with mux	52
I^2C	C16-C17 (Mode 0)	2
ECAP	U13 (Mode 5), C15 (Mode 2), C18 (Mode 0), E15 (Mode 4)	4

The remaining pins could be used in GPIO mode or assigned to unused peripherals on the AM3359 device.

2.3.1.2.3 MMC1 Micro SD-Card

Figure 10 shows the micro SD-Card interface including ESD protection device on the TIDA-00204. The TPD6E001 is a low-capacitance ±15-kV ESD-protection diode array designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steer ESD current pulses to VCC or GND. The TPD6E001 protects against ESD pulses up to ±15-kV human-body model (HBM), ±8-kV contact discharge (CD), and ±15-kV air-gap discharge, as specified in IEC 61000-4-2.

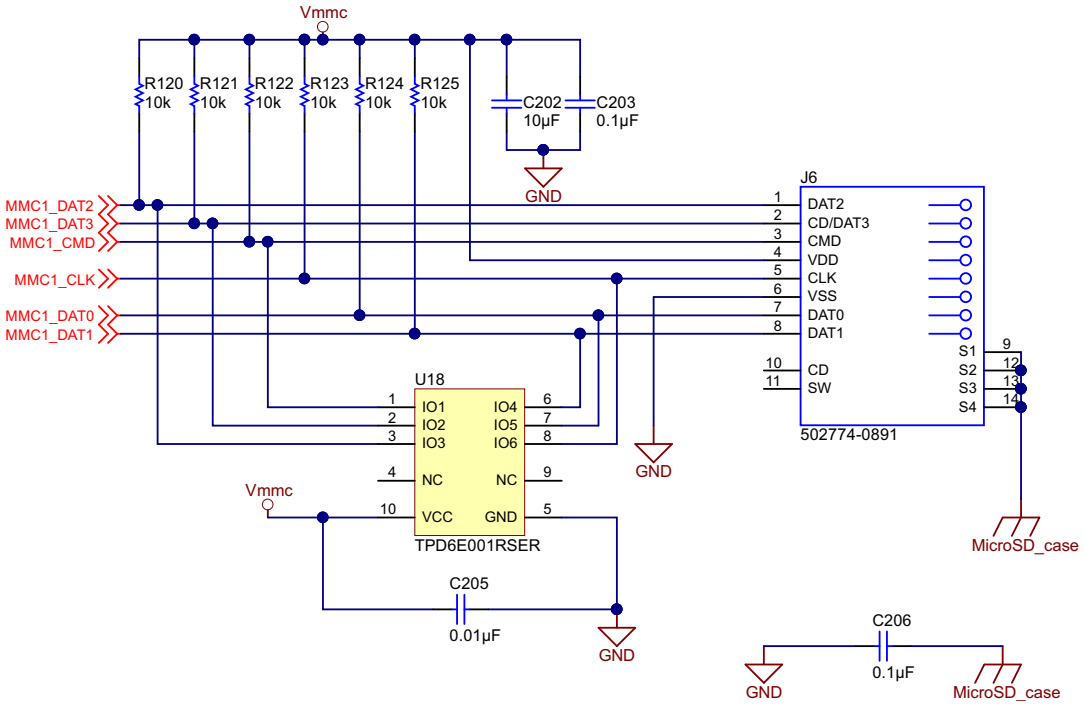


Figure 10. MMC1 Micro SD-Card Interface With ESD Protection

2.3.1.2.4 I²C Communication to PMIC and EEPROM

The I²C module 0 is used for communicating with both, the EEPROM, and the Power Management IC (PMIC). The PMIC I²C is hardcoded to the I²C address equal to 0101101 binary or 0x2D in hex.

The EEPROM was given the binary address 1010000 equal to 0x50 in hex. This is done by setting the A_2, A_1, and A_0 pin. This then forms the 7-bit address as "1010$A_2A_1A_0$".

2.3.1.2.5 DDR3 RAM

For this design, the MT41J128M16JT-125K TR DDR3 RAM was chosen to leverage experience from the TI AM3359 Industrial Communications Engine development platform with part number TMDSICE3359. This memory requires a 1.5-V supply with a rise time better than 200 ms. During this time a V_{TT} supply needs to be provided as this rail is a system supply for signal termination resistors. Once powered, the device needs to be reset before going into the initialization state. Then the memory is ready for operation.

Due to the speed of the signals to the DDR3 RAM, length matching and termination are important to ensure performance. For the data lines, length matching was done by defining different net classes with specific considerations. The concept of defining different net classes is important when routing high speed signals, as they can insure timing constraints or timing relationships. When defining these groups, it is important to understand the basics of the DDR3 memory signals. For DDR3, the signals can be divided into four different groups that have similar requirements.

Table 12. DDR3 Net Class Definitions

NET CLASS	SIGNALS
Data	DDR_D[15:0],DDR_DQM[1:0], DDR_DQS0[_P and _N], DDR_DQS1[_P and _N]
Address/Command	DDR_A[13:0],DDR_BA[2:0], DDR_CASN, DDR_RASN, DDR_WEN
Control	DDR_CKE, DDR_CSN, DDR_ODT, DDR_RESETN
Clock	DDR_CLK_N,DDR_CLK_P

For the different groups, it is possible with either software or hardware to shift the sampling point. Even with this feature of DDR3 RAM, it is still needed to do a timing budget calculation. With this calculation, it is possible to have an estimation of how the length matching needs to be. Length matching is needed due to the fact that the typical propagation delay for the FR4 PCB is approximately 6.5 ps/mm and so a length mismatch would lead to a delay of the signal compared to the other signal lines. As an example the net class data has been matched as seen in Table 13.

Table 13. DDR3 Trace Length on PCB for Net Class Data

SIGNAL	TRACE LENGTH (mm)	SIGNAL	TRACE LENGTH (mm)
DDR_D0	27.4776	DDR_D8	25.3669
DDR_D1	27.6777	DDR_D9	25.2680
DDR_D2	27.4567	DDR_D10	25.4147
DDR_D3	27.2947	DDR_D11	25.6113
DDR_D4	27.4070	DDR_D12	25.6584
DDR_D5	27.5413	DDR_D13	25.3574
DDR_D6	27.4398	DDR_D14	25.5648
DDR_D7	27.3044	DDR_D15	25.4486
DDR_DQM0	27.3479	DDR_DQM1	25.4907
DDR_DQS0_N	27.4755	DDR_DQS1_N	25.4209
DDR_DQS0_P	27.4726	DDR_DQS1_P	25.4285

Termination was done with parallel termination of 47 Ω to improve performance. Arrays were chosen here to minimize size.

Further general considerations are:

- All nets in the address and command fly-by groups shall have the same number of vias in each length-matched segment. Ground vias are placed to ensure a proper current return path. Minimize use of vias on signal traces as they negatively impact signal integrity.
- The single-ended Address/Command net class and the control net class needs external termination to V_{TT}.
- For the data net class within a byte lane, the data bits can be swapped to simplify routing.
- Organize the power, ground, and signal planes to eliminate or significantly reduce the number of split or cut planes present in the design (no splits are allowed under any DDR3 routes).
- Maintain an acceptable level of skew across the entire DDR3 interface (by net class).
- It is strongly recommended that all nets be simulated to assure proper design, performance, and signal integrity.
- Take into account the differences in propagation delays between microstrip and stripline nets when evaluating timing constraints. All long routes should be stripline to reduce EMI and timing skew, and any microstrip routed for BGA breakouts should be as short as possible.
- Routes along the same path and routing segment must have the same number of vias. Vias can be blind, buried, or HDI microvia for improved signal integrity, but are not required for standard data rates. Similarly, back drilling vias is not required for standard data rates but can be used to eliminate via stubs.
- For this design, the DDR3 layout was copied from the TI AM3359 Industrial Communications Engine development platform with part number TMDSICE3359 to leverage a working and fully tested design with the peripheral settings for the DDR3 interface.

2.3.1.2.6 AM3359 Clocking Options

For the clock, either a crystal or a digital clock source can be used. For both cases, the clock needs to be 19.2, 24, 25, or 26 MHz with a tolerance of ±50 ppm. For more details, see Section 6.2.2 of the AM3359 data sheet[5]. For this design, a 24-MHz crystal was chosen as used with the TMDSICE3359 AM3359 Industrial Communications Engine development platform.

The preferred option, as realized with revision E3 of this design, is to have all system clocks in the design synced to a single reference clock. This consolidation helps to reduce jitter between the individual clocks on the board. This option is a key feature for system performance between the PHY and the MAC layer communication, especially in real-time Ethernet systems. See Section 2.3.1.4.2 for more details.

The CDCE913 programmable 1-PLL VCXO clock synthesizer is used to generate the 24-MHz clock for the AM3359.

2.3.1.2.7 Power Supply Pins

For the decoupling capacitors on the different power rails of the AM3359, see Section 5.9 of the AM3359 data sheet[5].

2.3.1.2.8 USB Virtual COM Port and JTAG Interface

An FTDI chip connects to a micro USB port. This FTDI chip can be used for both JTAG (XDS100) and Virtual COM port functionality. A separate JTAG header is available too.

To use the FTDI chip, the onboard EEPROM, which is connected to the FTDI chip, needs to be programmed as follows:

- To program the EEPROM connected to the FTDI chip, get the tool "Mprog". To find this tool, go to the following webpage for the download link.
  http://processors.wiki.ti.com/index.php/XDS100#How_to_make_an_XDS100
- The EEPROM needs to be programmed in a specific way. To find an example image also called a *.ept file to write in the EEPROM, go to the following webpage:
  http://processors.wiki.ti.com/index.php/XDS100

A .ept file for the Mprog tool is available for the specific XDS100 version needed. Download a .ept file, which includes both JTAG and Virtual COM port functionality.

To verify the image is programmed correctly, power the board and connect the micro USB to the PC. Now go into the start menu and open the menu *Devices and Printers* for Windows® 7. The following connection should now be found (see Figure 11).

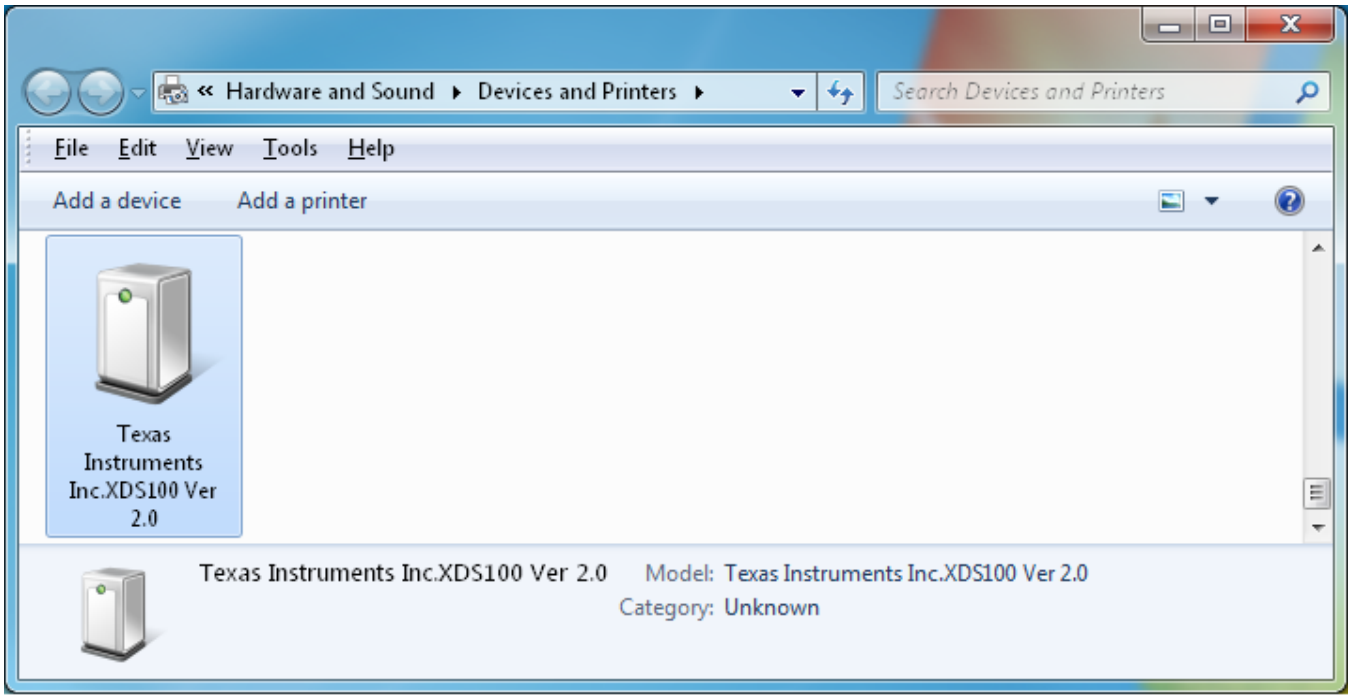


Figure 11. XDS100v2 Driver in Windows 7 Devices and Printers Menu

If Figure 11 does not appear, retry the previous steps.

When this is done properly, Code Composer Studio™ v6 can be used to connect to the AM3359 core through JTAG using the XDS100v2 driver.

2.3.1.3 Power Supplies

The power supplies are realized in three stages. The first stage is a 24-V to 5-V DC/DC to provide an intermediate 5-V rail to the other two stages. The second stage is a PMIC supplying the host processor, and the last stage is supplying the two Gigabit PHYs.

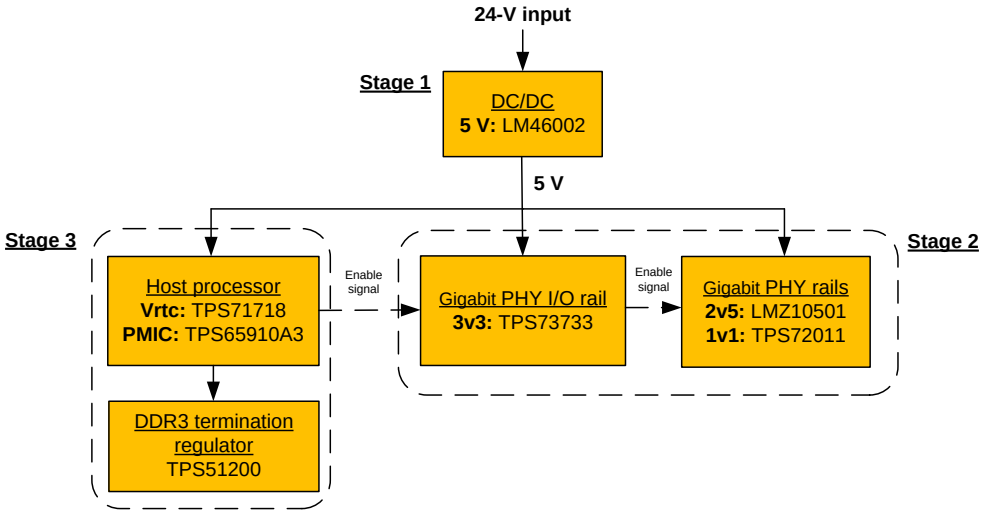


Figure 12. TIDA-00204 Power Supply Stages

2.3.1.3.1 24-V to 5-V DC/DC Buck Converter

For this stage, the LM46002 SIMPLE SWITCHER® regulator was chosen. It is an easy-to-use synchronous step-down DC-DC converter capable of driving up to 2 A of load current from an input voltage ranging from 3.5 to 60 V. The LM46002 provides exceptional efficiency, output accuracy, and drop-out voltage in a very small solution size. The family requires few external components. Pin arrangement allows for a simple, optimum PCB layout.

An extended family is available in various load current options with pin-to-pin compatible packages, including LM46001.

The schematic of the LM46002 is shown in Figure 13.

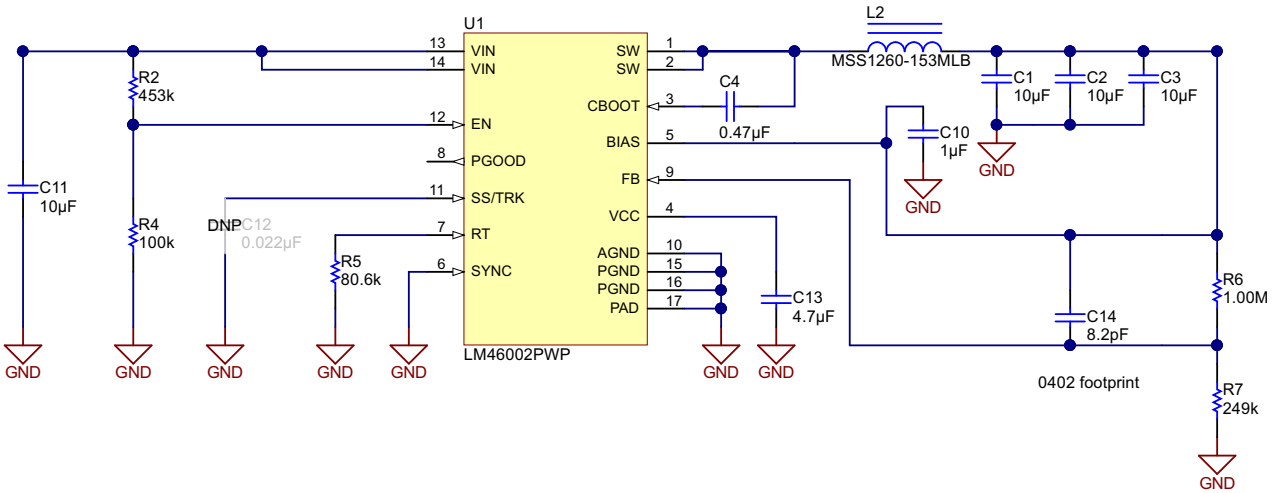


Figure 13. Schematic of 24-V to 5-V DC/DC Buck Converter With LM46002

2.3.1.3.1.1 Passive Components Calculations

The first step is to decide and set the switching frequency of the regulator. In the TIDA-00204, the switching frequency (F_{SW}) is set to 500 kHz thanks to R_5. Equation 1 indicates that R_5 should be 79.8 kΩ. 80.6 kΩ is then used as value for R_5.

$$R_5 = \frac{40200}{F_{sw}} - 0.6 \quad (1)$$

with

- F_{SW} in kHz and R_5 in kΩ

The default frequency is also 500 kHz, due to the internal oscillator precision of 20% it was chosen to use a resistor for the 500-kHz frequency. This gives a 10% precision. Secondly, during EMI test it can be useful for fine tuning to move the frequency up or down to change the harmonic spectrum of the converter.

Once the switching frequency is set, the size of inductance needed it chosen. For most buck converters, this value is chosen to achieve the wanted peak-to-peak ripple current that flows in the inductor along with the DC load current. A higher inductance gives lower ripple current, which then gives a lower output voltage ripple with the same output capacitors. An inductance that gives a ripple current of 20% to 40% at the maximum current is normally a good starting point. The minimum inductor value is calculated based on input voltage range (17 to 60 V), output voltage (5 V), maximum output current (2 A) and the switching frequency (500 kHz) as set in the previous step. The duty cycle (D) can be approximated as $D = V_{OUT}/V_{IN}$, assuming no loss power conversion.

$$\frac{(V_{IN} - V_{OUT}) \times D}{0.4 \times F_{sw} \times I_{OUT}} \le L_{min} \le \frac{(V_{IN} - V_{OUT}) \times D}{0.2 \times F_{sw} \times I_{OUT}} \quad (2)$$

The calculation gives that the inductor needs to be between 9 and 23 μH; for this design, 15 μH was chosen.

Besides the inductor size, the rated saturation current needs to be specified as per Equation 4.

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times D}{L_2 \times F_{sw}} \quad (3)$$

$$I_{L-peak} = I_{OUT} + \frac{I_{RIPPLE}}{2} \quad (4)$$

The inductor peak current is 2.305 A according to Equation 3 and Equation 4. A good practice is to use an inductor with the saturation current around 1.5 to 2 times higher than calculated.

The LM46002 has both valley current limit and peak current limit. During an instantaneous short, the peak inductor current can be high due to a momentary increase in duty cycle. The inductor current rating should be higher than the peak current limit. Select an inductor with a larger core saturation margin and preferably a softer roll off of the inductance value over load current.

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But a too low inductance can generate too large inductor current ripple such that over current protection at the full load could be falsely triggered. It also generates more conduction loss because the RMS current is slightly higher relative that with lower current ripple at the same DC current. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak current mode control, it is not recommended to have too small of an inductor current ripple. Enough of an inductor current ripple improves the signal-to-noise ratio on the current comparator and makes the control loop more immune to noise.

The maximum desired output voltage ripple and the transient response to load changes are the parameters to take into account for selecting the value of the output capacitors.

$$C_{OUT} > \frac{1}{F_{sw} \times r \times \Delta V_{OUT} / \Delta I_{OUT}} \times \left(\left(\frac{r}{12} \times \left(1 + \left(1 - D\right)\right) \right) + \left(\left(1 - D\right) \times \left(1 + r\right) \right) \right) \quad (5)$$

with

- ΔI_{OUT} equal load current (2 A)
- ΔV_{OUT} equal target output voltage undershoot (0.5 V)
- r the inductor ripple ratio ($\Delta I_L / I_{OUT}$)

Equation 5 indicates that C_{OUT} should be higher than 10.0 µF. A general guideline would be to pick C_{OUT} between the minimum required output capacitance, calculated in Equation 6, and multiply this minimum required capacitance by 10. Two 10.0 µF in parallel were chosen to fit the C_{OUT} requirements.

The second requirement is the maximum ESR of the capacitor, which can be found using Equation 6.

$$ESR < \frac{\left(1 - D\right)}{F_{sw} \times C_{OUT}} \times \left(\frac{1}{r} + 0.5 \right) \quad (6)$$

Equation 6 calculates the maximum ESR of the output capacitor to meet the maximum output ripple required. The equivalent ESR of the output capacitors C_3 and C_4 should be lower than 0.288 Ω.

The LM46002 requires high quality ceramic (X5R or X7R) input decoupling capacitors. The recommended value is between 4.7 to 10 µF. A good practice for ceramic capacitors is to choose a voltage rating of twice the maximum input voltage. If the placement of the LM46002 additional bulk capacitance is needed, this additional capacitor dampens voltage spikes caused by the lead inductance of the trace. The value is not critical but it must be rated to fit the voltage requirements.

The output voltage is externally adjusted with a resistor divider network. The divider network is comprised of top feedback resistor R_6 and bottom feedback resistor R_7. Equation 7 is used to determine the output voltage of the converter.

$$R_7 = \frac{V_{FB}}{V_{OUT} - V_{FB}} \times R_6 \quad (7)$$

R_6 is chosen to be 1 MΩ to minimize quiescent current, which improves light load efficiency in this application. With the desired output voltage set to be 5 V and the V_{FB} is equal to 1.01 V, the R_7 value can then be calculated using Equation 7. The equation gives the value 253.4 Ω. The chosen value for this design is a 249-kΩ resistor. For more details on the adjustable output voltage, see the LM46002 data sheet[11].

The LM46002 is internally compensated and the internal R-C values are 400 kΩ and 50 pF, respectively. Depending on the V_{OUT} and the frequency F_S, if the output capacitor C_{OUT} is dominated by low ESR (ceramic types) capacitors, it could result in low-phase margin. To improve the phase boost, an external feed forward capacitor C_{14} can be added in parallel with R_6. C_{14} is chosen such that the phase margin is boosted at the crossover frequency without C_{14}. A simple estimation for the crossover frequency without C_{14} (F_X) is shown in Equation 8.

$$f_X = \frac{4.35}{V_{OUT} \times C_{OUT}} \quad (8)$$

The following equation for C_{14} was tested:

$$C_{14} = \frac{1}{2 \times \pi \times F_X} \times \frac{1}{\sqrt{R_6 \times \left(R_6 \,||\, R_7\right)}} \quad (9)$$

Equation 9 indicates that the crossover frequency is geometrically centered on the zero and pole frequencies caused by the C_{14} capacitor.

For designs with higher ESR, C_{14} is not needed. When C_{OUT} has medium ESR, C_{14} calculated from Equation 9 should be reduced. With Low ESR used the calculated value. Table 2 of the LM46002 data sheet can be used as a starting point. The calculated value is 8.2 pF, and an 8.2-pF COG capacitor was selected for C_{14}.

The LM46002 needs a bootstrap capacitor C_4. The recommended bootstrap capacitor is 0.47 µF and rated at 6.3 V or higher. The bootstrap capacitor must be a high quality ceramic type with X7R or X5R grade dielectric for temperature stability.

The V_{CC} pin is the output of an internal LDO for the LM46002. The input for this LDO comes from either V_{IN} or bias. To ensure stability of the part, place a minimum of a 2.2-µF, 10-V capacitor from this pin to ground.

For an output voltage of 3.3 V or higher, the BIAS pin can be connected to the output in order to increase efficiency. This pin is an input for the V_{CC} LDO. When BIAS is not connected, the input for the V_{CC} LDO will be internally connected into V_{IN}. Because this is an LDO, the voltage differences between the input and output will affect the efficiency of the LDO. If necessary, a capacitor with the value of 1 µF can be added close to the BIAS pin as an input capacitor for the LDO.

The soft start capacitor (C_{12}) determines the minimum amount of time it will take the output voltage to reach its programmed value during start up. This also allows limiting the inrush current in the LM46002 (current require to charge the output capacitors to the programmed value). If this pin is left unconnected, the soft start time is 4.1 ms typically. Longer soft start times can be set by an external soft start capacitor per Equation 10.

$$C_{12} = I_{ssc} \times t_{ss} \tag{10}$$

with

- C_{12} equal the soft start capacitor value (µF)
- I_{SSC} the soft start charging current (µA)
- t_{SS} equals the desired soft start times

The I_{SSC} current is 2.2 µA, defining a soft start time of 10 ms would equal a soft start capacitor of 0.022 µF.

The undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_2 and R_4. R_2 is connected between the VIN pin and the EN pin of the device. R_4 is connected between the EN pin and the GND pin. The UVLO has two thresholds: one for power up when the input voltage is rising, and one for power down or brown outs when the input voltage V_{IN} is falling. Use Equation 11 to determine the $V_{UVLO\text{-}Falling}$ level.

$$R_2 = \left(\frac{V_{UVLO-Falling}}{V_{ENL}} - 1 \right) \times R_4 \tag{11}$$

The enable falling edge threshold (V_{ENL}) for the LM46002 is 1.8 V. R_4 was chosen to 100 k to minimize input current from the supply. If the desired VIN UVLO falling level is 10 V, the value of R_2 can be calculated using Equation 12. That is equal to 455.6 k. R_2 was chosen to be 453 k.

$$V_{UVLO-Rising} = V_{ENH} \times \frac{\left(R_4 + R_2\right)}{R_4} \tag{12}$$

The enable rising edge threshold (V_{ENH}) for the LM46002 is 2.1 V. Equation 12 can be used to calculate the required input voltage to meet the rising threshold to enable the converter. With the above chosen resistors, the LM46002 will enable at 11.6 V.

2.3.1.3.2 Power Supply for Two Gigabit Ethernet PHYs

The PHY power supplies need to provide three power rails. The 3.3-V V_{DDIO} power rail is sequenced from the 3.3-V PMIC rail (see Section 2.3.1.3.2.1). When the V_{DDIO} power rail is enabled, it will enable the remaining two rails 2.5 V and 1.1 V as seen in Figure 14. The information on the power consumption of the Gigabit Ethernet PHY can be seen in Section 6.5 of the DP83867IR data sheet[1].

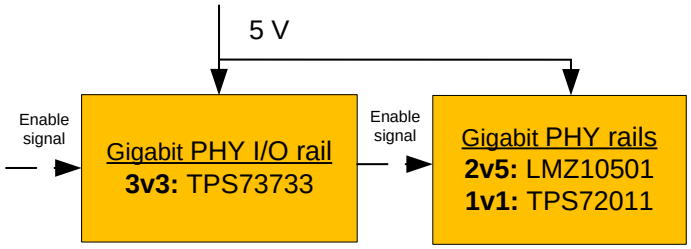


Figure 14. Power Stage for Two Gigabit Ethernet PHYs

2.3.1.3.2.1 DP83867IR Current Consumption

The DP83867IR has two power options. One option requires two rails for the core and one rail for the V_{DDIO}. In this setup, the PHY draws 565 mW. For the two-rail option, no sequencing is required. If power dissipation on the DP83867IR is critical, the second option uses three rails for core and one rail for V_{DDIO}. In this setup, the PHY draws 545 mW. V_{DDIO} can be 3.3, 2.5, or 1.8 V. See its data sheet for more details on the current consumption per rail and if a voltage other than 3.3 V is used in the V_{DDIO} rail[1].

Table 14. Power Consumption per Voltage Rail

RAIL	STANDARD POWER MODE (565 mW)	LOW POWER MODE (545 mW)
1.1 V	106 mA	106 mA
1.8 V	N/A	64 mA
2.5 V	157 mA	103 mA
V_{DDIO} (3.3, 2.5, or 1.8 V)	31 mA (1.8 V)	31 mA (1.8 V)

For this design, the power supply was designed for the two-rail standard power mode option to fit two DP83867IR PHYs.

The TPS72011 and LMZ105001 were chosen for the 1.1-V rail and the 2.5-V rail, respectively.

For the V_{DDIO} 3.3 V, the TPS73733 was chosen. This rail is also used as supply rail for other interfaces on board (for example, for the Gigabit Ethernet PHY LEDs and V_{DDIO} voltage rail, the EEPROM, the debug or JTAG circuitry, reset circuitry, and additional pull up resistors for data communication lines).

These parts were chosen because of their feature of industrial temperature range –40°C to 85°C and that they could dissipate the needed power at 85°C. Here it is important to choose the correct package of the device; several other part numbers could fit the electrical specification. However, their package would not be able to dissipate the needed power at the full current and temperature range. Knowing the voltage drop across the LDO and the power dissipation at 85°C, the maximum current that can be dissipated for the decided voltage rail can be calculated.

Table 15. 3.3-V and 1.1-V LDO Power Dissipation per Package

DEVICE	INPUT VOLTAGE	OUTPUT VOLTAGE	VOLTAGE DROP	MAX POWER DISSIPATION AT 85°C AMBIENT TEMPERATURE	RθJA	MAX CURRENT AT 85°C
TPS72011DRV	2.5 V	1.1 V	1.4 V	615 mW	65 K/W	439.29 mA
TPS73733DCQ	5 V	3.3 V	1.7 V	790 mW(1)	53.1 K/W	464.71 mA(1)

(1) Estimated power dissipation and max current at 85°C using junction-to-ambient thermal resistance.

The 2.5-V rail at LMZ10501 was chosen due to the fact that an LDO with the current needed would be a very expensive device and would dissipate a significant amount of power. When two PHYs are powered approximately 526 mA is required, with margin the 1-A LMZ10501 was chosen.

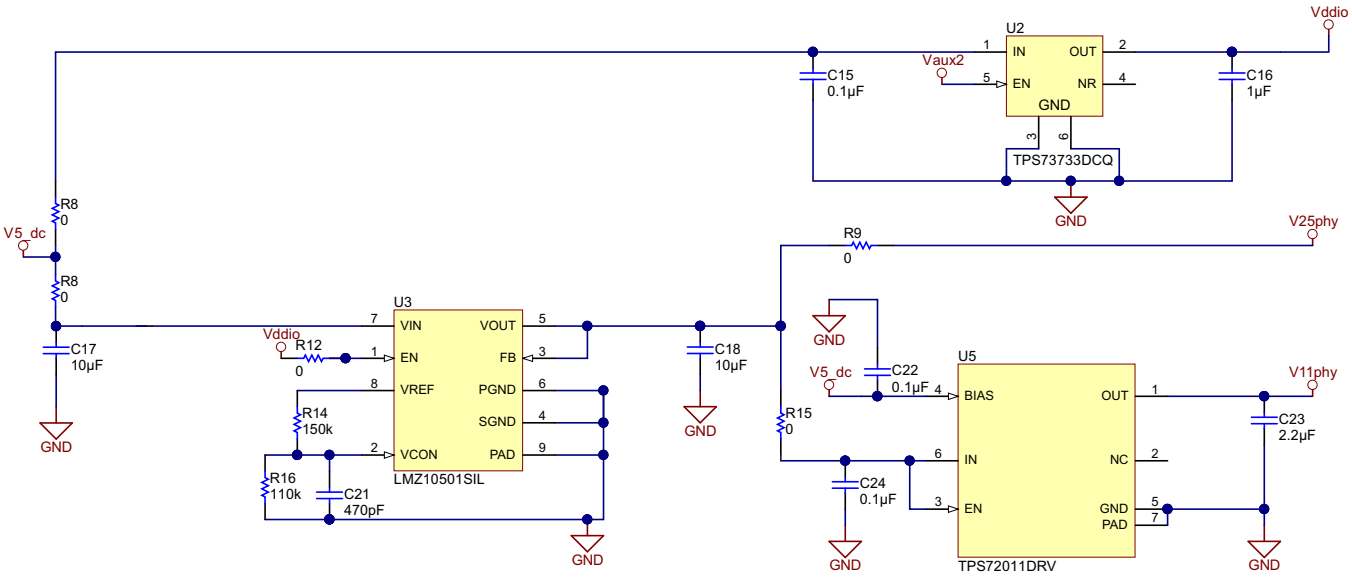


Figure 15. Schematic of Power Supply for Two DP83867IR Gigabit Ethernet PHYs

Use Equation 13 to calculate the output voltage for the LMZ10501.

$$R_{16} = \left(\frac{V_{OUT}}{5.875\ V - V_{OUT}} \right) \times R_{14} \tag{13}$$

R_{14} needs to between 80 and 300 kΩ and R_{16} can be calculated. R_{14} has to be minimum 80 kΩ to ensure that the V_{REF} output current loading is not greater than 30 µA and the reference voltage is maintained. This design needed a 2.5-V output voltage and the R_{14} was decided to be 150 kΩ and the R_{16} is now calculated to 111.1 kΩ. A 110-kΩ resistor was chosen. A small filter capacitor of 470 pF with a voltage rating of 6.3 V or 10 V is connected in parallel to R_{16}. The input and output capacitors are recommended to be X5R or X7R.

2.3.1.3.3 Power Stage for AM3359 Host Processor

The power stage for the AM3359 Sitara is realized using the PMIC TPS65910A3 and a DDR3 terminator regulator TPS51200. An additional TPS71718 LDO is used for the RTC circuit of the Sitara, as the TPS65910A3 RTC circuit has been turned off.

The TPS65910A3 can be configured through I^2C, this interface can be used to set internal registers of the PMIC. For more details on these registers, see the TPS65910A3 user's guide. The TPS65910A3 have the following power sources that can be used, each of the power supplies can be programmed to work at several voltages. For the TPS65910A3, there are several boot modes depending on the device that needs to be powered. Because the AM3359 is used, the EEPROM sequence has been chosen boot[1:0] = "10". For more information on this topic, see Section 8.

Table 16. TPS65910A3 Default Voltage Rails per "10" EEPROM Sequence

RAIL NAME	TYPE	VOLTAGE OPTIONS	DEFAULT VOLTAGE	POWER
VIO	SMPS	1.5, 1.8, 2.5, or 3.3 V	1.5 V	1000 mA
VDD1	SMPS	0.6 to 1.5 V in 12.5-mV steps Programmable multiplication factor: ×2, ×3 1.1 V	1.1 V	1500 mA
VDD2	SMPS	0.6 to 1.5 V in 12.5-mV steps Programmable multiplication factor: ×2, ×3 1.1 V	1.1 V	1500 mA
VDD3	LDO	5 V or OFF	N/A	100 mA
VDIG1	LDO	1.2, 1.5, 1.8, or 2.7 V	1.8 V	300 mA
VDIG2	LDO	1, 1.1, 1.2, or 1.8 V	1.8 V	300 mA
VPLL	LDO	1.0, 1.1, 1.8, or 2.5 V	1.8 V	50 mA
VDAC	LDO	1.8, 2.6, 2.8, or 2.85 V	1.8 V	150 mA
VAUX1	LDO	1.8, 2.5, 2.8, or 2.85 V	1.8 V	300 mA
VAUX2	LDO	1.8, 2.8, 2.9, or 3.3 V	3.3 V	150 mA
VAUX33	LDO	1.8, 2.0, 2.8, or 3.3 V	3.3 V	150 mA
VMMC	LDO	1.8, 2.8, 3.0, or 3.3 V	3.3 V	300 mA
VRTC	LDO	1.8 V or OFF	OFF	OFF

The TPS51200 is used for the DDR3 ram as the sink/source termination regulator. The DDR memory termination structure determines the main characteristics of the V_{TT} rail, which is to be able to sink and source current while maintaining acceptable V_{TT} tolerances. The V_{TT} accuracy has a direct impact on the memory signal integrity, it is imperative to understand the tolerance requirements on V_{TT}. The termination current demand of the DDR3 is less than 1 A of burst current. The TPS51200 ensures the regulator output voltage to be between V_{TTREF} – 25 mV < V_{TT} < V_{TTREF} + 25 mV.

2.3.1.4 System Clocks

There are several options to apply the clocks. For systems with distributed clocks, a clock distribution circuit can be used too. The initial design leverages a crystal on each DP83867IR as well as on AM3359 Sitara. This was due to initial test and debug to allow individual component testing.

2.3.1.4.1 Individual Crystals

The crystal manufacturers define the load capacitance of their crystal in their data sheet. This load capacitance C_L is the sum of the PCB parasitic stray capacitance C_S and the external load capacitors C_X and C_Y, respectively, as per Equation 14. Assuming that the external load capacitors are the same value, they can be calculated with Equation 14.

$$C_X = C_Y = 2 \times (C_L - C_S) \quad (14)$$

C_S is the stray capacitance (device and PCB) this value can be assumed to a few pF as a rule of thumb.

The load capacitors need to be NPO/COG type. Table 17 shows the selected load capacitors per crystal and per device on the TIDA-00204.

Table 17. Parallel Capacitors Needed for Oscillation Circuit

CRYSTAL	DEVICE	C_L	C_S	$C_X = C_Y$
ABM3-25.000MHZ-D2W-T	DP83867IR	18 pF	4 pF	27 pF
ABM3-24.000MHZ-D2W-T	AM3359	18 pF	4 pF	27 pF
ABM3-12.000MHZ-D2Y-T	FT2232HL	18 pF	4 pF	27 pF
MC-306 32.7680K-A0:ROHS	AM3359 (RTC)	12.5 pF	3 pF	19 pF

In this design, the default configuration is one crystal at each DP83867IR PHY. However, the hardware is prepared thanks to 0-Ω resistors to clock the second DP83867IR PHY from the PHY 1, as shown in Figure 16. If desired, this configuration can be tested.

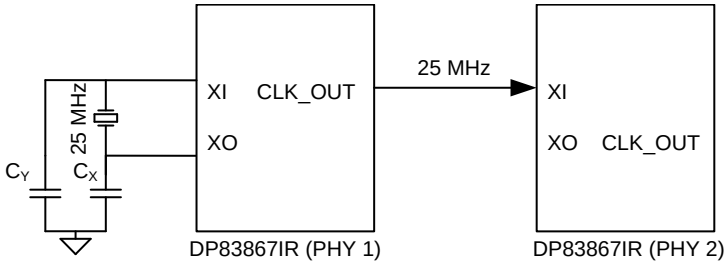


Figure 16. Crystal Configuration for DP83876IR and Option to Clock the Second DP83867IR PHY From the First DP83867IR

2.3.1.4.2 Clock Distribution Circuits

Alternatively to the XTAL clocking as implemented on the TIDA-00204 reference design, a more advanced clocking solution is possible. The following section describes how this could be implemented.

One reason for implementing a clock distribution circuit is to achieve high timing accuracy, which is required for the real-time Ethernet protocols. A crystal can typically have around ±50 ppm in combined tolerance and a stability specification at 25°C, which means that a 25-MHz crystal with 50 ppm can potentially run at 25 MHz ±1250 Hz.

When running several crystals, the phase shift between the two crystals can potentially be maximum negative and maximum positive, which Figure 17 shows.

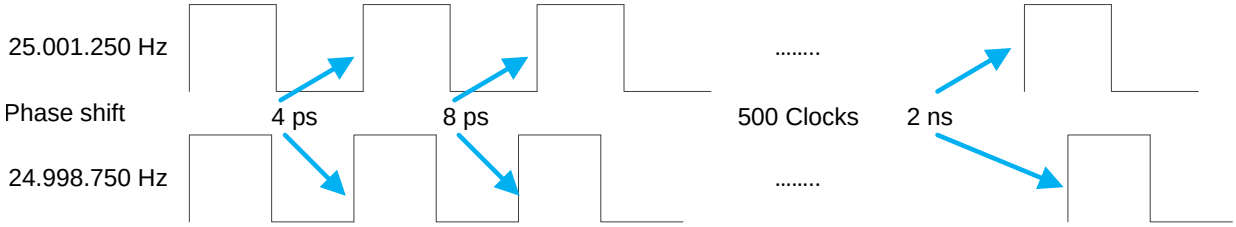


Figure 17. Crystal Phase Shift Diagram

This distribution means that, depending on how many clocks are seen on a signal package, the phase shift of the two clocks accumulates. Avoid this accumulation by adding a clocking distribution network. After this action, only the one clock cycle jitter requires consideration and the phase shift is no longer a concern.

The solution to this problem is to replace XTALs of the PHY and Sitara chips with a CDCE913 programmable 1-PLL VCXO clock synthesizer, with three outputs. If more than three clocks are required, the CDCE9xx device family is available with various output and maximum output clock frequency.

This solution yields several advantages in general:

- High accurate clocking with minimum frequency and phase shift
- Smaller component area used for clocking
- Potentially lower cost
- Possibility to extend easily

Figure 18 shows how a CDCE913 could be connected and used to provide three reference LVCMOS clocks.

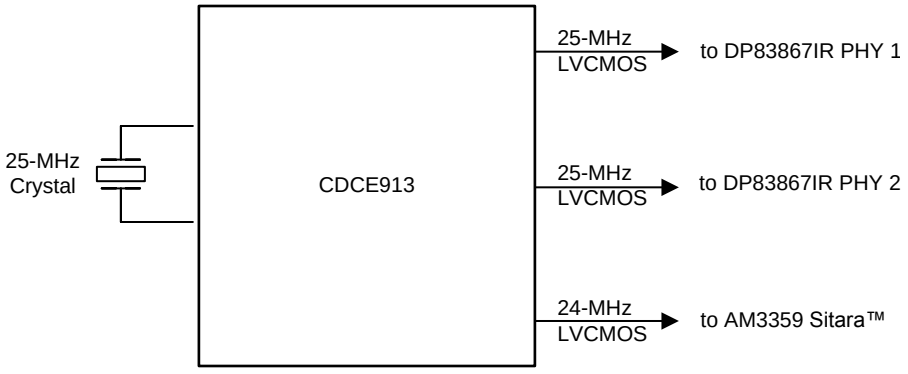
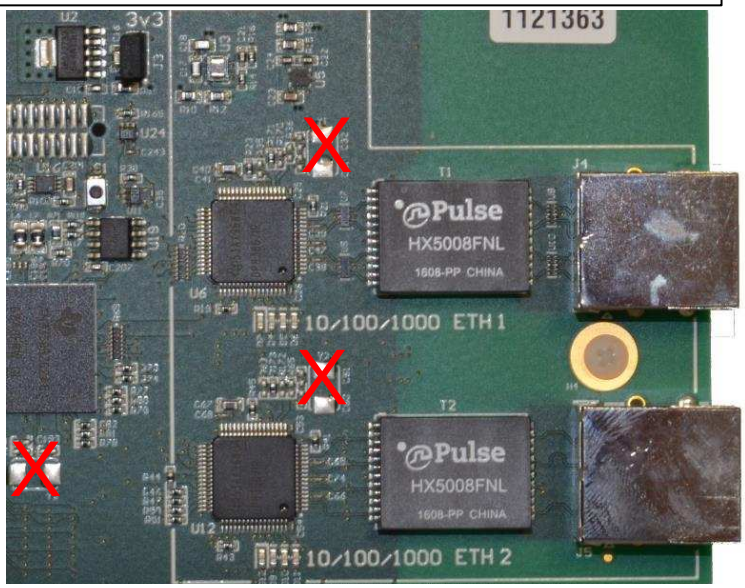


Figure 18. CDCE913 Clock Distribution Circuit Example

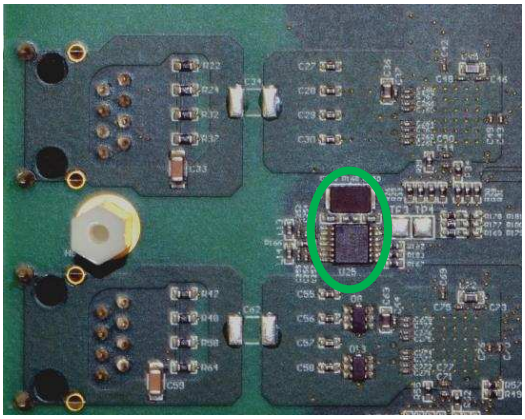
This new clocking source could be used to change the component floor plan as shown in Figure 19 with an Altium 3-D PCB simulation.

Step 1: Remove the oscillator circuitry used for the two DP83867 PHYs and the AM3359 Sitara as shown in the picture.

Step 2: Place CDCE913 and its supporting components on bottom side, between the PHYs and close to AM3359. This allows short routing distances.



PCB top view



PCB bottom view (flipped)

Figure 19. PCB Component Area Saving With CDCE913 Clock Generator

When using the CDCE913 part, programming the EEPROM of the part before soldering it may be an easier solution. TI provides the CDCEL9XXPROGEVM tool for this reason. This tool can be used to program the part defining its input clock and the output clocks desired as shown in Figure 20.

Use the following software to program using the EVM: http://www.ti.com/tool/clockpro.

Using this tool, the following setting was chosen for the CDCE913 for this design (see Figure 20).

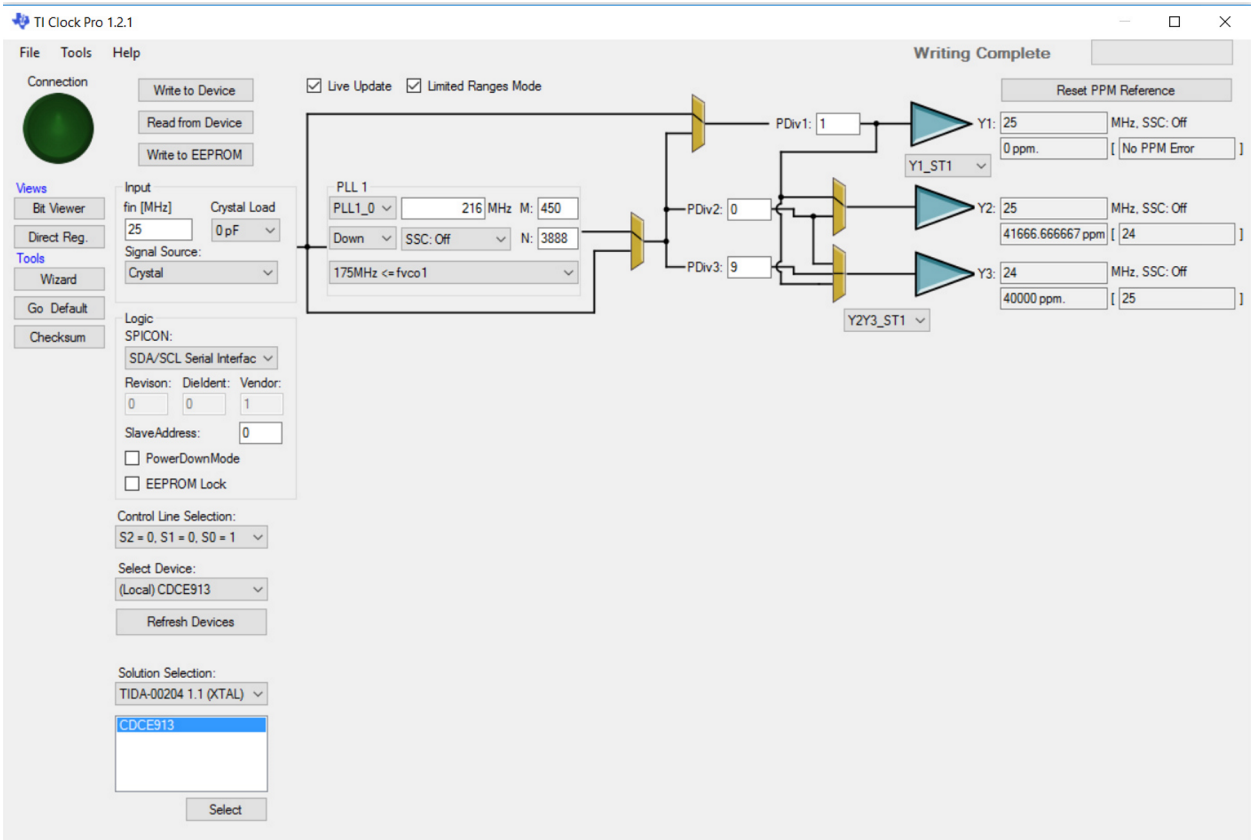


Figure 20. Settings Used to Program CDCE913 Device on TIDA-00204 Reference Design

The diagrams also shows that the load crystals can be removed and replaced by an internal crystal.

3 Software Design

3.1 Sitara AM3359 Firmware

The goal of the software design was to provide an example application firmware for evaluating Gigabit Ethernet, which boots from micro SD-Card automatically after the TIDA-00204 is powered. The application firmware implements a driver for the DP83867IR, UDP and TCP/IP stack, and HTTP web server examples. A USB virtual COM port offers optional user access to read or write to DP83867IR registers for custom configurations like RGMII Delay Mode, if required.

3.1.1 Functional Overview

The host processor Sitara AM3359 is configured to boot from MMC1/SD-Card. The AM3359 copies the TIDA-00204 example application binary file app from the SD-Card to DDR3 RAM and launches the example application. The flowchart of the SD-Card boot load process is shown in Figure 21.

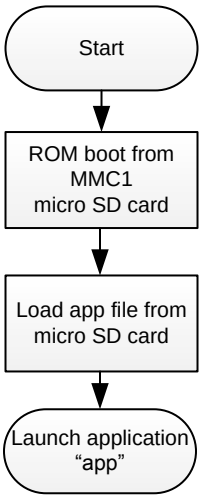


Figure 21. AM3359 Boot Load Process From MMC1 Micro SD-Card

The TIDA-00204 example application app consists of three major functional blocks.

The first part initializes the AM3359 peripherals like the Ethernet MAC, Ethernet Switch (CPWS), and UART. Then, the app initializes SYS/BIOS and sets up a UART task thread as well as an Ethernet task thread. After that, the app starts SYS/BIOS. Then, both the UART thread and the Ethernet thread are scheduled and run accordingly.

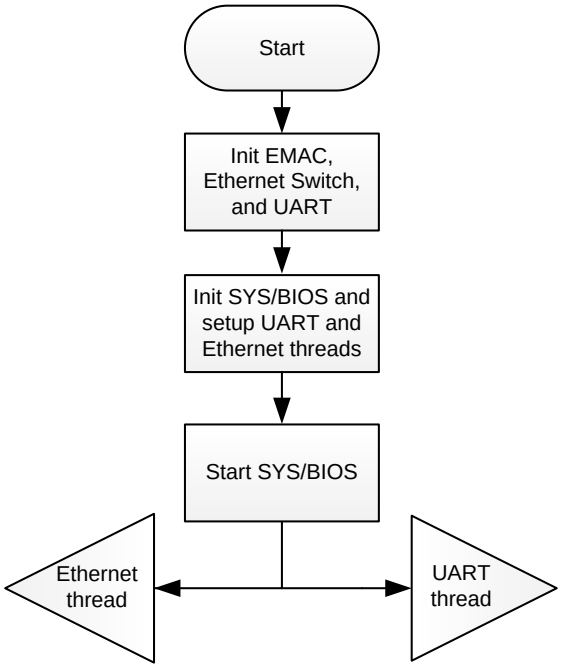


Figure 22. AM3359 Initialization

The Ethernet thread initializes the configuration registers of both DP83867IR Gigabit PHYs through SMI. For example, set RGMII mode, autonegotiation, indicator LEDs, and more. Then the thread enables the network layer with fixed IPv4 address 192.168.1.10 and TCP and UDP transport layer. Additionally, a HTTP web server example application is included.

The UART thread enables communication through virtual COM port and offers and additional option to read and write to the individual registers of the DP83867 Gigabit PHYs through SMI. For example, the user can adjust the RGMII Delay Mode according to the specific hardware, if desired.

The flowcharts of both threads are shown in Figure 23 and Figure 24.

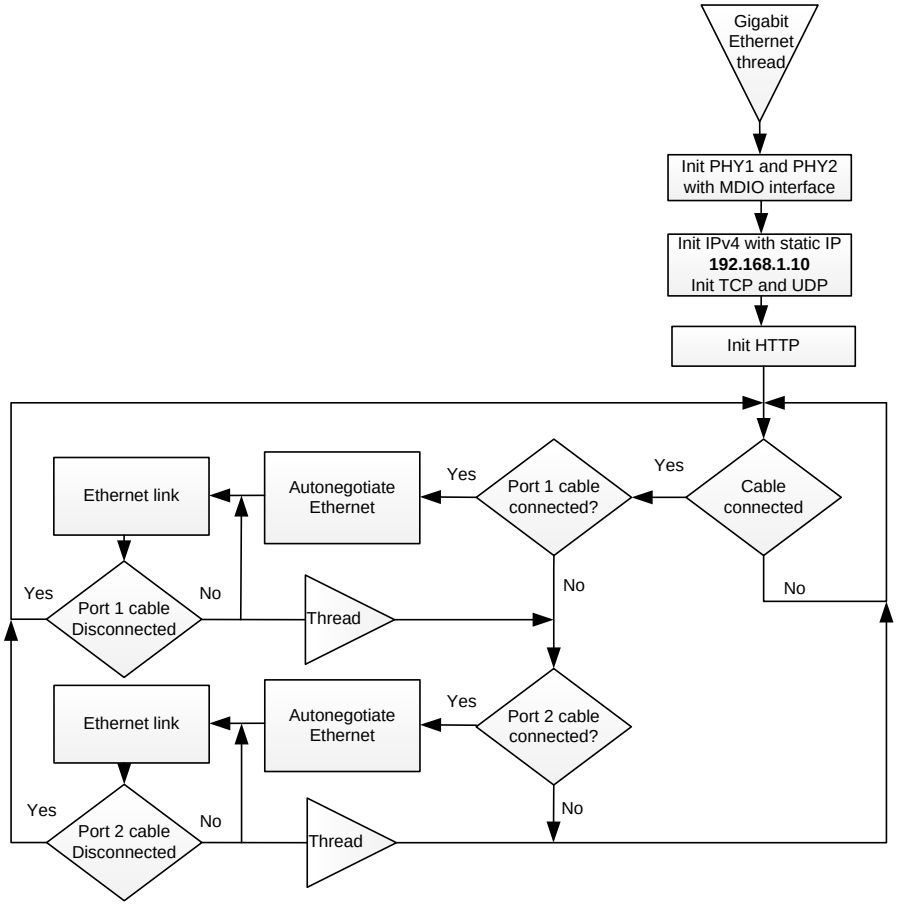


Figure 23. AM3359 Gigabit Ethernet Thread Flowchart

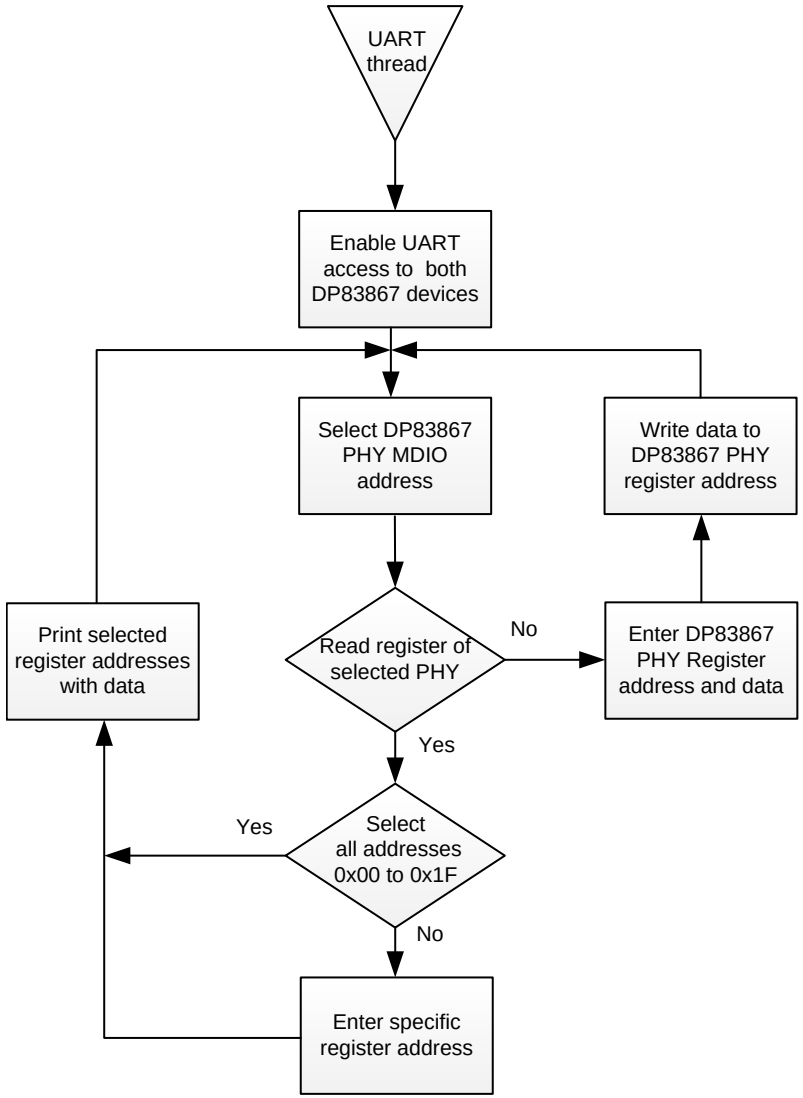


Figure 24. AM3359 UART Thread Flowchart

3.1.2 Software Components

The "TIDA-00204 SD-Card Image" consists of two binary files. The AM3359 boot loader binary file called "MLO" and the example application binary file called "app", as described in Section 3.1.1. Both binaries were compiled in separate CCS 6 projects.

3.1.2.1 "MLO" Binary File

The TIDA-00204 boot loader binary file "MLO" was developed with the Texas Instruments AM335x_SYSBIOS_Industrial_SDK_01_01_00_06 software package. This example project was modified to the TIDA-00204 hardware with boot from MMC1/SD-Card. The binary file was renamed after compilation to MLO to fit the AM3359 ROM boot loader and is part of the TIDA-00204_Firmware_AM3359_SD-Card_Image.

3.1.2.2 "app" Binary File

The TIDA-00204 example application binary file app was developed with the following Texas Instruments software packages:

- AM335x_SYSBIOS_Industrial_SDK 01_01_00_06: http://downloads.ti.com/sitara_indus/esd/AM335x_SYSBIOS_Industrial_SDK/latest/index_FDS.html
- SYS/BIOS 6_40_03_39: http://software-dl.ti.com/dsps/dsps_public_sw/sdo_sb/targetcontent/bios/sysbios/6_40_03_39/exports/bios_setupwin32_6_40_03_39.exe
- XDCtools 3_30_05_60: http://software-dl.ti.com/dsps/dsps_public_sw/sdo_sb/targetcontent/rtsc/3_30_05_60/index_FDS.html
- NDK 2_24_00_11: http://software-dl.ti.com/dsps/dsps_public_sw/sdo_sb/targetcontent/ndk/2_24_00_11/index_FDS.html
- NSP 1_10_02_09 Product Download Page: http://software-dl.ti.com/dsps/dsps_public_sw/sdo_sb/targetcontent/ndk/nsp_1_10_02_09/index_FDS.html

The example application uses only a few example projects including the source and header files.

3.1.3 Creating the Micro SD-Card Image

To create the TIDA-00204_Firmware_AM3359_SD-Card_Image to boot the demo application firmware from the micro SD-Card, the following equipment is required:

- A pre-formatted micro SD-Card with FAT file system
- A PC with a micro SD-Card reader
- Win32 Disk Imager installed on PC

Copy the MLO and app binary file to the micro SD-Card. After that, invoke the Win32 Disk Imager. See an example of the program shown in Figure 25.

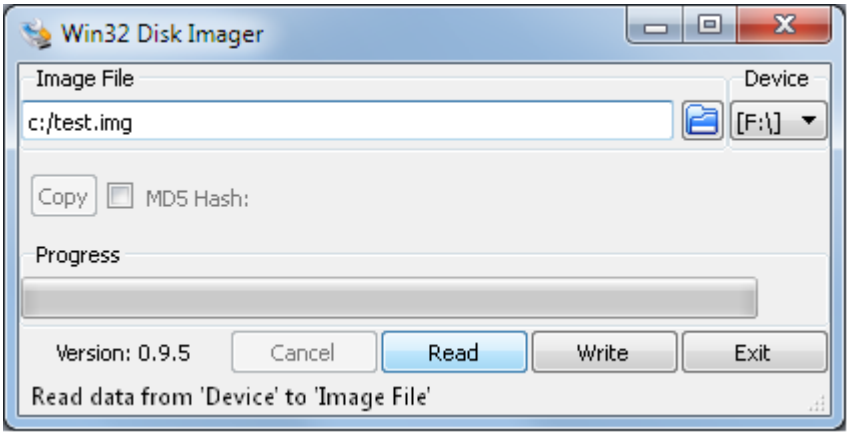


Figure 25. Procedure to Create SD-Card Image With Win32 Disk Imager

Select *Read* to write the current inserted micro SD-Card into the name image in this example called "test.img". This image was renamed to TIDA-00204_SD-Card_Image_rev1_0 and then included into the TIDA-00204 software package.

3.2 PC Test Software for UDP Packet Transfer Based on TI's NDK

The tests for the Gigabit Ethernet communication path developed with the Texas Instruments NDK 2_24_00_11 software package. From this software package, the following source file was used:

- c:\ti\ndk_2_24_00_11\packages\ti\ndk\winapps\testudp.c

For more information on the testudp files, see Section 2.2.3.3 of the NDK document[8].

With original executable testudp.exe, the utilization was around 1%, which was below the needs for this design; therefore, modification was done. The original source was modified adding hyper threading to enable higher utilization. To compile the source file, MinGW was used.

NOTE: To use the hyper threading on a Windows PC, add libwinpthread-1.dll in the same directory as the executable. The library file libwinpthread-1.dll can be downloaded from the internet.

With hyper threading, 25% utilization was achieved on a single Gigabit Ethernet port and 20% each in case of on dual Gigabit Ethernet port 1 and port 2.

Two variants were generated as explained in the following two sections.

3.2.1 UDP Throughput Test

The example UDP test file is called "TIDA-00204_UDP_throughput_test.exe". The software flow of the throughput example code can be seen in Figure 26.

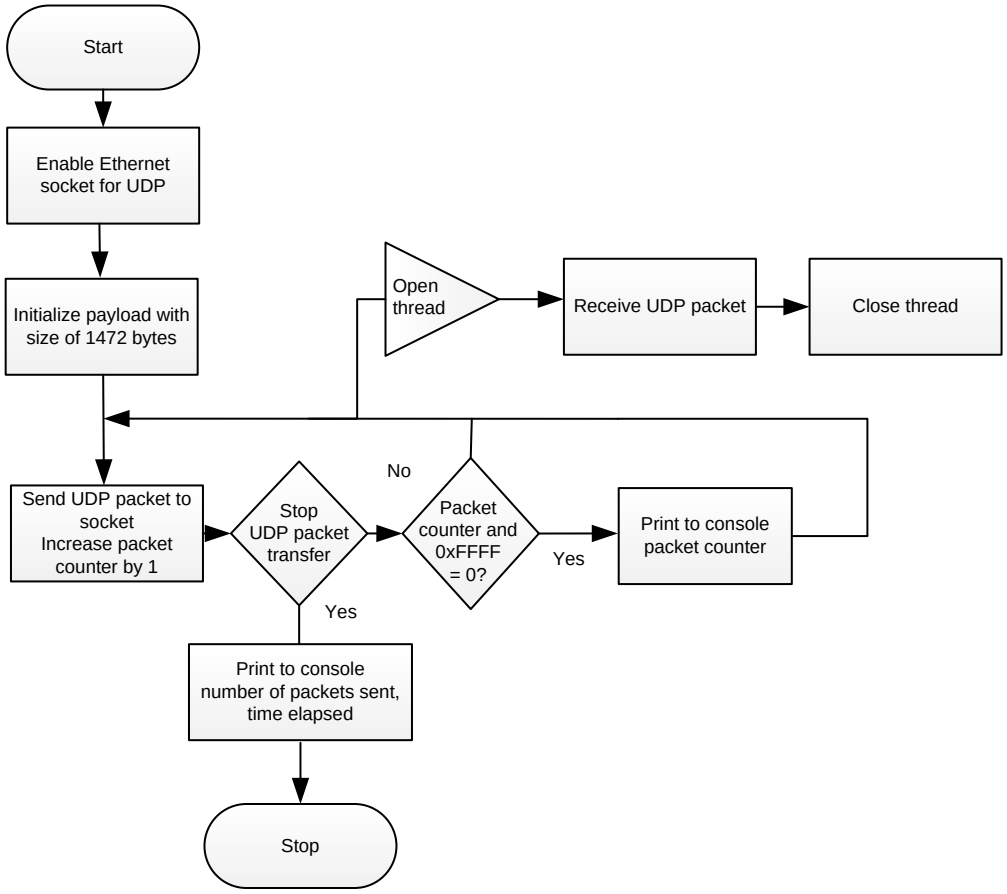


Figure 26. Flowchart of UDP Throughput Test Software

Figure 27 is an example console output can be seen of the example UDP throughput test software.

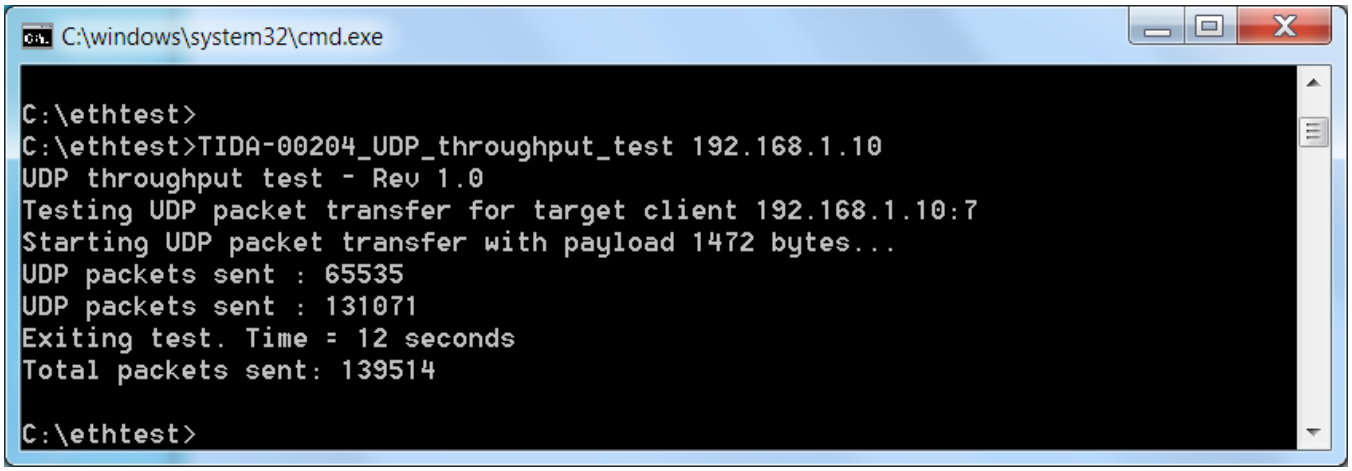


Figure 27. Command Prompt UDP Throughput Print

3.2.2 UDP Packet Error Test

The example UDP test file is called "TIDA-00204_UDP_throughput_test.exe". Figure 28 shows the software flow of the throughput example code can be seen.

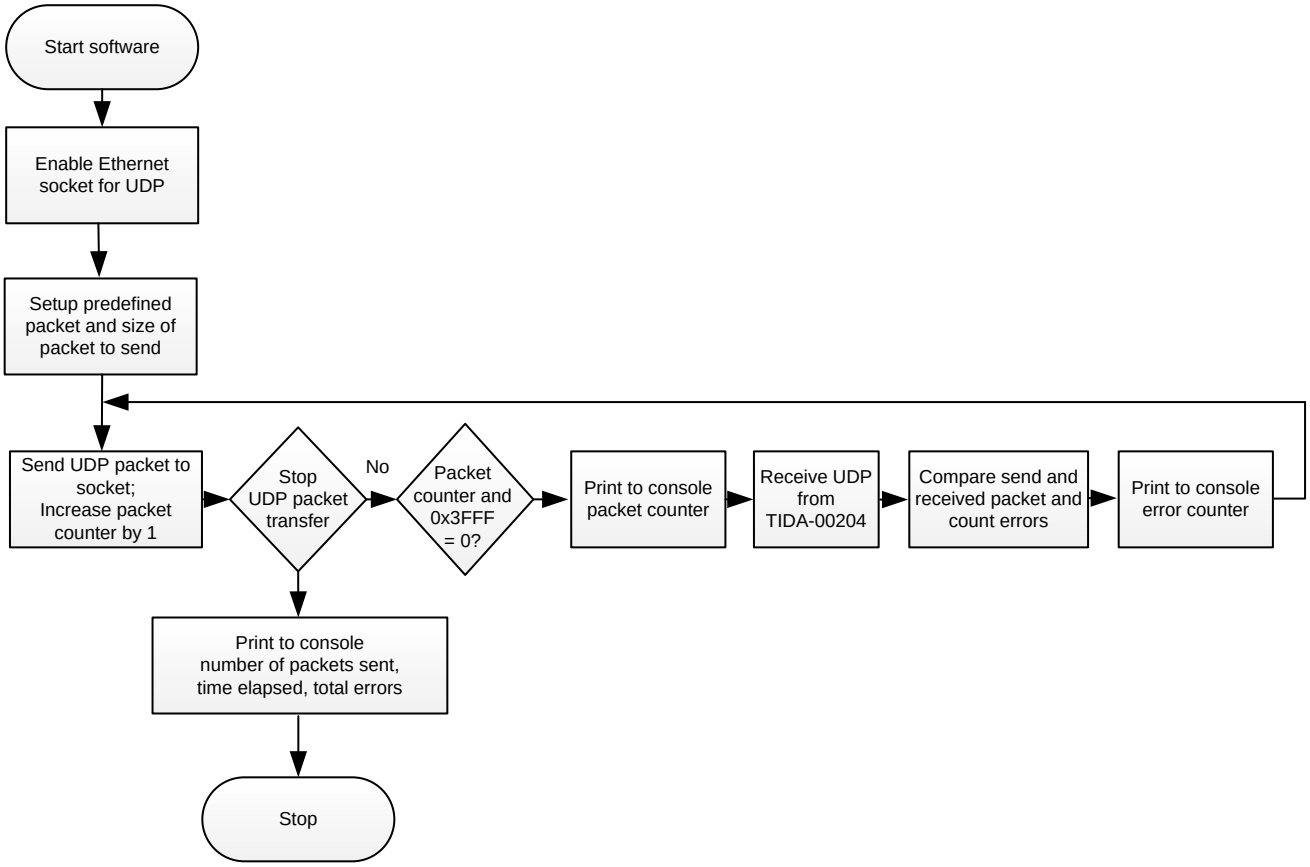


Figure 28. Flowchart of UDP Packet Error Test Software

The above example verifies, if the echoed back packets were corrupted. This functionality is needed check the signal integrity of the connection. Note that with this functionality enabled on the PC, the utilization of the Gigabit Ethernet connection was 5%.

An example console output of the example UDP packet error test can be seen in Figure 29.

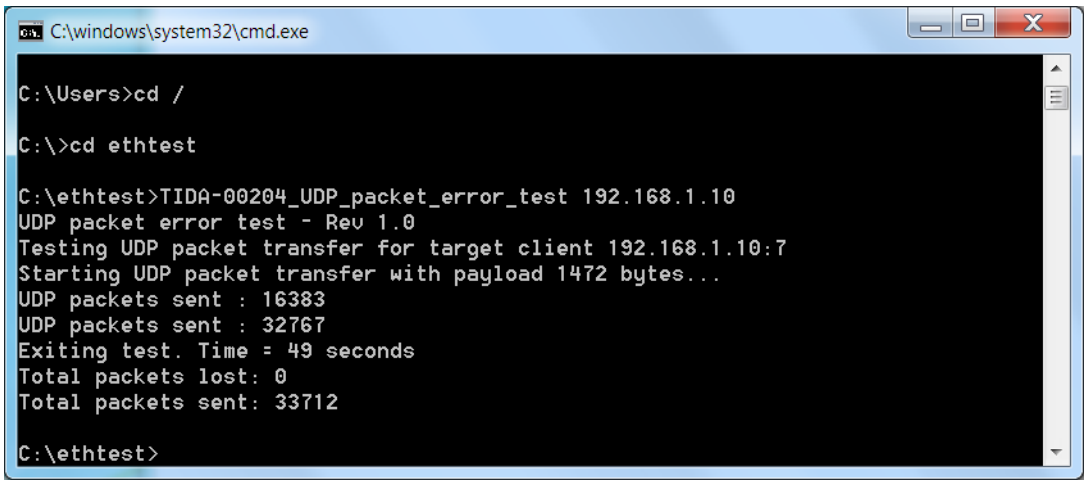


Figure 29. Command Prompt UDP Packet Error Test Print

4 Getting Started

4.1 PCB Overview

A picture of the PCB with key functional blocks is shown in Figure 30.

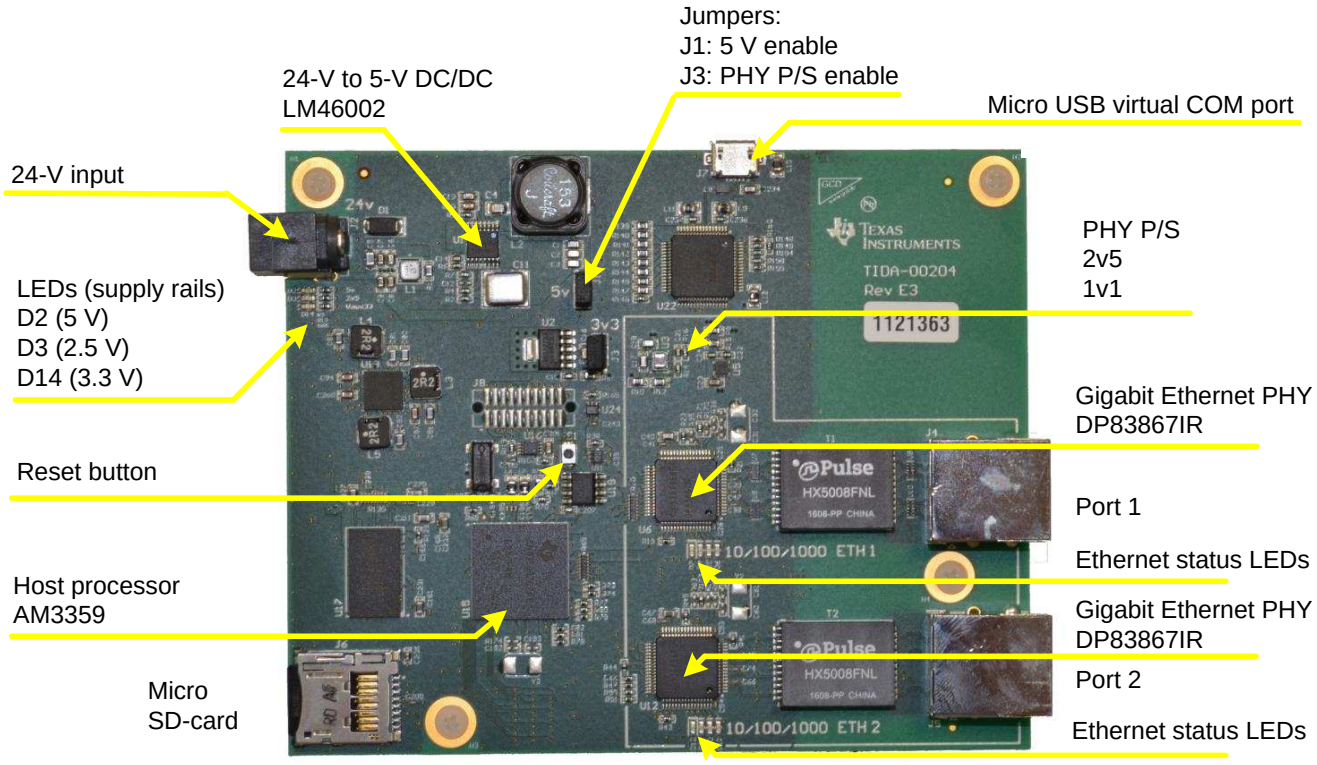


Figure 30. TIDA-00204 Top-Side PCB Photo With Key Functional Blocks

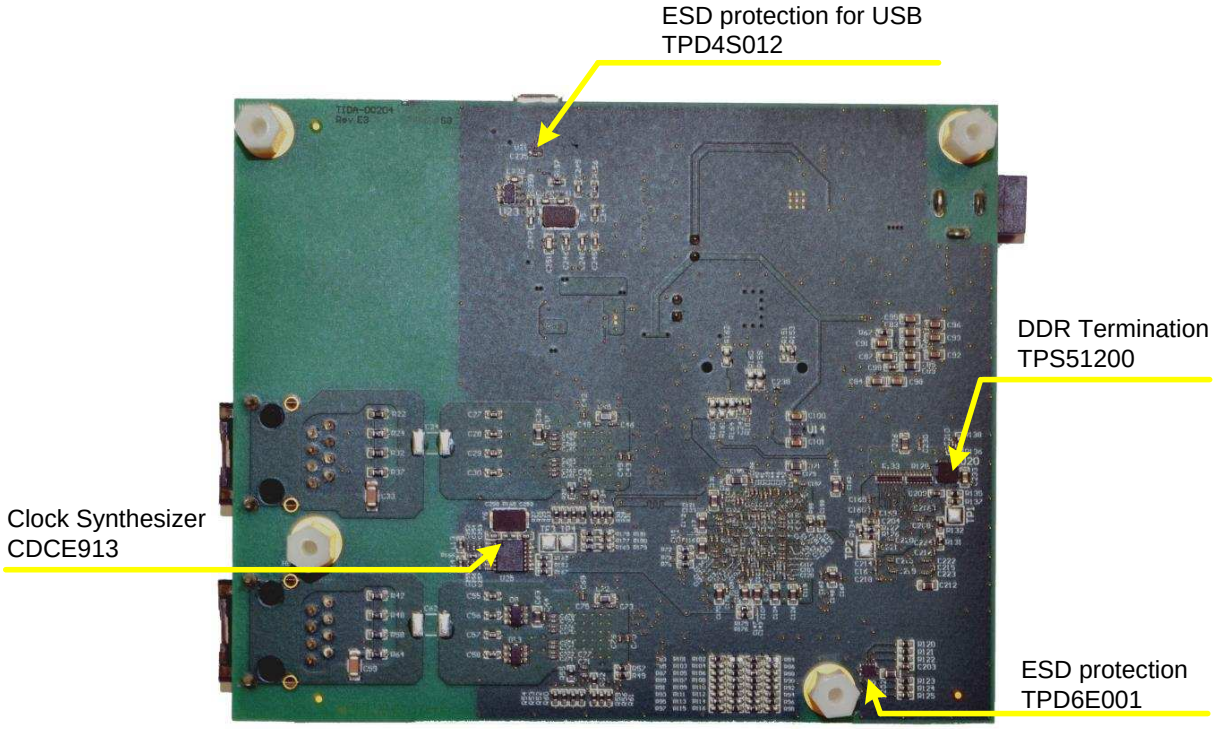


Figure 31. TIDA-00204 Bottom-Side PCB Photo With Key Functional Blocks

4.2 How to Run the Board

The next sections show the prerequisites and the steps to quickly start using the board.

4.2.1 Prerequisites

The following hardware equipment and software is required.

Table 18. Prerequisites

HARDWARE EQUIPMENT OR SOFTWARE	REQUIREMENTS
24-V power supply	24-V output power brick with at least a 250-mA output current Output connector 2.1-mm I.D. × 5.5-mm O.D. × 9.5-mm Female
PC	PC or Laptop with USB port and Gigabit Ethernet port
Ethernet cable	Recommended CAT7 twisted pair cable
Micro USB cable	N/A
Micro SD-card	Big enough to fit the micro SD-card TIDA-00204 image
TeraTerm v4.76 or newer	Download from web, or use any other terminal program of your choice
Win32 Disk Imager v0.9.5 or newer	Download from web
XDS100 v2 PC USB driver	To get this driver, install CCS 6.x
TIDA-00204 software package	Download from the TIDA-00204 web page
libwinpthread-1.dll	Download from web

4.2.2 Jumper Settings

CAUTION

The following two jumpers need to be set: J1 and J3.

The J1 jumper powers the host processor power stage and the J3 jumper enables the Gigabit Ethernet PHY power supply.

4.2.3 Prepare the Micro SD-Card

For easy standalone board operation, a micro SD-Card image is provided. The example image on the SD-Card is configured so the AM3359 reads the boot loader MLO from the micro SD-Card and enables the Sitara AM3359 in a mode. The Sitara AM3359 enables the needed peripherals to communicate with the two PHYs over the MDI and sets those PHYs in autonegotiate 10/100/1000 mode. It also enables a UART functionality where one can read out the PHY registers from the two DP83867 devices over virtual COM port.

Write the image "TIDA-00204_SD-Card_Image_rev1_0.img" to a micro SD-Card. Use Win32 Disk Imager to write the image to the SD-Card (see Figure 32).

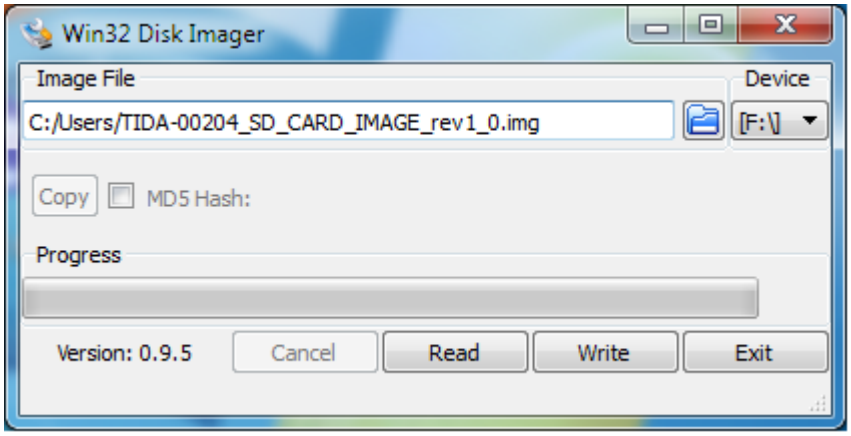


Figure 32. Win32 Disk Imager Image Showing the Write Function

Select the provided TIDA-00204 firmware image and click *Write* to flash the image to the micro SD-Card.

CAUTION

Ensure that the micro SD-Card is selected at the *Device* tab.

If the image is not being written with the onboard PC SD-Card slot, try using an external SD-Card reader.

CAUTION

If the micro SD-Card is not prepared like above, but the individual binary files MLO and app are copied to a preformatted micro SD-Card it might be that the AM3359 does not boot properly. For further details on this topic, see the Section 26.1.7.5.2 of the AM335x technical reference manual[6].

4.2.4 Powering the TIDA-00204 Reference Design

Insert the micro SD-Card with TIDA-00204 firmware image into the TIDA-00204 micro SD-Card cage.

Connect a 24-V power supply with at least a 250-mA output current. After that, the three green LEDs (D2, D3, and D14) will turn on. If the LEDs does not turn on, one of the jumpers J1 and J3 are not connected.

Connect the micro USB cable from the TIDA-00204 reference design to the PC. Now the XDS100 v2 PC USB driver is installed on the PC. If PC does not find this driver, install CCS 6 to get the driver.

Invoke a terminal program, like TeraTerm that can connect to the virtual COM port. Setup the terminal program in Serial Console Mode and set the parameters as seen in Table 19.

Table 19. Terminal Program Serial Console Configuration

BAUD RATE	DATA	PARITY	STOP	FLOW CONTROL
115200	8-bit	None	1-bit	None

Afterwards, press the reset button on the board. For the location of the reset button, see Figure 30.

Now on the terminal program, the boot sequence of the TIDA-00204 reference design is printed. See Figure 33 for terminal program printout.

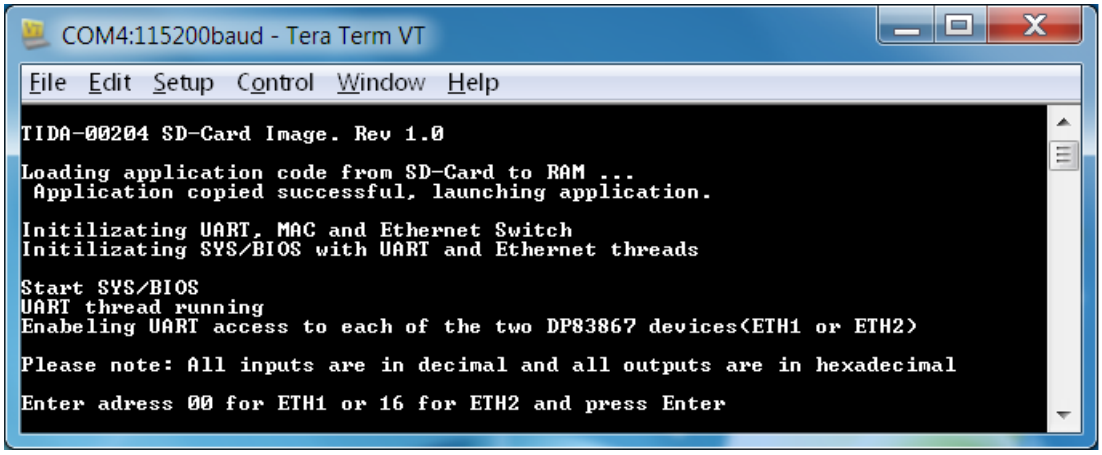


Figure 33. Virtual COM Port Connection During Boot

4.3 Evaluating the TIDA-00204 Dual-Port Gigabit Ethernet Reference Design

With the board powered up, the next step is to connect the Ethernet link partner.

Connect a link partner to either port 1 or port 2, depending on the link partner autonegotiate will setup 10/100/1000 network capability. Now the Ethernet LEDs will light up showing link status and Ethernet speed.

The status LEDs have the following functionality see Table 20.

Table 20. DP83867 Gigabit PHY Port 1 and Port 2 Status LED Configuration

LED #	D7 / D12	D4 / D9	D5 / D10	D6 / D11
Function	Not assigned to a specific function on TIDA-00204	Receive or transmit activity	1000-Mb link established	Link established

The status LEDs are explained from left to right when looking at the board picture.

The reference design is setup to use the IP address 192.168.1.10, that is a static IP. It does not have DHCP function enabled.

Setup the PC Network connection for static IP in the same address range as the TIDA-00204 reference design with subnet mask 255.255.255.0. For example: 192.168.1.30.

To test the Ethernet connection there are several options: ping, provided UDP test software and a HTTP web server. See examples below.

All Gigabit Ethernet examples demonstrated on both port 1 and port 2.

4.3.1 Ping

With the command prompt, the windows ping function can be used for initial connection test, see Figure 34.

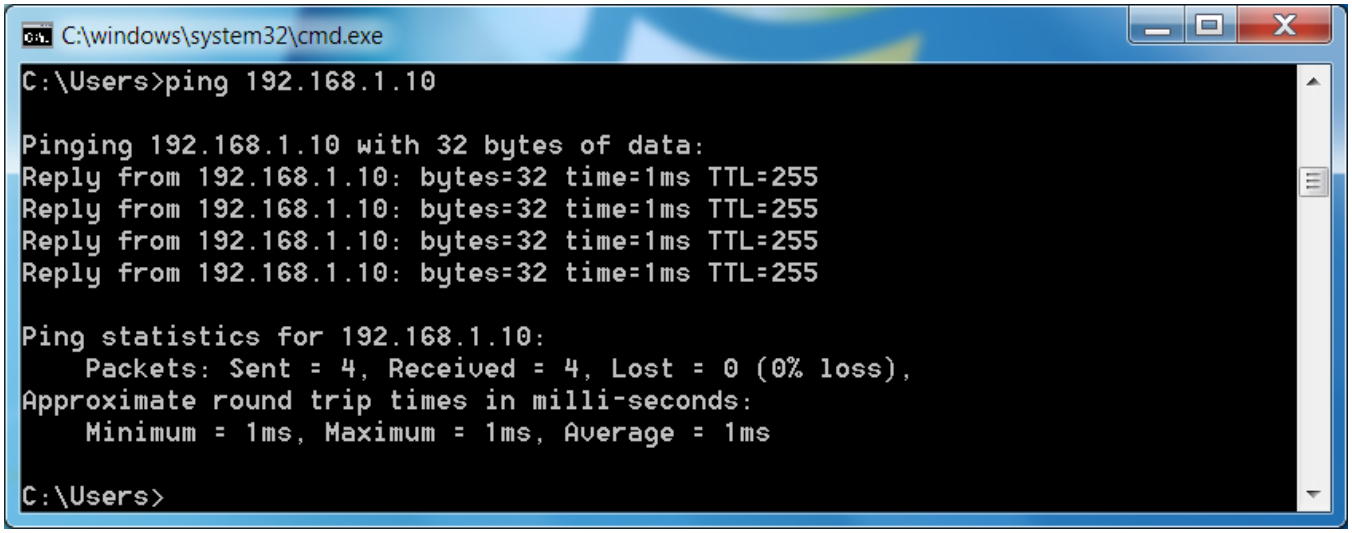


Figure 34. Command Prompt Ping Print

4.3.2 UDP Test Software

The two PC test programs as part of the TIDA-00204 software package can be used.

Insure that the libwinpthread-1.dll is located in the same folder as the TIDA-00204_throughput_test.exe and TIDA-00204_packet_test.exe. This library can be downloaded from the internet.

To invoke these programs, use a Windows PC with the command prompt, see Figure 35 and Figure 36 for example print outs.

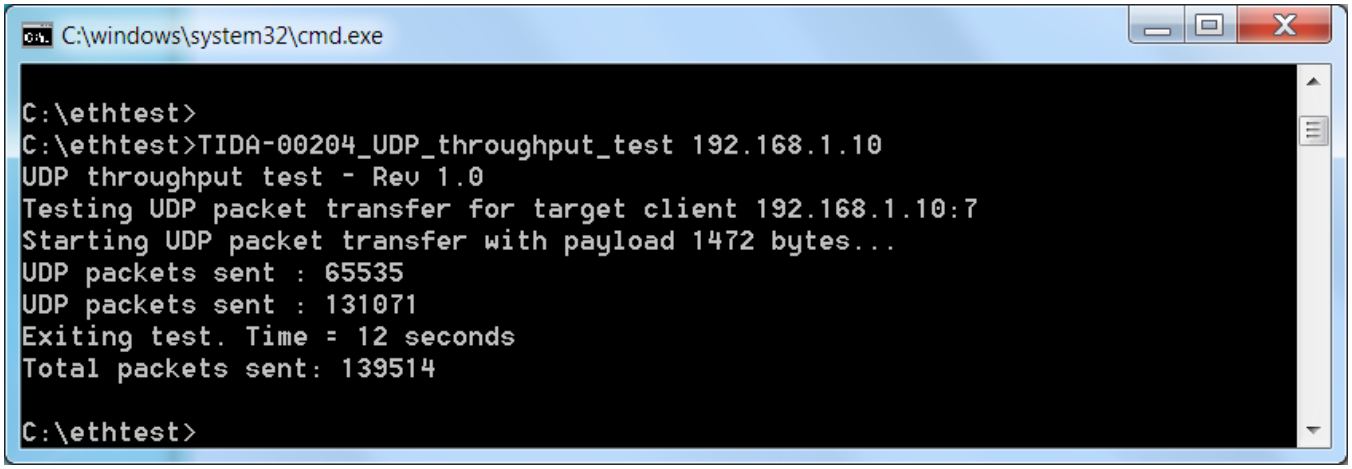


Figure 35. Command Prompt UDP Throughput Print

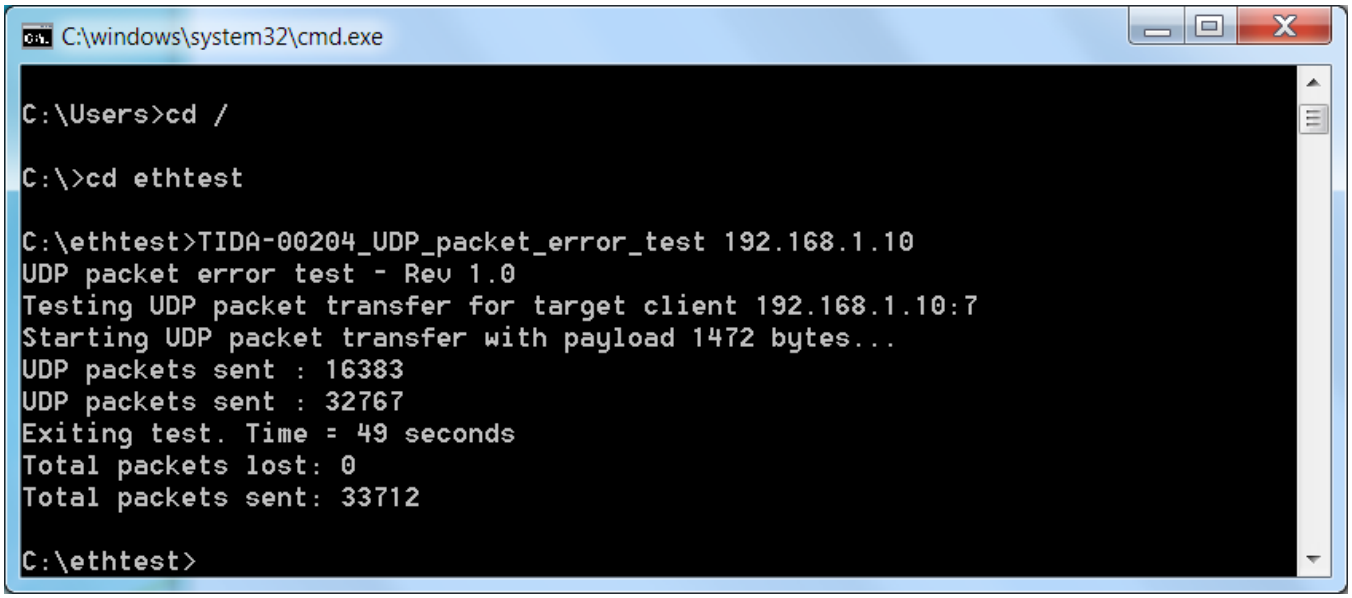


Figure 36. Command Prompt UDP Packet Error Test Print

4.3.3 HTTP Web Server Example

Open a browser and enter this address: http://192.168.1.10. See Figure 37 for a screenshot of the TIDA-00204 webpage.

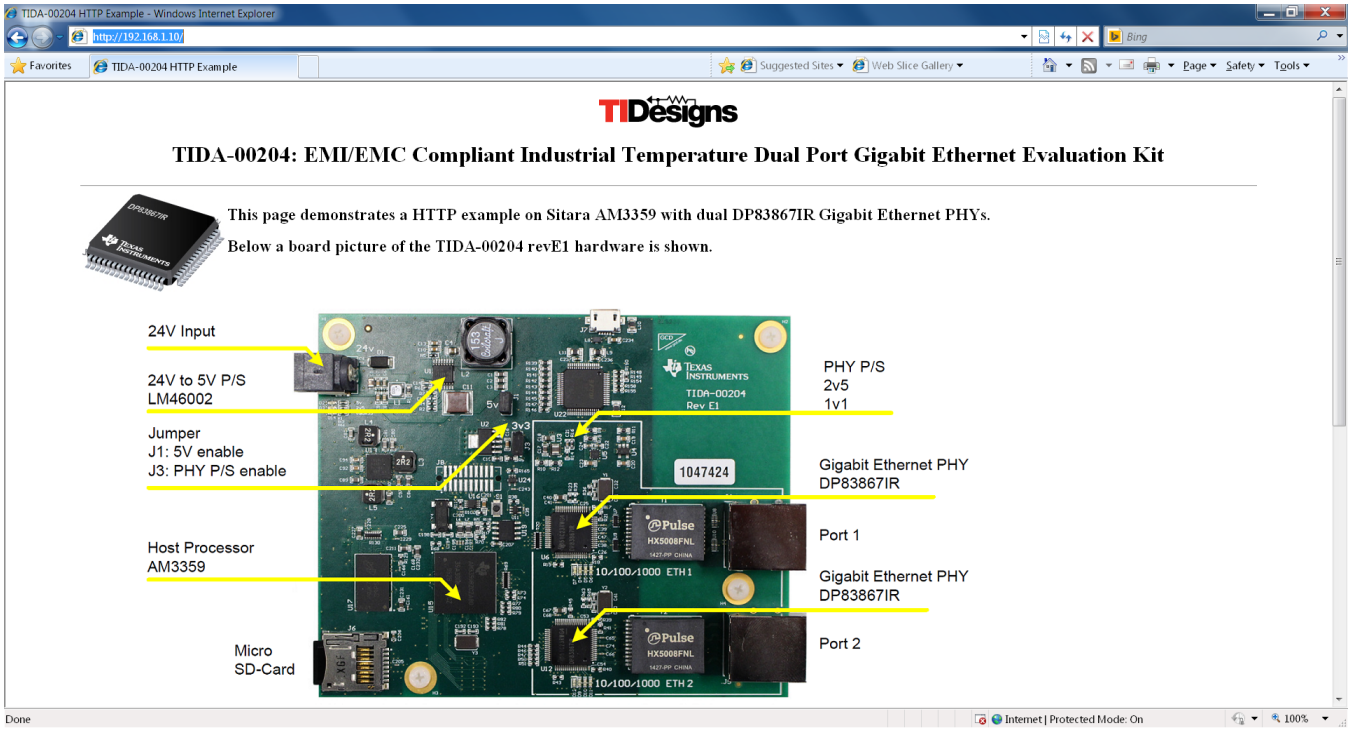


Figure 37. TIDA-00204 HTTP Web Server Example

4.3.4 Access to DP83867IR Registers Through USB Virtual COM Port

The virtual COM port connection can be used to read and write to both DP83867IR registers through SMI. With this, it is possible to configure the DP83867IR registers in a different configuration than default for additional test options.

CAUTION

All inputs are in decimal and all outputs are in hexadecimal.

Figure 38 shows an example screenshot for a register read from DP83867IR on Ethernet port 2.

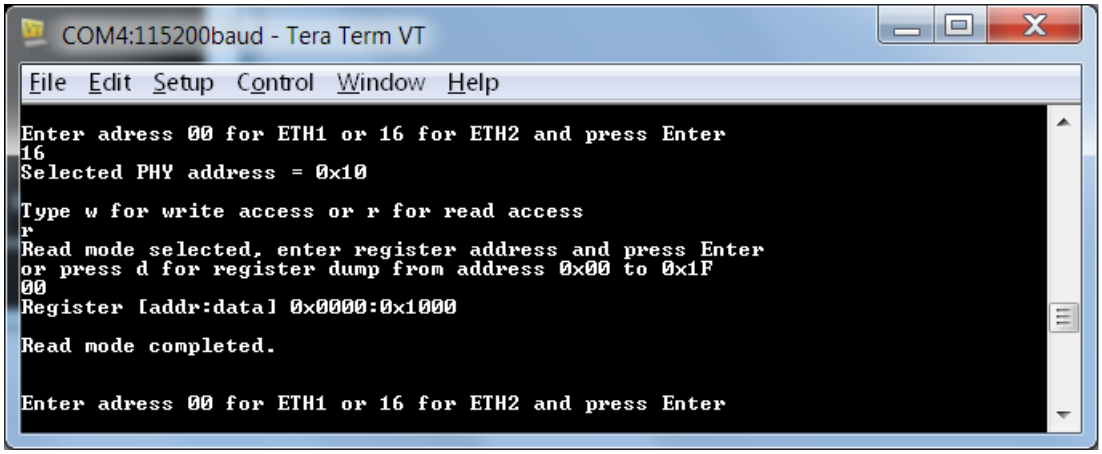


Figure 38. Virtual COM Port Connection for DP83867IR (ETH1) Register Read

To find the Gigabit Ethernet PHY DP83867IR register addresses, see the DP83867IR data sheet[1].

5 Test Results

For the TIDA-00204 tests, the following test equipment was used:

Table 21. Test Equipment for the TIDA-00204 Gigabit Ethernet Signal Integrity Tests

TEST EQUIPMENT	PART #
24-V power brick	V-Infinity 3A-621DN24
Power supply	Knürr-Heinzinger Polaris 125-5
Gigabit Ethernet adapter for PC	Digitus – USB 3.0 Ethernet adapter
PC	Latitude E6540 with Windows 7 64-bit
Ethernet cable	DRAKA UC900 super screen 27 CAT7 with a CAT6A connector
Oscilloscope	Tektronix TDS794D, P6339A probes Tektronix TDS2024B, P2220 probes
Electronic load	Chroma 63103 with Chroma 6314
Multimeter	FLUKE 179

5.1 Gigabit Ethernet Signal Integrity Tests

5.1.1 RGMII Signals

The RGMII signals between the MAC and the PHY are tested with a 1000-Mb connection on both PHY1 and PHY 2 RX and TX. Figure 39 through Figure 42 show the clock signal and corresponding RX_D1 and TX_D1 data signal. The other data signals D0, D2, and D3 were measured too and exhibited the same waveforms. This was expected because the design was optimized for impedance and matched length of the clock and data lines.

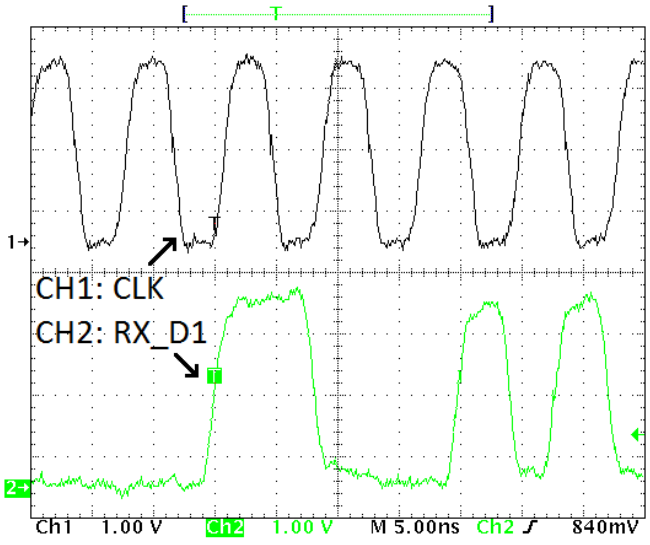


Figure 39. ETH1 RGMII RX Clock and Data Signal During Gigabit Ethernet Connection

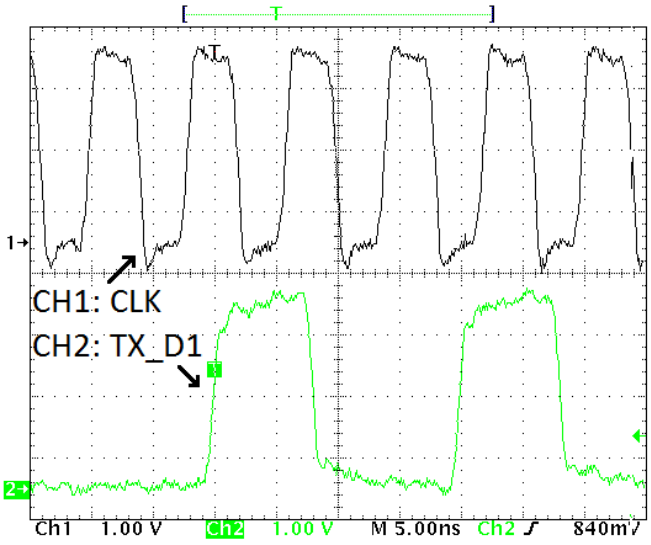


Figure 40. ETH1 RGMII TX Clock and Data During Gigabit Ethernet Connection

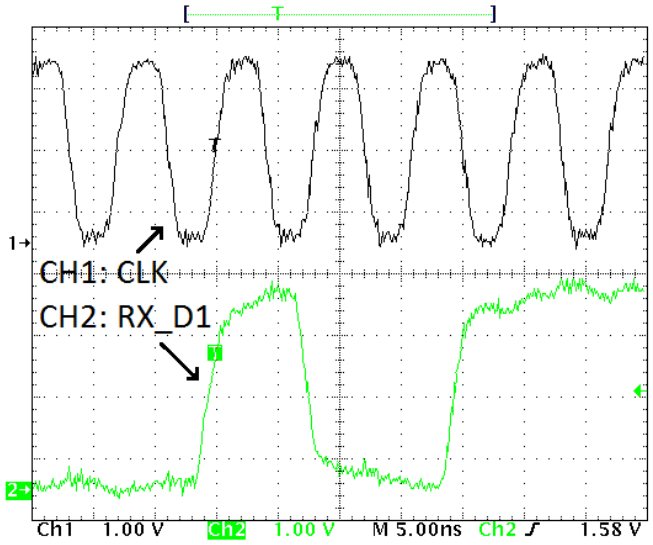


Figure 41. ETH2 RGMII RX Clock and Data Signal During Gigabit Ethernet Connection

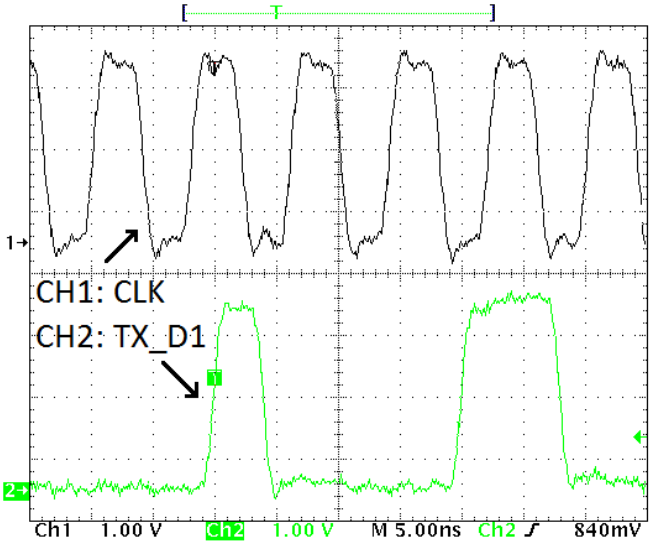


Figure 42. ETH2 RGMII TX Clock and Data Signal During Gigabit Ethernet Connection

5.1.2 Serial Management Interface (SMI)

The maximum clock frequency of the SMI of the Sitara AM3359 is 2.5 MHz. This test does not need to have an Ethernet connection running. Figure 43 and Figure 44 show the two signals MDC (Clock) and MDIO (I/O) between the Sitara AM3359 and the two DP83867IR for Gigabit Ethernet ETH1 and ETH2.

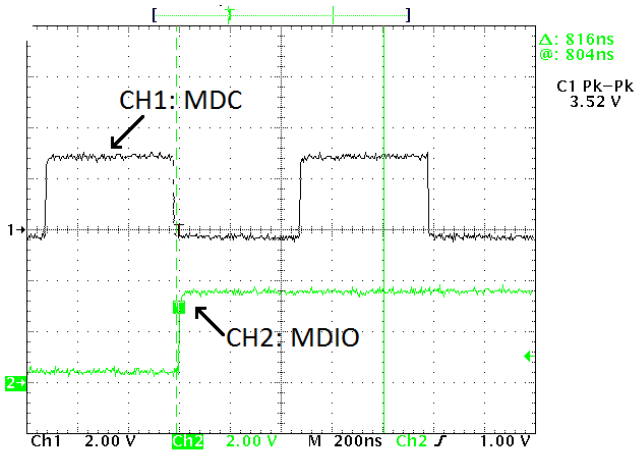


Figure 43. SMI Clock and Data Signal at 2.5 MHz at DP83867IR ETH1

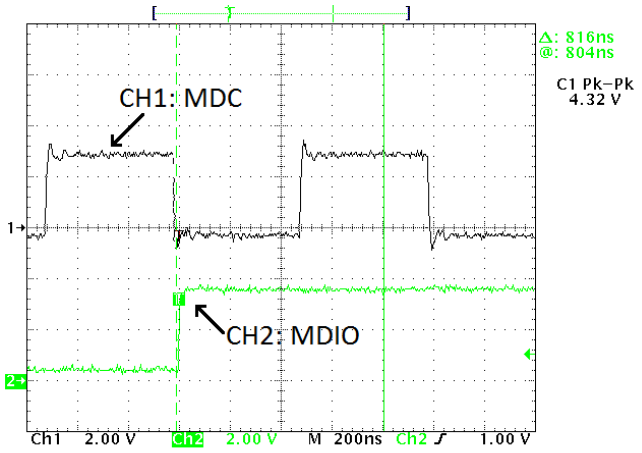


Figure 44. SMI Clock and Data Signal at 2.5 MHz at DP83867IR ETH2

5.2 Power Supply Tests

5.2.1 24-V to 5-V DC/DC Power Supply

The LM46002 was configured in this design to work with an input voltage range between 17 and 60 V.

The nominal load current was defined for the following configuration. The Sitara AM3359 running at 600 MHz executing the application code from DDR3, with both DP83867IR connected in Gigabit Ethernet mode with continuous UDP packet transfer at 20% network utilization on both ports. The minimum load current is set to 500 mA, the nominal load to 850 mA, and the maximum load to 1.2 A.

Three tests where done: Output voltage versus input voltage (Figure 45), output voltage versus load current (Figure 46), and the output voltage ripple (Figure 47).

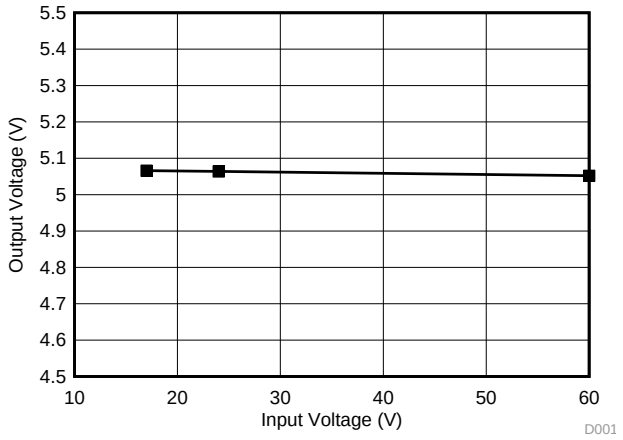


Figure 45. Output Voltage (V_{OUT}) at 850 mA Nominal Load Current With Varying Input Voltage (V_{IN})

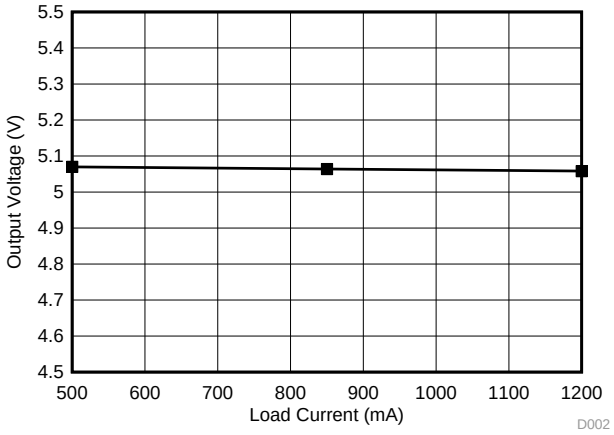


Figure 46. Load Regulation: V_{OUT} at 24-V Input Voltage at Varying Loads

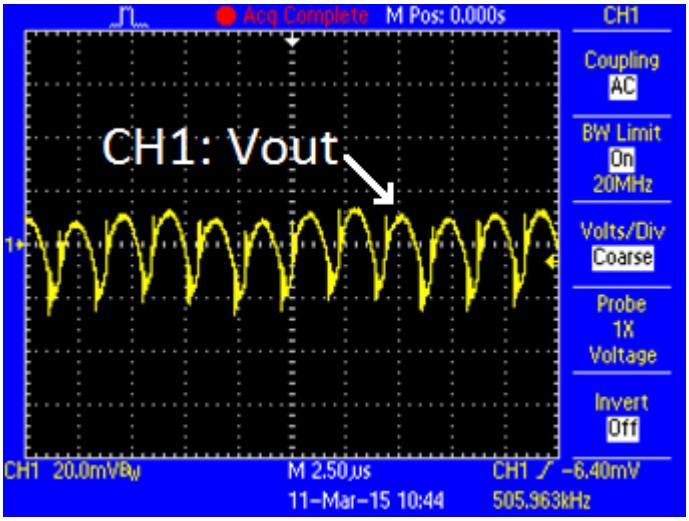


Figure 47. V_{OUT} Output Voltage Ripple at 850 mA Load Current and 24-V V_{IN} Input Voltage

5.2.2 Power Supply for the DP83867IR Gigabit Ethernet PHYs Tests

The voltages have been verified as shown in Table 22. The startup of the 3v3, 2v5, and 1v1 rails are shown in Figure 48.

Table 22. Measured Voltage Rails of the Gigabit Ethernet PHY

SUPPLY NAME PER SCHEMATICS	SPECIFIED VOLTAGE	MEASURED
3v3	3.3 V	3.31 V
2v5	2.5 V	2.47 V
1v1	1.1 V	1.10 V

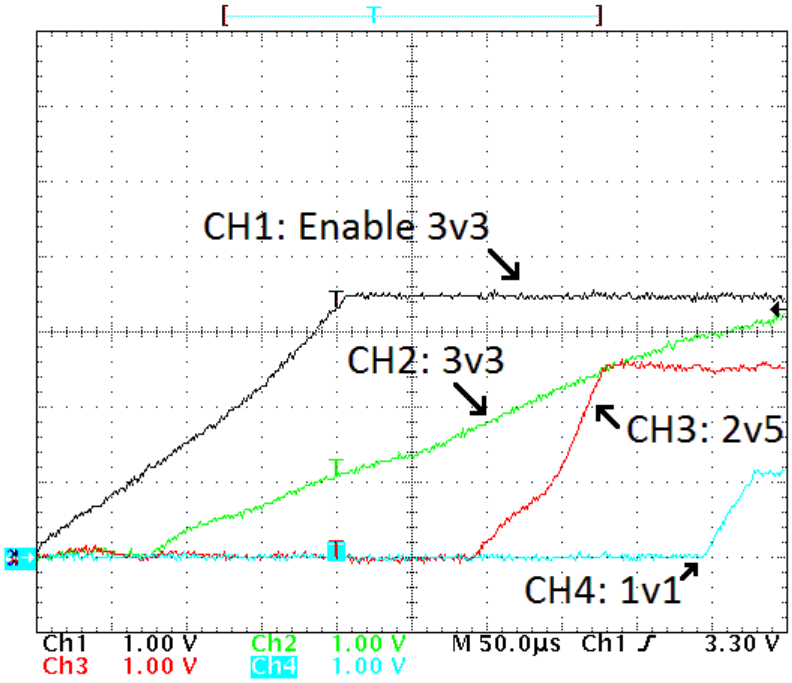


Figure 48. PHY Power Supply Voltage Rails During Startup

5.2.3 PMIC for Sitara AM3359 Host Processor

The TPS65910A3 output voltages were verified and compared against the expected voltages based on the TPS65910A3 EEPROM pin configuration.

Table 23. Measured Voltages on the PMIC TPS65910A3

SIGNAL	EXPECTED VOLTAGE	MEASURED VOLTAGE
VIO	1.5 V	1.52 V
VDD1	1.1 V	1.11 V
VDD2	1.1 V	1.11 V
VDD3	OFF	N/A
VDIG1	1.8 V	NC. VDIG1 pin was not connected in this design.
VDIG2	1.8 V	1.81 V
VPLL	1.8 V	1.82 V
VDAC	1.8 V	1.80 V
VAUX1	1.8 V	1.82 V
VAUX2	3.3 V	3.31 V
VAUX33	3.3 V	3.33 V
VMMC	3.3 V	3.32 V
VRTC	OFF	N/A

The sequencing has not been tested. Please see *TPS65910Ax User's Guide For AM335x Processors* for further details[7].

5.3 Gigabit Ethernet Functional Tests

The following functions have been tested: autonegotiate, ping, UDP transfer, and web server.

Table 24. Functional Tests of TIDA-00204 Reference Design

FUNCTION	TEST RESULT
Autonegotiate	PASS
Ping	PASS
UDP	PASS
Web server	PASS

5.3.1 Autonegotiate

Testing the autonegotiate is done using a network connection which can be programmed into a specific autonegotiate condition. Doing this ensures that the link negotiated is not going into a default setting defined in the IEEE 802.3ab standard. This can happen if one partner of the link is forced and the other is set to autonegotiate.

The default autonegotiate setting of the DP83867IR is set 10/100/1000-Mb half- or full-duplex mode. The DP83867IR recognizes the data rate supported by partner and sets the highest data rate supported by both.

Table 25 shows the different autonegotiate mode results.

Table 25. DP83867IR Autonegotiate Mode Test Results

DP83867IR SETTING	LINK PARTNER SPEED MODE SETTING	LINK PARTNER DUPLEX MODE SETTING	LINK CONNECTION ESTABLISHED
Autonegotiate: 10/100/1000 full duplex or half duplex	10/100/1000	Full duplex	1000 full duplex
	10/100/1000	Half duplex	1000 half duplex
	10/100	Full duplex	100 full duplex
	10/100	Half duplex	100 half duplex
	10	Full duplex	10 full duplex
	10	Half duplex	10 half duplex

5.3.2 Ping

Ping is invoked from the command prompt using the TIDA-00204 static IP address 192.168.1.10. Figure 49 presents a command prompt printout that shows the ping test.

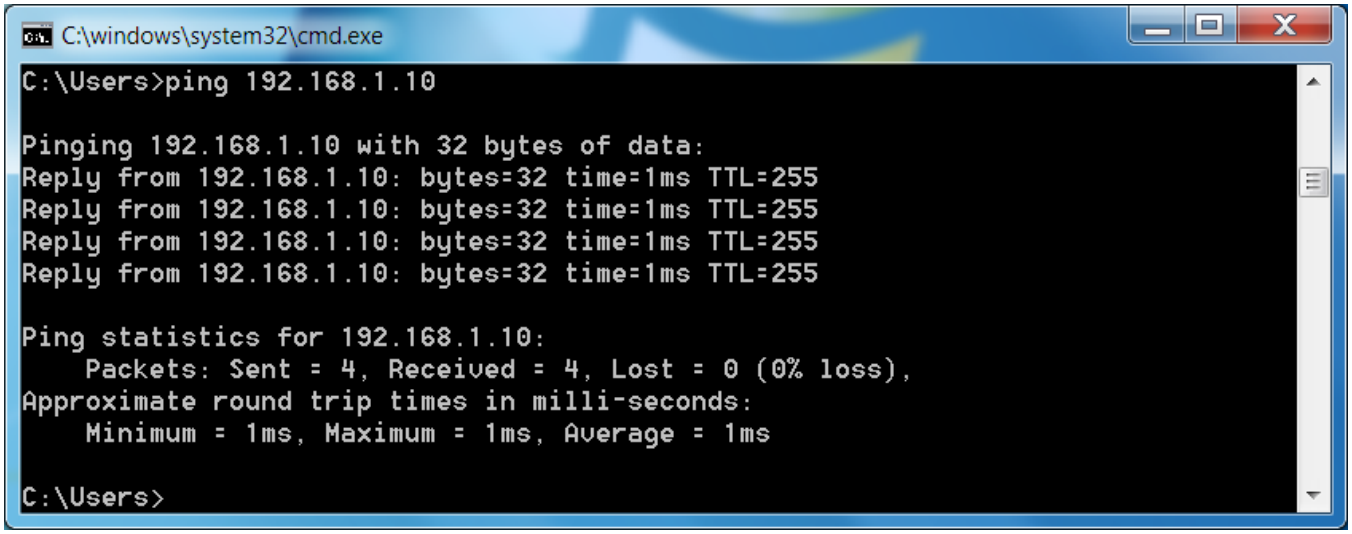


Figure 49. Command Prompt Ping Print

Wireshark was used to log the packet transfer during the ping test. In Figure 50, the Wireshark printout result can be seen.

No.	Time	Source	Destination	Protocol	Length	Info
1	0.000000000	ActionSt_12:d9:ed	Broadcast	ARP	42	Who has 192.168.1.10? Tell 192.168.1.30
2	0.001222000	TexasIns_f5:bb:ef	ActionSt_12:d9:ed	ARP	60	192.168.1.10 is at 88:33:14:f5:bb:ef
3	0.000149000	192.168.1.30	192.168.1.10	ICMP	74	Echo (ping) request id=0x0001, seq=1/256, ttl=128
4	0.001081000	192.168.1.10	192.168.1.30	ICMP	74	Echo (ping) reply id=0x0001, seq=1/256, ttl=255
5	0.992019000	192.168.1.30	192.168.1.10	ICMP	74	Echo (ping) request id=0x0001, seq=2/512, ttl=128
6	0.001234000	192.168.1.10	192.168.1.30	ICMP	74	Echo (ping) reply id=0x0001, seq=2/512, ttl=255
7	1.012331000	192.168.1.30	192.168.1.10	ICMP	74	Echo (ping) request id=0x0001, seq=3/768, ttl=128
8	0.000812000	192.168.1.10	192.168.1.30	ICMP	74	Echo (ping) reply id=0x0001, seq=3/768, ttl=255
9	1.013503000	192.168.1.30	192.168.1.10	ICMP	74	Echo (ping) request id=0x0001, seq=4/1024, ttl=128
10	0.001241000	192.168.1.10	192.168.1.30	ICMP	74	Echo (ping) reply id=0x0001, seq=4/1024, ttl=255

Figure 50. Wireshark Log of TIDA-00204 Ping Test

Using a Linux PC as the test machine when running ping tests gives a better indication of the Ethernet utilization. The Linux ping command gives the user more options to define the ping condition as well as the ping speed.

The ping command to use here is:

```
sudo ping 192.168.1.10 -s 1400 -p 5a -f
```

The following result is achieved with this command:

```
PATTERN: 0x5a
PING 192.168.1.10 (192.168.1.10) 1400(1428) bytes of data.
.^
--- 192.168.1.10 ping statistics ---
952050 packets transmitted, 952050 received, 0% packet loss, time 150052ms
rtt min/avg/max/mdev = 0.100/0.132/0.264/0.013 ms, ipg/ewma 0.157/0.137 ms
```

This test shows that the TIDA-00204 reference design can send large payload packages with high utilization of the Ethernet port and without any packet errors.

5.3.3 UDP

The UDP throughput test is invoked from the command prompt using the TIDA-00204 static IP address 192.168.1.10. Figure 51 presents a command prompt printout that shows the UDP throughput test.

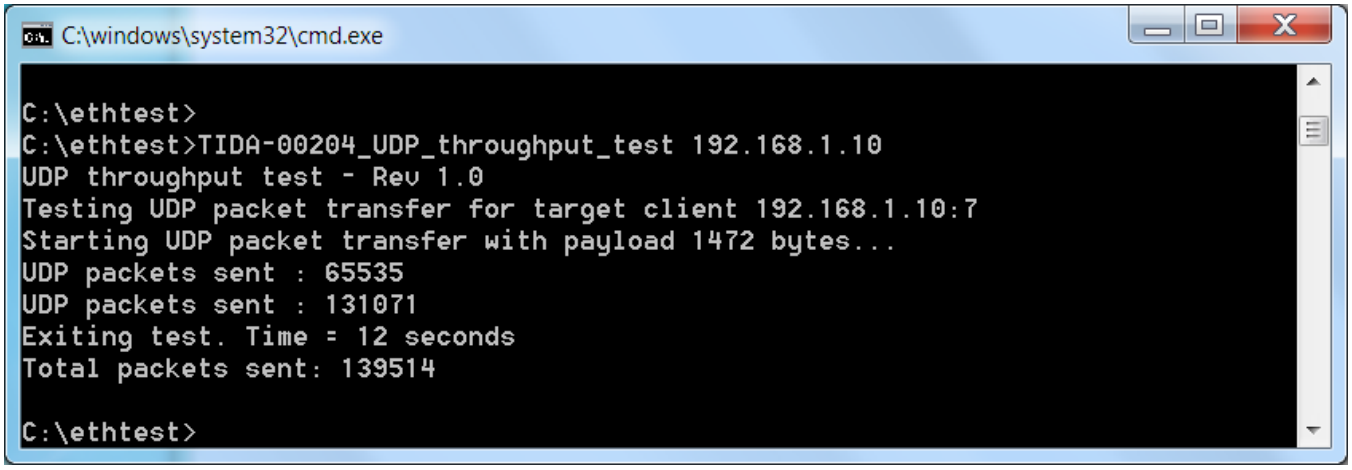


Figure 51. Command Prompt UDP Throughput Print

Windows Task Manager networking was used to log the packet transfer utilization during the UDP throughput test. Figure 52 shows the Windows Task Manager printout.

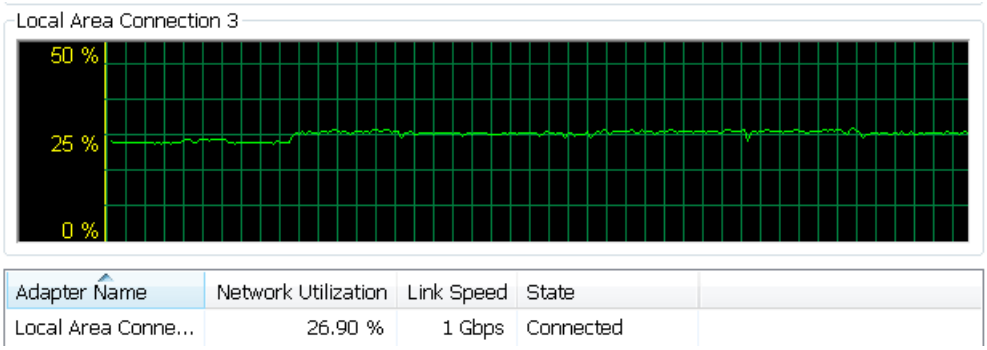


Figure 52. Utilization of One Port Connection With UDP Throughput Test Running

With the throughput test file, it is possible to achieve around 25% utilization of the Gigabit bandwidth. The slight change in the utilization on the curve is due to other network or CPU tasks.

When running this test on both ports simultaneously, the utilization will be 20% on each port.

For the UDP packet error test, the utilization is 5% independent of how many ports are connected, which is a limitation of the UDP packet error test software running on the PC.

5.3.4 HTTP Web Server

To test the HTTP web page example, the TIDA-00204's static IP address http://192.168.1.10 is entered into a browser (see Figure 53).

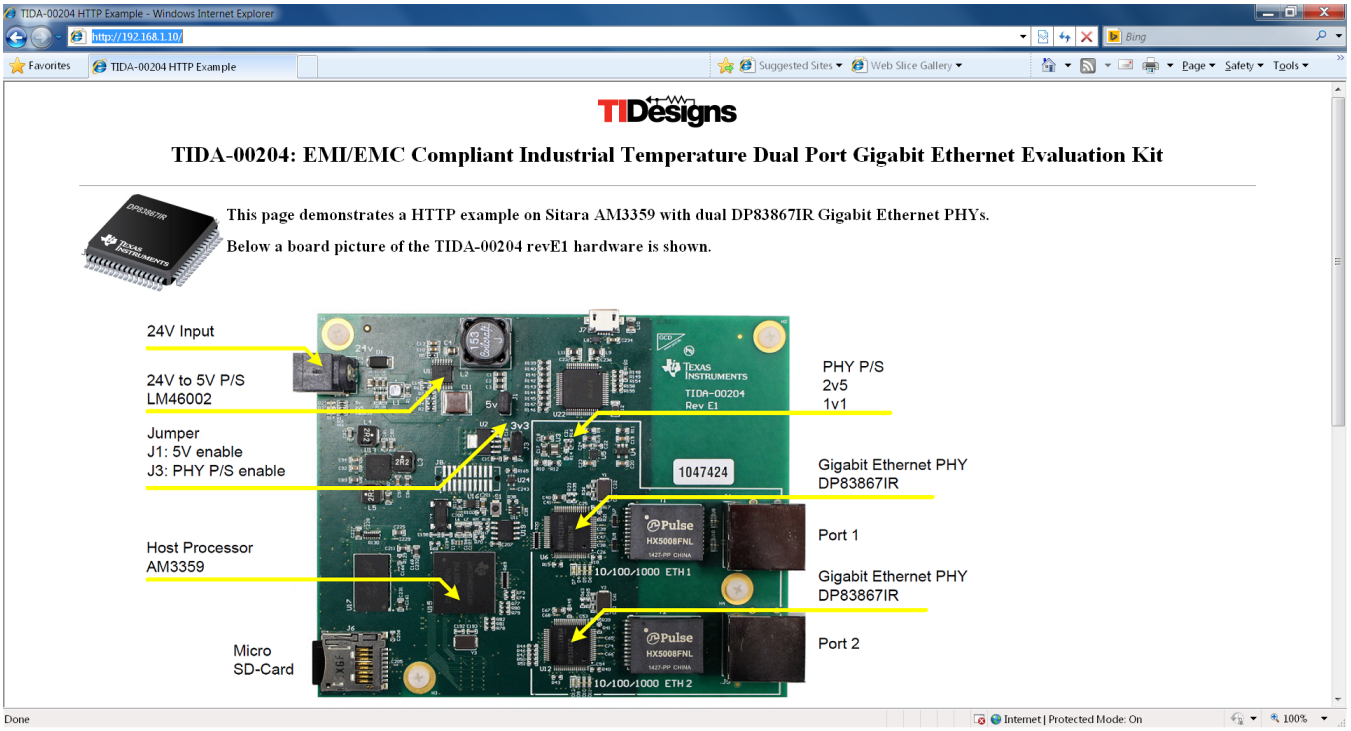


Figure 53. HTTP Web Server Example

For this test, Wireshark was used to log the traffic generated by initializing the web server and the loading of the page.

Figure 54 shows the traffic log from Wireshark.

No.	Time	Source	Destination	Protocol	Length	Info
1	0.000000000	0.0.0.0	255.255.255.255	DHCP	342	DHCP Discover - Transaction ID 0x8e450398
2	1.860607000	ActionSt_12:d9:ed	Broadcast	ARP	42	Who has 192.168.1.10? Tell 192.168.1.30
3	0.000942000	TexasIns_f5:bb:ef	ActionSt_12:d9:ed	ARP	60	192.168.1.10 is at 88:33:14:f5:bb:ef
4	0.000085000	192.168.1.30	192.168.1.10	TCP	66	64736→80 [SYN] Seq=0 Win=8192 Len=0 MSS=1460 WS=4 SACK_PERM=1
5	0.000886000	192.168.1.10	192.168.1.30	TCP	60	80→64736 [SYN, ACK] Seq=0 Ack=1 Win=4096 Len=0 MSS=1460
6	0.000099000	192.168.1.30	192.168.1.10	TCP	54	64736→80 [ACK] Seq=1 Ack=1 Win=64240 Len=0
7	0.000254000	192.168.1.30	192.168.1.10	HTTP	565	GET / HTTP/1.1
8	0.000890000	192.168.1.10	192.168.1.30	TCP	60	80→64736 [ACK] Seq=1 Ack=512 Win=3585 Len=0
9	0.000018000	192.168.1.10	192.168.1.30	TCP	97	[TCP segment of a reassembled PDU]
10	0.000067000	192.168.1.10	192.168.1.30	TCP	78	[TCP segment of a reassembled PDU]
11	0.000054000	192.168.1.10	192.168.1.30	HTTP	1127	HTTP/1.0 200 OK (text/html)
12	0.000106000	192.168.1.30	192.168.1.10	TCP	60	80→64736 [FIN, ACK] Seq=1141 Ack=512 Win=4096 Len=0
13	0.000030000	192.168.1.30	192.168.1.10	TCP	54	64736→80 [ACK] Seq=512 Ack=68 Win=64173 Len=0
14	0.000008000	192.168.1.30	192.168.1.10	TCP	54	64736→80 [ACK] Seq=512 Ack=1142 Win=63100 Len=0
15	0.000757000	192.168.1.30	192.168.1.10	TCP	54	64736→80 [FIN, ACK] Seq=512 Ack=1142 Win=63100 Len=0
16	0.000862000	192.168.1.10	192.168.1.30	TCP	60	80→64736 [ACK] Seq=1142 Ack=513 Win=4096 Len=0
17	0.002456000	192.168.1.30	192.168.1.10	TCP	66	64737→80 [SYN] Seq=0 Win=8192 Len=0 MSS=1460 WS=4 SACK_PERM=1
18	0.000887000	192.168.1.10	192.168.1.30	TCP	60	80→64737 [SYN, ACK] Seq=0 Ack=1 Win=4096 Len=0 MSS=1460
19	0.000113000	192.168.1.30	192.168.1.10	TCP	54	64737→80 [ACK] Seq=1 Ack=1 Win=64240 Len=0
20	0.000041000	192.168.1.30	192.168.1.10	TCP	66	64738→80 [SYN] Seq=0 Win=8192 Len=0 MSS=1460 WS=4 SACK_PERM=1
21	0.000165000	192.168.1.30	192.168.1.10	HTTP	425	GET /TIDesignsLogo.png HTTP/1.1
22	0.000670000	192.168.1.10	192.168.1.30	TCP	60	80→64738 [SYN, ACK] Seq=0 Ack=1 Win=4096 Len=0 MSS=1460
23	0.000070000	192.168.1.10	192.168.1.30	TCP	60	80→64737 [ACK] Seq=1 Ack=372 Win=3725 Len=0
24	0.000010000	192.168.1.10	192.168.1.30	TCP	112	[TCP segment of a reassembled PDU]
25	0.000057000	192.168.1.10	192.168.1.30	TCP	78	[TCP segment of a reassembled PDU]
26	0.000042000	192.168.1.10	192.168.1.30	TCP	1514	[TCP segment of a reassembled PDU]
27	0.000045000	192.168.1.10	192.168.1.30	HTTP	838	HTTP/1.0 200 OK (PNG)
28	0.000027000	192.168.1.10	192.168.1.30	TCP	60	80→64737 [FIN, ACK] Seq=2327 Ack=372 Win=4096 Len=0
29	0.000027000	192.168.1.30	192.168.1.10	TCP	54	64738→80 [ACK] Seq=1 Ack=1 Win=64240 Len=0
30	0.000008000	192.168.1.30	192.168.1.10	TCP	66	64739→80 [SYN] Seq=0 Win=8192 Len=0 MSS=1460 WS=4 SACK_PERM=1
31	0.000005000	192.168.1.30	192.168.1.10	TCP	54	64737→80 [ACK] Seq=372 Ack=83 Win=64158 Len=0
32	0.000007000	192.168.1.30	192.168.1.10	HTTP	421	GET /DP83867IR.png HTTP/1.1

Figure 54. Wireshark Log of TIDA-00204 HTTP Web Server Example

5.4 EMC/EMI Test Results

The TIDA-00204 TI design has been tested for EMI according to CISPR 11 / EN55011 Class A radiated emissions. For EMC immunity, the design has been tested according to IEC61800-3 and IEC61000-6-2 for ESD, EFT, and Surge with reference to standards IEC61000-4-2, IEC61000-4-4, and IEC61000-4-5, respectively.

The design is compliant to these standards and exceeds the voltage requirements according to IEC61800-3 EMC immunity requirements. A summary is shown in the following tables and more details in the following sections.

Table 26. CISPR 11 / EN55011 Class A Radiated Emission Requirements for Category 2 and Measured Level

REQUIREMENTS			TIDA-00204 MEASUREMENTS	
Phenomenon	**Basic standard**	**Category 2 electric field strength component quasi-peak dB (µV/m)**	**Measured minimum margin to limit**	**Test**
EMI	CISPR 11 / EN55011 Class A	40 (30 to 230 MHz) 47 (230 to 1000 MHz)	Horizontal: 10.6 dB (125 MHz) Vertical: 4.3 dB (125 Mhz)	PASS

Table 27. IEC61800-3 and IEC61000-6-2 EMC Immunity Requirements for Second Environment and Measured Voltage Levels and Class

REQUIREMENTS					TIDA-00204 MEASUREMENTS		
Port	**Phenomenon**	**Basic standard**	**Level**	**Performance (acceptance) criterion**	**Level**	**Performance Criterion**	**Test**
Enclosure ports	ESD	IEC61000-4-2	±4-kV CD or 8-kV AD, if CD not possible	B	±6-kV CD	B	PASS (EXCEED)
Ports for control lines and DC auxiliary supplies <60 V	EFT	IEC61000-4-4	±2-kV/5-kHz, capacitive clamp	B	±4 kV	B	PASS (EXCEED)
	Surge 1.2/50 µs, 8/20 µs	IEC61000-4-5	±1-kV; since shielded cable >20-m, direct coupling to shield (2 Ω/500 A)	B	±2 kV	A(1)	PASS (EXCEED)

(1) Class A is considered when there are less than two consecutive UDP packet losses and no major drop in network utilization. One UDP packet loss will be tolerated by the system if the following UDP packet is echoed back successfully. The test has been conducted with a UDP error packet test program at around 5% network bandwidth.

The performance (acceptance) criterion is defined as follows:

Table 28. Performance (Acceptance) Criterion

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module shall continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the module shall continue to operate as intended without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module shall continue to operate as intended automatically, after manual restart, or power off, or power on.

5.4.1 Test Setup

The TIDA-00204 TI design has been tested at the testing laboratory of CSA Group Bayern in Strasskirchen, Germany.

The TIDA-00204 with the test equipment is shown in the below picture. Each of the TIDA-00204 Gigabit Ethernet ports 1 and 2 are connected to a PC or Laptop with an external Gigabit Ethernet to USB3 adapter. Two different test programs ran of the laptops.

The first test program "tida-00204_udp_throughput_test.exe" transmits and receives continuous UDP packages with a payload size of 1472 bytes, yielding the maximum 1514 bytes per IPv4 packet. The firmware of the Sitara AM3359 receives the UDP packets and echoes them back. Each of the two Ethernet ports used around 20% of the network.

The second test program "tida-00204_udp_packet_error_test.exe" implements a UDP packet tester. It compares the transmitted packet with the received packet (echoed back from Sitara AM3359) for the corresponding Gigabit Ethernet port on the TIDA-00204. If a packet error is detected, it prints the number of the packet to the console. The maximum bandwidth/network utilization achievable with this test software was around 5% due to limitation on the PC test software "tida-00204_udp_packet_error_test.exe".

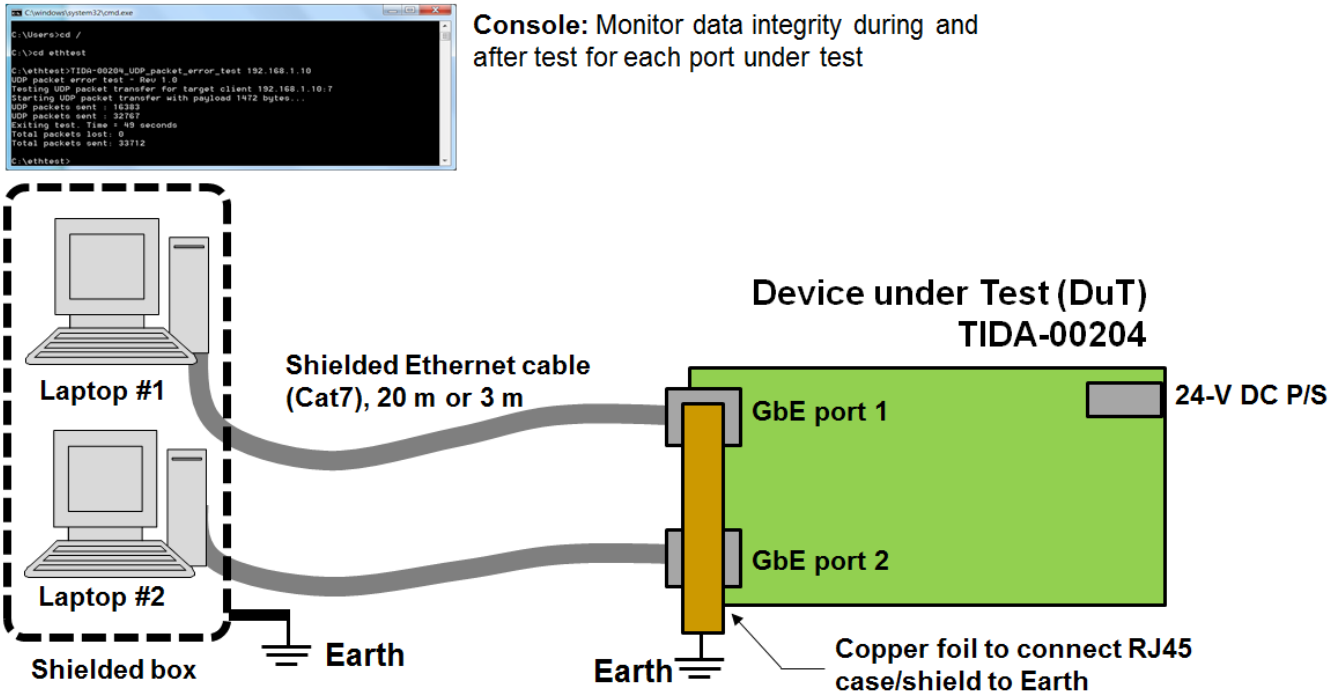


Figure 55. TIDA-00204 Test Equipment Overview for EMI/EMC Tests

The specific test setups for EMI (Section 5.4.2), ESD (Section 5.4.3), EFT (Section 5.4.4), and Surge (Section 5.4.5).

5.4.2 CISPR 11 / EN55011 Radiated Emission Test Results

The TIDA-00204 meets EN55011 / CSPR 11 Class A requirements for category 2 with **at least 4.3 dB** of margin (far-field measurements at 125 MHz, vertical polarization). The minimum margin in horizontal polarization was **10.6 dB** at 125 MHz as well.

An automatic pre-test with near-field measurement (3-m antenna distance to device under test [DuT]) was used to identify the frequencies of maximum EMI in each horizontal and vertical polarization as preparation for the final test with a 10-m antenna distance.

Figure 56 shows the test setup of the final measurement with a 10-m antenna distance to DuT.

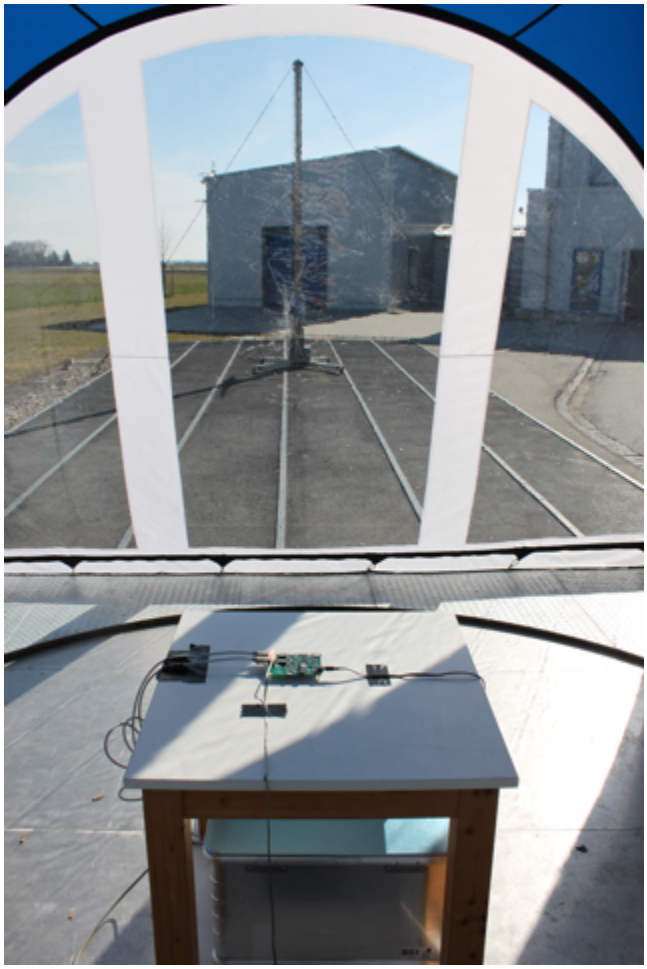


Figure 56. CISPR 11 / EN55011 Test Setup for Far-Field With 10-m Antenna Distance to TIDA-00204 DuT

Figure 57 and Figure 58 show the measured spectral density with the final measurement with a 10-m antenna at the critical frequencies identified during the pre-test. As mentioned earlier, the minimum margin was 4.3 dB in vertical and 10.6 dB in horizontal polarization, each at 125 MHz.

Table 29. Measured EMI Spectrum (Quasi-Peak) According to EN55011; 10-m Far-Field, Horizontal Polarization

FREQUENCY (MHz)	READING [dBµV] (QP)	CORRECTION (dB)	VALUES [dBµV/m] (QP)	LIMIT [dBµV/m] (QP)	MARGIN [dB] (QP)
125	18.6	10.8	29.4	40	10.6
250	21.1	15.2	36.3	47	10.7
375	16.6	18.8	35.4	47	11.6
500	12.9	21.8	34.7	47	12.3
875	4.9	27.3	32.2	47	14.8

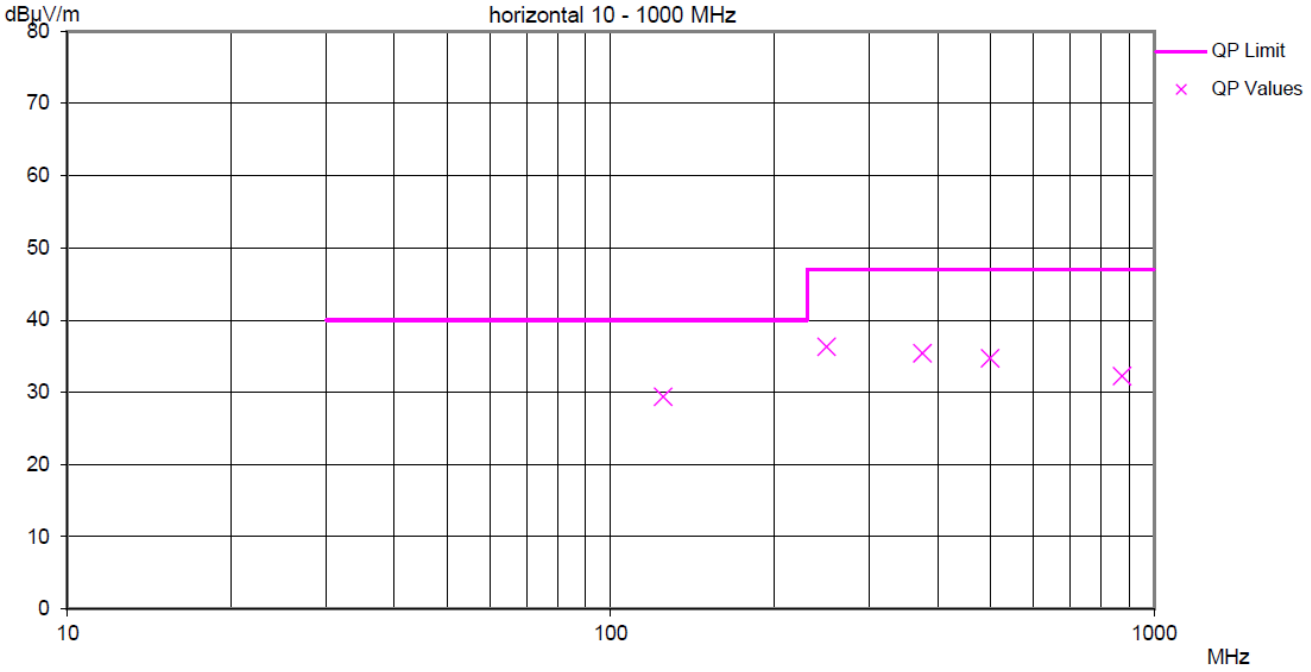


Figure 57. Measured EMI Spectrum (Quasi-Peak) According to EN55011; 10-m Far-Field, Horizontal Polarization

Table 30. Measured EMI Spectrum (Quasi-Peak) According to EN55011; 10-m Far-Field, Vertical Polarization

FREQUENCY (MHz)	READING [dBuV] (QP)	CORRECTION (dB)	VALUES [dBuV/m] (QP)	LIMIT [dBuV/m] (QP)	MARGIN [dB] (QP)
125	24.9	10.8	35.7	40	4.3
250	20.4	15.2	35.6	47	11.4
375	12.6	18.8	31.4	47	15.6
500	8.5	21.8	30.3	47	16.7
875	1.2	27.3	28.5	47	18.5

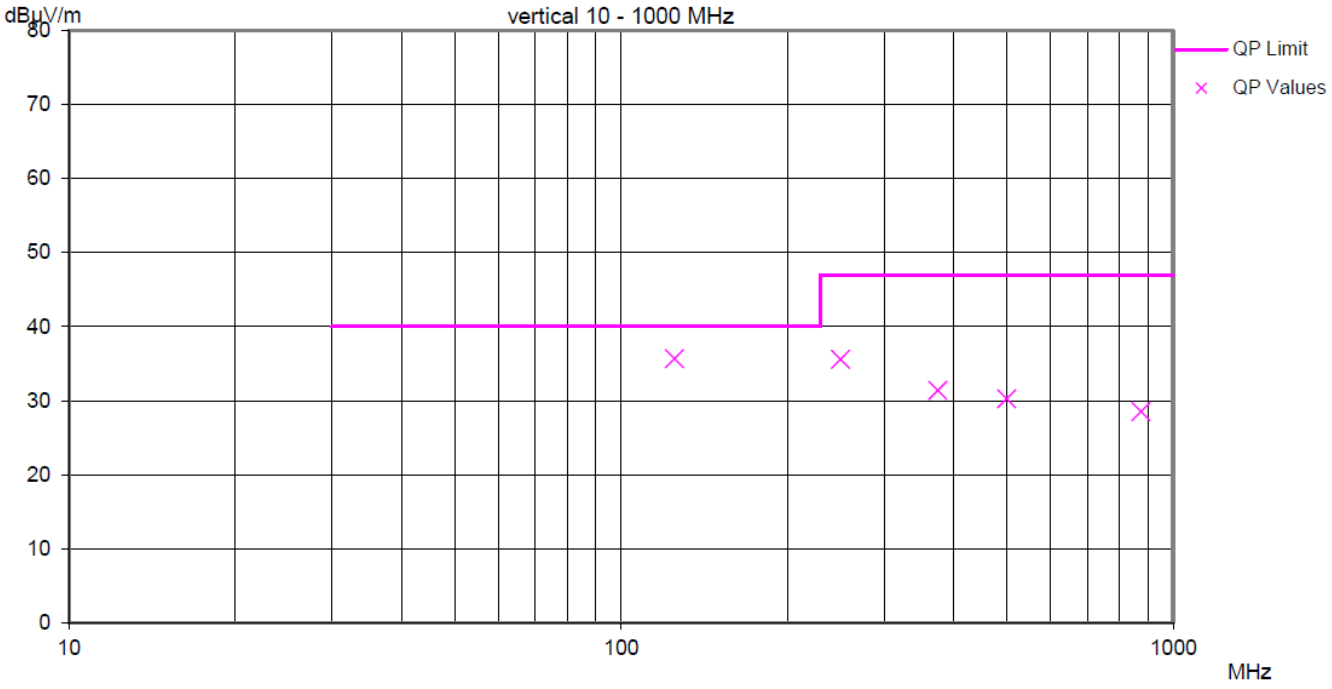


Figure 58. Measured EMI Spectrum (Quasi-Peak) According to EN55011; 10-m Far-Field, Vertical Polarization

5.4.2.1 Pre-Test Results With 3-m Antenna Distance

CAUTION

Due to the shorter distance (3 m instead of 10 m), the threshold for EN55011 for radiated EMI is higher by 10 dB as well. The setup is shown in Figure 59.

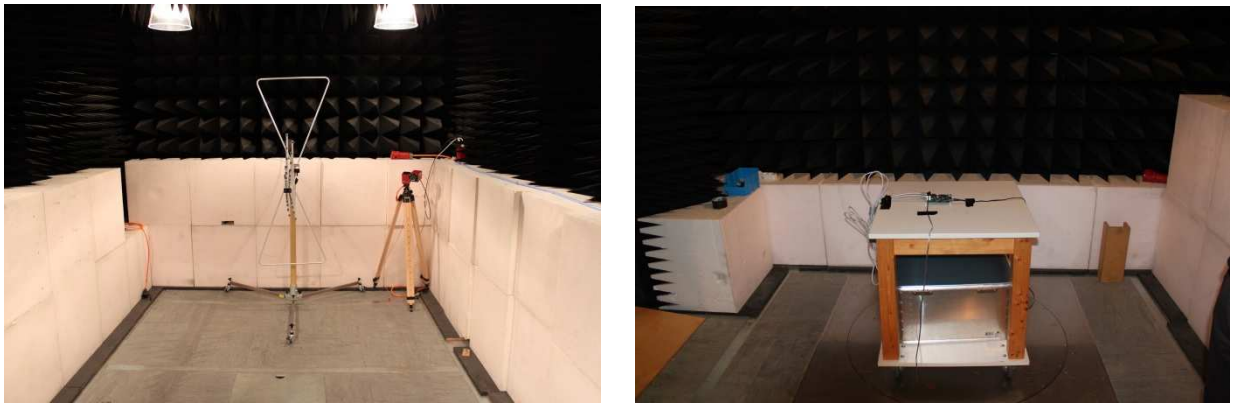


Figure 59. Automatic Pre-Test Setup for EMI With 3-m Antenna Distance to DuT (Left: Antenna, Right: TIDA-00204 DuT and Box With Shielded Laptops)

A pre-test was done to identify the critical frequencies on each polarization. This test has been done in a chamber with a 3-m distance to the antenna.

Table 31. Pre-Test Equipment Setup

TYPE	NAME
Antenna	A5_VULB9168_24-14-007
Cable	A5_Cable_50-13-018
Cable	A5_Cable_50-13-019
Preamplifier	Ohm1_MTS TVV-695_50-01-059
Receiver	Ohm1_FSP7_11-05-002
Turntable	CO1000

The measured spectrum of the pre-test is shown in Figure 60 for horizontal and in Figure 61 for vertical polarization.

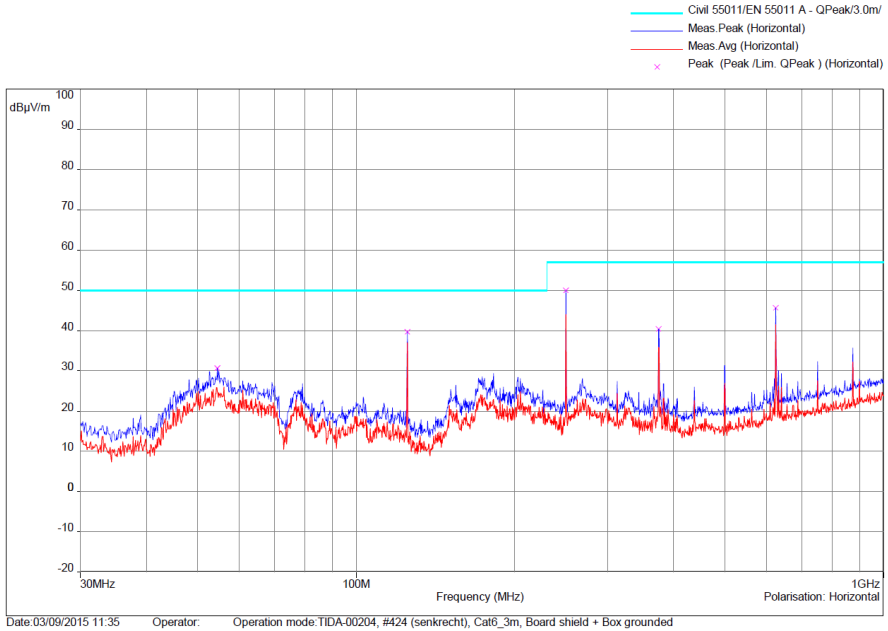


Figure 60. Measured EMI Spectrum According to EN55011; 3-m Near-Field, Horizontal Polarization (Pre-Test)

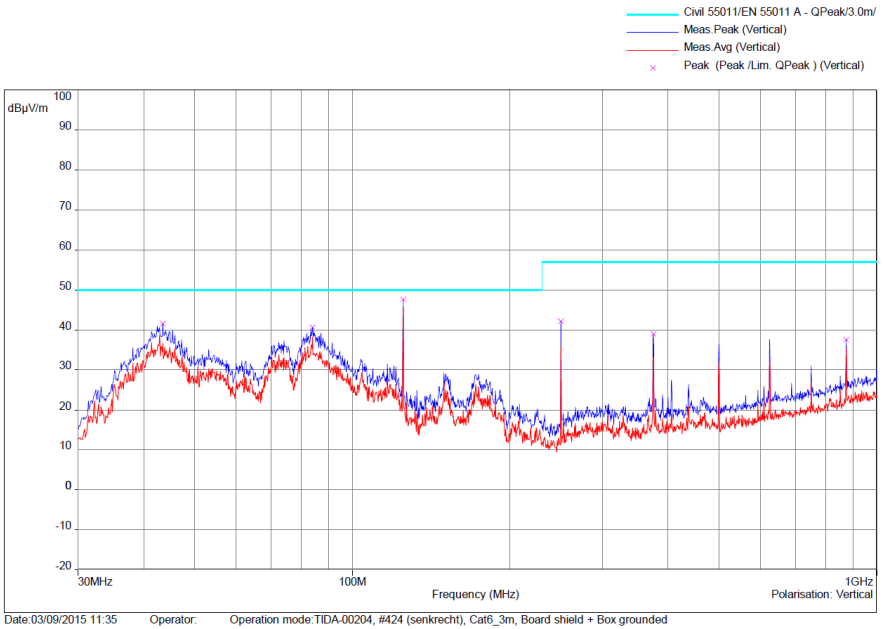


Figure 61. Measured EMI Spectrum According to EN55011; 3-m Near-Field, Vertical Polarization (Pre-Test)

5.4.3 IEC-61000-4-2 ESD Test Results

Figure 62 shows the ESD test setup. The ESD strike was applied to the RJ45 case or shield of port 1 and port 2. Both RJ45 cases were electrically connected with a conductive copper foil. During the ESD test, both Gigabit Ethernet ports were connected with a 20-m cable to the far-end laptops. A UDP packet transfer was launched on each Gigabit Ethernet link.

The test program "tida-00204_udp_throughput_test.exe" transmits and receives continuous UDP packages with a payload size of 1472 bytes, yielding the maximum 1514 bytes per IPv4 packet. The firmware of the Sitara AM3359 receives the UDP packets and echoes them back. The network utilization was around 20% on each of the two Ethernet ports.

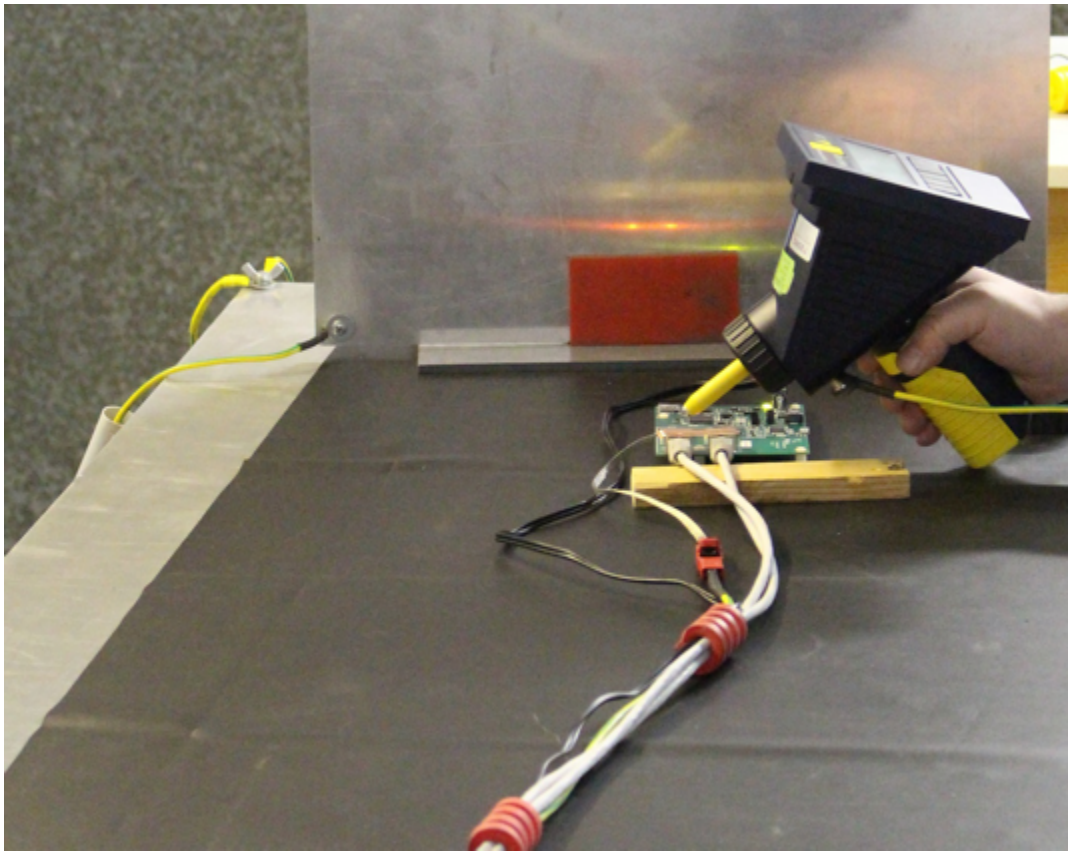


Figure 62. IEC61000-4-2 Test Setup for TIDA-00204 (Picture of 6-kV CD)

Table 32 shows the complete ESD test results for contact and air discharge (AD) at voltage levels, which also exceed the requirements per IEC61800-3. This is marked accordingly.

Table 32. IEC-61000-4-2 ESD Test Results for TIDA-00204

PHENOMENON	BASIC STANDARD	LEVEL	TIDA-00204 CONNECTOR UNDER TEST	PERFORMANCE CRITERION(1)	COMMENT
ESD	IEC61000-4-2	±4-kV CD	RJ45 port 1 and 2	B	
ESD	IEC61000-4-2	±6-kV CD	RJ45 port 1 and 2	B	Not required per IEC61800-3
ESD	IEC61000-4-2	±8-kV CD	RJ45 port 1 and 2	C	Not required per IEC61800-3
ESD	IEC61000-4-2	±8-kV AD	RJ45 port 1 and 2	B	
ESD	IEC61000-4-2	±15-kV AD	RJ45 port 1 and 2	B	Not required per IEC61800-3

(1) See Table 28 for performance descriptions.

Class B was claimed when there was a network utilization reduction, but no link loss. Only for 8-kV ESD CD was the link lost and a power-cycle of the boards was required. Figure 63 shows the network utilization during the entire ESD test for ±6-kV CD ESD strikes. It can be seen that the network utilization is reduced due to lost packets, but the link does not drop.

Figure 63. IEC61000-4-2 ±6-kV ESD CD: Network Utilization With UDP Packet Throughput Test on Port 1 and Port 2 (Measured on Two Separate Laptops)

5.4.4 IEC-61000-4-4 EFT Test Results

Figure 64 shows the EFT test setup. During the EFT test, both Gigabit Ethernet ports where connected with a 3-m CAT7 cable to far end laptops. The capacitive clamp can be seen in the foreground of Figure 64.

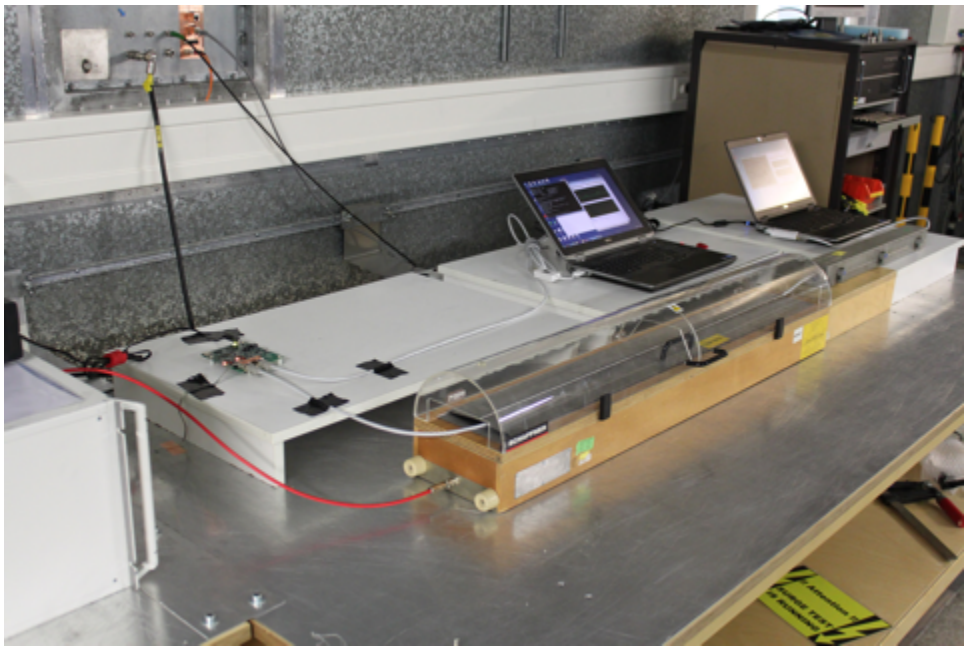


Figure 64. IEC61000-4-4 EFT Test Setup for TIDA-00204

During the EFT tests, a UDP packet transfer was launched on each Gigabit Ethernet port. Each test level and Gigabit Ethernet port was tested with two different PC software programs running on a laptop for analysis, as described earlier. The test results are shown in Table 33.

Table 33. IEC-61000-4-4 EFT Test Results for TIDA-00204

PHENOMENON	BASIC STANDARD	LEVEL	TIDA-00204 CONNECTOR UNDER TEST	PERFORMANCE CRITERION(1)(2)	COMMENT
EFT	IEC61000-4-4	±2-kV/5-kHz, cap clamp	RJ45 port 1	B	
EFT	IEC61000-4-4	±2-kV/5-kHz, cap clamp	RJ45 port 2	B	
EFT	IEC61000-4-4	±4-kV/5-kHz, cap clamp	RJ45 port 1	B	Not required per IEC61800-3
EFT	IEC61000-4-4	±4-kV/5-kHz, cap clamp	RJ45 port 2	B	Not required per IEC61800-3

(1) See Section 5.4.1 for test setup description.
(2) See Table 28 for performance descriptions.

To verify the number of packets lost the program during the EFT tests, a UDP packet transfer was launched on each Gigabit Ethernet port. Each EFT voltage test level and gigabit Ethernet port was tested with two different software programs running on the laptop for analysis of throughput and packet errors during an EFT event.

Class B was claimed as there was no significant network utilization reduction, from the average of around 20% during the UDP packet throughput test as shown in Figure 65. During the packet error test, the network utilization dropped from 5% to 1% due to a laptop issue when a packet lost was detected.

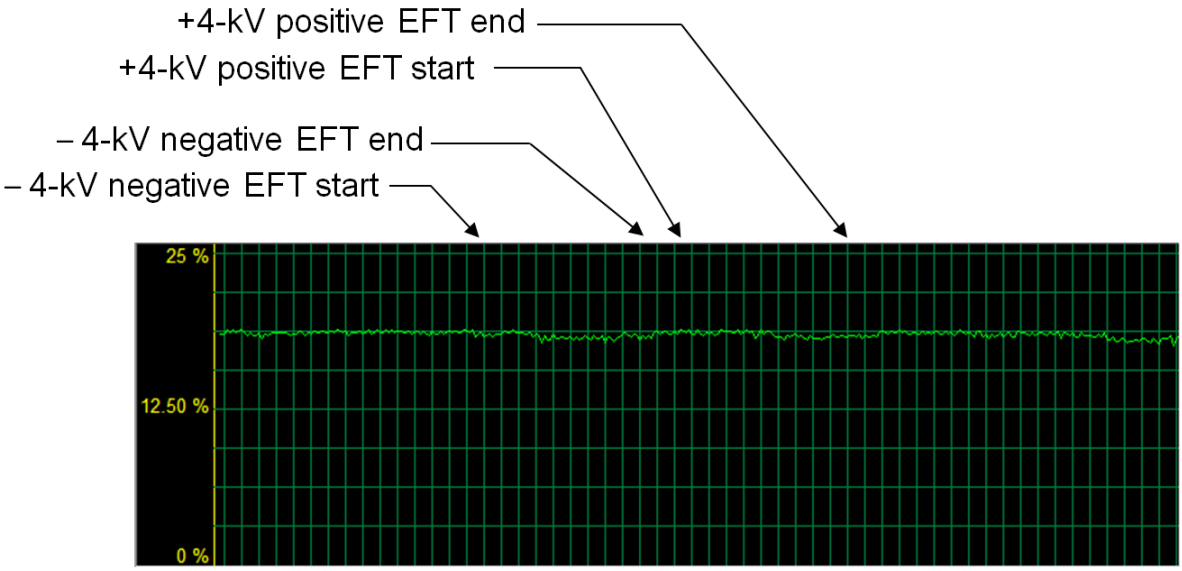


Figure 65. IEC61000-4-4 ±4-kV EFT: Network Utilization With UDP Throughput Test on Gigabit Ethernet Port 1

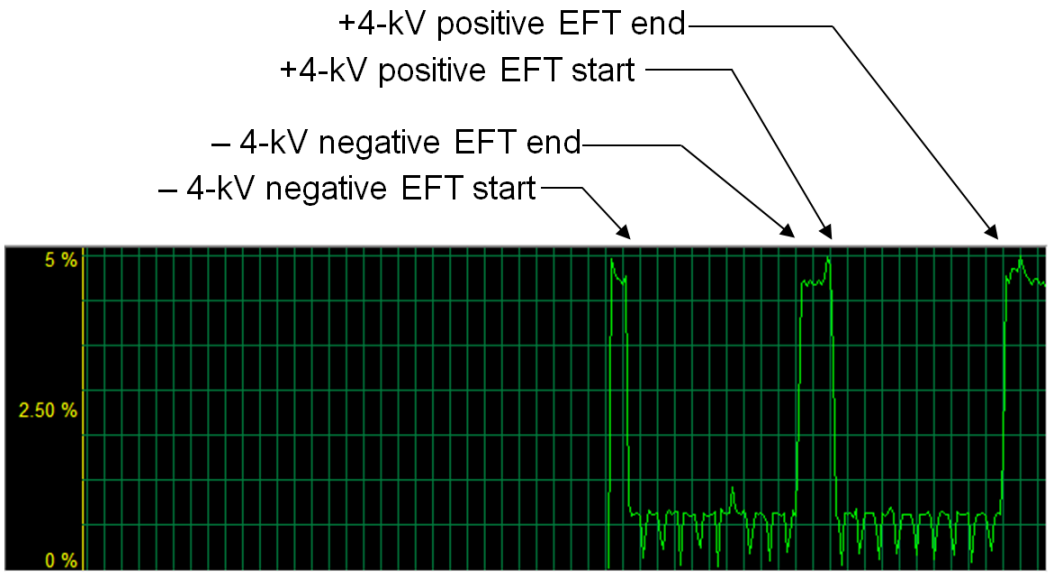


Figure 66. IEC61000-4-4 ±4-kV EFT: Network Utilization With UDP Packet Error Test on Gigabit Ethernet Port 1

During the test, the UDP packet error test program printed the packet number for every packet lost as well as the total submitted packets. The total number of submitted packets during the EFT event was 60,680 packets (1526 bytes each). The number of lost packets was 100. However, there was not a single event where two consecutive packets were lost. Therefore, every lost packet was re-submitted successfully.

5.4.5 IEC-61000-4-5 Surge Test Results

Figure 67 shows the surge test setup. During the surge test, both Gigabit Ethernet ports where connected. The port under test with a 20-m CAT7 cable and the other port, not under test with a 3-m cable to far end laptops, respectively. The surge generator is on the left-hand side outside the picture.

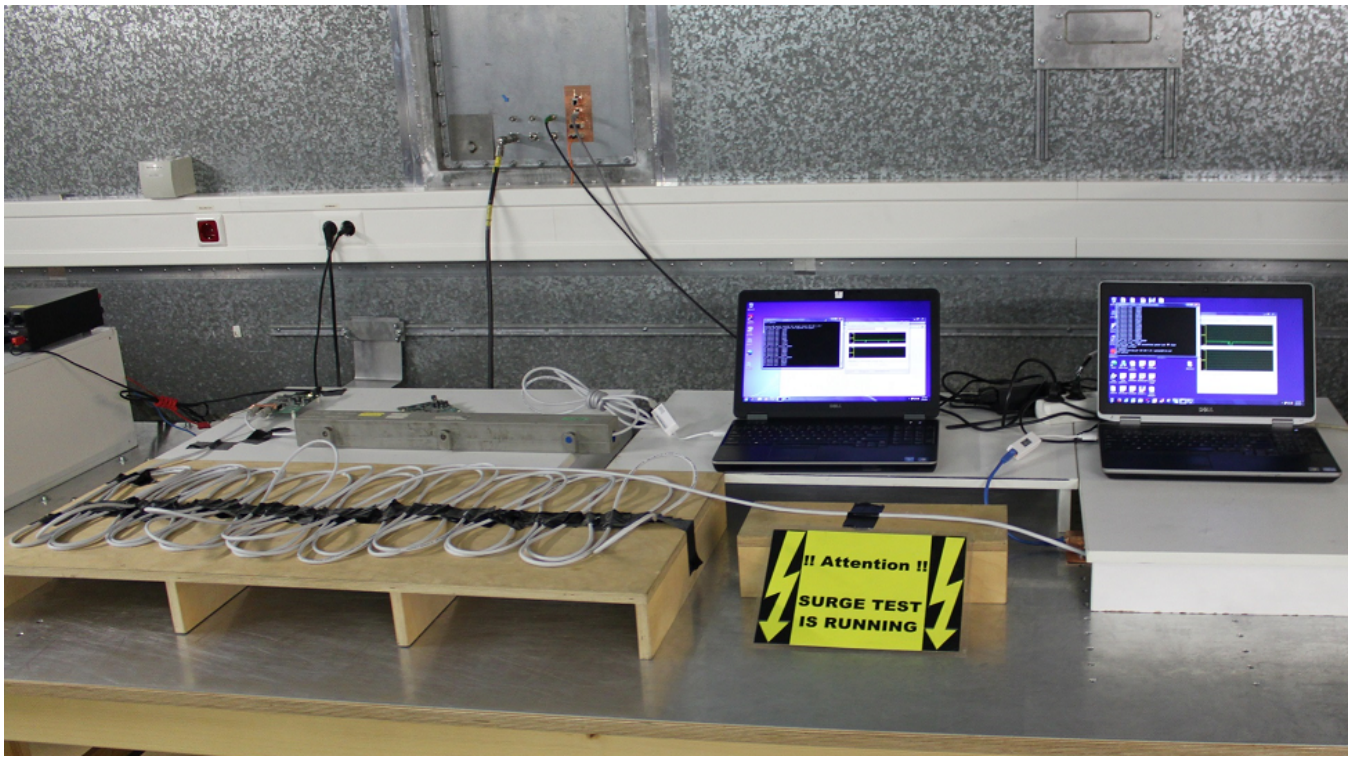


Figure 67. IEC61000-4-5 Surge Test Setup for TIDA-00204

During the surge tests, a UDP packet transfer was launched on each Gigabit Ethernet port. Each test level and Gigabit Ethernet port was tested with two different PC software programs running on a laptop for analysis, as described earlier. The test results are shown in Table 34.

Table 34. IEC-61000-4-5 Surge Test Results for TIDA-00204

PHENOMENON	BASIC STANDARD	LEVEL	TIDA-00204 CONNECTOR UNDER TEST	PERFORMANCE CRITERION(1)(2)	COMMENT
Surge	IEC61000-4-5	±1-kV, 2-Ω/500-A (20-m shielded CAT7 Ethernet cable)	RJ45 port 1	A	Exceeds IEC61800-3, only Class B required
Surge	IEC61000-4-5	±1-kV, 2-Ω/500-A (20-m shielded CAT7 Ethernet cable)	RJ45 port 2	A	Exceeds IEC61800-3, only Class B required
Surge	IEC61000-4-5	±2-kV, 2-Ω/500-A (20-m shielded CAT7 Ethernet cable)	RJ45 port 1	A	Exceeds IEC61800-3
Surge	IEC61000-4-5	±2-kV, 2-Ω/500-A (20-m shielded CAT7 Ethernet cable)	RJ45 port 2	A	Exceeds IEC61800-3

(1) See Section 5.4.1 for test setup description.
(2) See Table 28 for performance descriptions.

Class A is considered when there are less than two consecutive UDP packet losses and no major drop in network utilization. One UDP packet loss will be tolerated by the system, if the following UDP packet is echoed back successfully. The test has been conducted with a UDP error packet test program at around 5% network bandwidth (see Figure 68).

To verify the number of packets lost the program during the surge tests, a UDP packet transfer was launched on each Gigabit Ethernet port. Each surge voltage test level and Gigabit Ethernet port was tested with two different software programs running on the laptop for analysis of throughput and packet errors during a surge event.

Class A was claimed as there was no significant network utilization reduction, from the average of around 20% during the UDP packet throughput test. During the packet error test, the network utilization remained 5%. The total number of submitted packets during the surge event was 230,000 packets (1526 bytes each). Only one packet was lost. Higher network utilization may yield more packet error losses; however, this was not tested due to lack of test equipment.

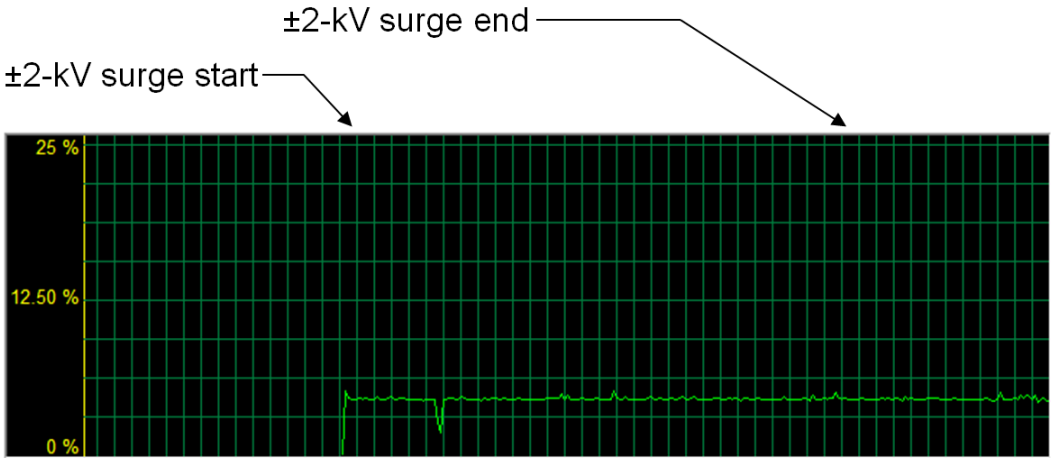


Figure 68. IEC61000-4-5 ±2-kV Surge: Network Utilization With UDP Packet Error Test on Gigabit Ethernet Port 1

```
UDP packet error test - Rev 1.0
Testing UDP packet transfer for target client 192.168.1.10:7
Starting UDP packet transfer with payload 1472 bytes...
UDP packets sent : 16383
UDP packets sent : 32767
UDP packets sent : 49151
UDP packets sent : 65535
Packet lost on transmit 77363
UDP packets sent : 81919
UDP packets sent : 98303
UDP packets sent : 114687
UDP packets sent : 131071
UDP packets sent : 147455
UDP packets sent : 163839
UDP packets sent : 180223
UDP packets sent : 196607
UDP packets sent : 212991
UDP packets sent : 229375
UDP packets sent : 245759
UDP packets sent : 262143
UDP packets sent : 278527
UDP packets sent : 294911
UDP packets sent : 311295
UDP packets sent : 327679
UDP packets sent : 344063
UDP packets sent : 360447
UDP packets sent : 376831
UDP packets sent : 393215
UDP packets sent : 409599
UDP packets sent : 425983
UDP packets sent : 442367
UDP packets sent : 458751
UDP packets sent : 475135
UDP packets sent : 491519
Exiting test. Time = 263 seconds
Total packets lost: 1
Total packets sent: 499038
```

Figure 69. IEC61000-4-5 ±2-kV Surge: Packet Error Analysis, Console Printout on Gigabit Ethernet Port 1

Additional tests were done with a modified board that did not have a TVS diode between the PHY and transformer. During ±1-kV surge (as per IEC61800-3), no significant changes were observed with or without TVS diode. However, at ±2-kV (exceeding the level required by IEC61800-3), the packet error losses significantly increase by a factor of 10. Therefore, if higher surge immunity is desired the TVS diode is recommend to be populated between the PHY and the transformer as per the TIDA-00204 schematics. The TVS diode between the transformer and the RJ45 connector on ETH1 (port 1) was an initial test option and not needed. It is marked DNP (not fitted) on the TIDA-00204 schematics.

6 Design Files

6.1 Schematics

To download the schematics, see the design files at TIDA-00204.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00204.

6.3 Layer Plots

To download the layer plots, see the design files at TIDA-00204.

6.4 PCB Layout Guidelines

6.4.1 Layer Stack

Ensure that the differential signal layers have a reference ground and that the PCB differential signal traces are matched to 100-Ω impedance. For the single-ended traces, the board is matched to 50 Ω.

A layer size of 0.018 mm was chosen for the top and mid layers. This size can be defined as the base thickness. When actually building the board, the mid layers will decrease in size and the outer layers will increase in size. This means that the expected top layer thickness would be 0.040 mm and a mid layer would have an expected thickness of 0.012 mm. This decrease and increase in thickness varies on the manufacturer. This variation is why it is very important when working with high-speed differential signals to define the layer stack and double check with the PCB manufacturer to ensure that the expected impedances are achieved.

Stack Up		Layer Stack				Calculated Values (by ISOLA MultiCal 6.0)			
Layer	Board Layer Stack	Name	Material	Thickness	Constant	Thickness Base / Expected	Zdiff=100R Line Width/Separation	Zdiff=90R Line Width/Separation	Z0=50R Line Width
1		Top Paste							
2		Top Overlay							
3		Top Solder	Solder Resist	0.015mm	3.9	0.015mm			
4		TopLayer - S1 (.GTL)	Copper	0.018mm		0.018 / **0.040** mm	0.101 / 0.215mm	0.130 / 0.210 mm	0.125 mm
5		Dielectric1	FR4, IS420ML, 1x 1080 (Prepreg)	0.085mm	4.36	0.089 mm			
6		MidLayer1 - S2 (.G1)	Copper	0.018mm		0.018 / **0.012** mm	REF GND	REF GND	REF GND
7		Dielectric2	FR4, IS420ML, 1x 2116 (Core)	0.101mm	4.72	0.101mm			
8		MidLayer2 - S3 (.G2)	Copper	0.018mm		0.018 / **0.012** mm	0.101 / 0.210 mm	-	0.119 mm
9		Dielectric3	FR4, IS420ML, 3x 2157 (Prepreg)	0.440mm	4.75	0.401mm			
10		MidLayer3 - S4 (.G3)	Copper	0.018mm		0.018 / **0.012** mm		GND	
11		Dielectric4	FR4, IS420ML, 1x 2116 (Core)	0.101mm	4.72	0.101mm			
12		MidLayer4 - S5 (.G4)	Copper	0.018mm		0.018 / **0.012** mm		Power	
13		Dielectric5	FR4, IS420ML, 3x 2157 (Prepreg)	0.440mm	4.75	0.401mm			
14		MidLayer5 - S6 (.G5)	Copper	0.018mm		0.018 / **0.012** mm	0.101 / 0.210 mm	-	0.119 mm
15		Dielectric 6	FR4, IS420ML, 1x 2116 (Core)	0.101mm	4.72	0.101mm			
16		MidLayer6 - S7 (.G6)	Copper	0.018mm		0.018 / **0.012** mm	REF GND	REF GND	REF GND
17		Dielectric 7	FR4, IS420ML, 1x 1080 (Prepreg)	0.085mm	4.36	0.089 mm			
18		BottomLayer - S8 (.GBL)	Copper	0.018mm		0.018 / **0.040** mm	0.101 / 0.215mm	-	0.125 mm
19		Bottom Solder	Solder Resist	0.015mm	3.9	0.015mm			
20		Bottom Overlay							
21		Bottom Paste							
	Height : 1.527mm								

Figure 70. Layer Stack

For a less complex processor design, the PCB layers for DP83867IR routing can be reduced to four layers. See the DP83867IR data sheet for examples[1].

6.4.2 Layout RGMII Signals

Looking at the layout, each RX or TX group of the RGMII signals are routed on the same layer with matched trace length as outlined in Section 2.3.1.

The goal for routing the signals is to minimize the trace length of both RGMII 1 and RGMII 2 interfaces, which is done using the following considerations.

The RGMII interface is a 125-MHz signal, which gives a full clock cycle of 8 ns.

The typical propagation delay in a FR4 stripline is 7.087 ns/mm, which means that the length of the RGMII interface introduces a delay that should be kept as small as possible. For the RGMII signal below 0.5 ns, this should be a delay that can be ignored. So the signal can be around 63.5-mm long, maximum.

A second important point is that when changing layers, a GND via is added next to the signal via to ensure a good matching as well offer a current return path close to the signal.

The PCB signals are impedance controlled to 50 Ω, and have series line termination. For the series termination at both the PHYs, 0-Ω resistors were chosen due to the DP83867IR internal 50-Ω impedance. These resistors were only added for test and debug. For the AM3359, 22-Ω series termination resistors were chosen.

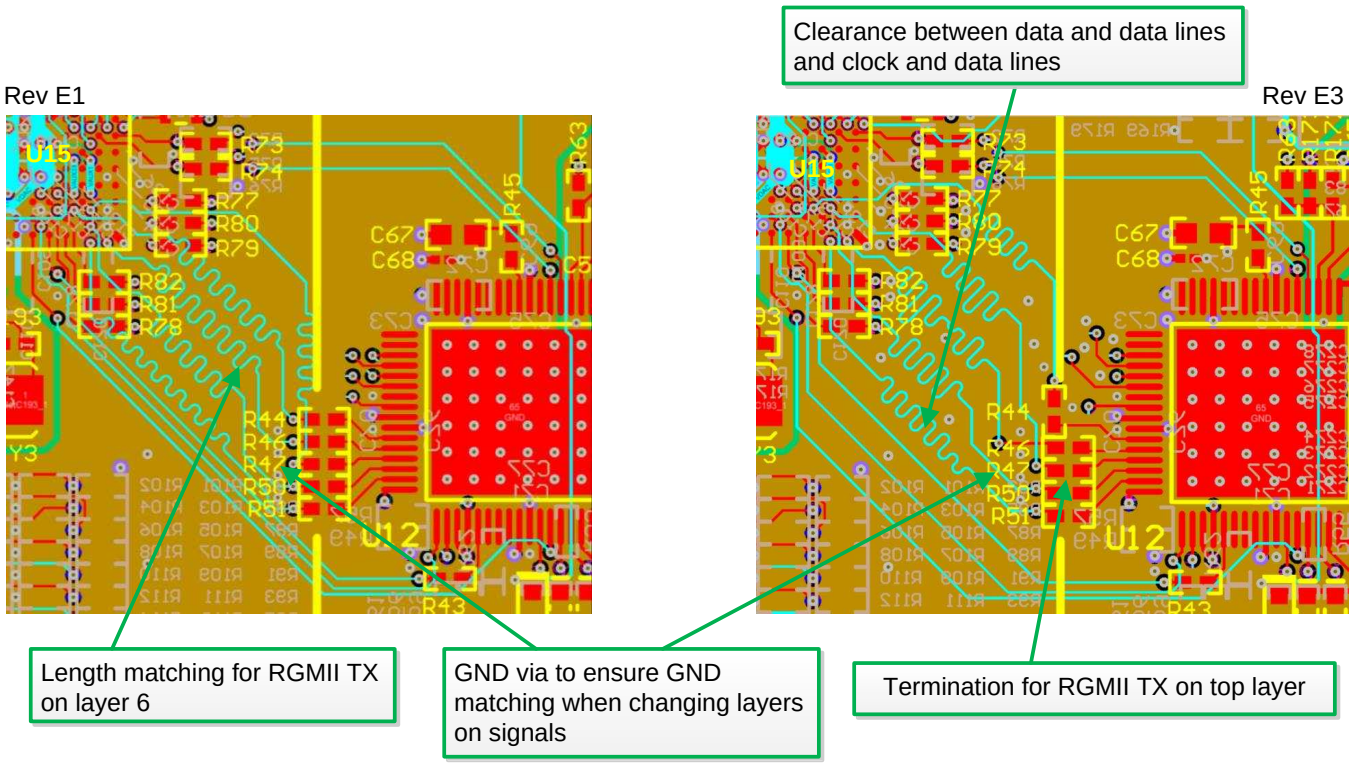


Figure 71. Layout Guidelines for RGMII TX Signals Comparing E1 and E3

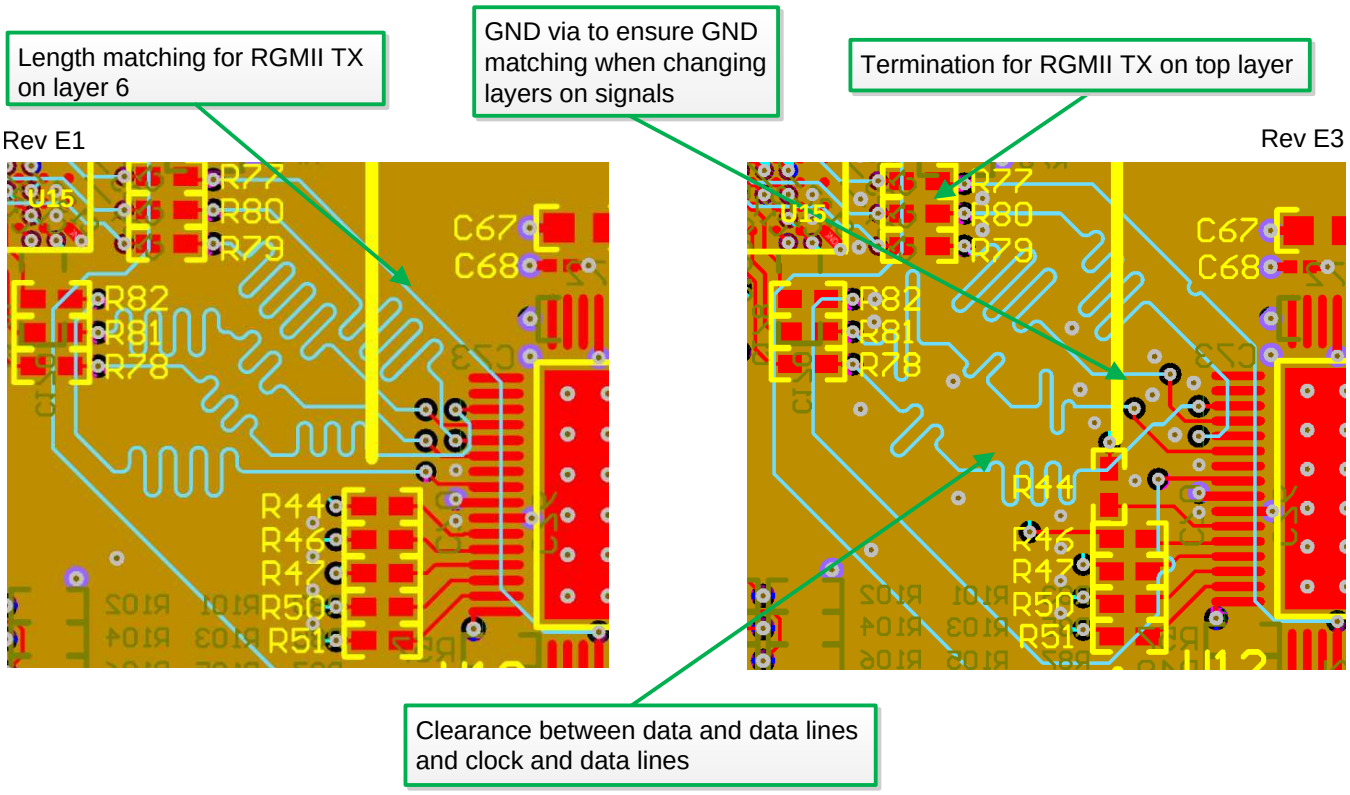


Figure 72. Layout Guidelines for RGMII RX Signals Comparing E1 and E3

6.4.3 Layout for Differential Gigabit Ethernet Signals

From the PHY to the magnetics the differential pairs are routed on the top layer with differential impedance control matching of 100 Ω. The reference GND is on mid layer 1. This is achieved by ensuring that isolation between top layer and mid layer 1 is smaller than the surrounding planes.

From the magnetics to the RJ45 the differential pairs A, C, and D are routed on the top layer while pair B is routed on mid layer 2. This is due to crossing the signals on the RJ45 Ethernet jack. Again, the differential pairs are impedance matched to 100 Ω with reference to GND on mid layer 1. Due to the GND being mid layer 1, there is no need for GND vias added around the B signal.

This routing achieves the minimum possible trace lengths from PHY to magnetics, magnetics to RJ45, and here a maximum delta of the trace lengths of 1 mm between the differential pairs.

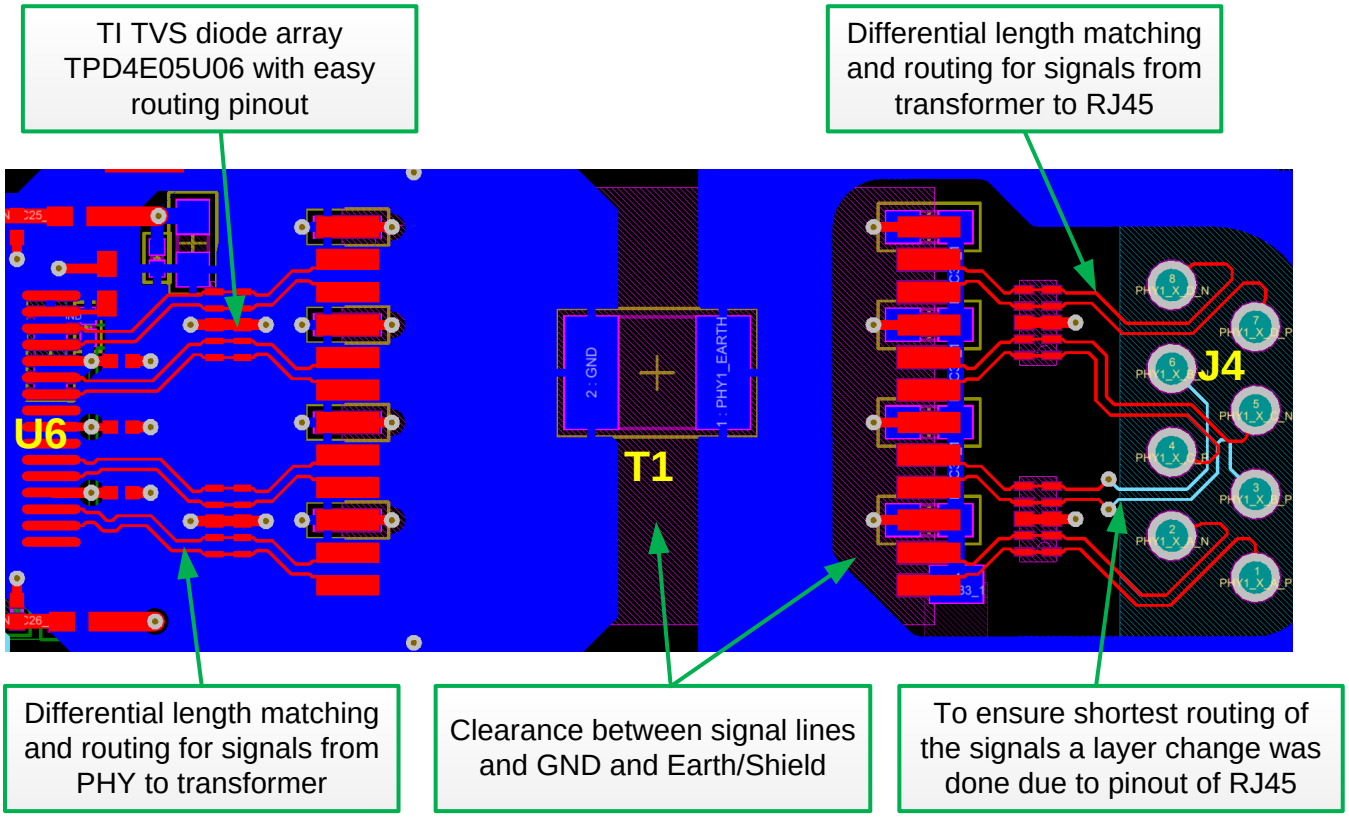


Figure 73. Layout Guidelines for PHY Differential Signals

6.4.4 Layout PHY Power Supply

For the 2.5-V LMZ rail, add a keep-out GND cut in mid layer 1 to decrease noise coupling. To additional thermal management, add as many vias as possible on the powerPAD of the 1.1-V and 1.8-V LDO and add an additional thermal release plane on the bottom side of the board.

Ensure wide enough traces when adding the 1.1-V and 2.5-V power rails. The 1.1-V rail is added as a solid supply plane below each PHY. Figure 74 shows the PCB layout of TIDA-00204.

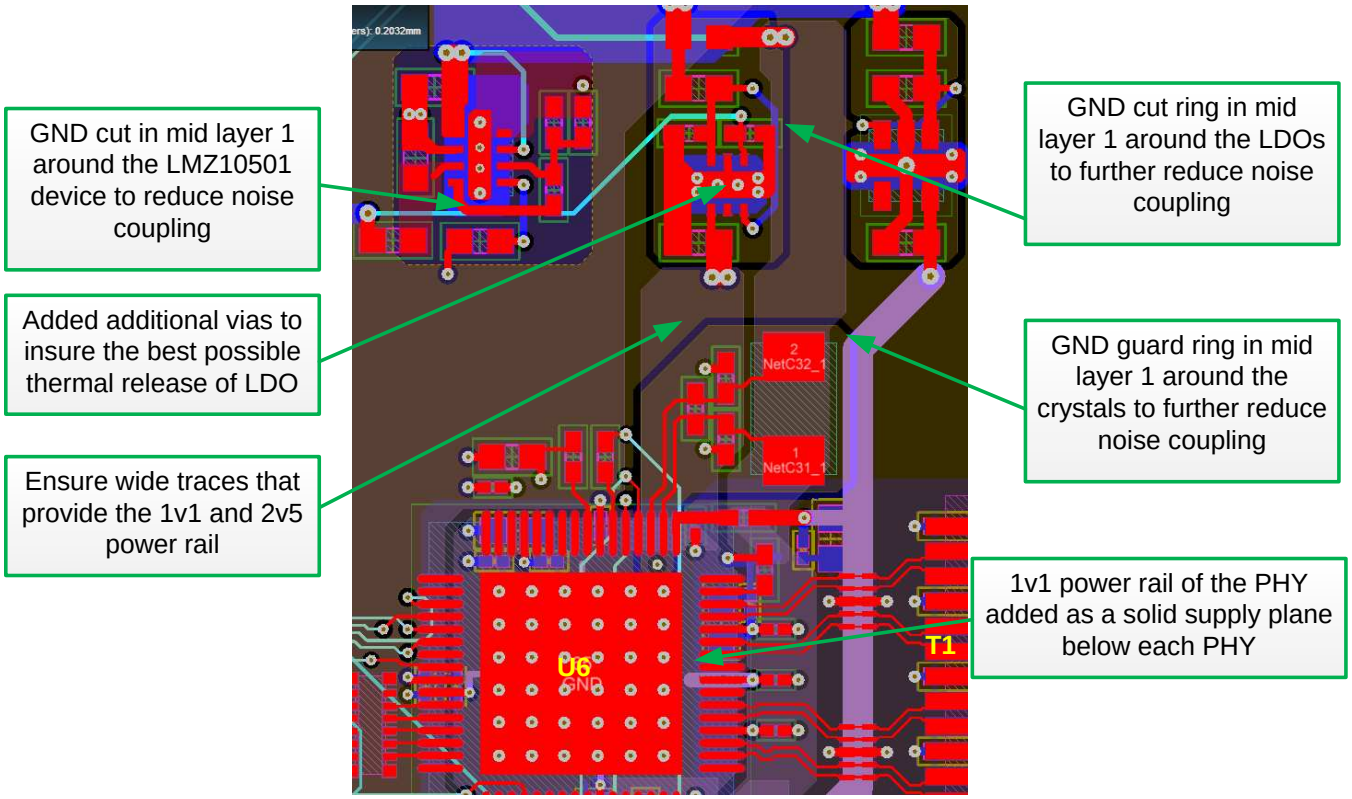


Figure 74. Layout Guidelines for PHY Power Supply

6.4.5 Layout of the 24-V to 5-V DC/DC Buck (LM46002)

Follow the layout guidelines from the LM46002 data sheet. Cut out layer 1 under LM46002 to avoid coupling into other layers. Ensure that current loop of the device is maintained as small as possible. The example layout of the LM46002 on TIDA-00204 is shown in Figure 75.

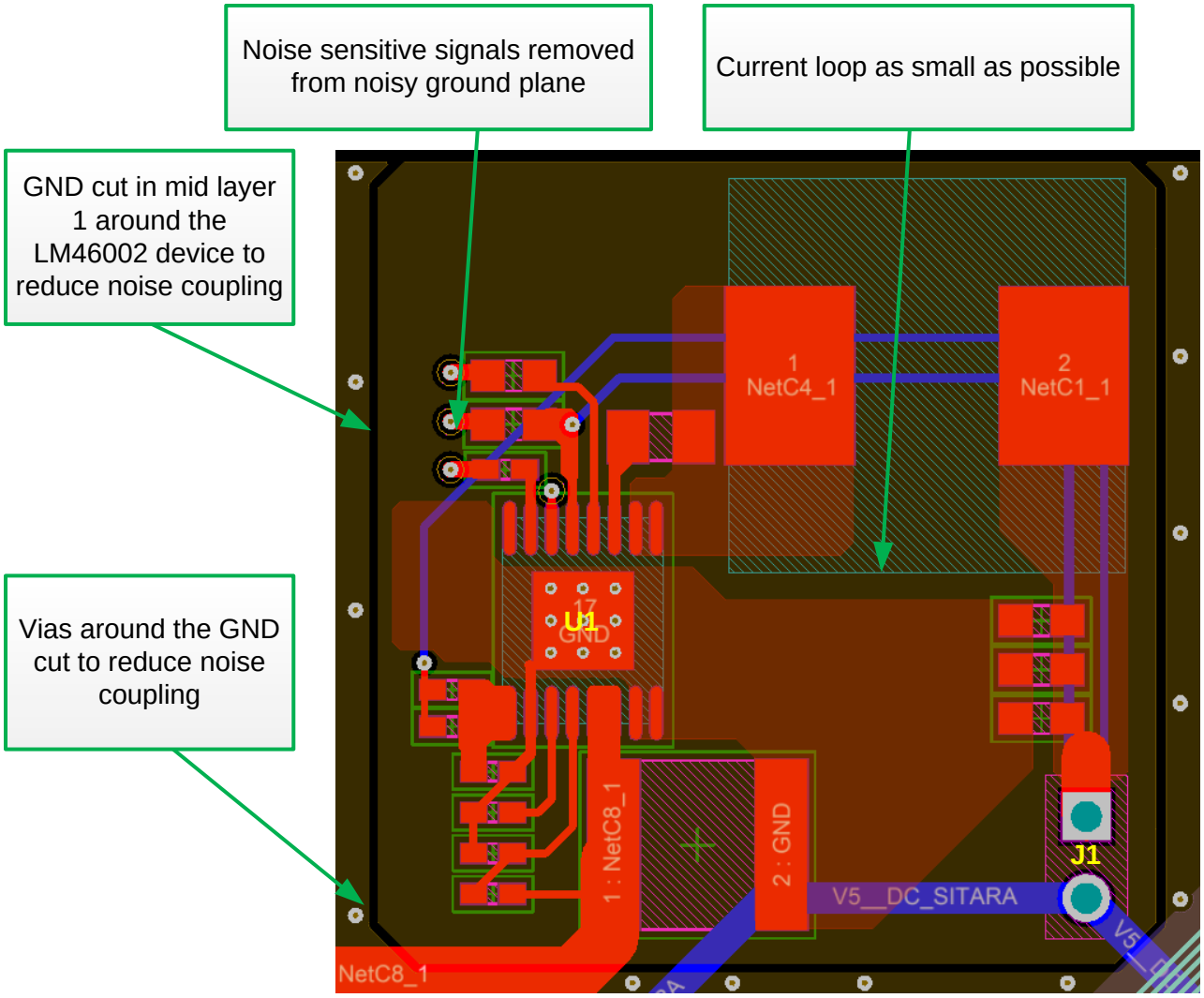


Figure 75. Layout Guidelines for 24-V to 5-V DC/DC Buck With LM46002

6.4.6 Layout Sitara Power Supply

For the Sitara power supply, the following guidelines were considered.

Routing the power tracks to the Sitara each power track as a GND plane as reference GND, mid layer 4 used as supply layer with supply planes for each high current power track. VMMC, VAUX33, and VAUX1 power track added in mid layer 2 and VDIG2 and VPLL power track added in mid layer 6.

VDAC intentionally does a u-trace as the DAC functionality is not used. If this functionality is needed, add additional traces for this power rail.

6.4.7 Layout DDR3

Layer 6 is GND reference for DDR3 (90-µm dielectric distance layer to layer). The other layers are 400 µm away. All DDR3 signals are on one layer.

6.5 Altium Project

To download the Altium project files, see the design files at TIDA-00204.

6.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00204.

7 Software Files

To download the software files, see the design files at TIDA-00204.

8 Related Documentation

1. Texas Instruments, *DP83867IR Robust, Low Power 10/100/1000 Ethernet Physical Layer Transceiver*, DP83867 Data Sheet (SNLS484)
2. Texas Instruments, *AN-1469 PHYTER Design & Layout Guide*, Application Report (SNLA079)
3. Texas Instruments, *EN55011-Compliant, Industrial Temperature 10/100-Mbps Ethernet PHY Brick*, TI Design (TIDU515)
4. Texas Instruments, *PCB Design Guidelines For Reduced EMI*, Application Report (SZZA009)
5. Texas Instruments, *High-Speed Interface Layout Guidelines*, Application Report (SPRAAR7)
6. Texas Instruments, *AM335x Sitara™ Processors*, AM335x Data Sheet (SPRS717)
7. Texas Instruments, *AM335x Sitara™ Processors*, AM335x Technical Reference Manual (SPRUH73)
8. Texas Instruments, *TPS65910Ax User's Guide For AM335x Processors*, TPS65910Ax User's Guide (SWCU093)
9. Texas Instruments, *TI Network Developer's Kit (NDK) v2.24*, NDK User's Guide (SPRU523)
10. Texas Instruments, Sitara Wiki Page (http://processors.wiki.ti.com/index.php/Sitara)
11. Texas Instruments, *AM3359 Industrial Communications Engine*, Evaluation Module, Part # TMDSICE3359 (http://www.ti.com/tool/tmdsice3359)
12. Texas Instruments, *LM46002 SIMPLE SWITCHER® 3.5 V to 60 V 2 A Synchronous Step-Down Voltage Converter*, LM46002 Data Sheet (SNVSA13)
13. IEEE, *802.3-2012 – IEEE Standard for Ethernet*, Section Three (http://standards.ieee.org)
14. HP, *Reduced Gigabit Media Independent Interface (RGMII) 4/1/2002 Version 2.0: Reduced Pin-count Interface for Gigabit Ethernet Physical Layer Devices* (http://www.hp.com/rnd/pdfs/RGMIIv2_0_final_hp.pdf)
15. Dirk S. Mohl, *IEEE 1588 Precision Time Protocol* (http://www.ieee1588.com)
16. CISPR11 / EN 55011+A1:2010-01-31, *EN 55011: Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement*
17. IEC, *Adjustable speed electrical power drive systems - Part 3: EMC requirements and specific test methods*, IEC 61800-3 ed2.0: 2004-08-12
18. IEC, *Amendment 1 - Adjustable speed electrical power drive systems - Part 3: EMC requirements and specific test methods*, IEC 61800-3-am1 ed2.0: 2011-11-14
19. Micron, *TN-41-08: Design Guide for Two DDR3-1066 UDIMM Systems*
20. Wireshark, v1.12.3 (http://www.wireshark.org)
21. TeraTerm, v4.76 (http://ttssh2.sourceforge.jp/)
22. GCD-Printlayout GmbH (http://www.gcd-printlayout.de/)
23. MinGW, *Minimalist GNU for Windows* (http://www.mingw.org/)
24. SourceForge, *Win32 Disk Imager* (http://sourceforge.net/projects/win32diskimager/)

8.1 Trademarks

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9 About the Authors

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (April 2015) to B Revision **Page**

- Added CDCE913 to *Resources* section 1
- Changed listed feature from "Hardware Support for Start of Frame (SOF) Detect Allows Implementation of IEEE 1588 PTP" to "Reduces Jitter and Phase Shift from Clocks by Using Clock Synthesizer to Generate System Clocks" 1
- Changed front-page board image to updated figure 1
- Changed front-page block diagram to updated figure 1
- Changed location of content from *TI Design Overview* section to *System Description* 2
- Changed title of *Design Features* section to *Key System Specifications* and moved under *System Description* 2
- Added new section hierarchy (*System Overview*) to house *Section 2.2.1*, *Section 2.2.2*, and *Section 2.2.3* 4
- Changed location of *Block Diagram* to under *System Overview* 4
- Changed *Figure 1* to updated block diagram 4
- Changed location of *Section 2.2.1*, *Section 2.2.2*, and *Section 2.2.3* to under *Design Considerations* 4
- Added new section *System Design Theory* 7
- Changed location of *Circuit Design and Component Selection* to under *System Design Theory* 7
- Changed number of MAC interface symbols for GMII from 24 to 25 10
- Changed *Table 7* to updated title *DP83867 RGMII Design Rules on TIDA-00204 PCB* and updated the listed rules and distances 10
- Changed *Figure 7* to updated schematic 11
- Added detail on clock option to sync all clocks using a clock distribution network for *DP83867IR Input Clock Selection* 12
- Added detail on clock option to sync all clocks using a clock distribution network for *AM3359 Clocking Options* 17
- Changed *Figure 17* to updated figure from *CDCE913 Clock Distribution Circuit Example* to *Crystal Phase Shift Diagram* 27
- Changed listed advantage of "Smaller component area used for clocking" to "High accurate clocking with minimum frequency and phase shift" 27
- Changed listed advantage of "Possibility to enable spread spectrum (SSC)" to "Smaller component area used for clocking" 27
- Changed *Figure 19* to updated image 28
- Added *Figure 20* 29
- Changed *Figure 30* to updated image 37
- Added *Figure 31* 38
- Added details about using the ping command during ping testing 51
- Deleted all embedded images from *Schematics*. Schematics have been updated; download the most recent from TI.com 68
- Deleted BOM table from *Bill of Materials*. BOM has been updated; download the most recent version from TI.com 68
- Deleted all embedded images from *Layer Plots*. Layer plot files have been updated; download the most recent from TI.com 68
- Changed *Figure 71* to updated image 69
- Changed *Figure 72* to updated image 70
- Added reference for *High-Speed Interface Layout Guidelines* 74

Changes from Original (March 2015) to A Revision **Page**

- Changed from preview page 1

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