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Isolated Current Shunt and Voltage Measurement for Motor Drives Using AM437x

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TIDA-00171	Tool Folder
AMC1304M05	Product Folder
AMC1304M25	Product Folder
SN6501	Product Folder
TPS7A3001	Product Folder
TLV70450	Product Folder
OPA211AI	Product Folder
INA826	Product Folder
CDCLVC1108	Product Folder
AM437x	Product Folder

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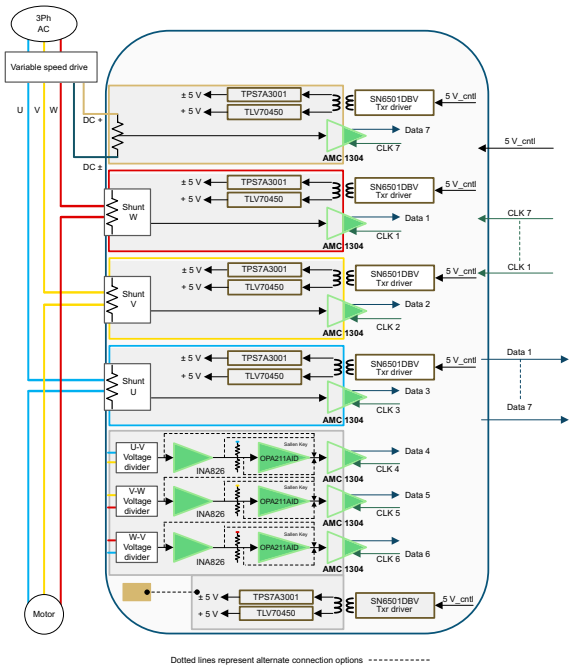
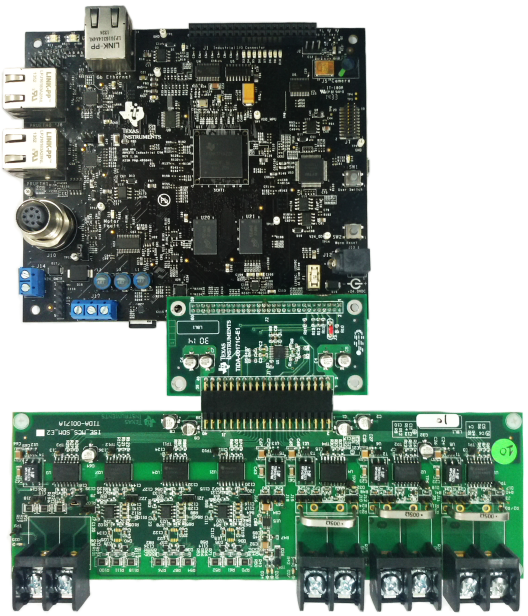
Design Features

- Isolated Shunt Feedback Measurements of Three-Phase Motor Currents and Voltages Using Isolated Delta-Sigma Modulator AMC130x
- Sinc3 Digital Filters on AM437x Sitara™ ARM® Cortex®-A9 Processor Using PRU-ICSS
- Calibrated Accuracy of ±0.2% at 25°C
- <4-µS Response Time for Short Circuit Protection Using Sinc3 Filter and OSR of 16
- Option of Powering Board from Bootstrap Power Supply from Inverter for System Level Testing
- Onboard Isolated Power Supply 5 to 3.3 V for Biasing AMC130x
- Run-Time GUI for Complete Performance Analysis of Modulator Clock, Sinc Filter Parameters, and Current and Voltage Waveforms

Featured Applications

- AC Motor Drives
- Uninterruptible Power Supplies
- Solar Inverters





1 System Description

This reference design implements the AMC130x reinforced isolated delta-sigma modulators along with the AM437x Sitara ARM Cortex-A9 Processor, which implements Sinc filters on PRU-ICSS. This design provides an ability to evaluate the performance of these measurements: three motor currents, three inverter voltages, and the DC Link voltage. This reference design provides firmware to configure the Sinc filters, set the modulator frequency, and receive data from Sinc filters. The design also provides a versatile run-time GUI to help the user validate the AMC130x performance and supports configuration changes to Sinc filter parameters in the Sitara processor.

Government regulations around the world are calling for higher efficiency of industrial motor drives because they account for a considerable amount of our total energy consumption. Higher efficiency requires optimization of the torque and rotor speed depending on the actual demand of the system, which can be achieved in part by increasing the accuracy of the motor current and voltage measurements.

Current measurement is an inherent part of any inverter-driven application. For speed and torque control in electrical drive systems, the converter output current has to be captured for online calculation of the PWM pattern. The current loop regulator typically works between 1 and 8 kHz. The signal used for this control loop must contain information from 10 to 40 kHz with a required resolution from 12 to 16 bits.

To increase the reliability and reduce the cost of the drive, a great effort has been made to eliminate the shaft speed or position sensor in most high performance induction motor drive applications. Rotor-speed estimators for induction motor drives use stator voltage and current measurements along with motor parameters for estimation. Dynamic performance of induction motor field-oriented controllers strongly depends on model parameter accuracy, which again depends on the measurement accuracy.

Both motor control and grid applications use the rotating reference frame to control currents in the so-called d–q rotating coordinate system. Regulation of the currents of the d and q axes requires at least two phase current measurements. The current components become quasi-DC and the control are simplified to a low requirement in bandwidth. The more accurate current and voltage measurements improve the performance of motor drives by reducing torque ripple on the motor shaft.

One industry trend that is gaining more traction is to use delta-sigma modulation for measuring current and voltage levels. The primary reason for this shift is that delta-sigma modulation reduces overall system cost while providing high performance.

Traditionally, Hall Effect sensors are used for the current and voltage measurement as they offered important electrical isolation. The Hall Effect sensor can be replaced with a current shunt resistor and isolated delta-sigma modulator, a more accurate and less expensive option, and provide direct measurement of current and voltage. A delta-sigma modulator converts an analog input signal into a high-frequency stream of single bits with out-off band noise. The advantage of moving the quantization noise to higher frequency bands include simple anti-aliasing filtering, low-cost solution by eliminating cost on drivers, and filters and scalable performance.

TI's latest isolated delta-sigma modulator, the AMC130x, is designed specifically for direct connection to current shunt resistors and has a galvanic isolation barrier. The AMC130x is a second-order, delta-sigma modulator that is reinforced and isolated, which is ideal for motor control. The device has two variants with 50-mV and 250-mV inputs. A 50-mV variant is used to measure current, and a 250-mV variant is used to measure voltage. By having a low-input voltage of 50 mV, the power dissipation in the shunt resistor can be reduced significantly. A block diagram of the new approach is shown in Figure 1 and Figure 2.

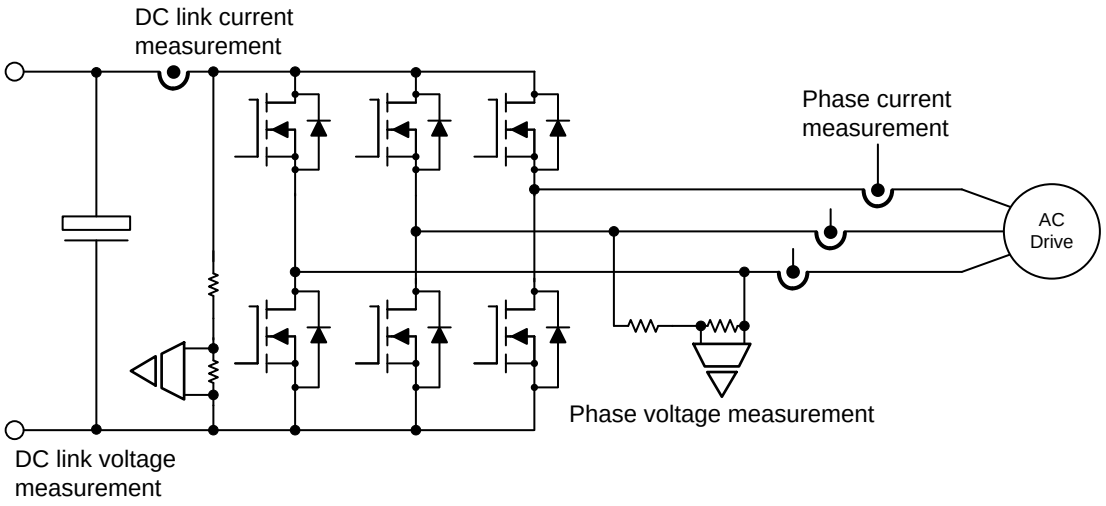


Figure 1. Current and Voltage Measurements in Three-Phase Inverters

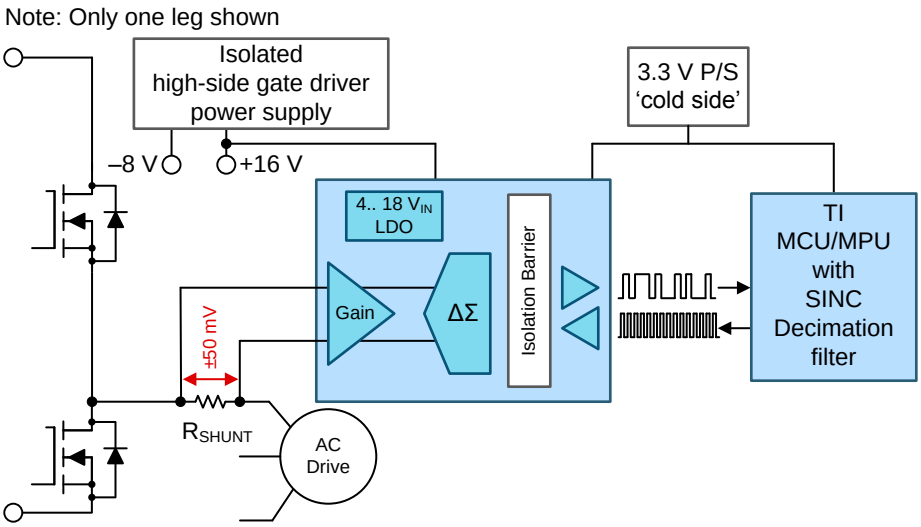


Figure 2. Delta-Sigma Modulator in Three-Phase Inverters

In motor control, up to eight signals need to be monitored. Therefore, it is most important to keep the costs for the sensors and their analog-to-digital conversion low. The cheapest method to measure currents is adding a resistor (shunt) into the current path and to measure the voltage drop across the resistor. A delta-sigma modulator is used to convert this voltage drop into a bit-stream. The AMC130x converts the shunt voltage (equal approximately current) across the shunt resistor into a digital high frequency (20 MHz) bit stream, which can be filtered using Sinc3 filter built into TI Delfino controllers. Similarly, a cost-effective method for measurement of the DC Link or inverter voltage is to use a resistive divider to step down the voltage to a level acceptable by the delta-sigma modulator.

When measuring current by using shunts, the user can minimize the power loss (P = I × V) in the shunt by using the AMC1304M05 with a ±50-mV input. Hence the voltage drop across the shunts remains as small as possible. The AMC1304 delta-sigma modulators are very robust in respect to noise and offset. Even such low voltages can be converted to high resolutions. Also, the shunt and the modulator are often at a floating potential, so that the digital output (bit-stream) of the modulator must be galvanically isolated. The AMC1304 has reinforced isolation, which provides the galvanic isolation for functioning of the application and required safety aspect to protect the user. The bit-stream is a two-wire interface, a data and clock signal. A high-resolution signal is extracted from the bit-stream with an appropriate low-pass filter – $Sinc^K$ filters. The filter structure can be adjusted to the applications needs in respect of resolution and speed.

See Section 1.2 and 1.3 of the TIDA-00171 design guide *Isolated Current Shunt and Voltage Measurement Kit* for explanations of the AMC130x and Sinc filters [1].

This reference design based on AMC130x along with Sitara AM437x processor provides ways to measure currents and voltage:

- Three motor currents
- DC Link voltage
- Three inverter voltages (phase and line voltages)

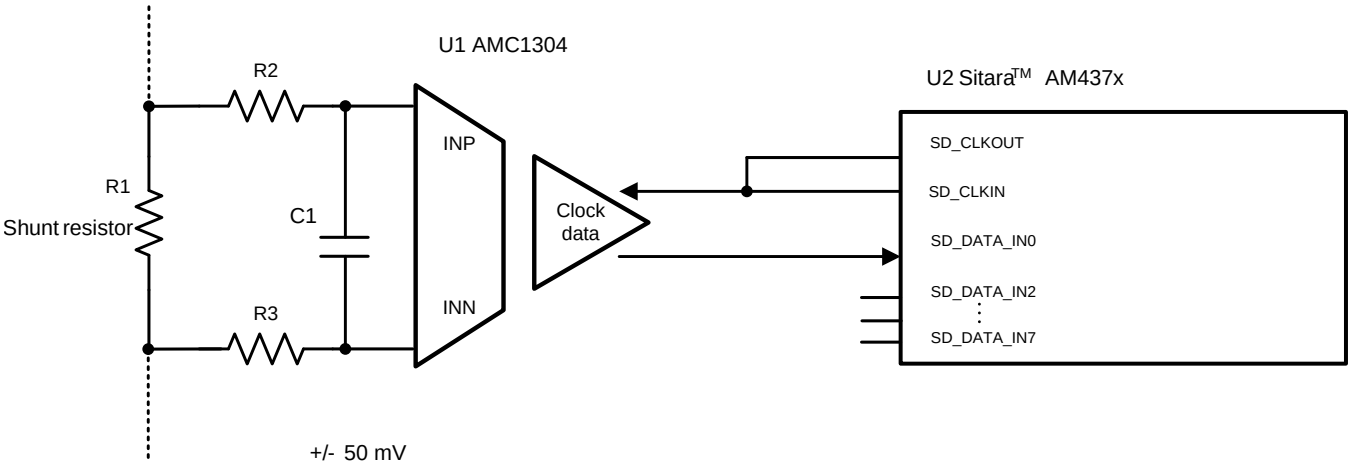


Figure 3. Current Measurement Using AMC130x and Sitara AM437x Processor

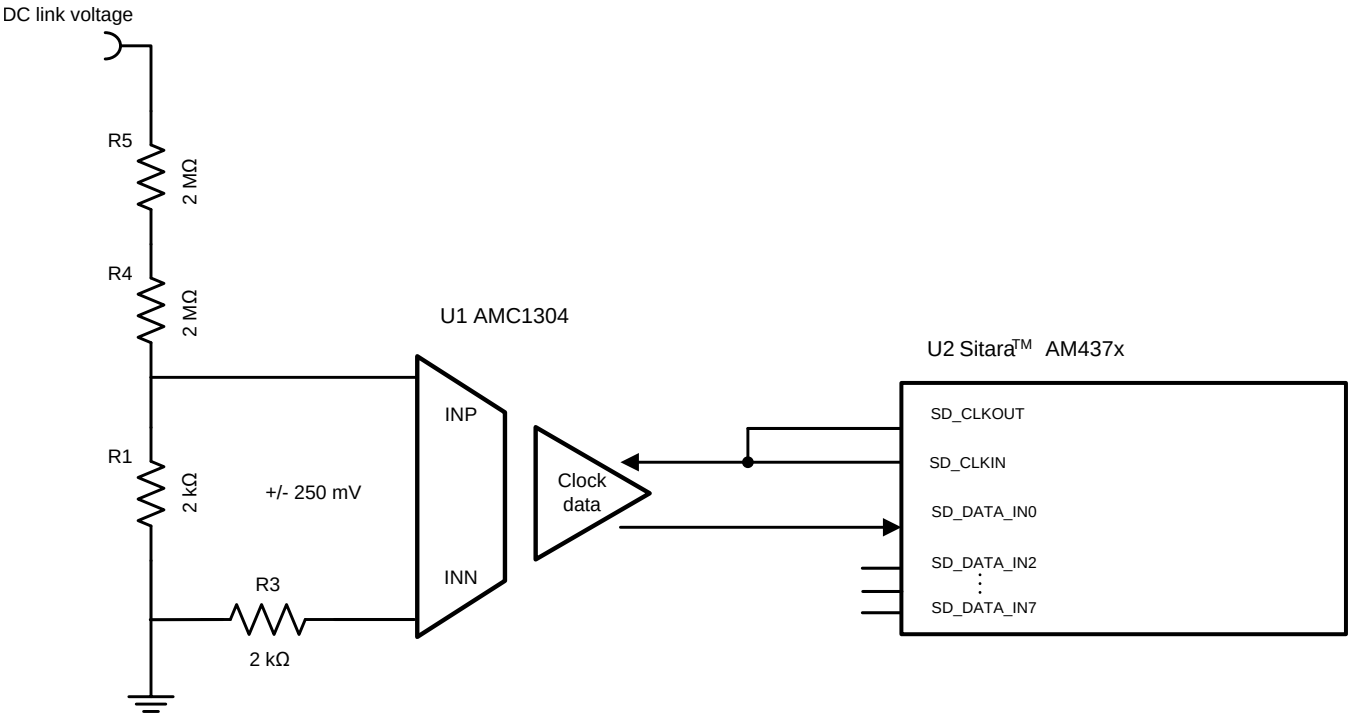


Figure 4. Voltage Measurement Using AMC130x and Sitara AM437x Processor

2 Design Features

The following are the design specifications of the Isolated Current Shunt and Voltage Measurement for Motor Drives Using AM437x reference design.

Table 1. TIDA-00209 Design Specifications

PARAMETER	SPECIFICATION AND FEATURES
Measurement parameter	Three-phase motor currents
	Three-phase inverter voltage
	DC Link voltage
	(Seven total channels)
Current	7 A_{RMS}
Voltage	550-V DC for DC Link measurement 390-V AC for inverter voltage measurement
Measurement accuracy, post calibration	±0.2% over the temperature range: –25°C to 75°C
Resolution	16-bit
Module calibration	Offset and gain calibration for entire signal chain. Calibrated to remove error due to solder joint resistance and error due to shunt resistor variation
Isolation	Reinforced, IEC60747-5-2
Operating temperature range	25°C to 75°C
Modules	Delta-sigma module, adaptor card, AM437x industrial development kit; These three boards are integrated by appropriate board-to-board connectors.

3 System Configuration and Block Diagram

Implementation of the current and voltage measurement system has been split into three boards: the AM437x industrial development kit (IDK), an adaptor card, and a delta-sigma module (DSM). The DSM has been described in detail in the TIDA-00171 design guide *Isolated Current Shunt and Voltage Measurement Kit*, which is reused in this design [1].

1. The AM437x IDK incorporates the AM437x Sitara processor. The IDK is a self-contained EVM for the AM437x Sitara processor with on-board memory, power supplies and power management.
   - A 24-V input is stepped down using buck convert to generate all power rails required for the AM437x processors and memory. The 5 V and 3.3 V generated are tapped to supply the other boards in the circuit.
   - An onboard XDS100V2 for JTAG connection using a micro USB connector. The XDS100V2 also provides a UART connection to the Sitara processor, used to provide communication to the GUI.
   - The IDK supports various expansion headers interfacing with other boards. A 2×30 header is used to interface to the adapter card.
2. The DSM comprises of the entire signal chain for current and voltage sensing. The board has three channels for motor current sensing, three channels for inverter voltage sensing, and one channel to measure the DC Link voltage. Each of the channels is provided with ESD protection diodes and a low-pass RC filter. The filtered signal is converted into a one-bit modulated stream by the AMC130xM05 (±50-mV max input) or AMC130xM25 (±250-mV max input). This bit stream is then demodulated by a Sinc filter implemented within the Sitara processor on the IDK.
3. An adaptor card is used to connect the AM437x IDK and DSM. The adaptor card is used to route signals between the two boards. A fan-out clock buffer is used to generate seven clocks from a single clock generated from the processor. The adaptor board also has bulk capacitors for the 5-V and 3.3-V power rails.

The three PCBs are integrated by the board-to-board connectors form the Isolated Current Shunt and Voltage Measurement Kit as shown in Figure 5.

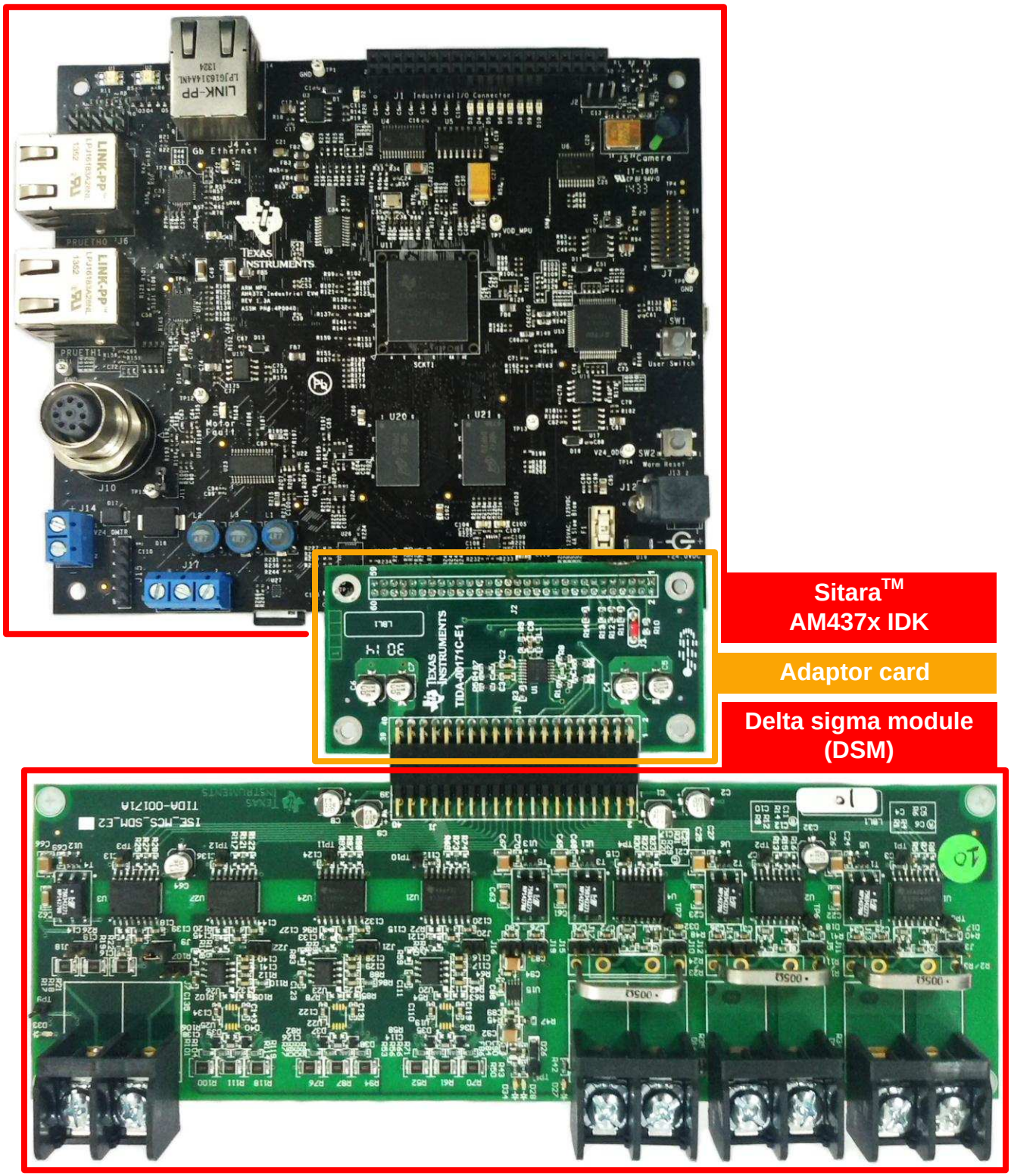


Figure 5. Picture of Isolated Current and Voltage Measurement Kit

3.1 DSM Board

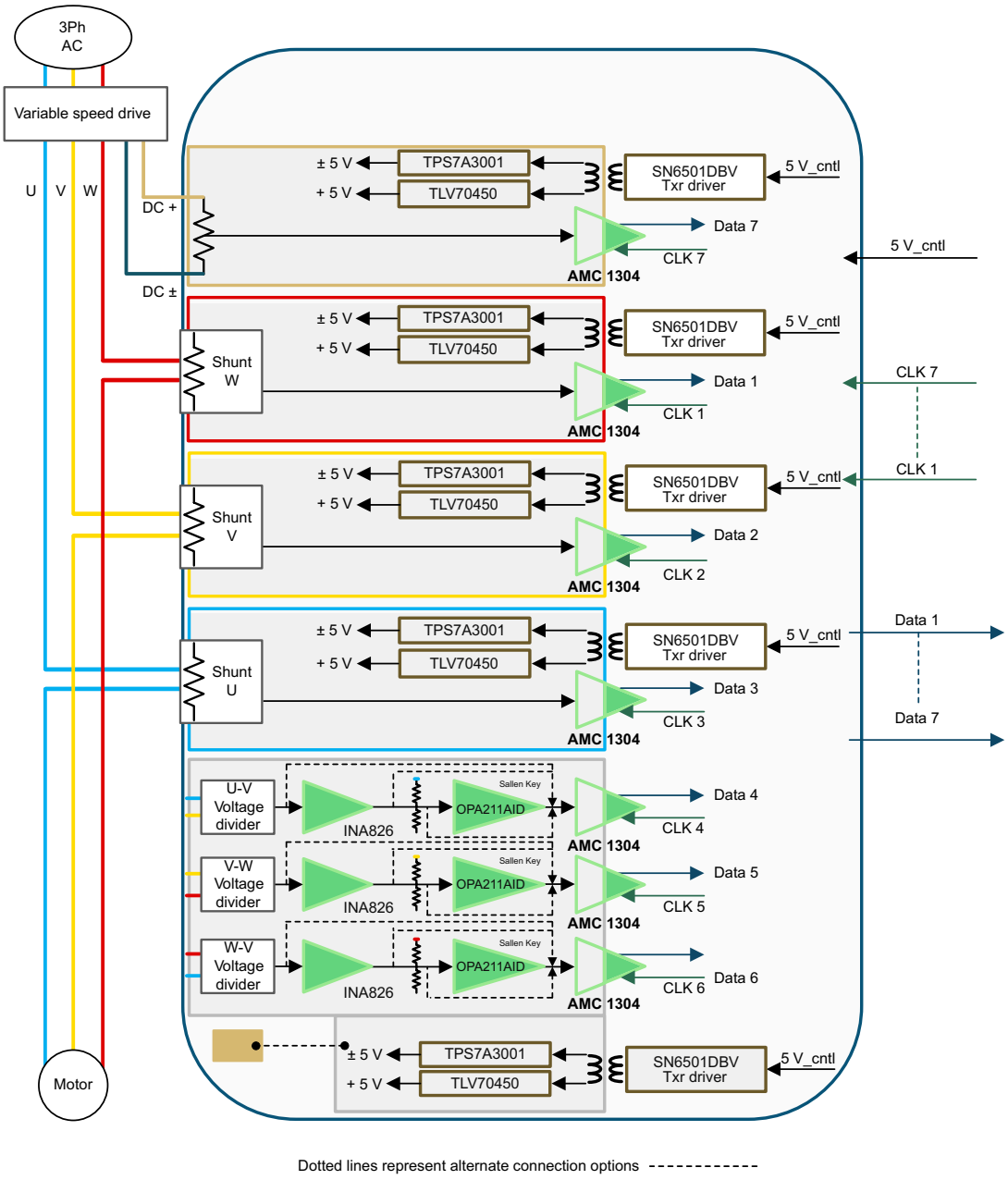


Figure 6. Block Diagram of DSM

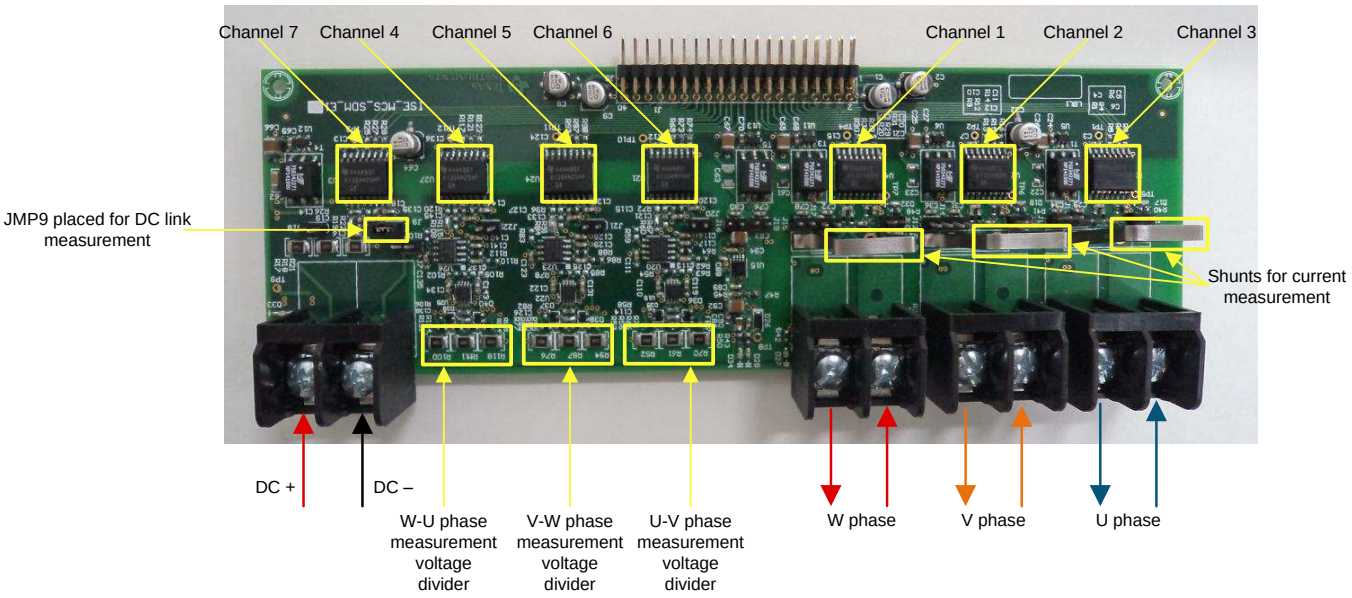


Figure 7. DSM Board

The DSM board features the following:

- *Isolated Power Supply*: As shown in Figure 6, five isolated DC power supplies power the high side of the AMC1304. Each of the three current channels is provided with separate isolated 5-V and –5-V DC converters. Options are also provided to power the AMC130x device using gate-drive power supplies. The AC voltage measurement channels are provided with a common isolated 5-V DC. The DC Link voltage measurement channel has its own isolated 5-V DC power supply.
- *Inverter Measurements*: The AC motor is driven from a three-phase inverter. The inverter voltage and motor current are measured by the isolated delta-sigma convertor AMC130xM25 and AMC130xM05. Each of the seven AMC130x isolated digital output (DOUT) converters of the modulator provide a stream of digital ones and zeroes that is synchronous to the clock source, provided at CLKIN pin, with a frequency in the range of 5 to 20.1 MHz. The time average of this serial bit-stream output is proportional to the analog input voltage.
  - *Inverter Voltage Measurement*: The PWM output voltages on the U, V, and W lines are scaled down through resistive dividers and then filtered for attenuating the noise. Options are provided to include or bypass an additional Sallen-Key filtering. The filtered output is provided to each of the three AMC1304M25 devices. The Sallen-Key filter attenuates frequencies above 20 KHz. This device can measure up to ±250 mV, which corresponds to 389-V_{RMS} of phase-to-phase AC voltage. For a wider range, the potential divider circuit needs to be modified accordingly.
  - *Motor Current Measurement*: The currents through motor windings are measured as voltage across 5-mΩ shunts. This voltage is then measured by the AMC1304M05. This device can measure up to ±50 mV, which corresponds with up to 7-A_{RMS} AC current. For a higher measurement range, reduce the shunt resistance accordingly.

    NOTE: The accuracy of the shunt and the PCB layout are critical factors in the overall measurement accuracy. Use a four-wire shunt for a highly accurate system.

  - *DC Link Voltage Measurement*: The DC Link voltage is stepped down to 250 mV through a resistive divider and is measured using AMC130xM25s. The maximum DC voltage that can be measured is ±550-V DC.
- *Connectors*: The DSM board has connectors to interfaces with the adaptor board as well as with the drive and motor. Jumpers provide some specific, optional functions. The footprint of connectors is as highlighted in Table 2.

Table 2. DSM Board Connectors

CONNECTOR ON DSM	FUNCTION	CONNECTOR TYPE
J1	DSM to adaptor card	2×20 pins, right angle, female, board-to-board
J2, J4, J8	U,V,W inputs or outputs	4×1, terminal block, 2.54-mm pitch
J6	DC Link input	4×1, terminal block, 2.54-mm pitch
J3, J5, J9, J10, J20, J21, J22	Jumper to connect AVDD pin of the AMC1304 to external AVDD (gate drive power supply)	2 pin, male header
J11, J12, J13, J14, J15, J16, J17, J18, J19	Jumper to enable or disable the isolated ±5 V to the corresponding LDOs	2 pin, male header

3.2 Adaptor Card

An adaptor card is needed to connect between the IDK and the DSM board. This card routes signals from the IDK available on a 2×30-pin connector and DSM board interface on a 2×20-pin connector. Also, the board routes buffer the clocks and has the bulk capacitors for the 5-V and 3.3-V power rails.

3.3 AM437x IDK

The AM437x IDK is an application development platform for evaluating the industrial communication and control capabilities of Sitara AM4379 and AM4377 processors for industrial applications.

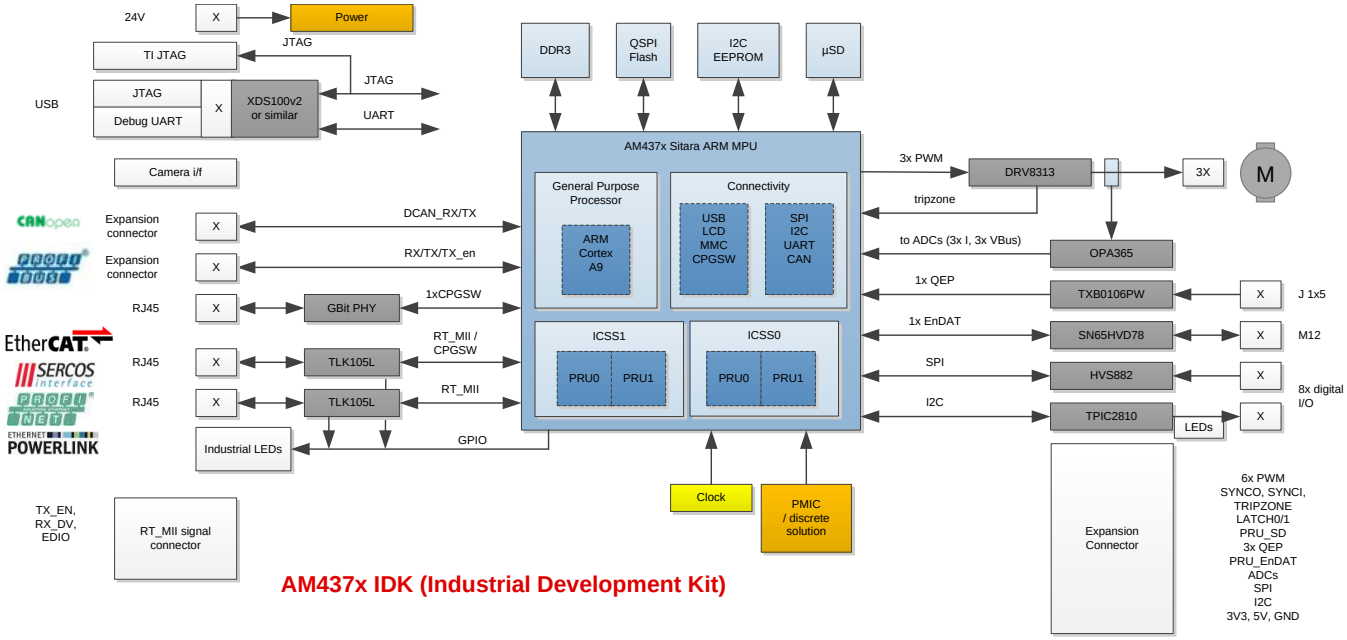


Figure 8. Block Diagram of AM437x IDK

The AM437x IDK features:

- Connectivity: The IDK supports many connectivity options used in motor drives like EtherCAT®, EnDat 2.2 BiSS, PROFINET, CANOpen, PROFIBUS®, POWERLINK, Ethernet/IP, SERCOS III, and IEC61850
- Position encoder interface
- Three-phase motor driver
- microSD card: used to store the application software
- Onboard Isolated JTAG Emulation: the JTAG interface supported by the onboard XDS100V2 emulator is used for a convenient interface with Code Composer Studio™ (CCS). The XDS100V2 also interfaces with the AM437x UART, which connects to the GUI.
- Multiple expansion headers: breakout for digital inputs and outputs (I/O), PWM, SPI, and sigma-delta decimation filter

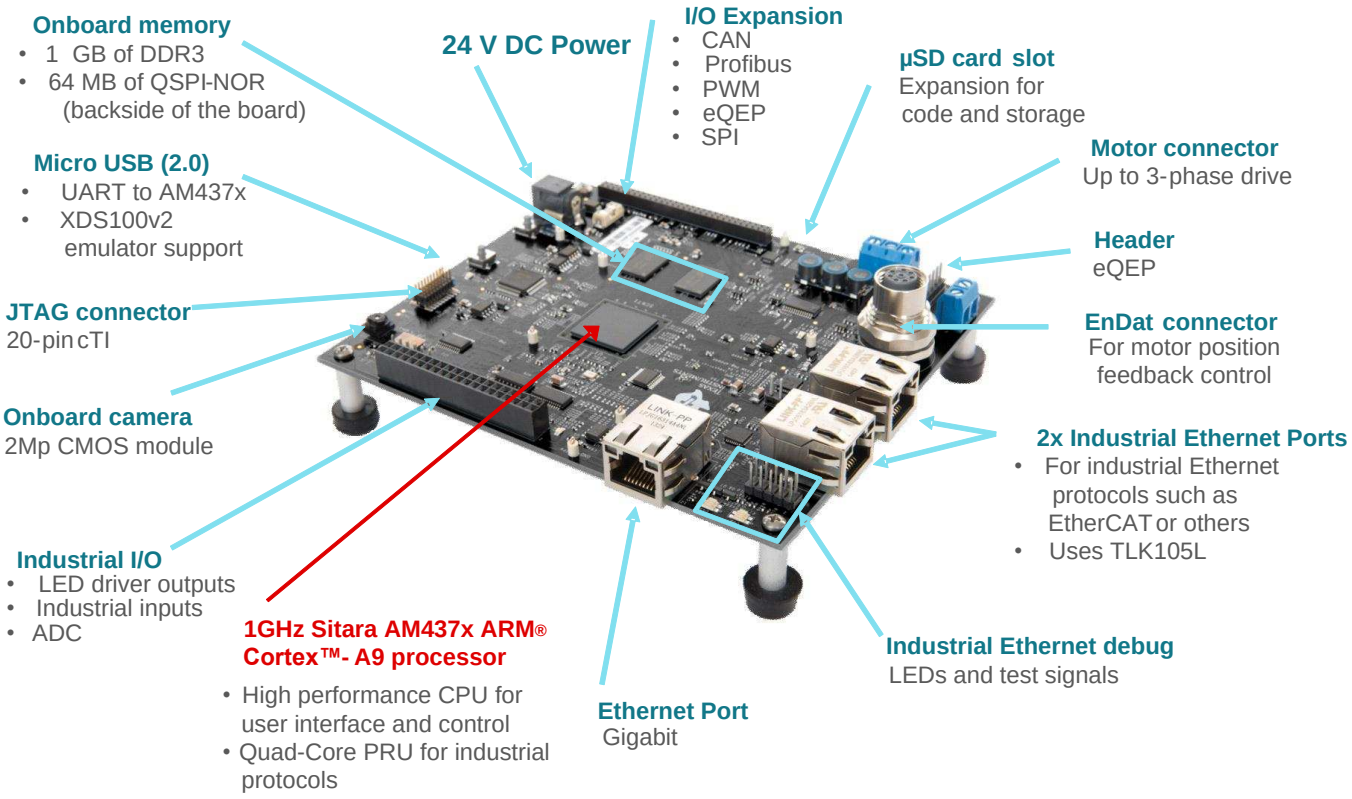


Figure 9. AM437x IDK

4 Circuit Design and Component Selection

The circuit design of the DSM board used in this design has been explained in Section 4.1 of the *Isolated Current Shunt and Voltage Measurement Kit* design guide [1].

4.1 Adaptor Card

The adaptor card is used to interface the AM437x IDK with the DSM.

4.1.1 Clock Buffer CDCLVC1108

The AM437x generates one clock, which is available on the header J2 of the adaptor card. This clock needs to be fed to seven AMC130x devices. A clock buffer is selected to provide the required source and sink currents. The CDCLVC1108 is a high-performance, general-purpose clock buffer that can supply up to eight outputs. This part belongs to CDCLVC11xx family of devices. The CDCLVC11xx family has low-jitter and low-skew LVCMOS fan-out buffer outputs.

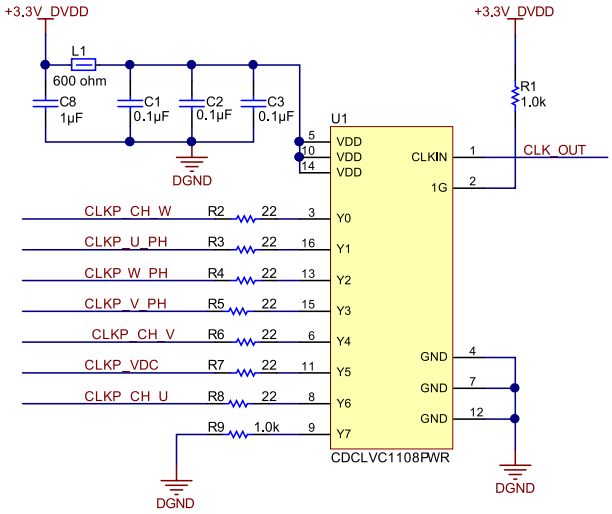


Figure 10. Clock Buffer

The power supply to the clock buffer has bulk capacitors and bypass capacitors. Bulk capacitors eliminate the low-frequency noise from the power supply, and the bypass capacitors provide the very low-impedance path for high-frequency noise and guard the power supply system against fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). The bypass capacitors are placed close to the power supply terminals. Also, a ferrite bead is placed between the board power supply and the chip power supply to isolate the high-frequency switching noises generated by the clock buffer; this bead prevents the switching noise from leaking into the board supply.

4.1.2 Connectors

The adaptor card routes the signals from the DSM card to AM437x IDK.

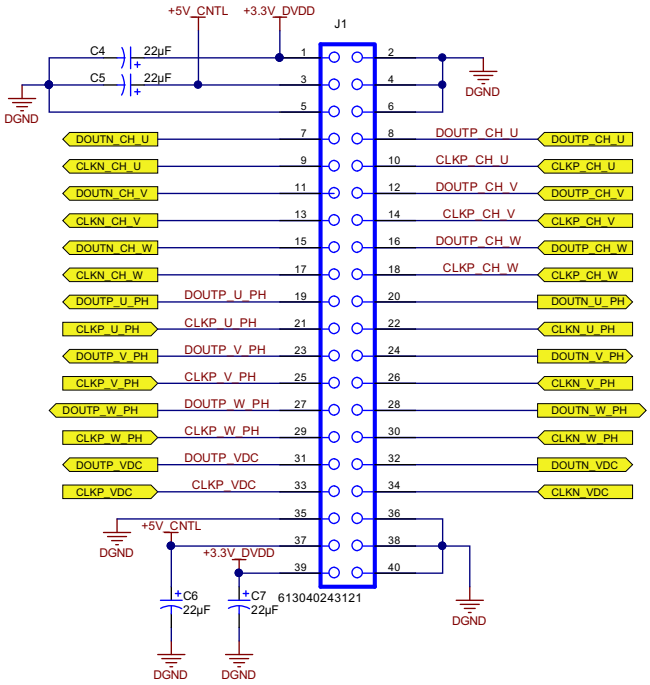


Figure 11. 2×10 Connector Interface With DSM Board

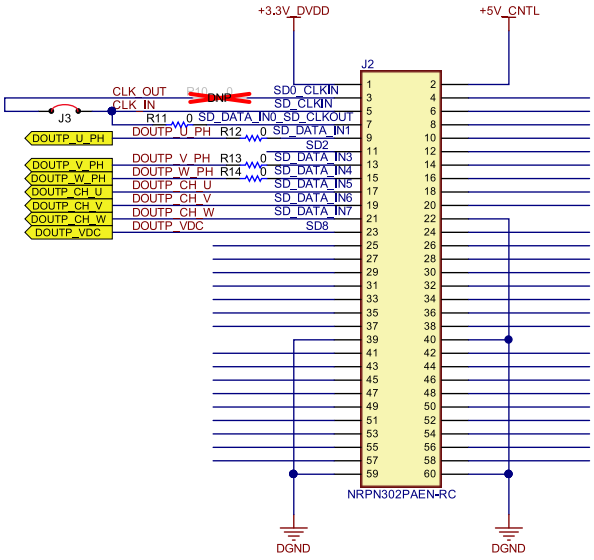


Figure 12. 2×30 Connector Interface With AM437x IDK

Table 3. Signal Mapping From DSM Board to AM437x IDK

GUI CHANNEL	SIGNAL NAME ON DSM BOARD	SIGNAL ON CONNECTOR J1	SIGNAL NAME ON AM437x CONNECTOR	SIGNAL ON CONNECTOR J2
Channel 6	DOUTP_U_PH	J1.19	SD_DATA_IN1	J2.9
Channel 5	DOUTP_V_PH	J1.23	SD_DATA_IN3	J2.13
Channel 4	DOUTP_W_PH	J1.27	SD_DATA_IN4	J2.15
Channel 3	DOUTP_CH_U	J1.8	SD_DATA_IN5	J2.17
Channel 2	DOUTP_CH_V	J1.12	SD_DATA_IN6	J2.19
Channel 1	DOUTP_CH_W	J1.16	SD_DATA_IN7	J2.21
Channel 7	DOUTP_VDC	J1.31	SD8	J2.23
—	CLK_OUT		SD0_CLKIN	J2.3
—	CLK_IN		SD_CLKIN	J2.5
—	CLK_IN		SD_DATA_IN0_SD_CLKOUT	J2.7

4.2 Sitara AM437x Processor

The Sitara AM437x processor family is based on the powerful ARM Cortex-A9 Core. Figure 13 shows the block diagram of the processor and integrated peripherals. It integrates a quad-core programmable real-time unit (PRU) that has been designed to implement deterministic, real-time processing of industrial communication protocols such as EtherCAT, PROFIBUS, and position encoder interfaces like EnDat2.2, BiSS, and sigma-delta demodulator interfaces. This make AM437x processors ideal for industrial communications, industrial control, and industrial drives applications. The processor has a rich peripheral set for industrial interfaces, motor control, graphics, and security. The device can boot from various sources including QSPI, NAND. The JTAG interface all cores including PRUs, the PRU can be debugged using CCS. Parallel debug of ARM and PRUs is supported. The reference document for AM437x can be found at http://www.ti.com/product/AM4379.

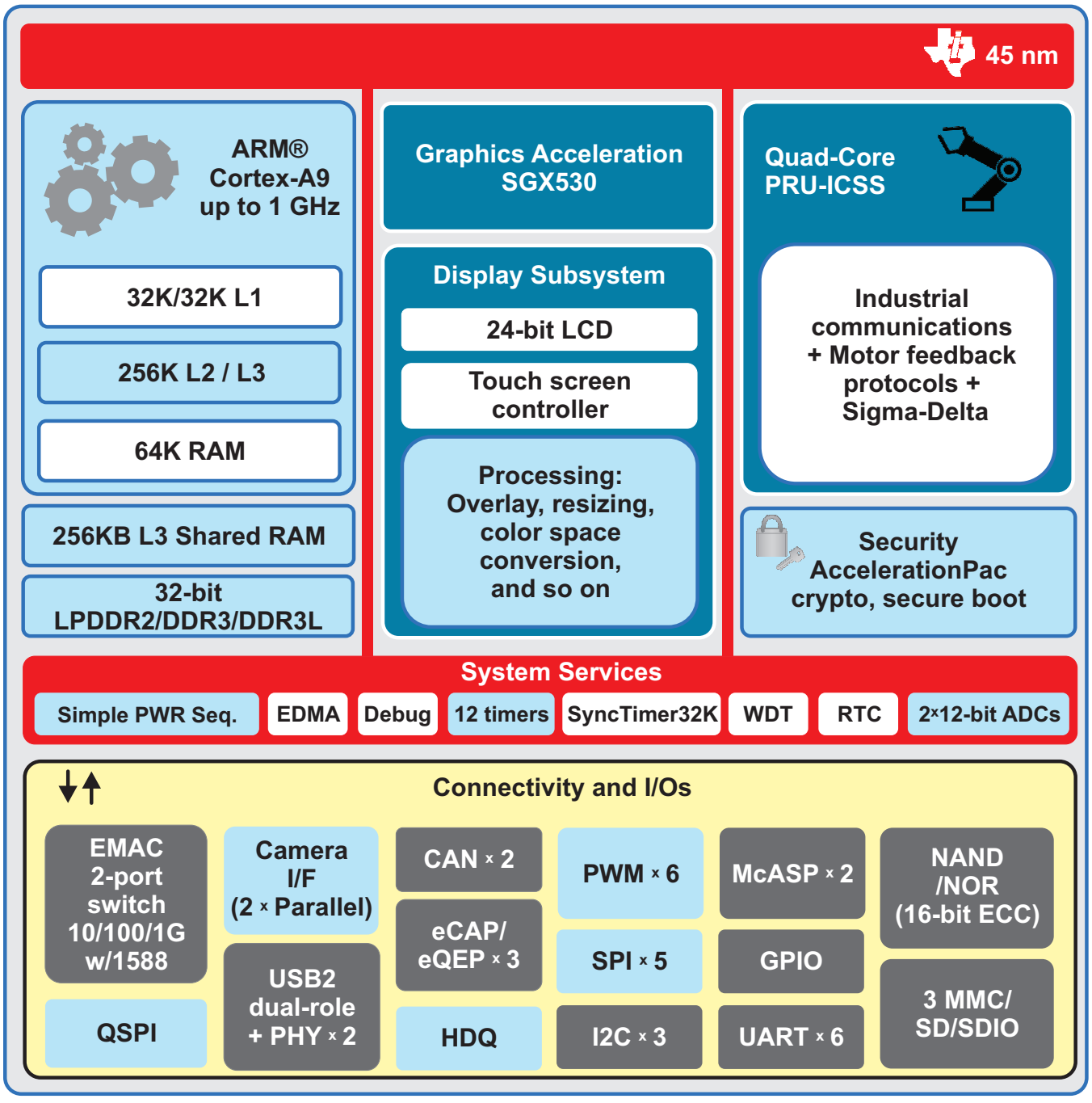


Figure 13. AM437x Functional Block Diagram

4.2.1 PRU-ICSS

The programmable real-time unit (PRU-ICSS) is a separate processing unit from the ARM core. The PRU can operate independent of the ARM core after initialization. Also, the PRU is clocked independently for greater efficiency and flexibility and can be used for offloading tasks from ARM. Alternatively PRU-ICSS can be used to implement additional peripheral interfaces and real-time protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink, Sercos3, EnDat2.2, and sigma-delta de-modulator. The PRU core runs at a 200-MHz frequency and each PRU instruction takes 5 ns to execute. This feature makes the PRU perfect for implementing real-time communication and control systems. Each PRU core has its own instruction and data memory, have access to all parts of SoC, pins and can talk to all memories and I/Os except ARM CPU memory, interrupt ARM and receive events from ARM. The PRU can interact with other processors as defined by the firmware loaded into instruction memory. Two ICSS blocks (each with two PRU cores), namely ICSS0 and ICSS1, are available for industrial Ethernet and motor side communication. The block diagram of both PRUs is shown in Figure 14. For more details on PRU-ICSS, refer to the *AM437x ARM Cortex-A9 Processors Technical Reference Manual*.

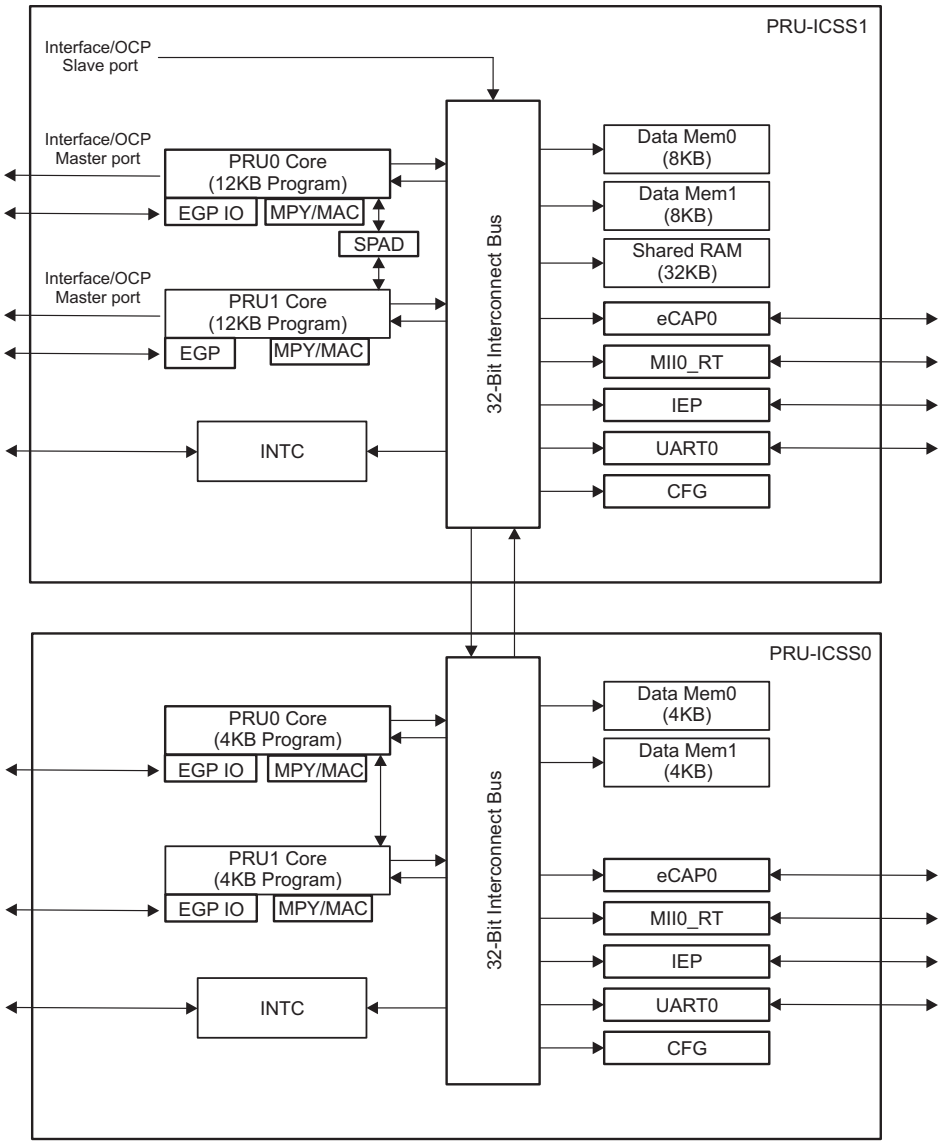


Figure 14. PRU-ICSS Block Diagram

4.2.1.1 Sigma-Delta Decimation Filter

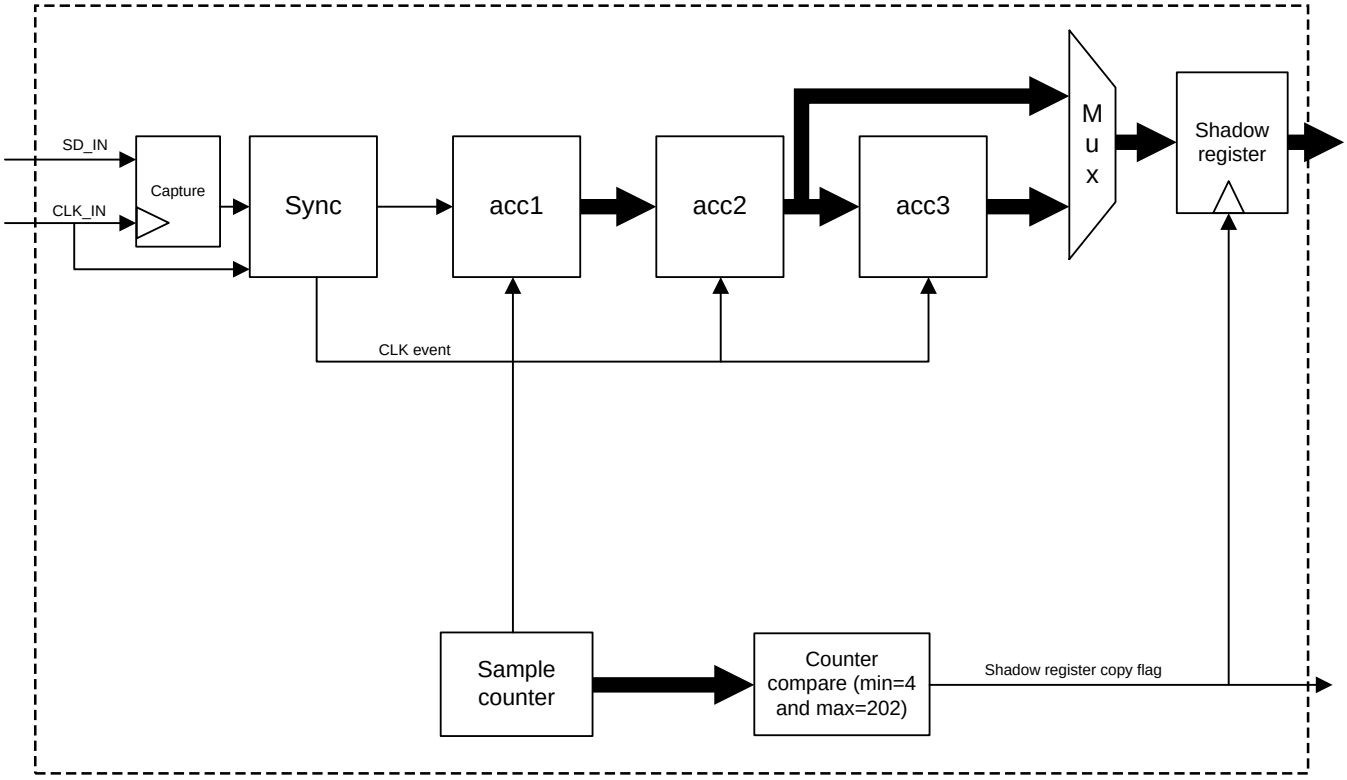
Sigma-delta Sinc filtering is achieved by the combination of PRU hardware and firmware. PRU hardware provides hardware integrators that do the accumulation part of Sinc filtering, while the differentiation part is done in firmware. In the following topic, the filter implementation is explained for Sinc3 implementation; however, the same method can be used to implement Sinc2 filtering.

Integration (PRU Hardware)

Both ICSS0 and ICSS1 implement the integrators of the sigma-delta demodulators in the Enhanced General Purpose Input Output (EGPIO) peripheral of the PRU. The integrator serves to count the number of 1's per clock event. Each channel has three cascaded counters, which are the accumulators for the Sinc3 filter. Each counter is 24 bits, giving a maximum count of 16,777,215. Each channel has a free running rollover clock counter. This sample counter updates the count value on the effective clock event for that channel. Each channel also contains a programmable counter compare block, and the compare register has a size of 8 bits. However, the minimum value is 4 and maximum value is 202 due to the 24-bit accumulator. Once sample counter compare value is reached, the shadow register copy is updated and the shadow register copy flag is set.

Features of the integrators in PRUs EGPIO:

- Up to nine channels with concurrent counting
- Flexible clock source configuration for each channel; option of independent clock source for each channel or one clock source for three channels
- Programmable, 8-bit sample counter compare register; used to set the OSR of Sinc filter
- Three 24-bit cascaded counters per channel for accumulation, only Sinc3 and Sinc2 modes supported
- Common channel enable (all channels are active or none are)



Note:

All acc are simple 24 bit adders
acc1 input is 1-bit
acc2 and acc3 inputs are 24-bit, rollover will occur at 0xff_ffff

Example: if acc2 = 0x10 and acc3 = 0xff_ffff,
next clk_event will have acc3 = 0x0_000f

Every rising edge of CLK_OUT then
acc1 = acc1 + sd_sync
acc2 = acc2 + acc1
acc3 = acc3 + acc2
sample_count = sample_count +1

Note:

1) if (over_sample_counter = over_sample_size)
   then
   Update shadow copy
   set shadow_update_flag
   reset over_sample_counter

2) snoop is optional method to read acc2 or acc3 directly

3) when sample_counter_select = 1
   then
   sample_count is read,
   if snoop = 1
   then
   direct read of active counter

Figure 15. Integrator Block Diagram in ICSS-PRU

Differentiation (PRU Firmware)

An overview of the firmware functions is shown in Figure 16. The firmware functions mainly consist of a set of difference equations, referred to as the filter calculations. This firmware function is repeated for each channel. There are two data paths per channel shown in the firmware function: One path does a Sinc3 decimation part of the filter calculation at higher OSR used for accuracy, and the other path is at a lower OSR used to quickly respond to short circuit conditions. The results of the higher OSR filter calculation are used by the application software. The digital value obtained with this filter is copied to a circular buffer of 126 samples, beginning of the buffer contains write pointer that points to latest sample in the buffer.

The lower OSR filter is a parallel data path to the higher OSR filter. The output of the lower OSR filter is compared with a threshold value in PRU firmware. If the threshold is exceeded, the PRU indicates this event on a GPIO with a signal transitioning from low to high. This path is faster to calculate the result as it uses a smaller OSR; therefore, the path is used for input fault detection. The OSR is configurable in both data paths.

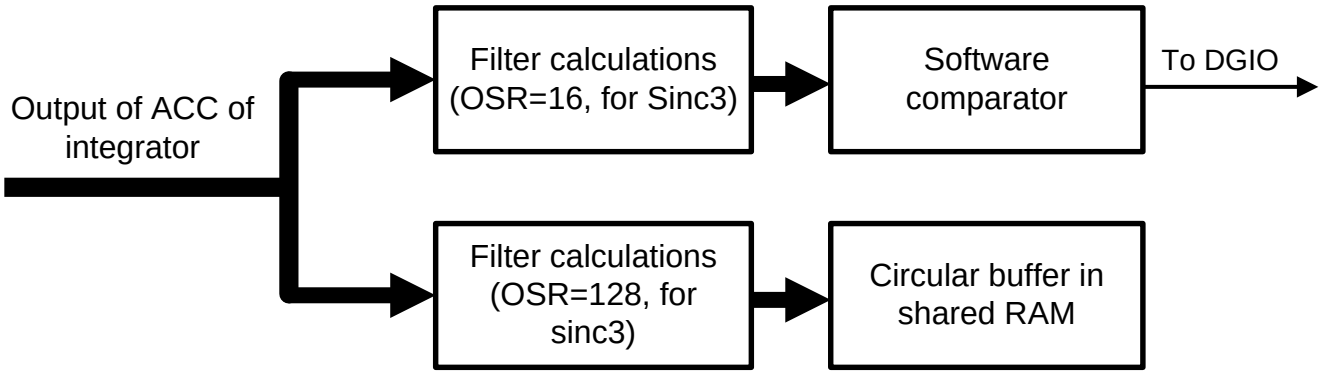


Figure 16. Firmware Functions Overview

The implementation within the filter calculation block of Figure 16 is shown in Figure 17. Figure 17 is the differentiation, or the delta part, of the Sinc filter. The filter for both the high OSR filter and low OSR filter is of the same type.

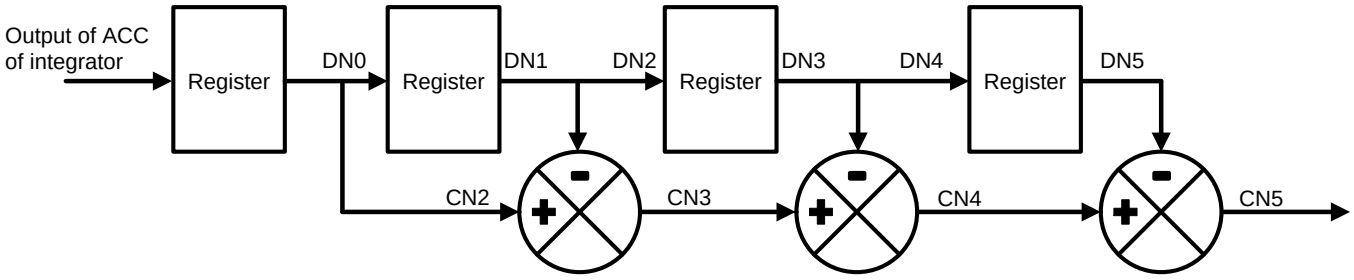


Figure 17. Sinc3 Filter Differentiation Implementation in PRU

The calculation done in PRU to implemented the differentiation block is given here:

```
dn1  =  dn0
cn3  =  dn0 – dn1
dn3  =  cn3
cn4  =  cn3 – dn3
dn5  =  cn3
cn5  =  cn4 – dn5
dn5  =  cn4
cn5  =  cn4 – dn5
```

‘dn0’ is the accumulated value for Sinc3 filter. This value is read from PRU hardware explained above. ’cn5’ is the conversion result of the sigma-delta Sinc3 filtered. Other values are initialized to zero in the beginning.

The sample counter compares register sets up the OSRs of the filters. The shadow register copy flag is used to initiate the filter calculation, and the shadow register copy flag is generated when the sample counter overflows when it is equal to the sample counter compare register. However, because there is only one flag per channel, the sample counter compare register is set up for the lower OSR. The higher OSR filter calculation is done by decimating the shadow register copy flag, which is done by a software counter.

For example, for a lower OSR of 16 and a higher OSR of 128, the sample counter compares register is 16 (that is, the lower OSR). For the higher OSR filter, the filter calculation is done every eighth time the shadow copy flag is generated, resulting in an OSR of 128 as 16 × 8 = 128. This also implies the higher OSR has to be a multiple of the lower OSR.

The firmware can be modified to have a different OSR. Overcurrent detection can be modified to either use Sinc2 or accumulator value of Sinc2 or Sinc3 based on the requirement.

The firmware implements for four channels: 1, 5, 6, and 7. The firmware implements only four channels because some of the pins used for sigma-delta demodulation have been allocated for other functions on the IDK. A custom design can support up to nine channels of sigma-delta demodulators.

5 Application Software Description

Interaction between the ARM, PRU, and sigma-delta modulator card is shown in Figure 18:

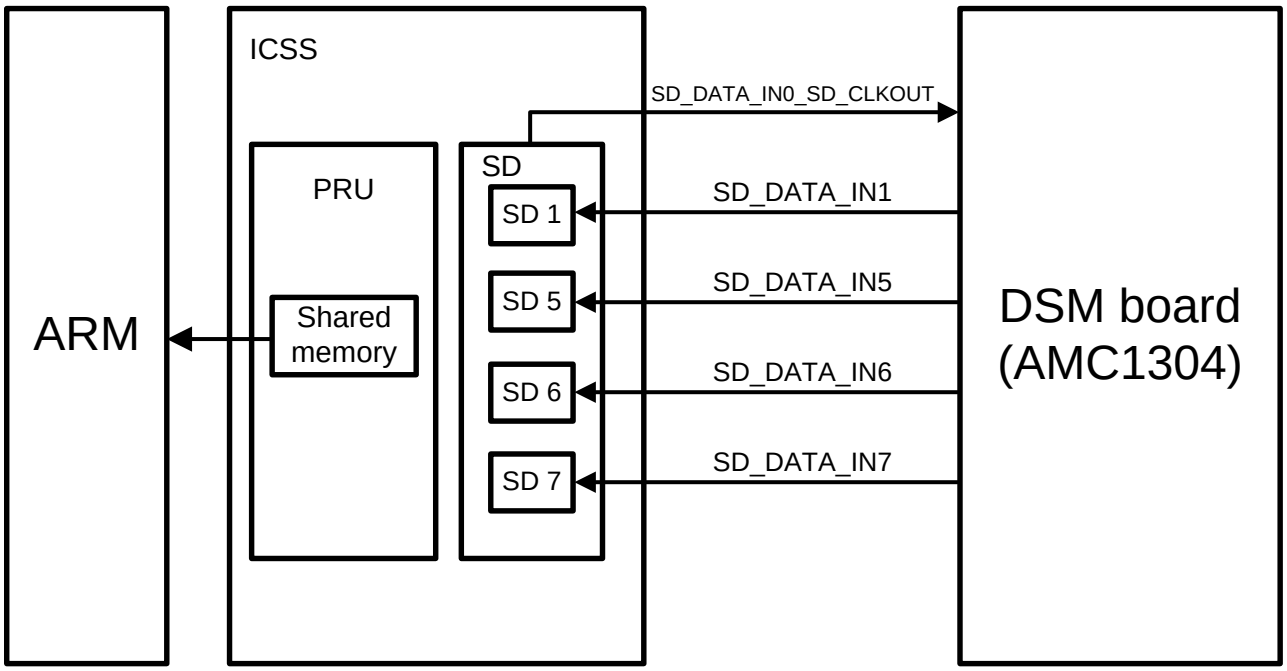


Figure 18. Application Interface With PRU Sigma-Delta Firmware

Software is developed as a SYSBIOS CCS project. SYSBIOS contains starterware library for handling various peripherals on the AM437x. The purpose of the software is to setup the pinmux, start PRU execution, handle UART port (available over USB through onboard FTDI) to interface with GUI in host PC for user to validate AMC1304 performance, and configure the OSR and sigma-delta modulator clock frequency.

Software initially sets up pin mux for sigma-delta clock and signal lines and PRU digital I/Os. Then, it initializes PRU1 of ICSS_L, loads Sigma-Delta firmware onto its instruction memory, and starts its execution. UART is then setup using starterware libraries. The clock for the sigma-delta modulator is provided by the AM437x, and software configures PRU for providing clock frequency as required. The GUI in the host PC can configure OSR. Software mostly functions like a client for the GUI and handles configuring PRU sigma-delta OSR accordingly. Software also handles transferring sampled values through UART so that the GUI can display it. As the GUI expects 16-bit signed data, sample value is made signed and most significant 16 bits are extracted and then sent to the GUI.

5.1 Getting Started

The compiled application software and the source given inside the IDK can be found at a time to be determined. This software has been compiled from CCS. The SD card is loaded with two files: 'app', the generating executable binary, and 'mlo', the bootloader. On power up, the AM437x loads the application from the SD card located in the micoSD card slot on the IDK. Details of the creating these files from source code is given in the *AM437x SYSBIOS Industrial SDK 02.00.00.02 User Guide* [2].

6 GUI User Guide

This section describes the functionality of the isolated current and voltage measurement test bench.

6.1 GUI Software Installation

The following section explains the location and the procedure for installing the software properly. The GUI assumes SD card is loaded with relevant binaries for Sitara IDK.

6.1.1 Installing Run-Time Engine

Follow these steps to download and install the LabVIEW™ run-time engine to use the IVIM Test Bench:

1. Click on the link to install the LabVIEW Run-Time Engine 2010 SP1 (32-bit Standard RTE): http://www.ni.com/download/labview-run-time-engine-2010-sp1/2292/en/
2. Run LVRTE2010_SP1f5std.exe to install the LabVIEW 2010 SP1 Run-Time Engine (32-bit).
3. Follow the installation wizard and complete the installation.

The installation files for the run-time engine are automatically extracted to a directory on disk. The installer does not remove the files after installing. To remove these files from the disk, note their location during the unzipping process.

6.1.2 Installing VISA

Follow these steps to download and install the VISA driver to communicate with the device:

1. Click the link to install the NI-VISA 5.0.3: http://www.ni.com/download/ni-visa-5.0.3/2251/en/
2. Run visa503full_downloader.exe.
3. Follow the installation wizard and complete the installation.

6.1.3 Installing IVIM Test Bench

The GUI can be found at TIDA-00209:

1. Select the *Destination Directory* for IVIM Test Bench and click *Next.*

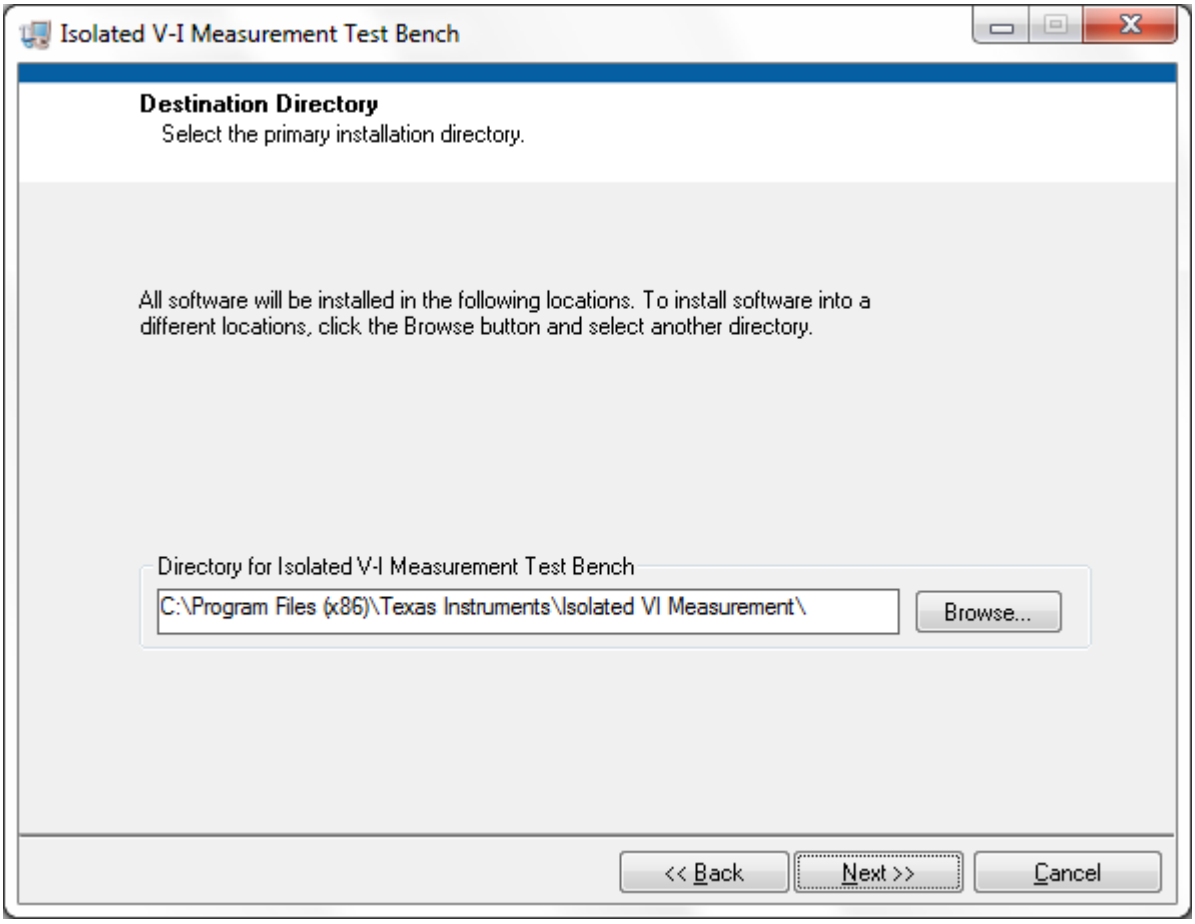


Figure 19. Destination Directory Selection Window for IVIM Test Bench

2. Figure 20 shows the list of files that will be added or modified with this installation. Click *Next*.

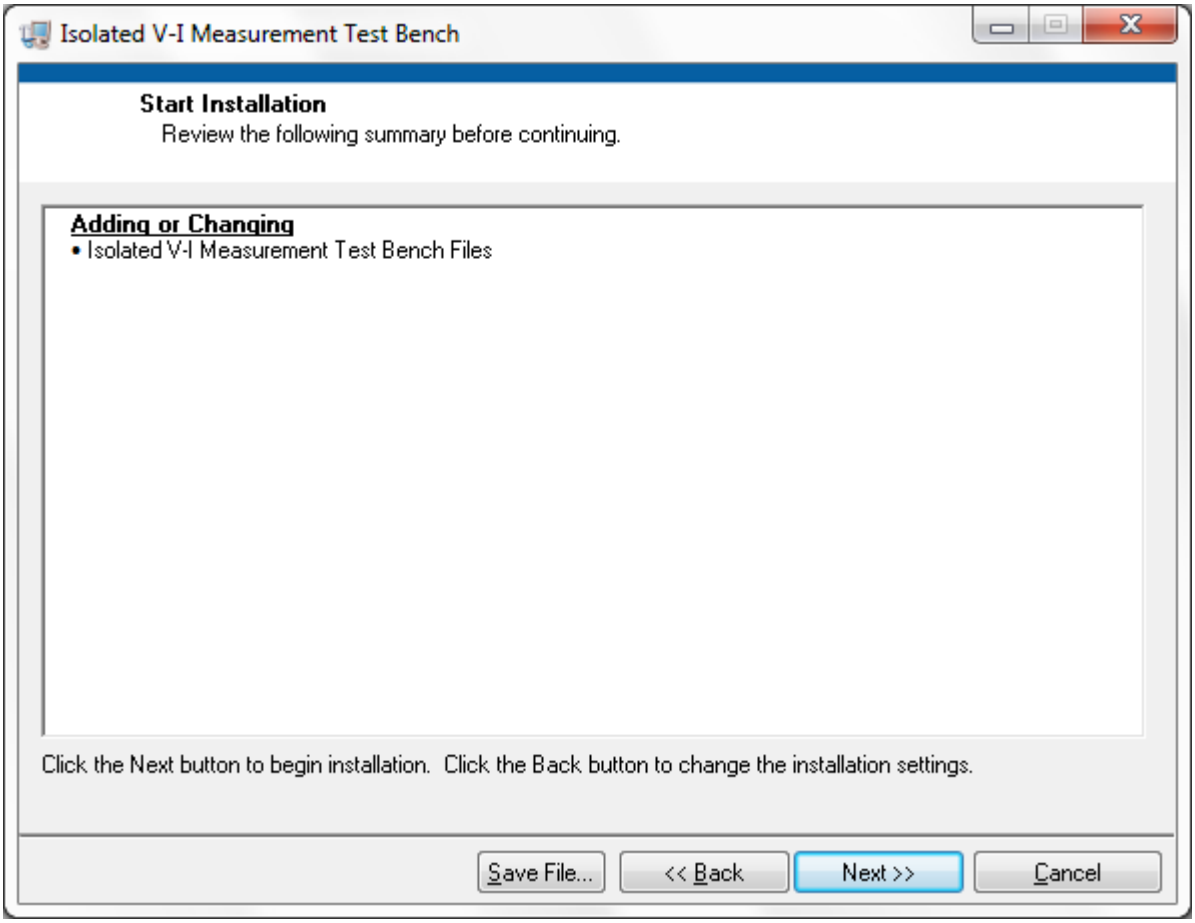


Figure 20. List of Files Added or Modified With Installation

3. Once the installation starts and finishes as shown in Figure 21, click *Finish*.

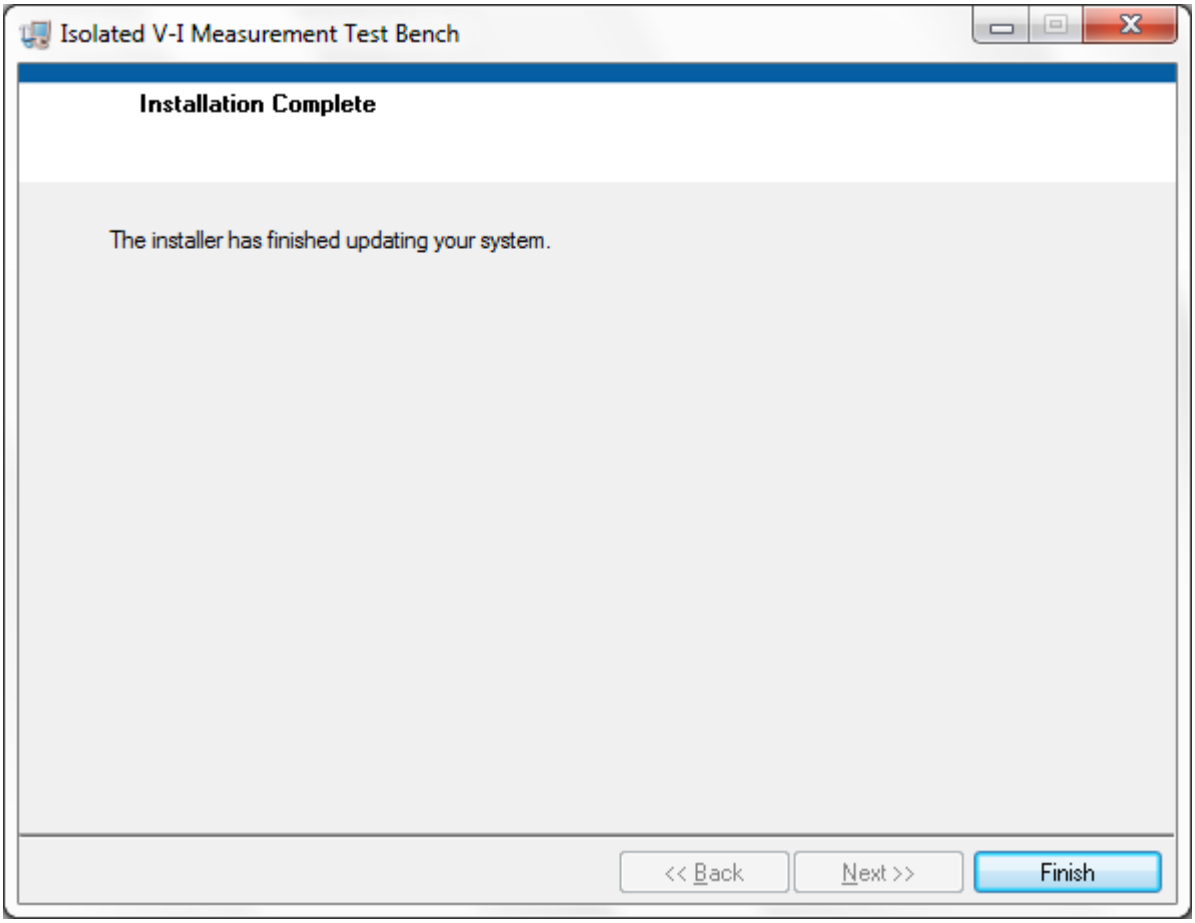


Figure 21. Window After Successful Installation

6.2 Launching IVIM Test Bench

Follow these steps to launch the IVIM Test Bench:

1. Locate the IVIM Test Bench through any of these approaches:
   - Desktop shortcut
   - Start menu shortcut
   - Installed folder location. Default location is Win 7: C:\Program Files (x86)\Texas Instruments\Isolated VI Measurement\
2. Double click on Isolated V-I Measurement.exe

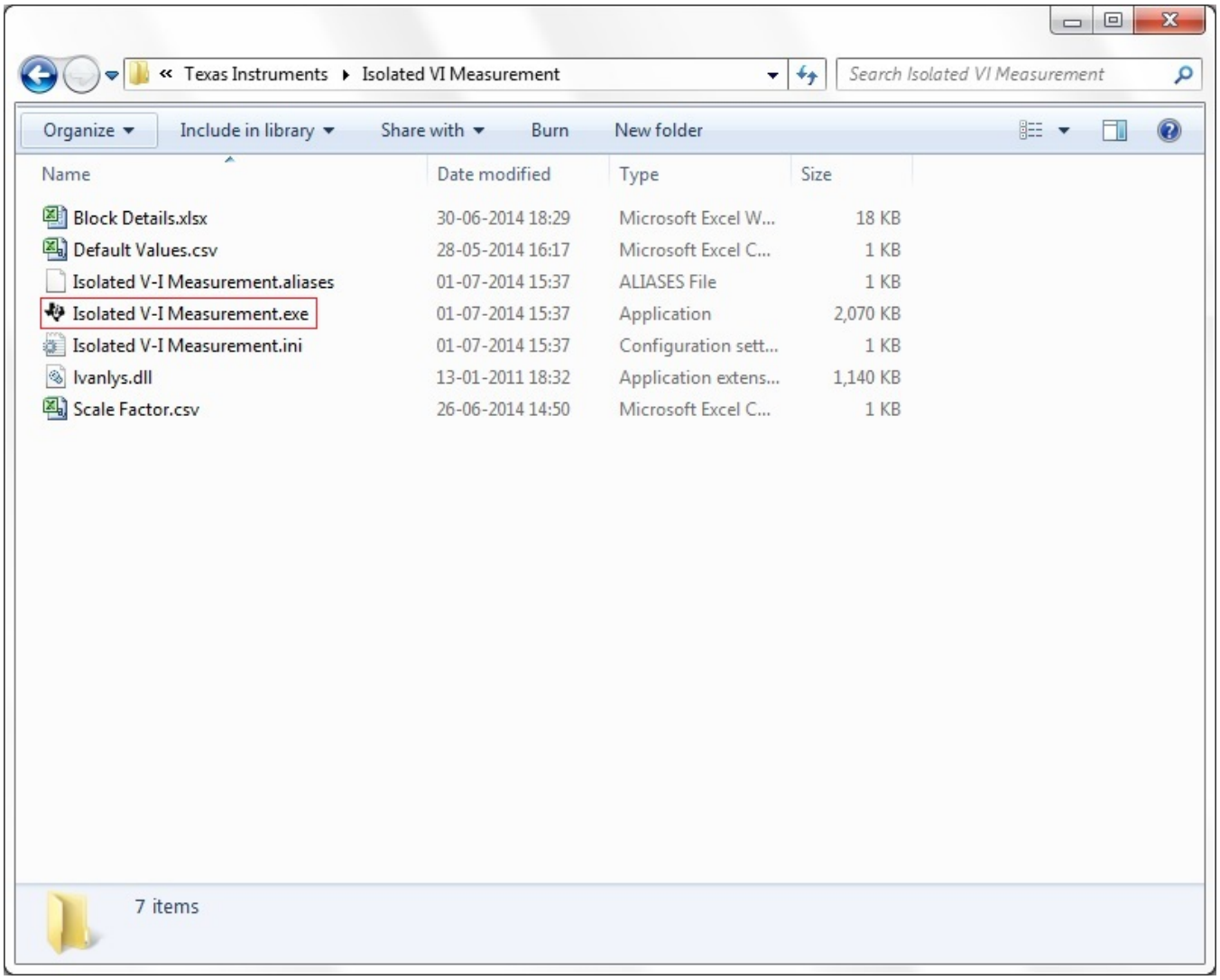


Figure 22. Isolated VI Measurement Folder Structure

6.3 Mode Selection

The *Select a Mode* dialog box pops up as the application is launched (Figure 23). Select *Sitara* and the corresponding VISA resource name.

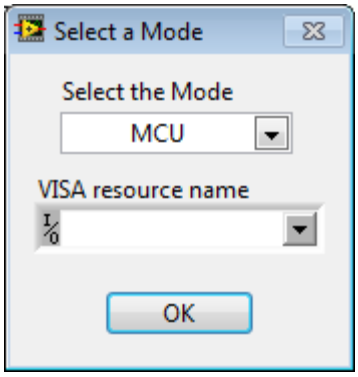


Figure 23. Mode Selection

As soon as the user selects the mode, the GUI starts to initialize.

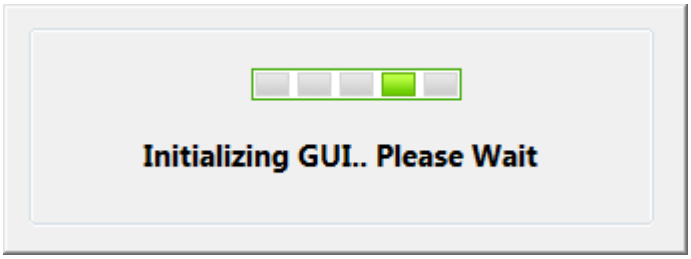


Figure 24. GUI Initialization

Proceed to use the GUI after the initialization completes.

6.4 IVIM Pages

The IVIM Test Bench has three pages:

1. System Layout
2. Config
3. Graph

6.4.1 System Layout

The *System Layout* page has the block diagram with description of the parts used in the isolated current and voltage measurement. Moving the mouse pointer over any of the blocks shows the description of the same on the right side of the page with web links for reference. Refer to Figure 25.

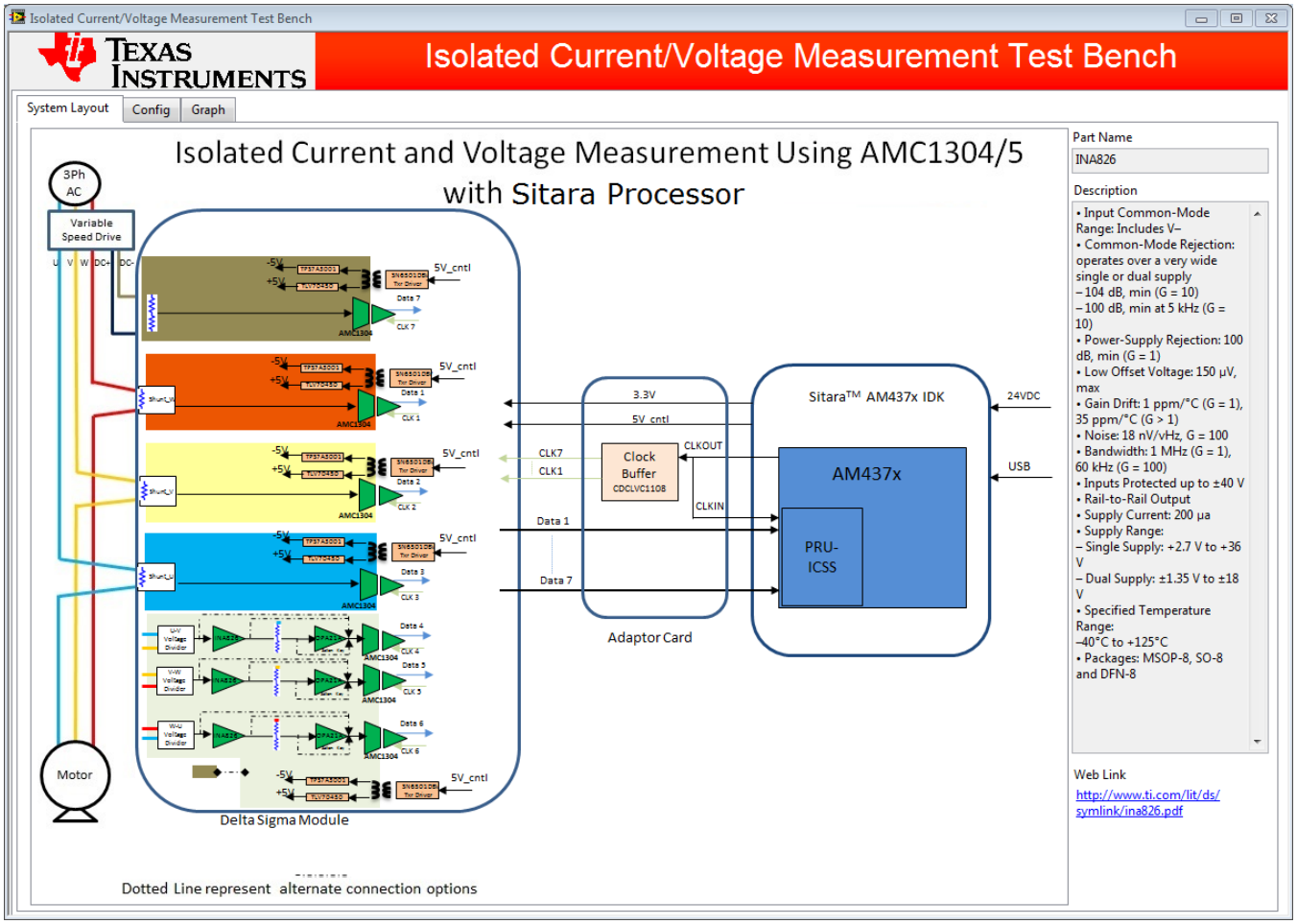


Figure 25. System Layout

- *Block Diagram*: The block diagram gives the detailed description of the parts used for isolated voltage and current measurement.
- *Part Name*: This box displays the part name selected.
- *Description Box*: This box displays a brief description about the part in the block diagram.
- *Web Link Box*: This box displays the web reference of the part.

6.4.2 Config Page

This page allows the user to configure the delta-sigma filter parameters.

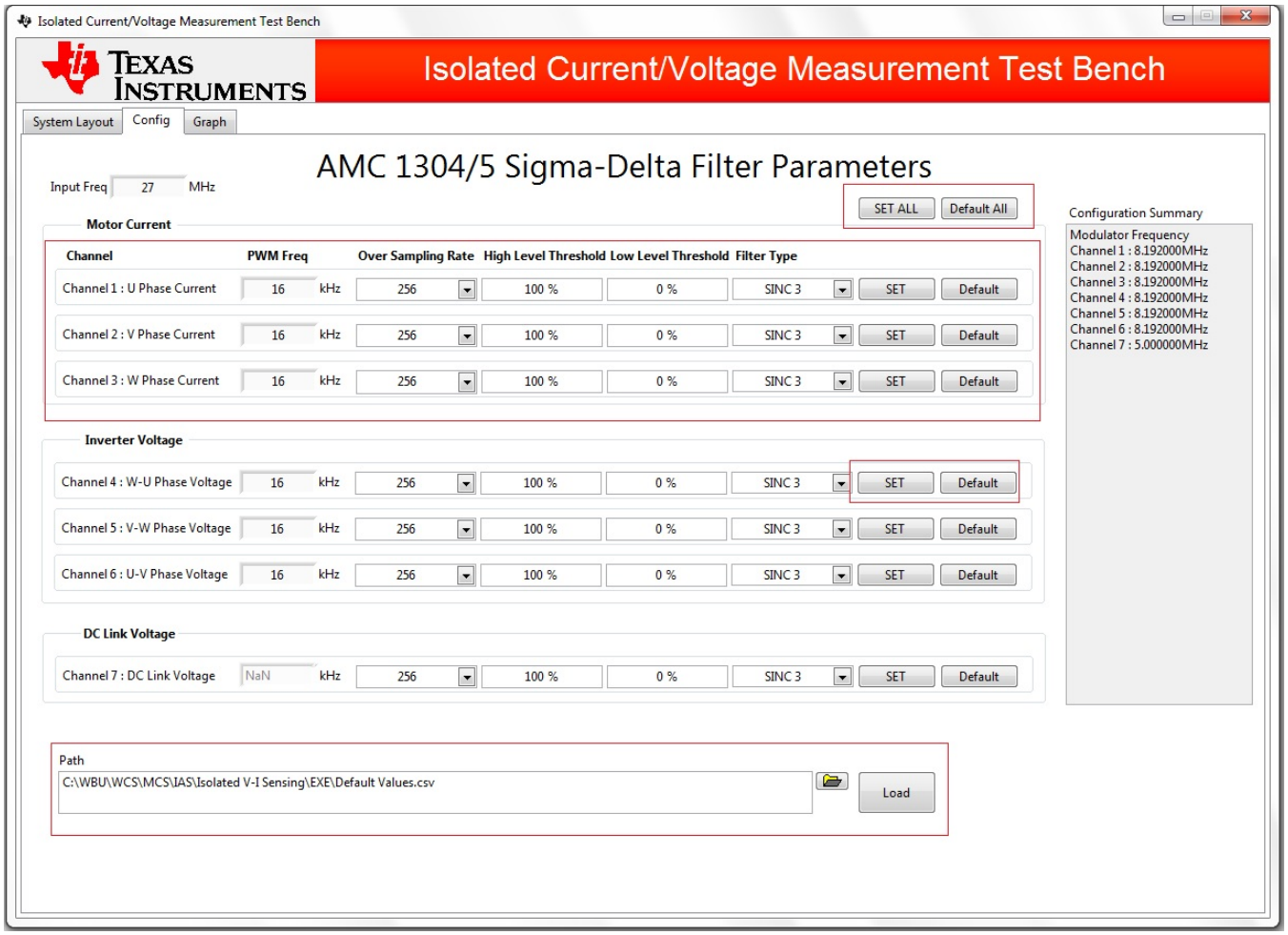


Figure 26. Config Page

- *Motor Current*: This option contains the settings for three channels to be configured for respective phase current.
- *Inverter Voltage*: This option contains the settings for three channels to be configured for respective phase voltage.
- *DC Link Voltage*: This option contains the setting for a channel to be configured for DC Link voltage.
- *Set*: This button sets the configured settings for the corresponding row.
- *Set All*: This button sets the configured value for all channels.
- *Default All*: This button sets the default values for all channels.
- *Load*: This button loads the values for each parameter form the file specified in the in the path dialog box.
- *Configuration Summary*: This option displays the modulated frequency for each of the channels.

6.4.2.1 Setting PWM Frequency and Oversampling Rate

- *PWM Frequency*: Enter the value of the MOSFET or IGBT switching frequency of the motor drive. The GUI will use this value along with the OSR value to calculate modulator frequency. The frequency value can be entered in the given text box in kHz.
- *Oversampling Rate*: Enter the desired OSR for the Sinc filter. The oversampling rate can be selected from the list.

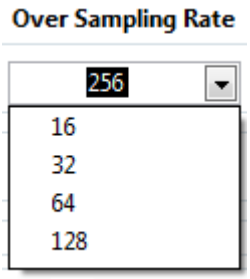


Figure 27. Oversampling Rate Selection

- *Modulator Frequency*: This is a calculated value, which is the frequency of the clock signal given to the delta-sigma modulator. The modulator frequency depends on the PWM frequency and oversampling rate. Considering two samples are required for every PWM period, the required sampling rate is twice the PWM frequency. The modulator frequency is calculated as 2 × (PWM Frequency) × OSR. The two samples requirement is a suggestion; however, it can be changed depending on the application requirement. The modulator frequency is limited to 20 MHz.
- *Input Frequency*: Enter the frequency of the input clock or crystal on the board. The GUI use this value along with the required modulator frequency to calculated the PLL configuration registers and clock dividers on the board.

6.4.2.2 Setting Filter Type

Select the desired filter type for each channel from the list shown in Figure 28:

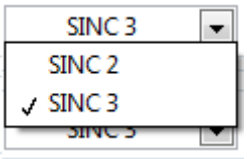


Figure 28. Channel Filter Type

6.4.2.3 High Level Threshold and Low Level Threshold

Enter the high level and low level threshold values in percentage of the full scale reading (FSR). The output of the sigma-delta figure is from 0 to the FSR. The FSR is dependents on the Sinc filter and the OSR used for the short circuit detection. On the Sitara processor, it is Sinc3 and an OSR of 16. All of the full scale reading (100%) corresponds to the maximum full-scale differential voltage input of the delta-sigma modulator, and 0% corresponds to the minimum full-scale differential voltage input. For the AMC1304M05, the maximum full scale voltage is 62.5 mV, corresponding to 100%, and the minimum full scale voltage is –62.5 mV, which corresponds to 0%, and 0 V is 50%.

6.4.2.4 Setting Default Value

Each channel can be configured to their default values using the *Default* button provided for each channel. The user can also use the *Default All* button to set default values to all the channels.

6.4.2.5 Configuration Summary

The configuration summary box gives the calculated modulator frequency for each channel. The modulator frequency has a limit of 5 to 20 MHz. When the set values exceed the limit, the values are coerced and the summary box indicates the error with a notification as shown in Figure 29.

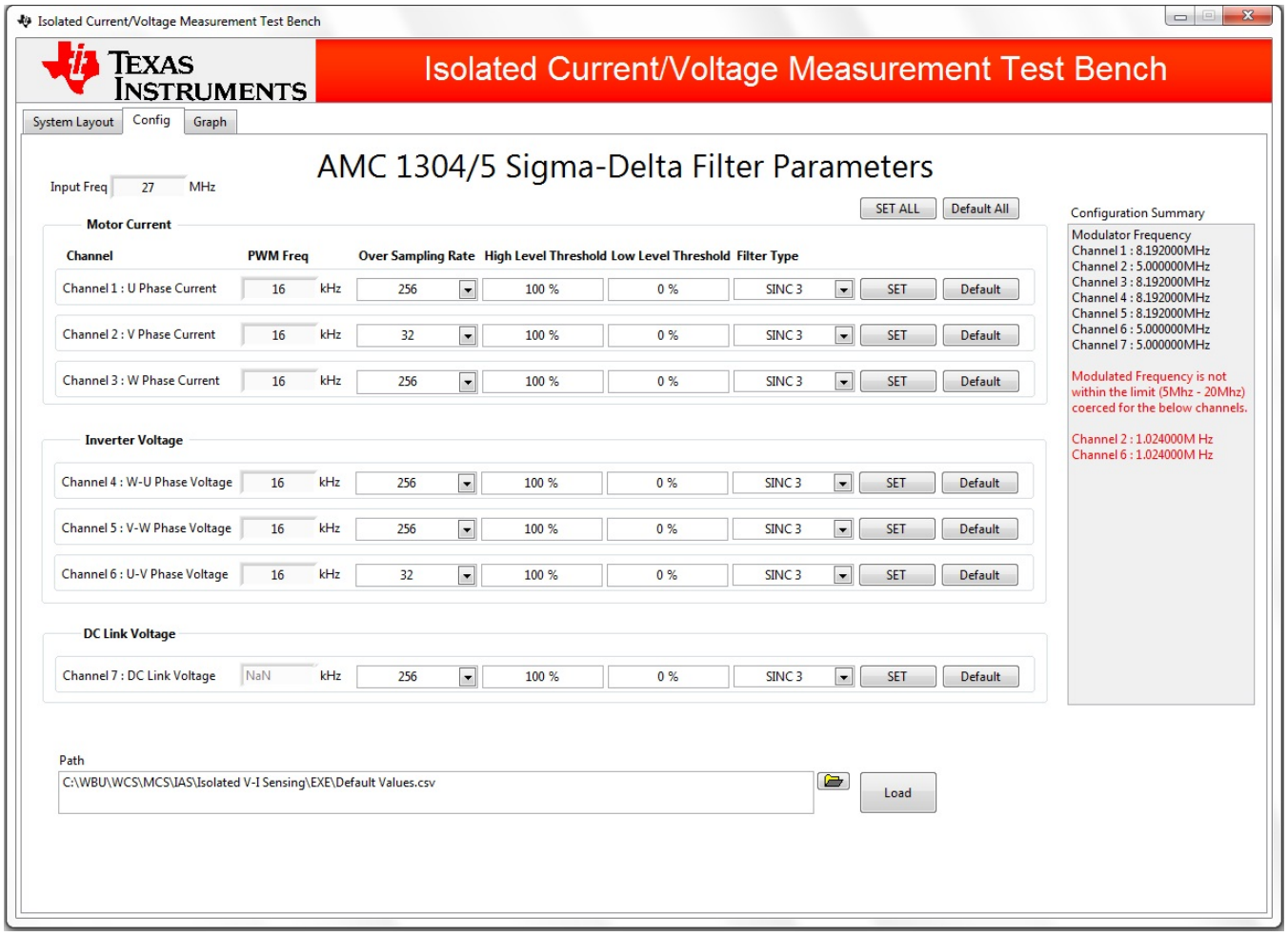


Figure 29. Configuration Summary

6.4.2.6 Loading the Default Value File

Select the default value file using the path control available. Click on the *Load* button to load the settings to the user interface.

Figure 30. Load Default Values File

6.4.2.7 Setting Configuration

Set the final channel configuration by using the *Set* buttons provided with each channel or the *Set All* button to set all channels configuration. When the *Set All* button is pressed, all the details in the *Config* page is sent to the MCU as previously selected.

6.4.3 Graph Page

The *Graph* page is the result display and processing page. The captured values are displayed as graphs in this page as either in time domain or frequency domain.

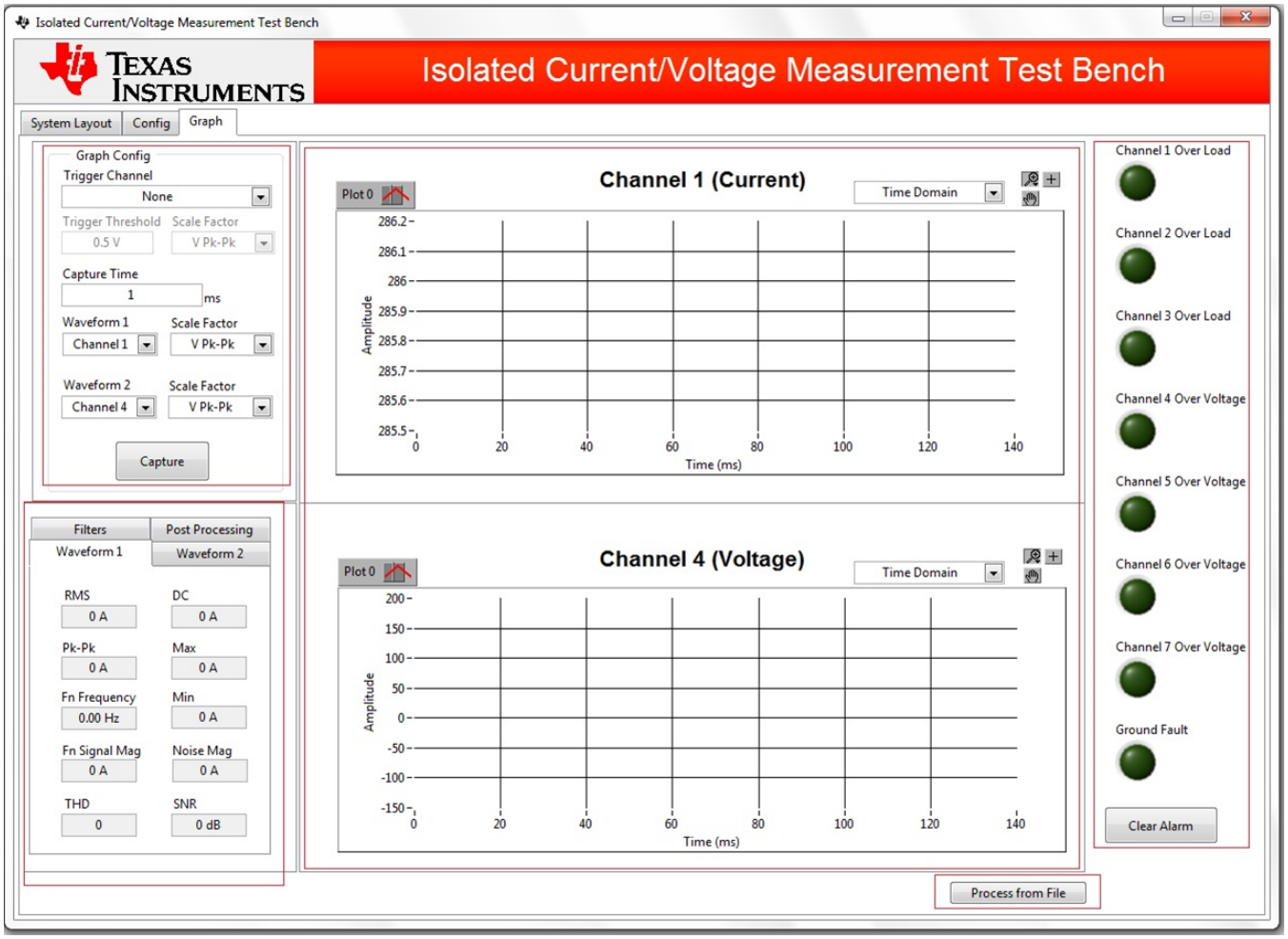


Figure 31. Graph Page

- *Graph Config*: This pane sets the trigger modes and select waveforms to display.
- *Waveform Parameter*: This pane displays the parameters of the selected waveform.
- *Graph Pane*: The captured data is plotted in the form of graph in this pane.
- *Error Indicators*: The graph page has eight indicators to detail the error. *Clear Alarm* erases the indications.
- *Process from File*: This button plots the data from the file in a graph.

6.4.3.1 Setting Trigger Channel and Capture Time

The trigger channel can be set using the *Trigger Channel* control. Select any of the channels available. Set the trigger threshold of the selected channel in *Trigger Threshold* control, The trigger channel and trigger threshold vales are sent to the target, where the target waits for the input on this channel to cross the trigger threshold value.

Select the scale factor from the *Scale Factor* control to calculate the digital value corresponding to the trigger threshold value.

Set the capture time in milliseconds (ms) in the *Capture Time* control. The maximum value is 100 ms; the limit is due to amount of memory reserved for buffering the samples. The GUI can request for more than 100 ms, but the data will be clipped due to rollover from the buffer pointer inside the firmware of Sitara.

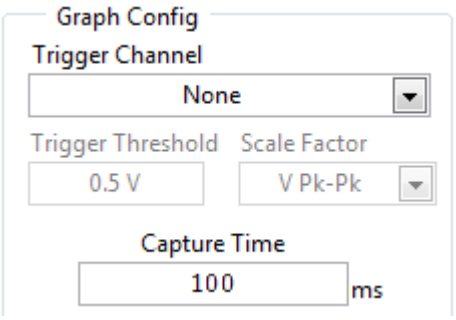


Figure 32. Trigger Configuration

6.4.3.2 Selecting Waveform and Scale Factor

The waveform to be displayed and its corresponding scale factors can be selected from the *Waveform 1* and *Waveform 2* control. The scale factors are selected from their respective controls. The scale factor here selects how the digital value received for the target corresponds to voltage or current values on the waveform.

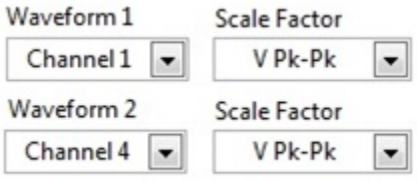


Figure 33. Waveform Settings

6.4.3.3 Selecting Filter

The *Filters* tab shows the post processing options that can be done by the GUI. Select the configuration from the *Filters* tab.

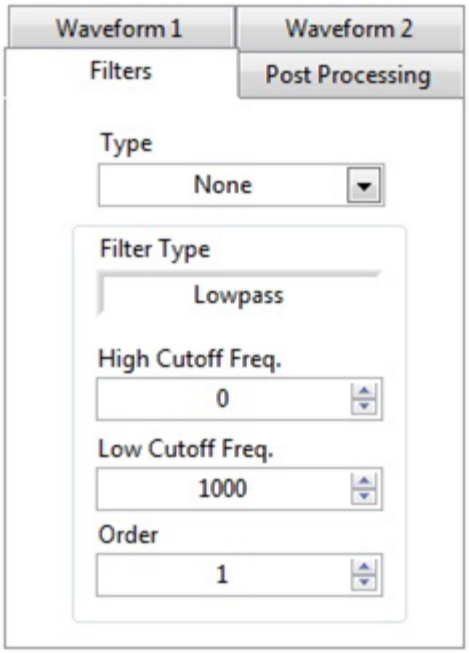


Figure 34. Filter Selection

The filter can be selected from the *Type* control.

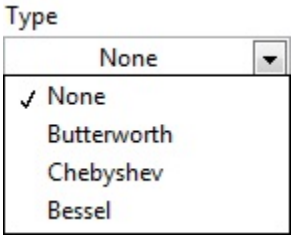


Figure 35. Filter Type Selection

The filter characteristics can be selected using the *Filter Type*, *High and Low Cutoff Freq*, and *Order* controls. The low-pass filter will ignore the *High Cuttoff Freq* setting, and the high-pass filter will ignore the *Low Cutoff Freq* filter setting.

6.4.3.4 FFT Window Selection

FFT windows can be selected using the *FFT-Window* control in the *Post Processing* tab. This selection affects the FFT graph if the graph is selected to display FFT of the waveform captured.

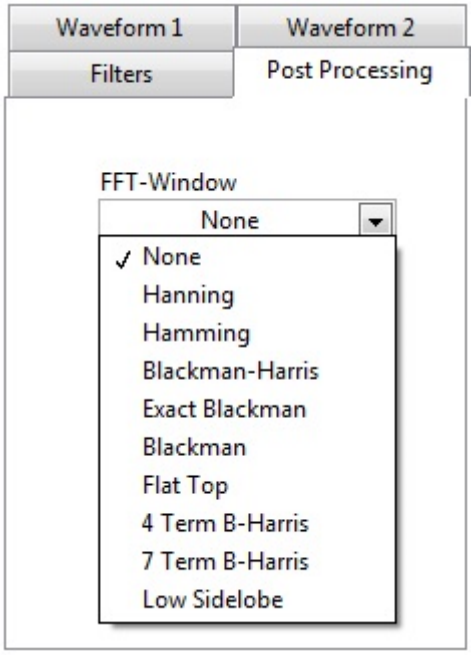


Figure 36. FFT Window Selection

6.4.3.5 Waveform Parameter Display

The parameters of the selected channel waveform can be noted from the waveform page as in Figure 37.

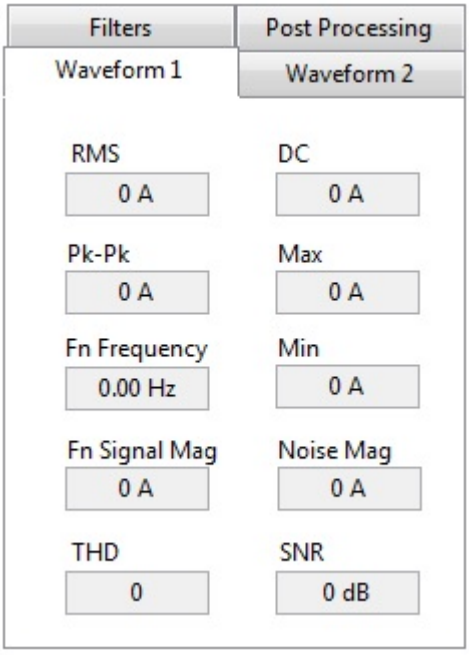


Figure 37. Waveform Parameter Display

6.4.3.6 Data Capture

Click on the *Capture* button shown in Figure 38 to obtain the results.

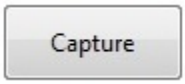


Figure 38. Data Capture Button

Capture mode sends the corresponding settings to the target, gets the data for the time specified, and displays it in the graph once.

6.4.3.7 Selecting Domain

Select the graph domain using the control provided for each graphs and the time or frequency domain using the control displayed in Figure 39.

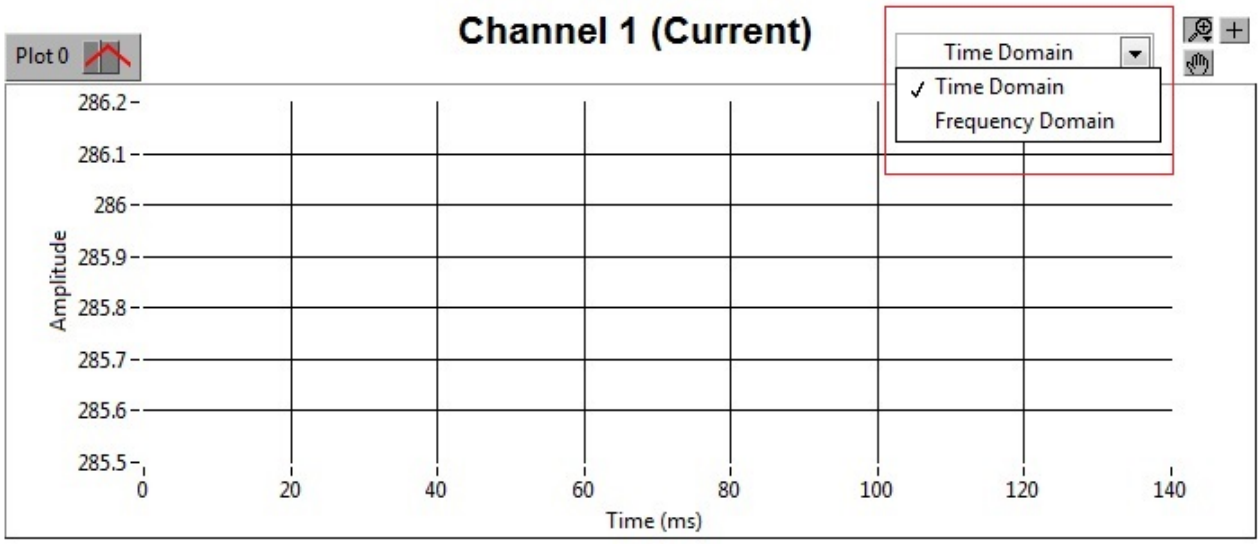


Figure 39. Graph Domain Selection

6.4.3.8 Emergency Indicators

The emergency indicators activate during overload and overvoltage conditions. The user can clear these indicators by pressing the *Clear Alarm* button available in the user interface.

6.5 Editing the Scale Factor

The scale factor values are read from the "Scale Factor.csv" file and then loaded to the user interface. The scale factor file is placed in the same folder of the executable. For Win 7, it is "C:\Program Files (x86)\Texas Instruments\Isolated VI Measurement\". The scale factor is the value used to convert the raw data into the equivalent voltage or current specified by the user. Offset is the value used to calibrate the fixed offset errors. This value will be subtracted from the raw value received from MCU. The structure of the scale factor file is as shown in Table 4.

Table 4. Scale Factor Structure

SCALE LABEL	SCALE FACTOR	OFFSET
V Pk-Pk	0.023103	0
V at APC	0.00021	0
Current	3.81E-05	0
V_Inamp	0.021437137	0
Raw	1	0
CH1 CAL	3.83E-05	0
CH2 CAL	3.81E-05	0

The user can give a suitable scale label and the corresponding scale factor and offset value.

NOTE: Do not change the structure of the file by adding or deleting any columns. The user can only add or delete the rows.

6.5.1 Editing Default Values

The default value for each channel is read from the "Default Values.csv" file. The structure of this file is as shown in Table 5:

Table 5. Default Values File Structure

CHANNEL NAME	MODULATOR CLOCK FREQUENCY	OSR	HIGH-LEVEL HRESHOLD	LOW-LEVEL THRESHOLD	FILTER TYPE
1	16	256	100	0	Sinc3
2	16	256	100	0	Sinc3
3	16	256	100	0	Sinc3
4	16	256	100	0	Sinc3
5	16	256	100	0	Sinc3
6	16	256	100	0	Sinc3
7	16	256	100	0	Sinc3

The user can edit the necessary field and save the changes.

NOTE: Do not change the structure of the file by adding or deleting any columns or rows.

7 Test Results

The board was tested for claimed performance with respect to accuracy for three-phase motor voltage, DC Link voltage, and AC current measurements. The results of the test are given here.

7.1 Voltage Measurement Accuracy

7.1.1 Test Setup for AC Voltage Accuracy

The diagram of the test set up for validating the AC voltage measurement is shown in Figure 40. The test was conducted for phase-to-phase voltage configuration. The test is performed using a 6 ½ digit multimeter as the reference meter. The reading is taken at 25°C. The results calculated using the theoretical scale factor is discussed in the TIDA-00171 design guide, *Isolated Current Shunt and Voltage Measurement Kit* [1]. For AC voltage measurement, gain correction was performed. The reading was taken again at 25°C.

The test was done with a modulator clock at 5 MHz and a Sinc3 filter with an OSR of 128.

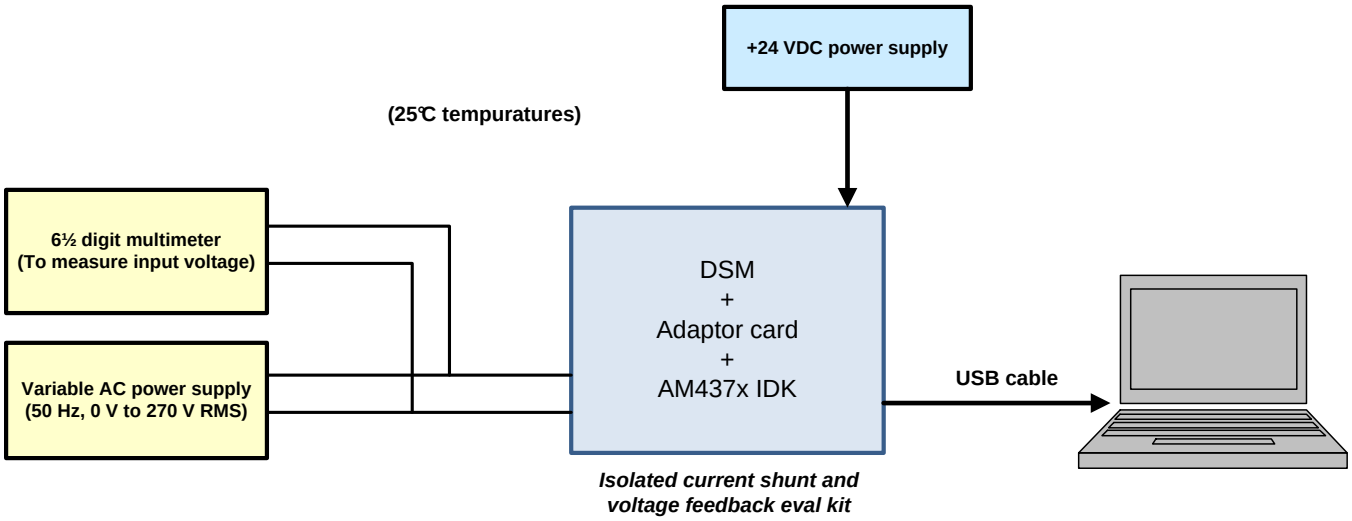


Figure 40. Test Setup for AC Voltage Measurement Accuracy

7.1.2 Results

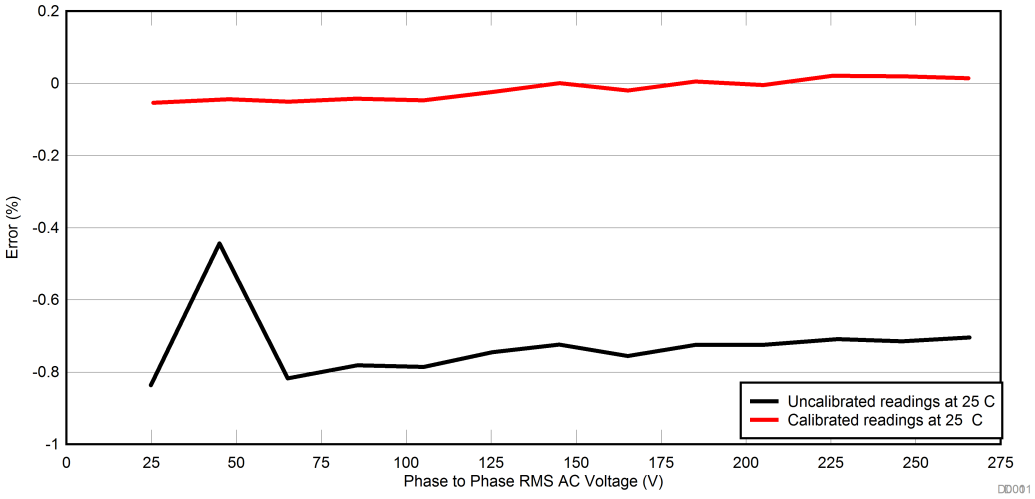


Figure 41. Phase-to-Phase Voltage versus Error

The AMC130x with an INL of just 4 LSB enables the system to achieve 16-bit of resolution with 13-bit ENOB results in a 0.2% accuracy. The device has a smaller temperature drift (20 ppm per degree) in gain error along with a Sinc digital filter implemented in the AM437x to decimate the bit stream.

7.1.3 Test Setup for DC Link Voltage Measurement Accuracy

The diagram of the test setup for validating the DC Link voltage measurement is shown in Figure 42. A 6½-digit multimeter was used as reference to calculate error. The first reading is taken at 25°C. The results calculated using the theoretical scale factor are discussed in the TIDA-00171 design guide, *Isolated Current Shunt and Voltage Measurement Kit* [1]. For the DC Link measurement, both the offset error correction and gain correction were performed. The reading was retaken at 25°C.

The test was done with a modulator clock at 5 MHz and a Sinc3 filter with an OSR of 128.

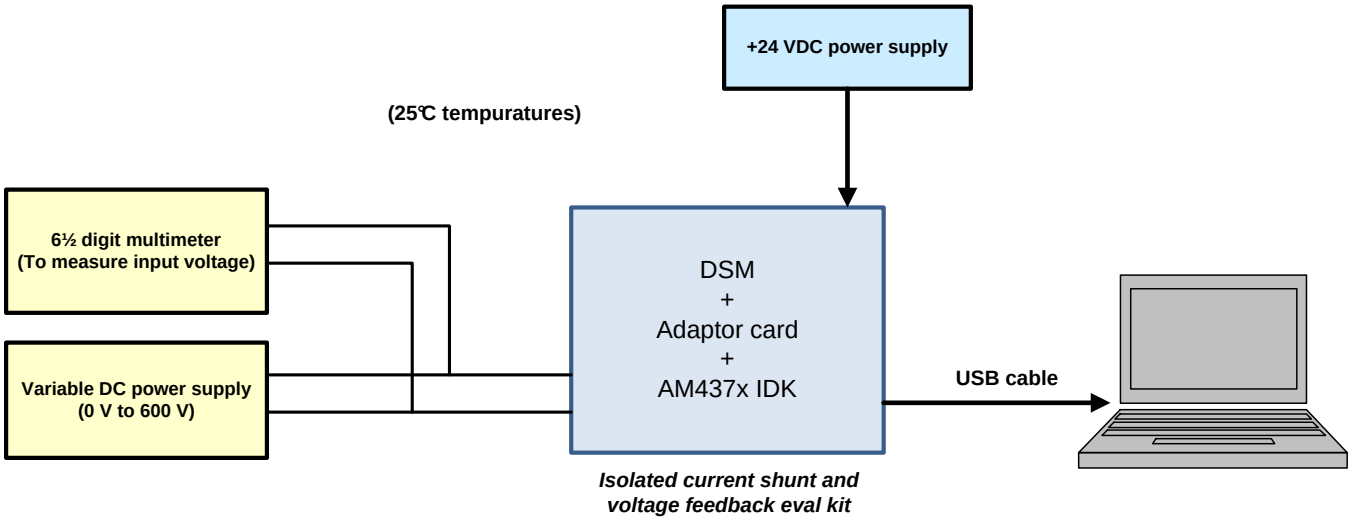


Figure 42. Test Setup for DC Link Voltage Measurement Accuracy

7.1.4 Results

Figure 43 and show the error versus applied DC Link voltage. The uncalibrated error at a lower voltage is due to an offset error.

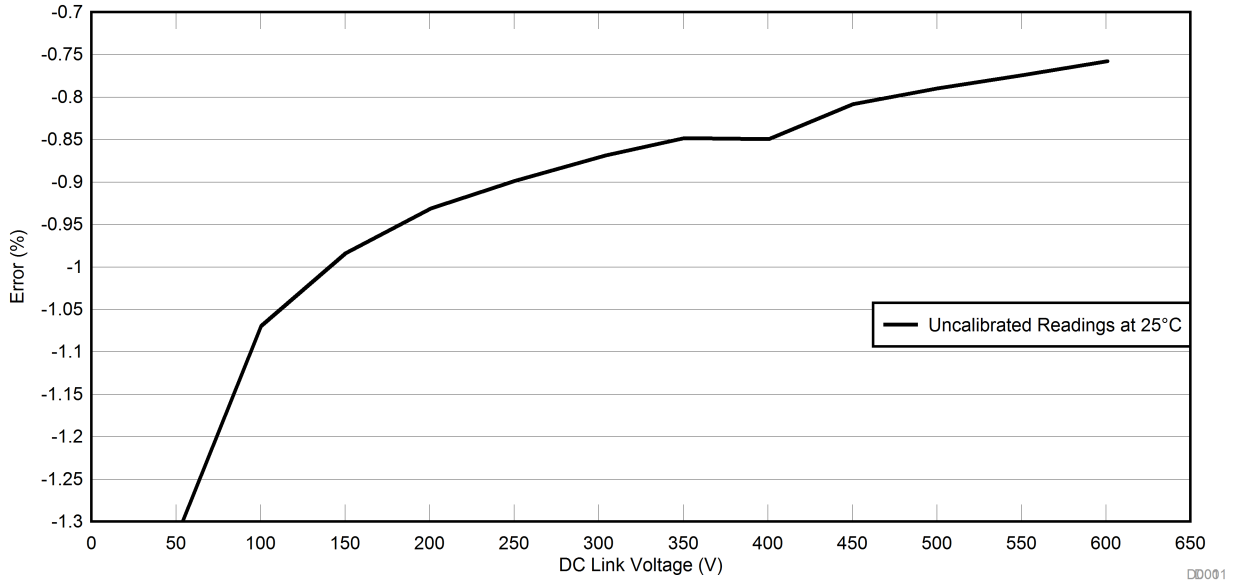


Figure 43. DC Link Voltage versus Error, Uncalibrated Readings at 25°C

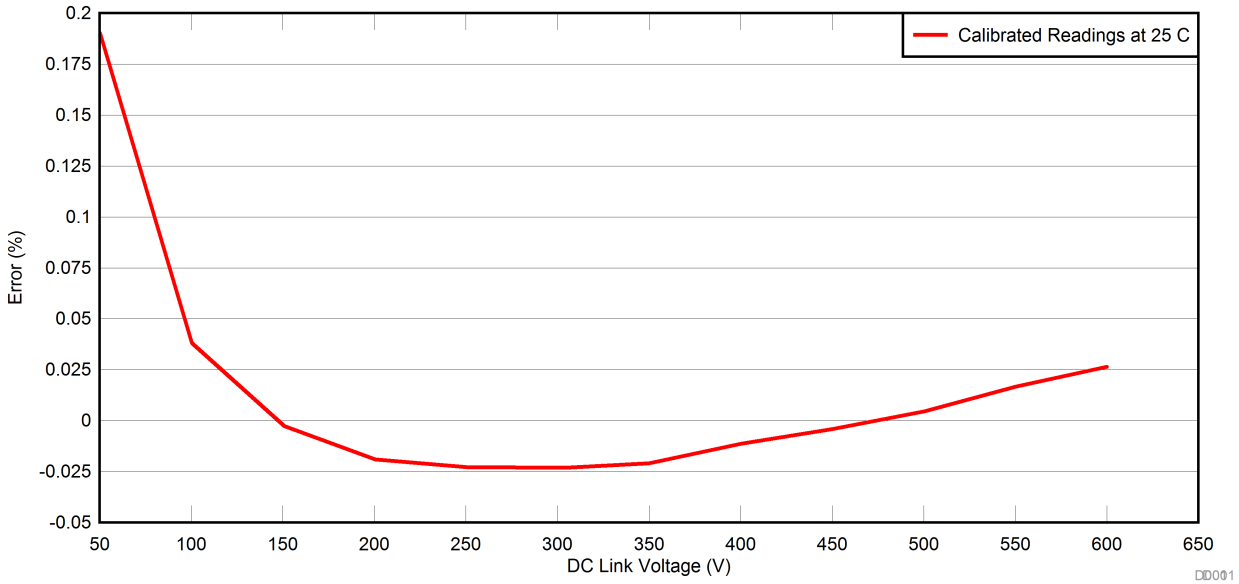


Figure 44. DC Link Voltage versus Error

7.2 Current Measurement Accuracy

7.2.1 Test Setup for AC Measurement Accuracy

The diagram of the test setup for validating the AC measurement is shown in Figure 45. The AC is measured using a 6½-digit multimeter, which is used as the reference meter. The reading is taken at 25°C. The results calculated using the theoretical scale factor are discussed in the TIDA-00171 design guide, *Isolated Current Shunt and Voltage Measurement Kit* [1]. For AC measurement, a gain correction was performed and the reading was taken again at 25°C.

The test was done with a modulator clock at 5 MHz and a Sinc3 filter with an OSR of 128.

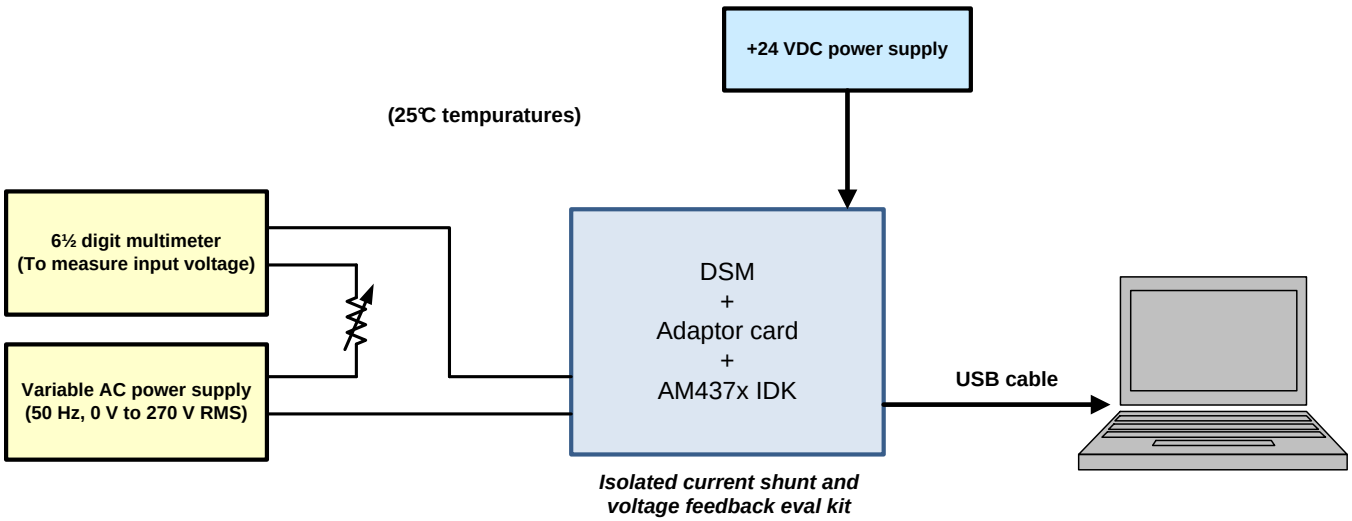


Figure 45. Test Setup for AC Current Measurement Accuracy

7.2.2 Results

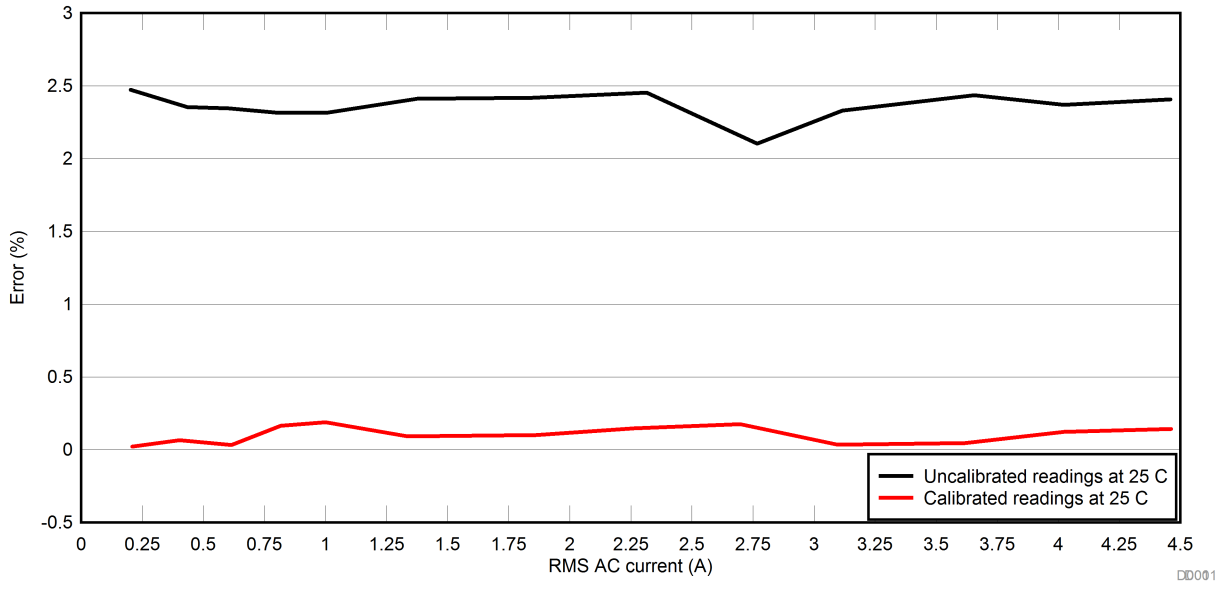


Figure 46. AC Current versus Error

7.3 Short Circuit Accuracy and Response Time

The shunts used to validate the short circuit alarm are 50 mΩ. The threshold was set to 1.25 A as discussed in the TIDA-00171 design guide, *Isolated Current Shunt and Voltage Measurement Kit* [1]. The test setup for short circuit test is shown in Figure 47. The PC GUI is used to set the threshold settings and modulator clock frequency to 8.192 MHz. The initial current in the circuit is set below the threshold value. Upon closing the switch, the current in circuit exceeds 1.25 A.

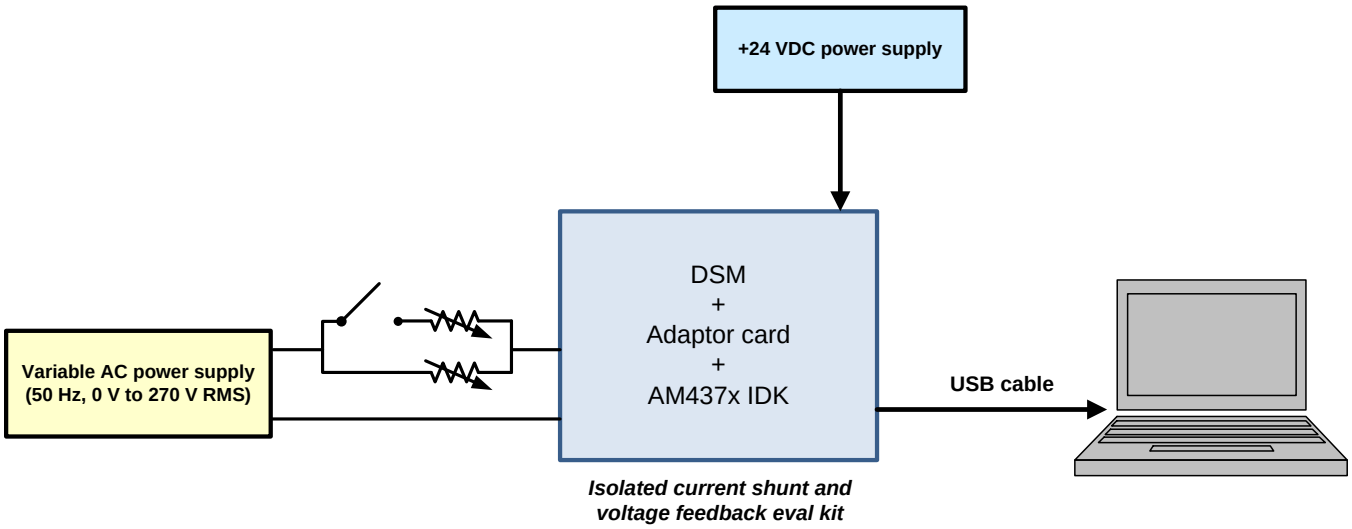


Figure 47. Test Setup for Short Circuit Testing

Figure 48 shows the current waveform captured on an oscilloscope by a current probe when the switch is closed. This waveform is shown in yellow. The second waveform in red is from a GPIO on Jumper J2.8 of the IDK. This GPIO from the AM437x is used to signal the short circuit event. A current probe provides the isolation while measuring signal from different ground references and is needed for conducting this test safely. To compare the accuracy of the short circuit detection on the graph, the value 1.110 A represents 1.25 A because of the current probe attenuation.

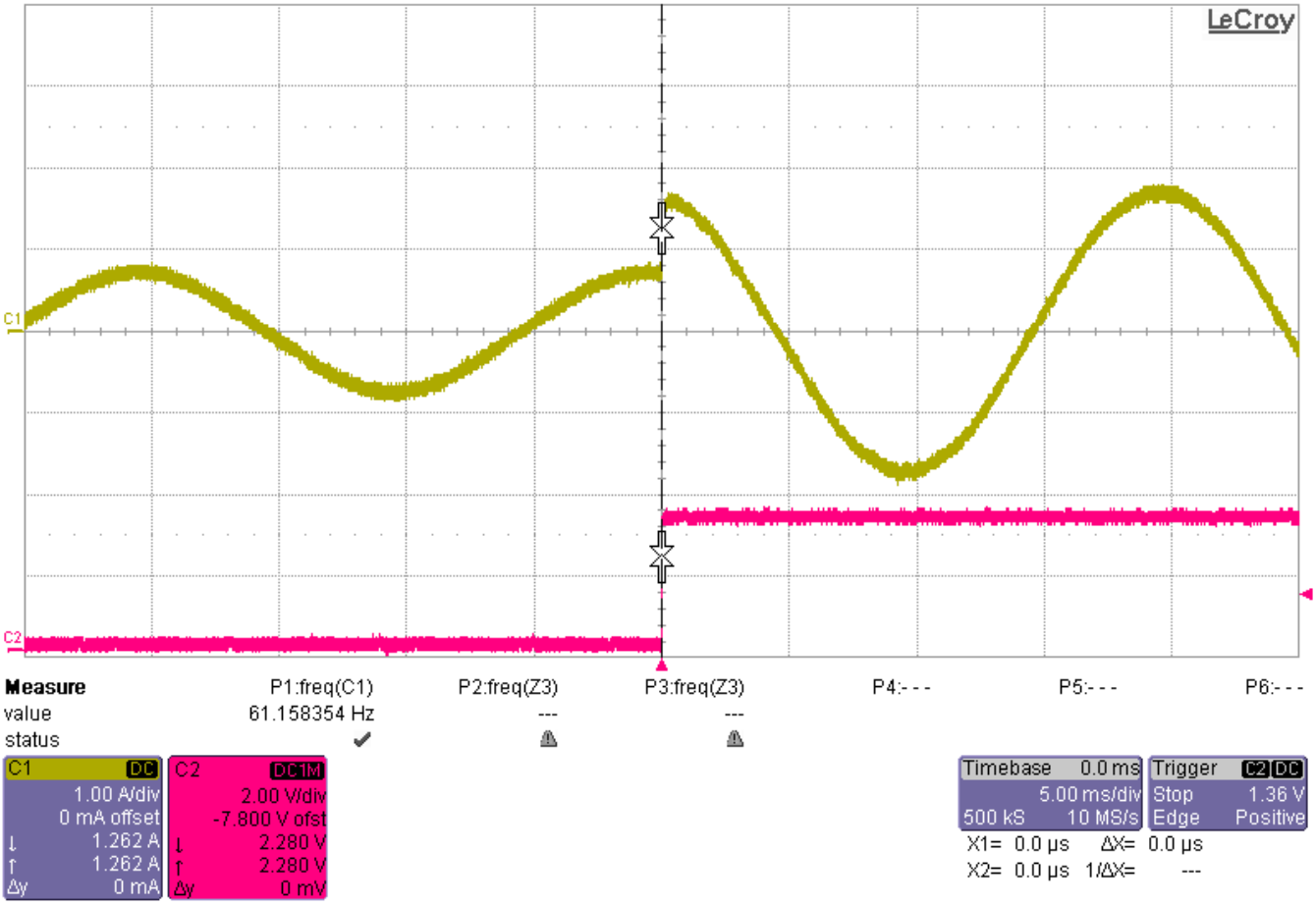


Figure 48. Short Circuit Current Waveform (Yellow) and Signal From AM437x (Red)

In this method, it is difficult to ascertain the exact point where the short circuit event occurred. The waveform shape did change when switch was closed, but at this point the current at the input has not reached the threshold. The time it takes to reach the threshold value in the external circuit is not included as part of the short circuit response time. Therefore, the design needs an ideal waveform from the source, which provides an instantaneous jump from a low value to above the threshold value. This limitation was overcome by removing the AC source and the shunt and using a signal generator. The signal generator is used to apply a signal at the AMC input representing a short circuit condition. A signal generator is set to a square form with peaks crossing ±62.5 mV to represent an equivalent voltage of 1.25 A.

Figure 49 shows the waveform capture. The blue waveform is from the signal generator, and the yellow waveform is the short circuit signal generated by a GPIO on AM437x. The edge of the square wave signal from the generator represents the initiation of short circuit. The time difference from the falling edge of the signal generator to the event being detected is 2.68 µs. The theoretical time delay is equal to the time taken to complete one sample conversion by the comparator module in the SDFM peripheral. The oversampling rate set for short circuit detection is 16 using a Sinc3 filter the time taken is 3 × 16 = 48 clocks; therefore, the time delay is calculated as the time taken to complete 48 modulator clock cycles at 20 MHz. This is 48 × 1 / (20 MHz) = 2.4 µs. The additional delay is due to the GPIO rise time.

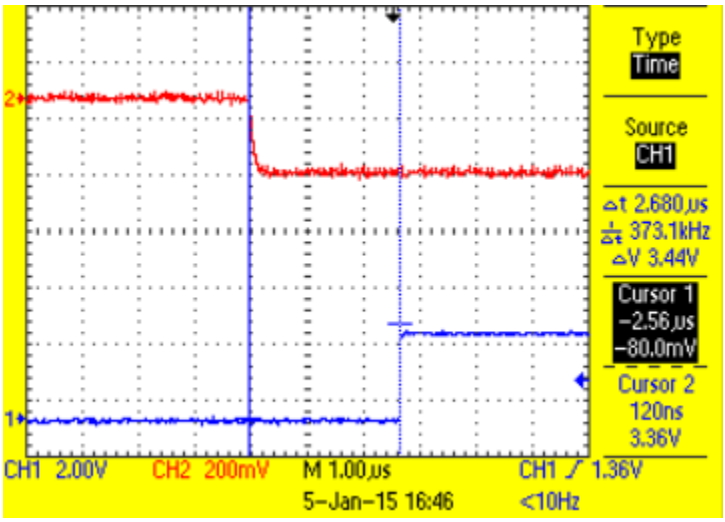


Figure 49. Short Circuit Signal Applied to AMC1304 (Red) and Signal From AM437x (Blue)

8 Design Files

The design files for DSM and AM437x are available on their respective TI Design webpages given below. This section documents only the adaptor card design files.

The design files and schematics for the DSM board can be downloaded from http://www.ti.com/tool/tida-00171.

The design files for SitraTM AM437x IDK can be downloaded from http://www.ti.com/tool/TMDXIDK437X.

8.1 Schematics

To download the most recent schematics, see the design files at TIDA-00209.

8.2 Bill of Materials

To download the most recent bill of materials (BOM), see the design files at TIDA-00209.

8.3 Layer Plots

To download the most recent layer plots, see the design files at TIDA-00209.

8.4 Altium Project

To download the most recent Altium project files, see the design files at TIDA-00209.

8.5 Gerber Files

To download the most recent Gerber files, see the design files at TIDA-00209

8.6 Assembly Drawings

To download the most recent assembly drawings, see the design files at TIDA-00209.

8.7 Software Files

The firmware for Sitara can be found at a date to be determined.

To download the most recent GUI software files, see the design files at TIDA-00171.

9 Terminology

DSM— Delta-Sigma Module

IDK— Industrial Development Kit

GUI— Graphical User Interface

USB— Universal Serial Bus

XDS100V2— USB to JTAG Emulator used for debugging

SoC— System on Chip

OSR— Oversampling Ratio

10 References

1. Texas Instruments, *Isolated Current Shunt and Voltage Measurement Kit*, TIDA-00171 Design Guide (TIDU499)
2. Texas Instruments, *AM437x SYSBIOS Industrial SDK 02.00.00.02 User Guide* (http://processors.wiki.ti.com/index.php/AM437x_SYSBIOS_Industrial_SDK_02.00.00.02_User_Guide)

11 About the Author

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