

TIDA- 00169**Automotive TFT LCD Display Solution - Test Data**

This document shares the test results of the FPD-LinkIII connection between the DS90UH925Q-Q1 EVM and the SAT0059 reference design. Results provided are the Eye Diagram.

Eye Diagram

The test data shown illustrates the quality of the differential signal received by the FPD-Link III deserializer. The FPD-Link III signal is transmitted by the serializer over the shielded twisted pair cable, and the signal quality enhanced by the built-in adaptive equalizer within the deserializer. The eye diagram is measured at the CMLOUT test-point offering a view of the internally equalized differential signal. The CMLOUT test point should always be used to measure the quality of the differential signal for two reasons: 1) this includes the effect of the adaptive equalizer, and 2) since FPD-Link III includes a bi-directional control channel, the quality of the differential signal cannot be measured directly on the input pins of the deserializer. The CMLOUT is enabled via I2C register control.

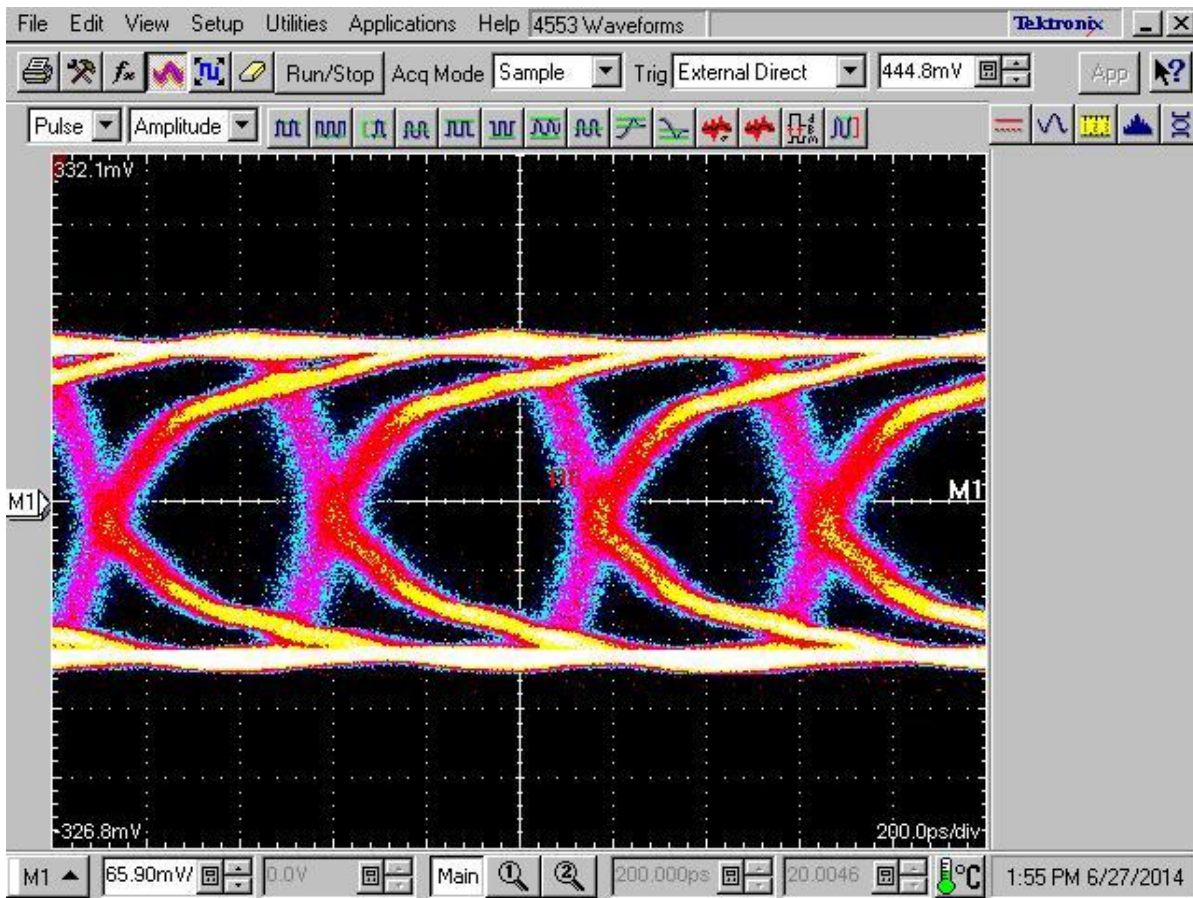


Figure 1. Eye diagram for DS90UB925/926. Clock speed was 27Mhz

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