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TI Designs – Precision: CerTIfied Design

Two-Channel Source/Sink Combined Voltage & Current Output, Isolated, EMC/EMI Tested Reference Design

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Design Resources

Design Archive	All Design files
DAC8563	Product Folder
XTR300	Product Folder
ISO7641	Product Folder

Circuit Description

This two channel combined voltage and current analog output module features two independent outputs that can source and sink voltage and current over the standard industrial output ranges. The possible outputs of the design include: ±24 mA, 4-20 mA, 0-24 mA, 0-5 V, 0-10 V, ±5 V, ±10 V. The design has been successfully tested for immunity to the IEC61000-4 tests.

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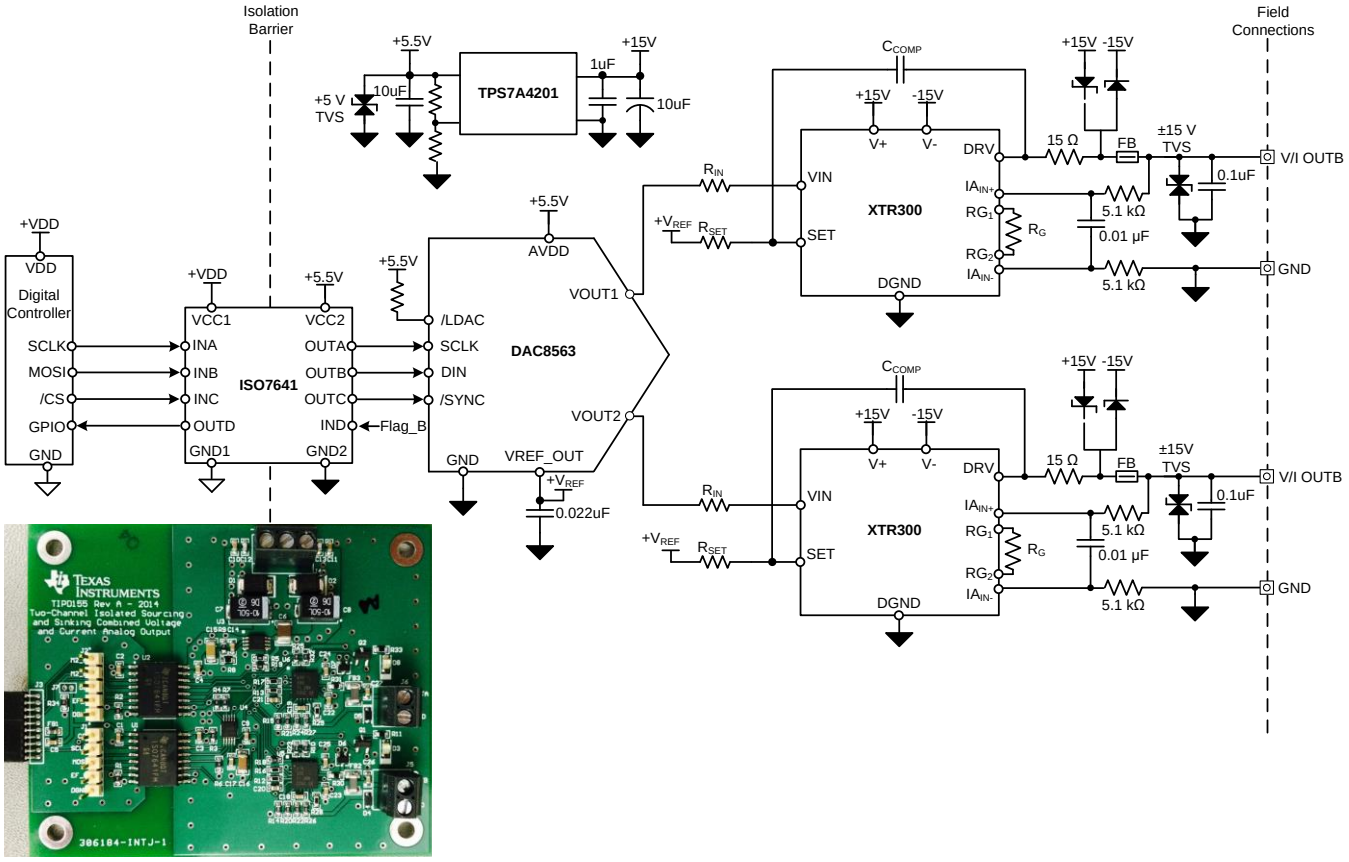

1 Design Summary

The design requirements are as follows:

- Supply Voltage: ±15 V
- Analog Output Channels: 2
- Resolution: 16-Bit
- Digital Input: 3-Wire SPI, ≥ 4 kV Isolation
- Voltage Outputs: ±10 V
- Current Outputs: ±24 mA
- Circuit Protection: Immunity to IEC61000-4 Transient Testing

The design goals and performance for ±10 V and ±24 mA outputs are summarized in Table 1. Figure 1 depicts the total unadjusted error (TUE) of the design measured in both voltage and current output modes. Figure 2 displays the current and voltage output error after a two-point calibration is applied.

Table 1: Comparison of Design Goals, Simulated, and Measured Performance

	Current (±24 mA)			Voltage (±10 V)		
Specification	**Goals**	**Calculated**	**Measured**	**Goals**	**Calculated**	**Measured**
Total Unadjusted Error (TUE)	0.15 %FSR, (0.072 mA)	0.111 %FSR, (0.0533 mA)	0.016 %FSR, (0.0077 mA)	0.15 %FSR, (0.03 V)	0.149 %FSR, (0.029 V)	0.025 %FSR, (0.005 V)
Calibrated Output Error	0.01 %FSR, (0.0048 mA)	0.0117 %FSR, (0.0056 mA)	0.0052 %FSR, (0.0025 mA)	0.01 %FSR, (0.002 V)	0.0117 %FSR, (0.0023 V)	0.0075 %FSR, (0.0015 V)
IEC61000-4 Immunity	Pass	n/a	Pass	Pass	n/a	Pass

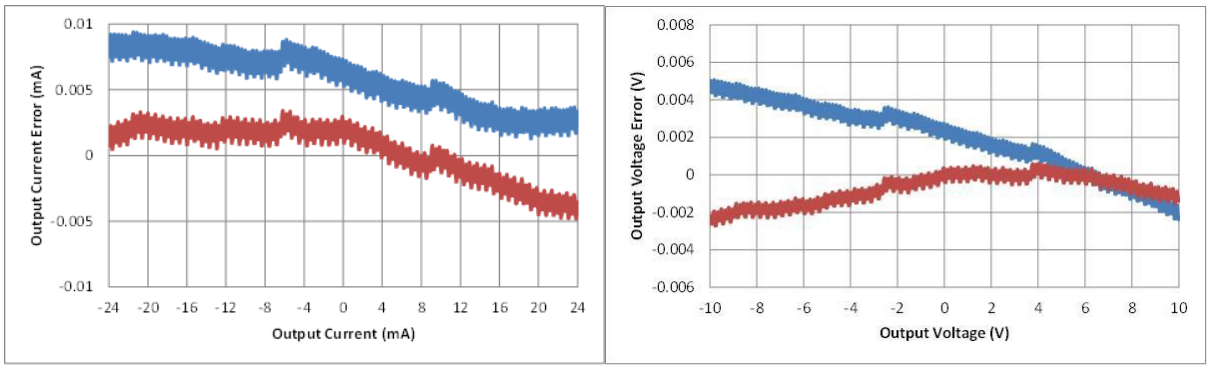

Figure 1: Measured Unadjusted Output Current and Output Voltage Error

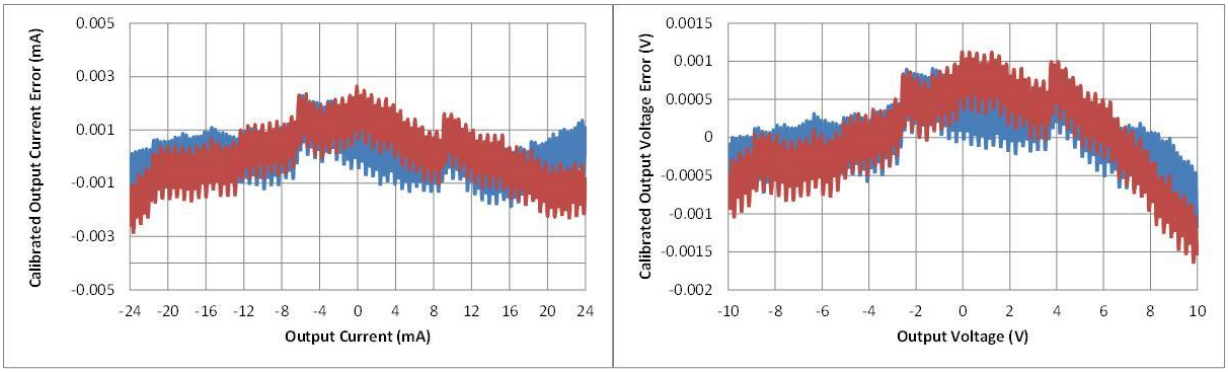

Figure 2: Calibrated Output Current and Output Voltage Error

2 Theory of Operation

The analog output circuitry for this two-channel combined voltage and current output driver is realized with a dual output digital-to-analog converter (DAC) and two industrial voltage/current output driver integrated circuits. The integrated output driver allows for digital selection between voltage, V_{OUT}, and current, I_{OUT}, modes on a combined output pin, reducing connector and wiring costs. Digital isolation for the SPI and GPIO control signals is accomplished using two 4-channel digital isolators. A detailed schematic for the design is shown in Figure 3.

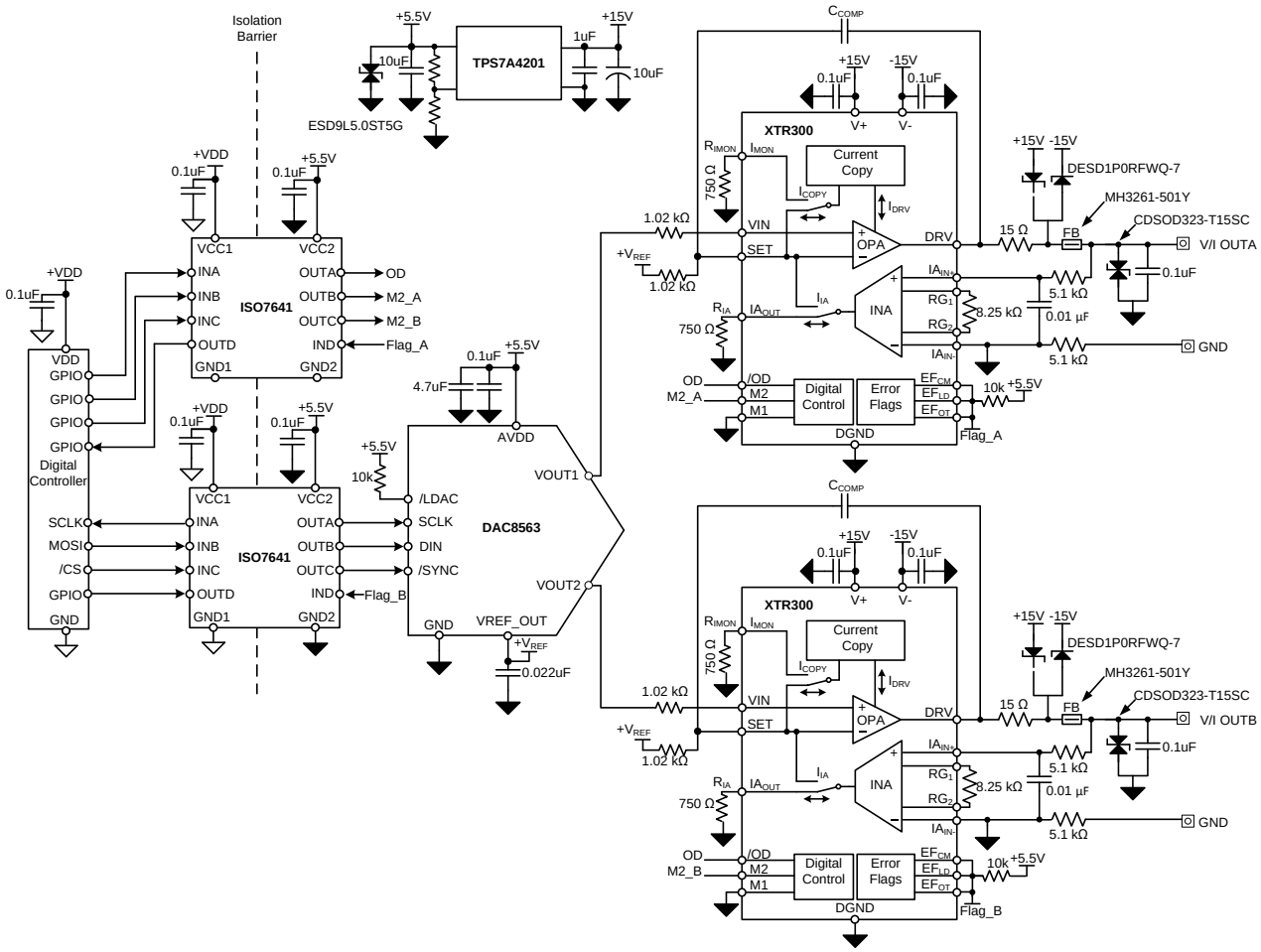

Figure 3: Detailed Schematic

2.1 I_{OUT} Mode

When configured for current mode, the output of the current copy circuitry internal to the XTR300 is routed to the SET pin. This provides feedback for the internal OPA driver based on 1/10th of the output current, resulting in a voltage to current transfer function. To achieve the bipolar current outputs from the single-ended DAC output voltage, V_{DAC}, an offset must be applied to the XTR300 SET pin. This is accomplished by connecting the resistor, R_{SET}, from the SET pin to V_{REF} resulting in the transfer function shown in Equation 1. Figure 4 displays the output driver configured for current mode.

$$I_{OUT} = 10 * \left(\frac{V_{DAC} - V_{REF}}{R_{SET}} \right) \quad (1)$$

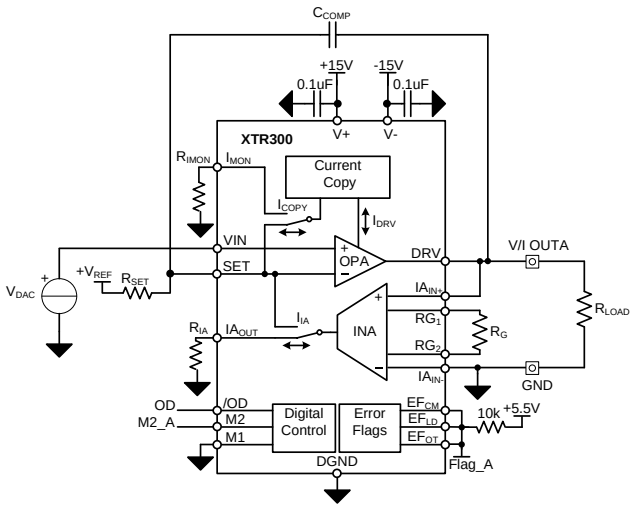

Figure 4: XTR300 Configured for I_{OUT} Mode

While it was not utilized in design, the output of the INA can be monitored at the IA_{OUT} pin which can be used to calculate the load voltage, resistance, and power dissipation.

2.2 V_{OUT} Mode

When configured for voltage mode, the output of the INA internal to the XTR300 is routed to the SET pin creating feedback for the internal amplifier based on INA input voltage. The feedback from the INA provides high impedance remote sensing of the voltage at the output load which can be used to overcome errors from PCB traces and protection component impedances. While it was not utilized in design, a 1/10th copy of the output current of the OPA can be monitored at the I_{MON} pin which can be used to calculate the load resistance or load power.

In V_{OUT} mode the transfer function includes the gain of the INA which is determined by the value of the external gain setting resistor, R_G. Figure 5 displays the output driver configured for voltage mode and Equation 2 displays the transfer function.

$$V_{OUT} = \frac{R_G}{2} * \left(\frac{V_{DAC} - V_{REF}}{R_{SET}} \right) \quad (2)$$

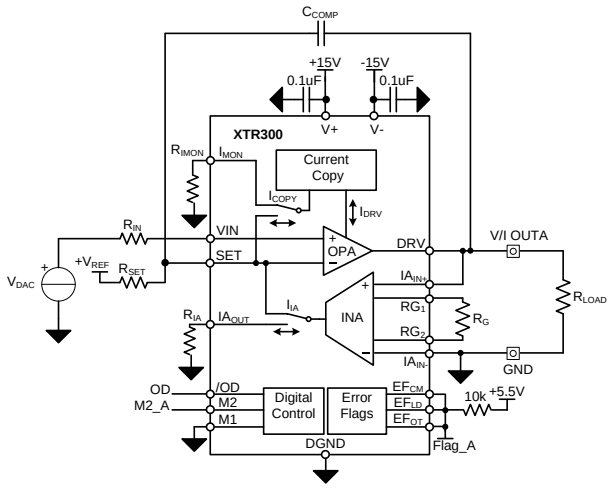

Figure 5: XTR300 Configured for Voltage Mode

3 Component Selection

3.1 DAC – DAC8563

To meet the requirements of this design, a 16-bit dual channel, rail-to-rail voltage-output DAC with an integrated 2.5 V reference is required. Errors from gain, offset, and V_{REF} inaccuracy should be lower than the total unadjusted goals of 0.15 %FSR and the linearity errors should be less than 0.01% to meet the calibrated error goals.

The DAC8563 meets the requirements of the design and offers strong dc performance with typical offset errors of 1 mV, gain errors of 0.01%FSR, and integral non-linearity (INL) errors of ±4 LSB. The max differential non-linearity (DNL) specification of ±1 least significant bit (LSB) provides fully monotonic operation. The internal reference has an initial accuracy of ±5 mV with 4-ppm/°C temperature drift and can source or sink up to 20 mA at the V_{REFIN} /V_{REFOUT} pin.

The DAC8563 device incorporates a power-on-reset circuit that configures the DAC output to mid-scale voltage at power-up which will set the output of the XTR300 to 0V / 0mA at power-up. The versatile 3-wire serial interface is compatible with SPI, QSPI, Microwire interface standards, as well as the serial peripheral in most embedded processors.

3.2 Output Driver – XTR300

The XTR300 is a complete single-channel output driver for industrial and process control applications. It is capable of sourcing and sinking voltage and current over the standard industrial output ranges which are configured through external gain setting resistors. The output can be configured for I_{OUT} or V_{OUT} mode based on a digital control signal. The XTR300 features strong dc performance with typical offset voltage of 400 µV and drift of 1.6 µV/°C. Typical gain errors of 0.04% FSR and linearity errors of 0.01% FSR make this a good choice given the accuracy goals in this design.

The three open collector error signals are provided to indicate output related error. These include over-current or open-load errors (EF_{LD}), exceeding the common-mode input range at the IA inputs (EF_{CM}), and over-temperature warnings (EF_{OT}). Isolated monitoring of the error flags for both XTR300 devices is accomplished in this design by OR'ing the three open-collector error flags for each XTR300 and then sending them individually through the digital isolator.

Load monitoring is possible in both V_{OUT} and I_{OUT} modes using the I_{MON} and IA_{OUT} pins..

3.3 Digital Isolator – ISO7641FC

In order to maintain isolation from the host controller, the digital signals used to control the DAC and XTR300 must be isolated through a digital isolator. The ISO764XFC family of digital isolators supports data rates up to 25 MBPS with greater than 4 kV of galvanic isolation.

There were a total of six digital outputs and two digital inputs required to communicate with the DAC and control and monitor the XTR300 outputs. Therefore two ISO7641 devices were used which each feature three output channels and one input channel.

3.4 Passive Component Selection

The R_{SET} and R_G resistor values are determined based on the desired output ranges and the V_{DAC} and V_{REF} voltages. Equation 1 can be rearranged to calculate R_{SET} for the desired ±24 mA output range as shown in Equation 3. The system will be designed with a V_{DAC} voltage range of 0.04 V to 4.96 V to operate the DAC8563 in the specified linear output range from codes 512 to 65024.

$$R_{SET} = 10 \cdot \left(\frac{V_{DAC} - V_{REF}}{I_{OUT}} \right) = 10 \cdot \left(\frac{4.96\,V - 2.5\,V}{0.024\,A} \right) = 1025\Omega \quad (3)$$

R_{SET} was selected to be 1.02 kΩ based on availability of 0.1% tolerance components. Lower unadjusted error can be achieved by selecting a lower tolerance R_{SET} resistor to match the 0.01% typical gain error specification of the XTR300.

Equation 2 can be rearranged to calculate the R_G value based on the same V_{DAC} voltage range and the desired ±10 V V_{OUT} voltage range as shown in Equation 4.

$$R_G = \frac{2 \cdot V_{OUT\_MAX} \cdot R_{SET}}{V_{DAC} - V_{REF}} = \frac{2 \cdot 10\,V \cdot 1020\Omega}{4.96\,V - 2.5\,V} = 8292\Omega \quad (4)$$

The closest standard 0.1% tolerance resistor values are 8.25 kΩ and 8.45 kΩ. While the 8.25 kΩ resistor results in output voltages slightly outside of the specified V_{DAC} linear output range it was selected due to closer proximity to the calculated value. Again, lower unadjusted error can be achieved by selecting a lower tolerance R_{SET} resistor to match the 0.01% typical gain error specification of the XTR300.

The V_{DAC} voltages corresponding to the specified maximum and minimum outputs for both I_{OUT} and V_{OUT} are shown in Table 2.

Table 2: V_{DAC} Outputs for Desired I_{OUT} and V_{OUT} Ranges

Output Level	V_{DAC} (V)	V_{DAC} SPAN (V)
-24 mA	0.0520	4.896
+24 mA	4.9480	
-10 V	0.0273	4.9454
+10 V	4.9727	

The inputs to the INA have been filtered to reduce extrinsic noise sources at frequencies above 4 kHz. The filter resistors have been selected to be 5.1 kΩ to protect the XTR inputs from low-level transient voltages that are above the XTR300 supply voltage but below the clamp voltage of the external protection circuitry. The capacitor was sized to be 0.01 µF resulting in the differential filter cutoff frequency shown in Equation 5.

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot (5100 + 5100) \cdot 0.01\mu F} = 3.98\,kHz \quad (5)$$

R_{IMON} and R_{IA} have been selected to be 750 Ω to properly load the monitor outputs.

The C_{COMP} capacitor compensates the control loop for the XTR300 providing a stable output with output capacitance. The datasheet recommended value of 47 nF has been selected based on the 100 nF output capacitor and INA input filter.

3.5 Protection Component Selection

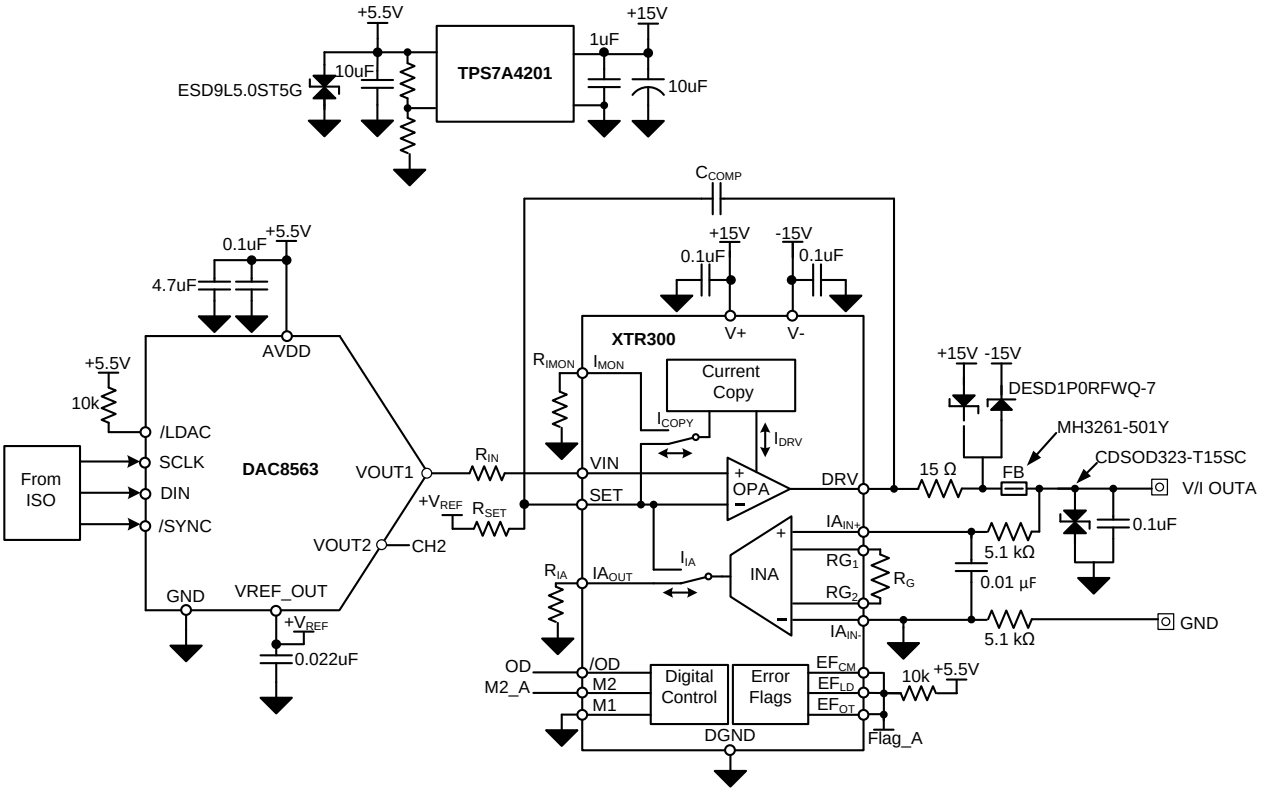

Figure 6: Simplified Schematic Showing Output Protection Components

The protection scheme in this design, shown in Figure 6, is intended to provide immunity to transient voltage disturbances as described in the IEC61000-4 tests. The IEC61000-4 transients have two components: a high frequency component and a high energy component. Therefore the protection strategy focuses on attenuating the high frequency transients and diverting the energy from the high energy components away from the sensitive circuitry.

Attenuation is achieved through resistors and capacitors that attenuate high-frequency transients and also limit series current. Ferrite beads are used to maintain dc accuracy while still limiting current from high frequency transients. Capacitors placed directly at the output terminals help attenuate transient energy from high frequency tests such as electrostatic discharge (ESD) and electrically fast transients (EFT).

Diverting the large energy transients to GND or the supply rails is accomplished using transient voltage suppressor (TVS) diodes and clamp-to-rail diodes. The protection scheme must limit the level of the voltage transients to a level less than the absolute maximum rating for the output of the XTR300. More information on the IEC61000-4 tests and the protection circuitry requirements can be obtained in TIPD153.

3.5.1 Passive Components

The capacitors placed on the output terminals of the voltage and current outputs are used in combination with the transient generator's source impedance to attenuate the transient energy before it is diverted by the TVS diodes or Schottky diodes. The 0.1 µF size of the capacitor plays a key role in delivering class A performance in the IEC61000-4 ESD and EFT tests, at the cost of system bandwidth.

A 15 Ω resistor and a ferrite bead are placed between the XTR300 output and the output terminal. The resistor will limit the dc current and the ferrite bead has an impedance of 500 Ω at 100 MHz providing a large series impedance for high frequency transients. The ferrite bead also acts as a pass element to limit the current between the TVS diode and the Schottky diode.

3.5.2 TVS Diode

A bidirectional TVS diode can be used to divert high voltage transients to ground for systems that utilize symmetrical supply voltages, such as ±15 V. For non-symmetrical supply voltages two unidirectional TVS diodes must be used. In both cases, diode selection is based on working voltage, breakdown voltage, and power rating.

To match the ±15 V power-supply voltages, a bidirectional TVS diode with a working voltage of ±15 V, a breakdown voltage of ±16.7 V and power rating of 400 W was chosen.

3.5.3 Schottky Diode

All Schottky diodes feature low forward voltage drop for lower currents, but the forward voltage drop will increase when exposed to excessive current. The Schottky diode used in this design must maintain low enough forward voltage drop to keep the voltage at the input terminals within the absolute maximum ratings for all components connected to the output terminals. The diode used in this design features forward voltage drop of 1.5 V when 1 A is flowing through the diode.

4 Circuit Performance Calculations

4.1 I_{OUT} Accuracy

The I_{OUT} circuit performance is based on the specifications of the DAC8563, XTR300, and the R_{SET} transfer function setting resistor. The typical dc performance specifications of the DAC8563 are displayed in Table 3.

Table 3: Typical DAC8563 Performance Specifications

DAC8563 Specification	Typical Value
Offset (mV)	±1
DNL (LSB)	±0.2
INL (LSB)	±4
Gain error (%FSR)	±0.01
V_{REF} Accuracy (mV)	±0.1

To achieve the current output of ±24 mA, the output range of the DAC8563 is from 0.052V to 4.948V resulting in an input voltage span of 4.896V. Using the input span and the specifications of the DAC8563, the total unadjusted error, TUE, of the DAC8563 can be calculated as shown in Equation 6.

$$I_{TUE\_DAC}(\%FSR) = \left(\sqrt{\left(\frac{V_{OS}}{V_{IN\_SPAN}}\right)^2 + \left(\frac{INL_{LSB}}{N_{BITS}}\right)^2 + \left(\frac{Gain_{ERROR}\%}{100}\right)^2 + \left(\frac{V_{REF\_ERROR}}{V_{REF}}\right)^2} \right) \times 100$$

$$I_{TUE\_DAC}(\%FSR) = \left(\sqrt{\left(\frac{1mV}{4.896V}\right)^2 + \left(\frac{4}{2^{16}}\right)^2 + \left(\frac{0.01}{100}\right)^2 + \left(\frac{0.1mV}{2.5V}\right)^2} \right) \times 100 = 0.0239\%FSR \quad (6)$$

Applying a two-point calibration to the design will remove the effects of gain and offset errors leaving only the linearity errors of the DAC8563 as shown in Equation 7.

$$I_{CAL\_DAC}(\%FSR) = \left(\sqrt{\left(\frac{INL_{LSB}}{N_{BITS}} \right)^2} \right) \times 100$$
$$I_{CAL\_DAC}(\%FSR) = \left(\sqrt{\left(\frac{4}{2^{16}} \right)^2} \right) \times 100 = 0.0061\%FSR \quad (7)$$

The XTR300 performance specifications in I_{OUT} mode, including the effects of R_{SET}, are displayed in Table 4. Errors from V_{REF} form an offset error in the XTR300 circuit performance because V_{REF} is used to offset the DAC output voltage and is part of the XTR300 circuit transfer function.

Table 4: Typical XTR300 Circuit I_{OUT} Performance Specifications

Output Range	XTR300 Specification	Typical Value
Current (±24 mA)	Offset (mV)	±0.4
	Nonlinearity (%FSR)	±0.01
	Gain Error (%FSR)	±0.04
	V_{REF} Accuracy (mV)	±0.1
	R_{SET} Tolerance (%)	±0.1

Using these specifications and the DAC8563 output range, the TUE of the XTR300 can be calculated as shown in Equation 8. The calculations show that the R_{SET} resistor tolerance is the largest error source. Lower tolerance resistors can be used to decrease the total unadjusted error at the expense of increased system cost.

$$I_{TUE\_XTR}(\%FSR) = \left(\sqrt{\left(\frac{V_{OS}}{V_{IN\_SPAN}} \right)^2 + \left(\frac{Gain_{ERROR}(\%)}{100} \right)^2 + \left(\frac{Nonlinearity(\%)}{100} \right)^2 + \left(\frac{V_{REF\_ERROR}}{V_{IN\_SPAN}} \right)^2 + \left(\frac{R_{SET\_TOL}}{100} \right)^2} \right) \times 100$$
$$I_{TUE\_XTR}(\%FSR) = \left(\sqrt{\left(\frac{0.4mV}{4.896V} \right)^2 + \left(\frac{0.04}{100} \right)^2 + \left(\frac{0.01}{100} \right)^2 + \left(\frac{0.1mV}{4.896V} \right)^2 + \left(\frac{0.1}{100} \right)^2} \right) \times 100 = 0.1085\% \quad (8)$$

Applying a two-point calibration to the design will remove the effects of gain and offset errors leaving only the linearity errors of the XTR300 as shown in Equation 9.

$$I_{CAL\_XTR}(\%FSR) = \left(\sqrt{\left(\frac{Nonlinearity(\%)}{100} \right)^2} \right) \times 100$$
$$I_{CAL\_XTR}(\%FSR) = \left(\sqrt{\left(\frac{0.01}{100} \right)^2} \right) \times 100 = 0.01\%FSR \quad (9)$$

Since the DAC error and the XTR error are uncorrelated, a probable full system TUE for ±24mA outputs can be calculated by taking the root of the sum of squares (RSS) of the individual errors from the DAC8563 and XTR300 as shown in Equation 10.

$$I_{TUE\_TOTAL}(\%FSR) = \sqrt{I_{TUE\_DAC}(\%FSR)^2 + I_{TUE\_XTR}(\%FSR)^2} = \sqrt{(0.024\%)^2 + (0.108\%)^2} = 0.111\% \quad (10)$$

The final calibrated results are shown in Equation 11.

$$I_{CAL\_TOTAL}(\%FSR) = \sqrt{I_{CAL\_DAC}(\%FSR)^2 + I_{CAL\_XTR}(\%FSR)^2} = \sqrt{(0.00611)^2 + (0.01)^2} = 0.0117\%FSR \quad (11)$$

For worst case analysis using the maximum datasheet values, see Appendix A.3.1.

4.2 V_{OUT} Accuracy

The V_{OUT} accuracy is based on the errors from the DAC8563, XTR300, R_{SET}, and R_G. The same performance specifications apply for the DAC8563 in V_{OUT} mode as they did in I_{OUT} mode. However, the DAC output voltage has a span of 4.945 V for a ±10 V output resulting in a slightly lower error as shown in Equation 12.

$$V_{TUE\_DAC} = \left(\sqrt{\left(\frac{V_{OS}}{V_{IN\_SPAN}}\right)^2 + \left(\frac{INL_{LSB}}{N_{BITS}}\right)^2 + \left(\frac{Gain_{ERROR}\%}{100}\right)^2 + \left(\frac{V_{REF\_ERROR}}{V_{REF}}\right)^2} \right) \times 100$$

$$V_{TUE\_DAC} = \left(\sqrt{\left(\frac{1mV}{4.945V}\right)^2 + \left(\frac{4}{2^{16}}\right)^2 + \left(\frac{0.01}{100}\right)^2 + \left(\frac{0.1mV}{2.5V}\right)^2} \right) \times 100 = 0.0237\%FSR \quad (12)$$

The XTR300 performance specifications in V_{OUT} mode, including the effects of R_{SET} and R_G, are displayed in Table 5.

Table 5: Typical XTR300 Circuit VOUT Performance Specifications

Output Range	XTR300 Specification	Typical Value
Voltage (±10 V)	Offset (mV)	±0.4
	Nonlinearity (%FSR)	±0.01
	Gain error (%FSR)	±0.04
	V_{REF} Accuracy (mV)	±0.1
	R_{SET} Tolerance (%)	±0.1
	R_G Tolerance (%)	±0.1

The TUE of XTR300 in V_{OUT} mode is calculated in Equation 13. The calculations show that the R_{SET} and R_G resistor tolerances are the largest error sources. Lower tolerance resistors can be used to reduce the total unadjusted error.

$$V_{TUE\_XTR}(\%FSR) = \left(\sqrt{\left(\frac{V_{OS}}{V_{IN\_SPAN}}\right)^2 + \left(\frac{Gain_{ERROR}(\%)}{100}\right)^2 + \left(\frac{Nonlinearity(\%)}{100}\right)^2 + \left(\frac{V_{REF\_ERROR}}{V_{IN\_SPAN}}\right)^2 + \left(\frac{R_{SET\_TOL}}{100}\right)^2 + \left(\frac{R_{G\_TOL}}{100}\right)^2} \right) \times 100$$

$$V_{TUE\_XTR}(\%FSR) = \left(\sqrt{\left(\frac{0.4mV}{4.945V}\right)^2 + \left(\frac{0.04}{100}\right)^2 + \left(\frac{0.01}{100}\right)^2 + \left(\frac{0.1mV}{4.945V}\right)^2 + \left(\frac{0.1}{100}\right)^2 + \left(\frac{0.1}{100}\right)^2} \right) \times 100 = 0.1494\%FSR \quad (13)$$

A two-point calibration will reduce the V_{OUT} errors to the linearity error of the XTR300 as shown in Equation 14.

$$V_{CAL\_XTR}(\%FSR) = \left(\sqrt{\left(\frac{Nonlinearity(\%)}{100}\right)^2} \right) \times 100$$

$$V_{CAL\_XTR}(\%FSR) = \left(\sqrt{\left(\frac{0.01}{100}\right)^2} \right) \times 100 = 0.01\%FSR \quad (14)$$

The V_{OUT} circuit TUE is calculated in Equation 15 using the DAC8563 and XTR300 TUE results.

$$V_{TUE\_TOTAL}(\%FSR) = \sqrt{V_{TUE\_DAC}(\%FSR)^2 + V_{TUE\_XTR}(\%FSR)^2} = \sqrt{(0.023\%)^2 + (0.14754\%)^2} = 0.1494\% \quad (15)$$

The final calibrated V_{OUT} results are calculated in Equation 16.

$$V_{CAL\_TOTAL}(\%FSR) = \sqrt{V_{CAL\_DAC}(\%FSR)^2 + V_{CAL\_XTR}(\%FSR)^2} \left(\sqrt{(0.00610)^2 + (0.01)^2} \right) \times 100 = 0.0117\%FSR \quad (16)$$

For worst case analysis using the maximum datasheet values, see Appendix A.3.2.

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.1.

5.1 PCB Layout

For optimal performance of this design follow standard precision PCB layout guidelines, including proper decoupling close to all mixed signal integrated circuits and providing adequate power and GND connections with large copper pours. The INA input signals should be routed directly from the output terminal to reduce errors from PCB wiring resistance that would be present if it was connected to V_{OUT} before the output terminal.

Additional considerations must be made for providing robust EMC/EMI immunity. All protection elements should be placed as close to the output connectors as possible to provide a controlled return path for transient currents that does not cross sensitive components. Optimal dissipation of the transient energy occurs with wide, low-impedance, low-inductance traces along the output signal path and protection elements. When possible, copper pours are used in place of traces. Stitching the GND pours provides an effective return path around the PCB and helps reduce the impact of radiated emissions.

The layout for the design is shown in Figure 7.

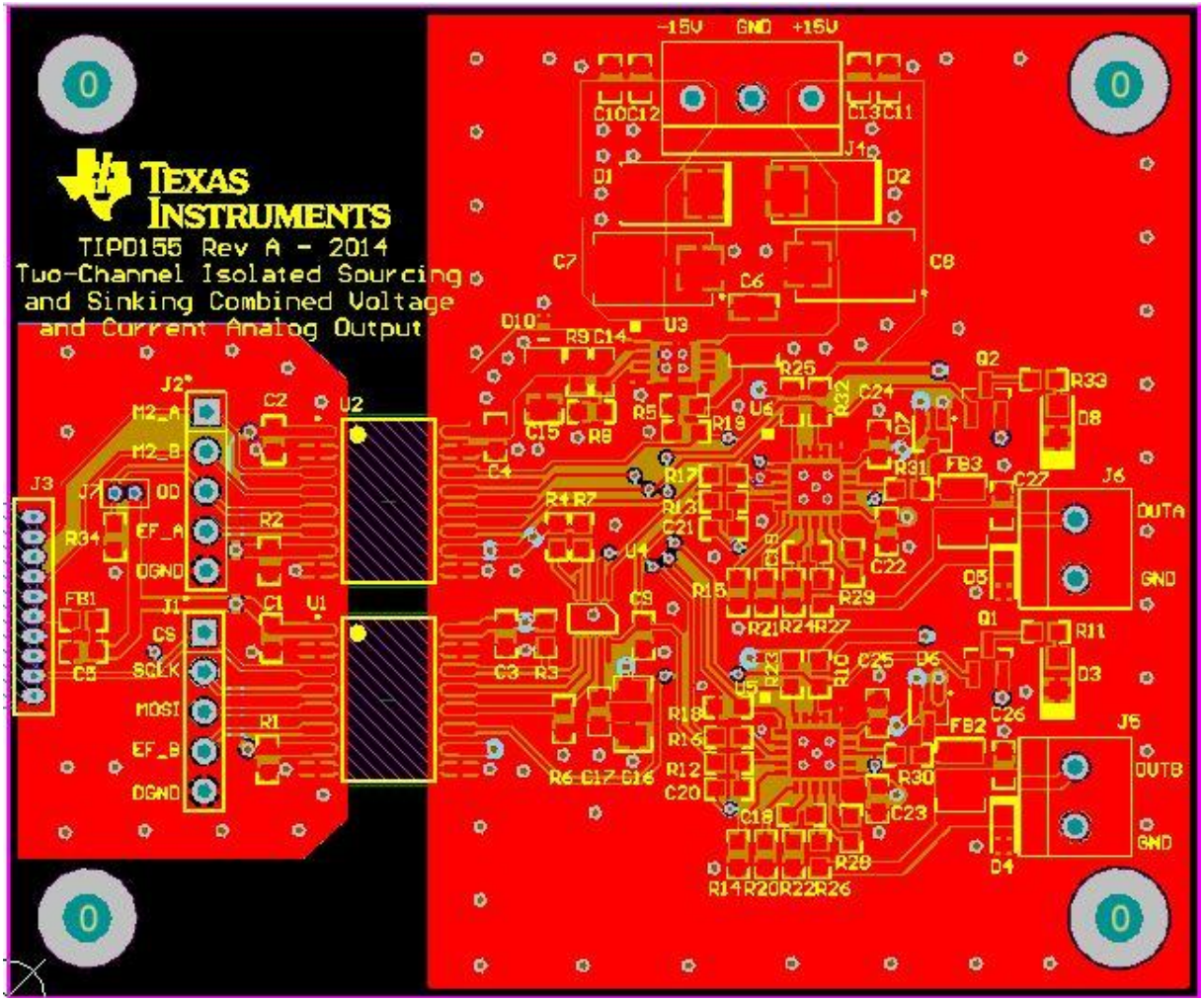

Figure 7: Altium PCB Layout

6 Verification and Measured Performance

6.1 ±24 mA I_{OUT} Results

DC transfer function data for both I_{OUT} channels in ±24 mA mode was collected using 8.5 digit multi-meters to measure the output current of the circuit while driving 500 Ω loads. The measurement results are shown in Figure 8.

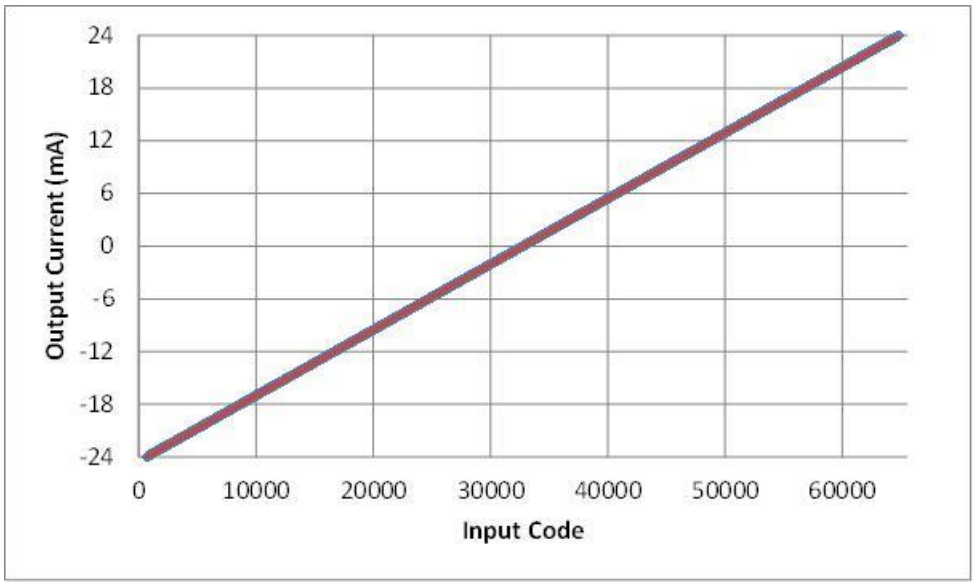

Figure 8: Output Current vs. Input Code for CH1 (red) and CH2 (blue)

The measured output current error for both channels is shown in Figure 9. The unadjusted current output of CH2 showed higher error at around 8 µA. This correlates to 0.016%FSR for the ±24 mA output span, which is much less than the calculated value of 0.111%FSR. The discrepancy between the measured and calculated results was a result of the tested R_{SET} resistances being more precise than the maximum tolerance of 0.1% used in the calculations.

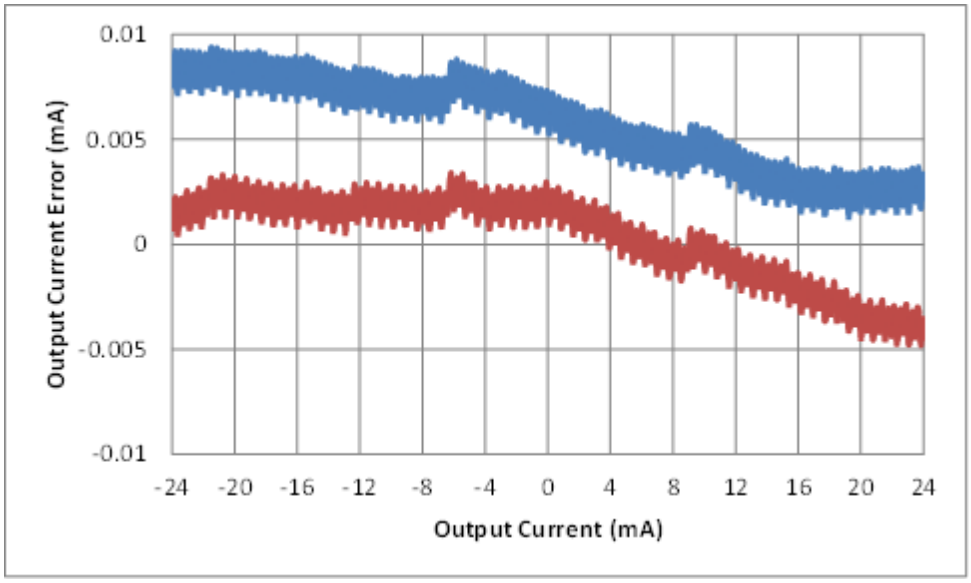

Figure 9: Output Current Error vs. Input Code for CH1 (red) and CH2 (blue)

Applying a two-point gain and offset calibration to the results produces the final results shown in Figure 10. The final calibrated error is about 2.5 µA or 0.0052% FSR which is within the range of the calculated value of 0.0117% FSR.

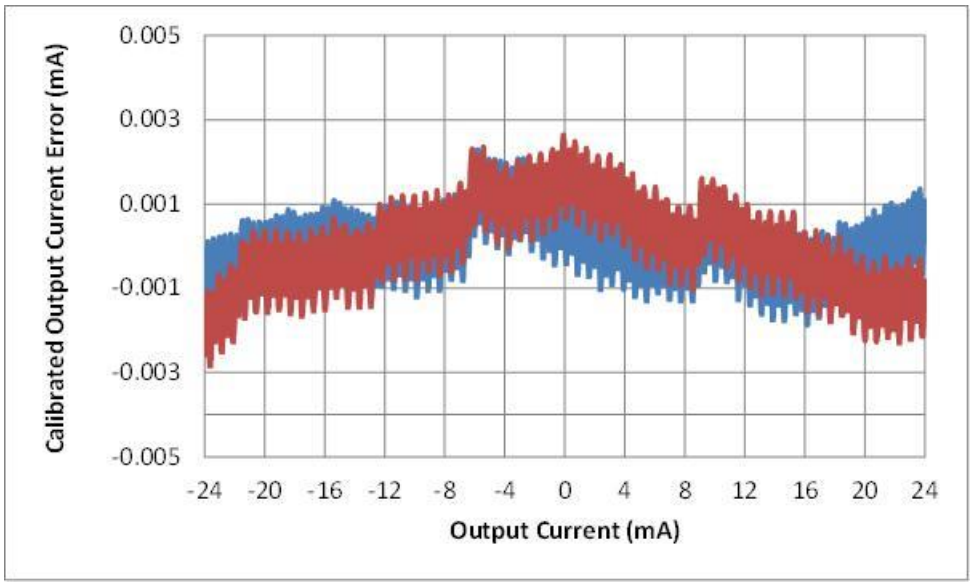

Figure 10: Calibrated Output Current Error vs. Input Code for CH1 (red) and CH2 (blue)

Measurements showing the errors of the DAC8563 and XTR300 separately can be seen in Appendix A.4 and Appendix A.5 respectively.

6.2 ±10 V V_{OUT} Results

DC transfer function data for both V_{OUT} channels in ±10 V mode was collected using 8.5 digit multi-meters to measure the output voltage of the circuit while driving 1 kΩ loads. The measurement results are shown in Figure 11.

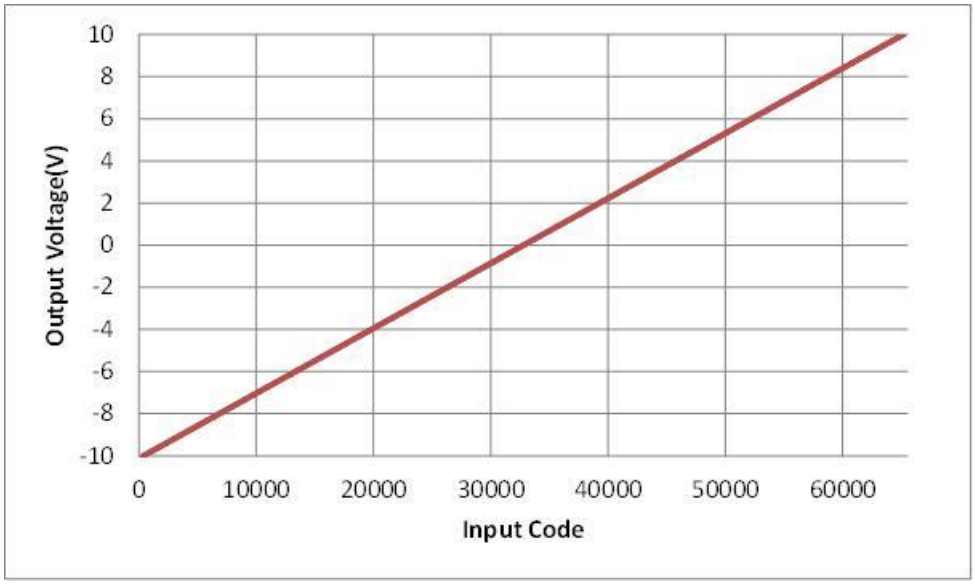

Figure 11: Output Voltage vs. Input Code for CH1 (red) and CH2 (blue)

The output voltage error for both channels is shown in Figure 12. The unadjusted voltage output of CH2 displays higher error at around +5 mV. This correlates to 0.025%FSR for the ±10 V output span.

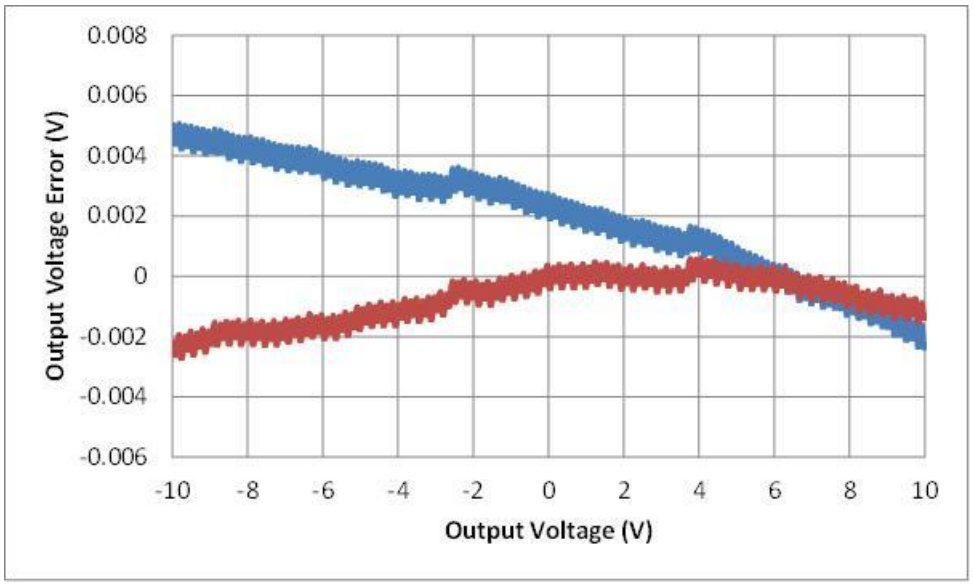

Figure 12: Output Voltage Error vs. Input Code for CH1 (red) and CH2 (blue)

Applying a two-point gain and offset calibration to the results produces the final results shown in Figure 13. The final calibrated error is about 1.5 mV or 0.0075% FSR.

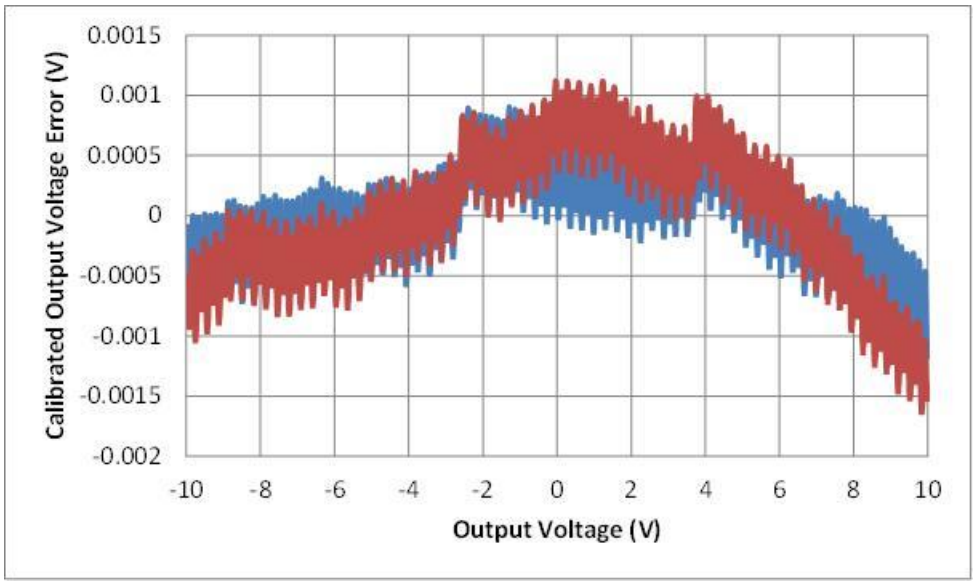

Figure 13: Calibrated Output Voltage Error vs. Input Code for CH1 (red) and CH2 (blue)

Measurements showing the errors of the DAC8563 and XTR300 separately can be seen in Appendix A.4 and Appendix A.6 respectively.

6.3 Measured Result Summary

The measured performance is summarized in Table 6.

Table 6: Comparison of Design Goals, Simulated, and Measured Performance

	Current (±24 mA)			Voltage (±10 V)		
Specification	**Goals**	**Calculated**	**Measured**	**Goals**	**Calculated**	**Measured**
Total Unadjusted Error (TUE)	0.15 %FSR, (0.072 mA)	0.111 %FSR, (0.0533 mA)	0.016 %FSR, (0.0077 mA)	0.15 %FSR, (0.03 V)	0.149 %FSR, (0.029 V)	0.025 %FSR, (0.005 V)
Calibrated Output Error	0.01 %FSR, (0.0048 mA)	0.0117 %FSR, (0.0056 mA)	0.0052 %FSR, (0.0025 mA)	0.01 %FSR, (0.002 V)	0.0117 %FSR, (0.0023 V)	0.0075 %FSR, (0.0015 V)

The calculated results are much higher than the measured results because the resistor tolerance specification used in the calculations is a maximum specification producing a worst-case calculation. Typical specification values were used for the DAC8563 and XTR300 to represent a typically produced system. Using a lower tolerance resistor will increase the design cost but will lower the calculated performance values.

7 Certification Testing Results

Class A performance for this EUT will be assigned for outputs that stay within 0.1% FSR of their intended value, during exposure to each IEC61000-4 disturbance. The DAC outputs were programmed to static dc levels before the tests and were not communicated with while the tests were active. The immunity testing was performed on both the voltage and current outputs with the outputs programmed to both ¼ and ¾ scale to test the immunity while sourcing and sinking. The IEC61000-4 certifications do not specify what supporting equipment is used to monitor the output of the EUT. For this design, an Agilent 34401A 6.5 digit digital multi-meter with resolution set to fast 5.5 digit mode was selected to monitor the outputs in either current or voltage mode.

7.1 IEC61000-4-2: ESD (Electrostatic Discharge)

ESD tests were conducted at ±8 kV vertical and horizontal coupling plane and ±15 kV air discharge. ESD had minimal effect on the current and voltage outputs of the system. During and after the tests the output stayed within 0.1% FSR of the output value. Table 7 summarizes the results of the ESD tests. Figure 14 through Figure 19 show the outputs during each test.

Table 7. IEC61000-4-2 Results

Output	Test	Level	Result	Class
Current (±24 mA)	**Horizontal Coupling Plane**	8 kV	Pass	A
	Vertical Coupling Plane	8 kV	Pass	A
	Air Discharge	15 kV	Pass	A
Voltage (±10 V)	**Horizontal Coupling Plane**	8 kV	Pass	A
	Vertical Coupling Plane	8 kV	Pass	A
	Air Discharge	15 kV	Pass	A

7.1.1 I_{OUT} ESD Results

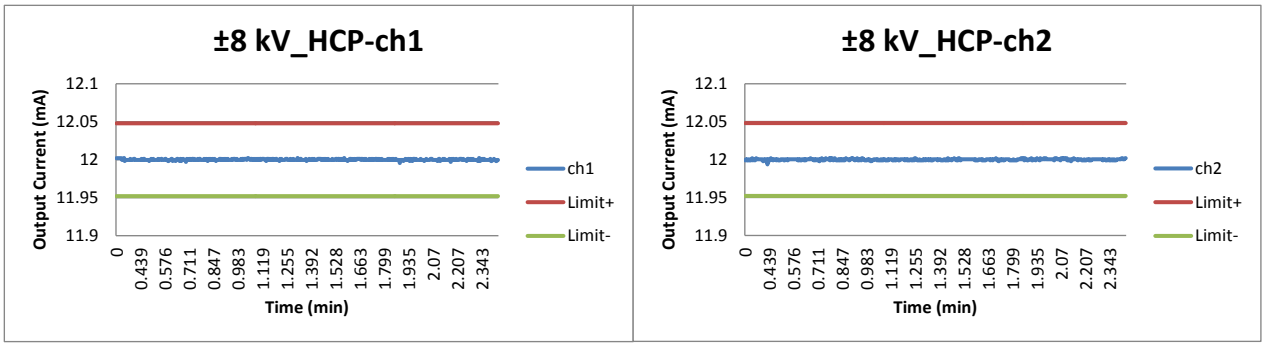

Figure 14: I_{OUT} ±8 - kV ESD Horizontal Coupling Plane (HCP) ch1 and ch2

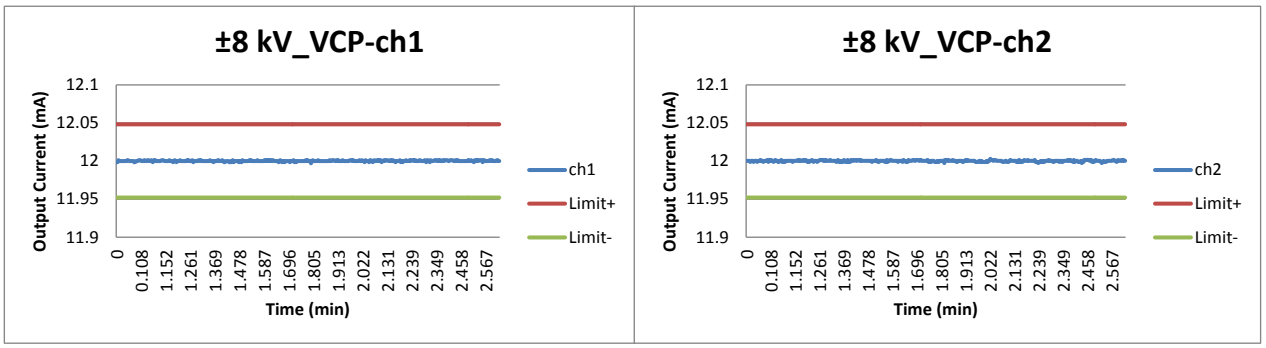

Figure 15: I_{OUT} ±8 - kV ESD Vertical Coupling Plane (VCP) ch1 and ch2

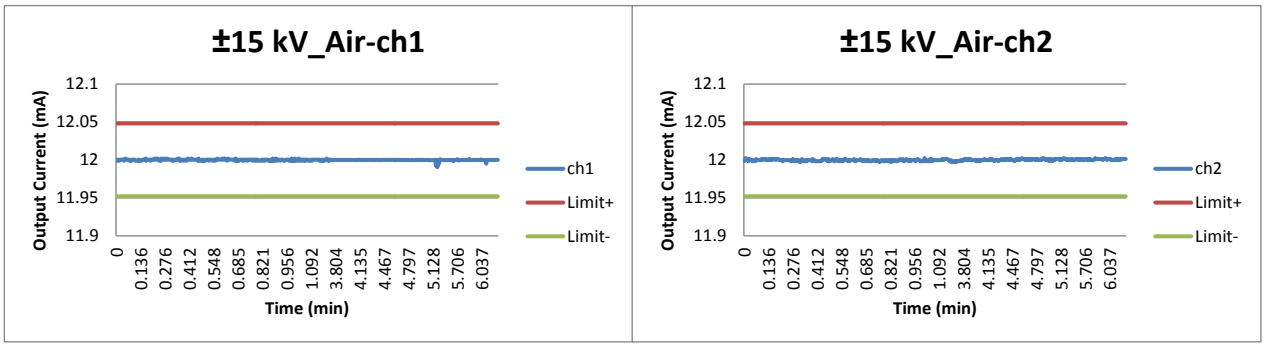

Figure 16: I_{OUT} - ±15 kV ESD Air Discharge ch1 and ch2

7.1.2 V_{OUT} ESD Results

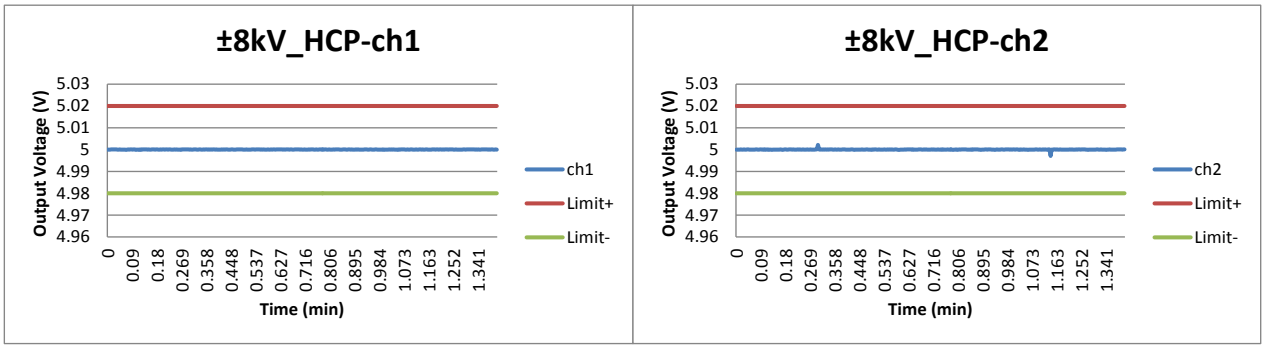

Figure 17: V_{OUT} - ±8 kV ESD Horizontal Coupling Plane (HCP) ch1 and ch2

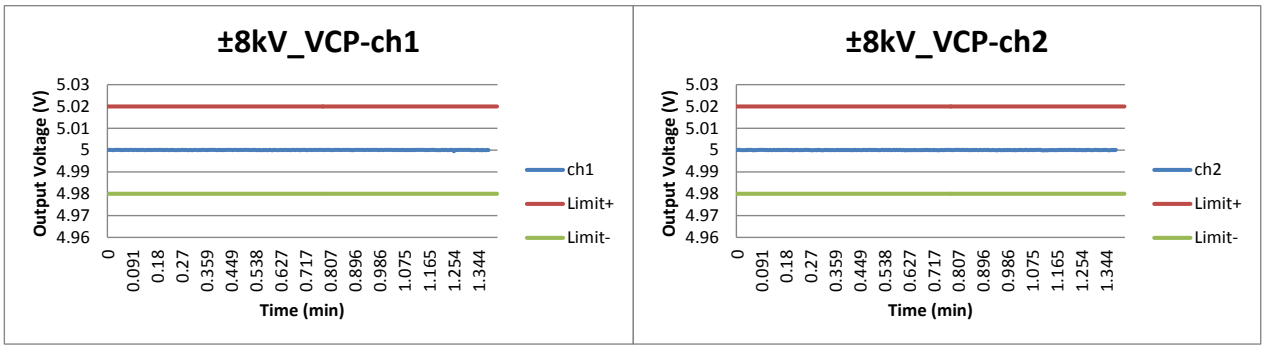

Figure 18: V_{OUT} - ±8 kV ESD Vertical Coupling Plane (VCP) ch1 and ch2

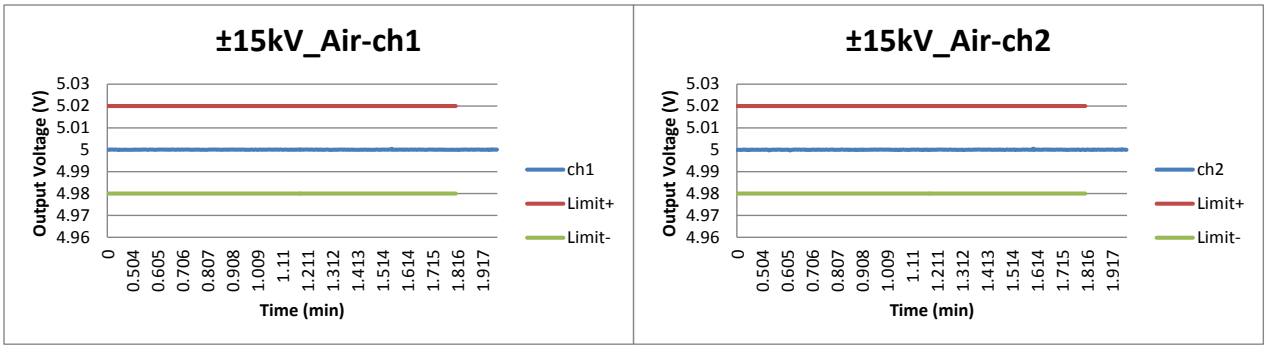

Figure 19: I_{OUT} - ±15 kV ESD Air Discharge ch1 and ch2

7.2 IEC61000-4-3: RI (Radiated Immunity)

Exposure to radiated emissions with field strength of 20 V/m caused the current output to deviate slightly but caused almost no deviations on the voltage output. After the test was completed both the voltage and current outputs returned to normal operation without deviation. Table 8 summarizes the results of each test and Figure 20 and Figure 23 show the outputs during each test. A list of the test frequencies versus the test time can be seen in Table 19.

Table 8. IEC61000-4-3 Results

Output	Antennae Orientation	Level	Result	Class
Current (±24 mA)	**Vertical**	20 V/m	Pass	A
	Horizontal	20 V/m	Pass	A
Voltage (±10 V)	**Vertical**	20 V/m	Pass	A
	Horizontal	20 V/m	Pass	A

7.2.1 I_{OUT} RI Results

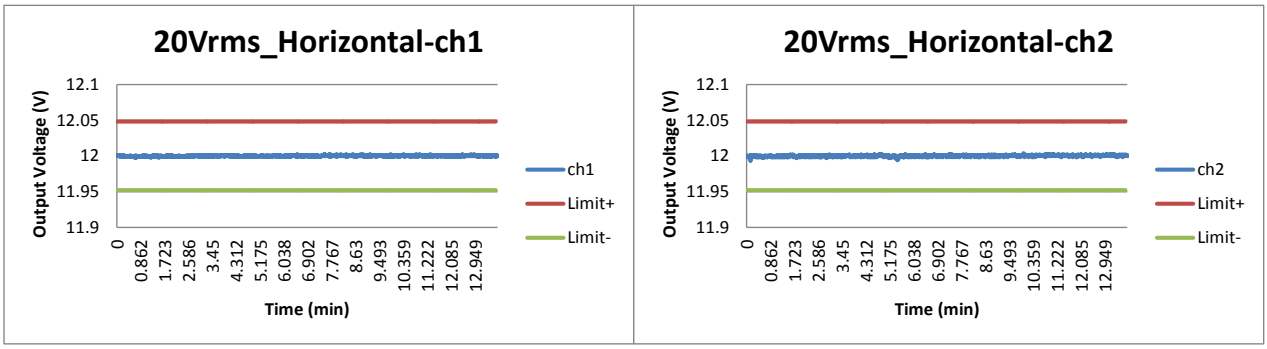

Figure 20: I_{OUT} - Horizontal Polarity 20 V/m

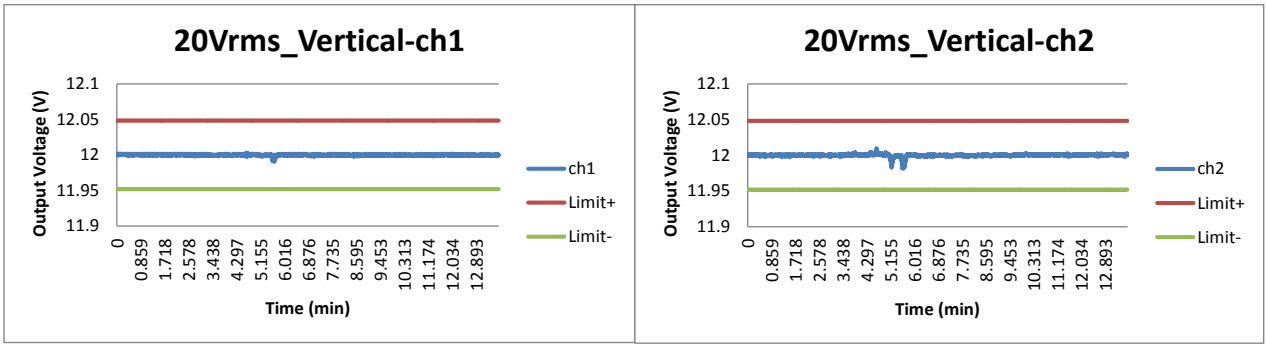

Figure 21: I_{OUT} - Vertical Polarity 20 V/m

7.2.2 V_{OUT} RI Results

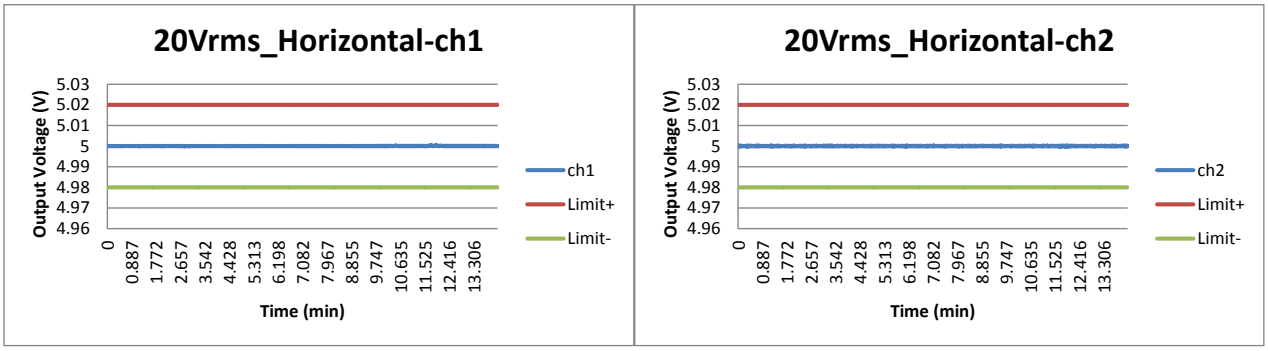

Figure 22: V_{OUT} - Horizontal Polarity 20 V/m

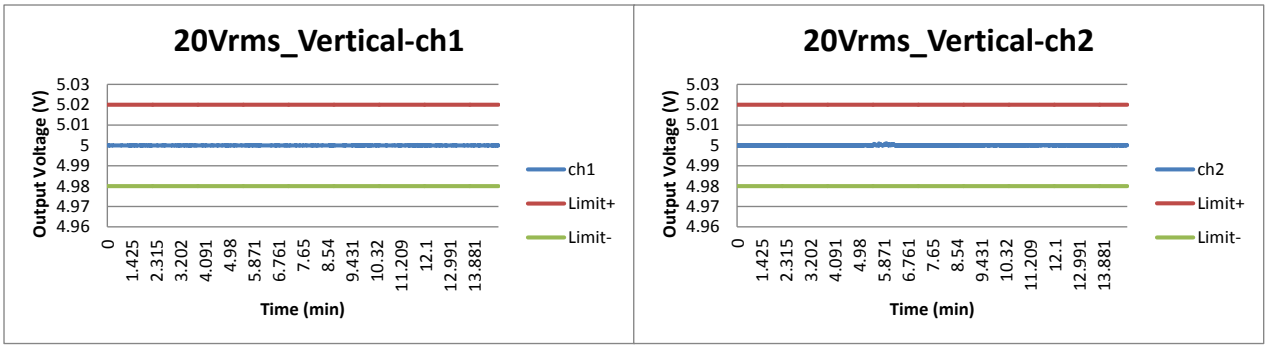

Figure 23: V_{OUT} - Vertical Polarity 20 V/m

7.3 IEC61000-4-4: EFT (Electrically Fast Transient)

The electrical fast transient bursts had almost no effect on the voltage output. The current output had noticeable deviations for both positive and negative EFT bursts, with more sensitivity towards negative bursts. After testing was complete normal functionality was restored. Table 9 summarizes the results of each test. Figure 24 and Figure 25 show the current and voltage outputs during each test.

Table 9. IEC61000-4-4 Results

Output	Level	Result	Class
Current (±24 mA)	**+2 kV**	Pass	A
	-2 kV	Pass	A
Voltage (±10 V)	**+2 kV**	Pass	A
	-2 kV	Pass	A

7.3.1 I_{OUT} EFT Results

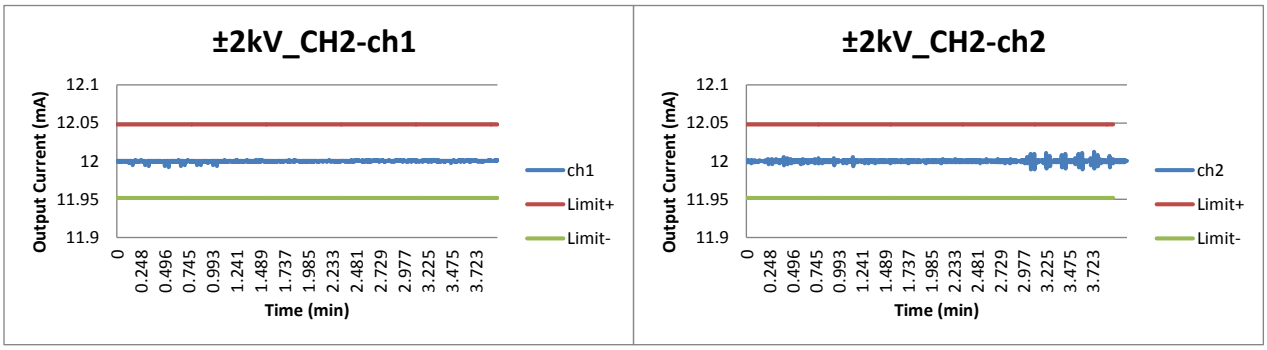

Figure 24: I_{OUT} - ±2 kV EFT Applied to CH2

7.3.2 V_{OUT} EFT Results

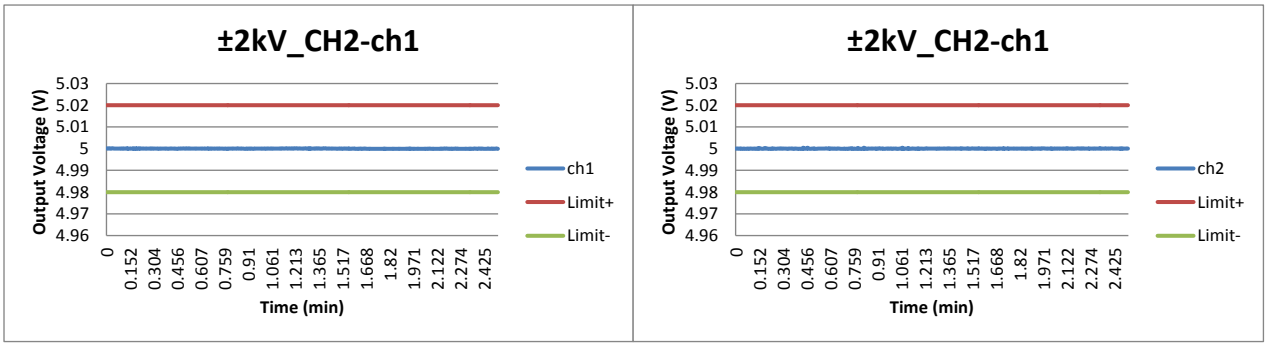

Figure 25: V_{OUT} - ±2 kV EFT Applied to CH2

7.4 IEC61000-4-5: Surge

The electrical lightning surge bursts had little effect on the voltage and current outputs. After testing was complete normal functionality was restored. The Line-to-Line configuration connects the surge generator directly between the V_{OUT}/I_{OUT} terminal and the board GND. Line-to-GND configurations connect the generator between either the V_{OUT}/I_{OUT} terminal or board GND and the generator chassis GND.

Table 10 summarizes the results of each test Figure 26 through Figure 31 show the voltage and current outputs during each test.

Table 10. IEC61000-4-5 Results

Output	Configuration	Source Impedance	Level	Result	Class
Current (±24 mA)	Line-to-Line	47 Ω	±2 kV	Pass	A
	Line-to-GND - Output	47 Ω	±2 kV	Pass	A
	Line-to-GND - GND	47 Ω	±2 kV	Pass	A
Voltage (±10 V)	Line-to-Line	47 Ω	±2 kV	Pass	A
	Line-to-GND - Output	47 Ω	±2 kV	Pass	A
	Line-to-GND - GND	47 Ω	±2 kV	Pass	A

7.4.1 I_{OUT} Surge Results

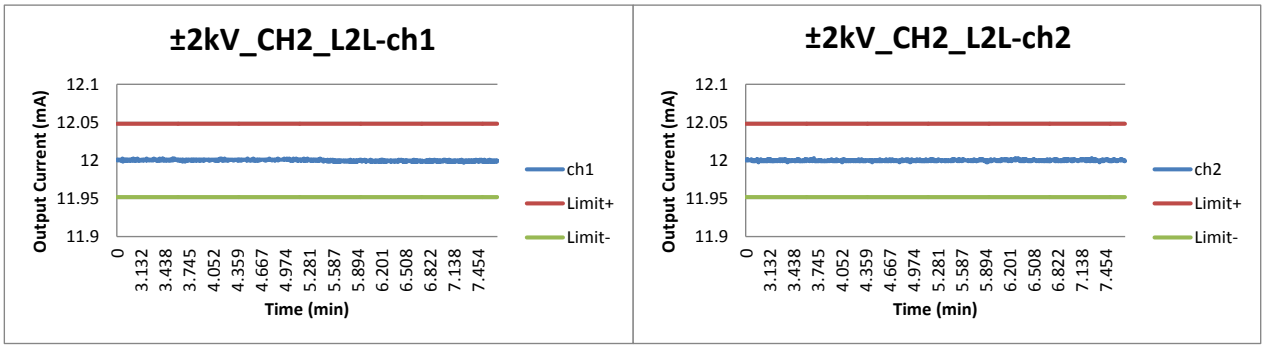

Figure 26: I_{OUT} +12 mA - ±2 kV Surge - Line-to-Line Applied between CH2 Output and GND

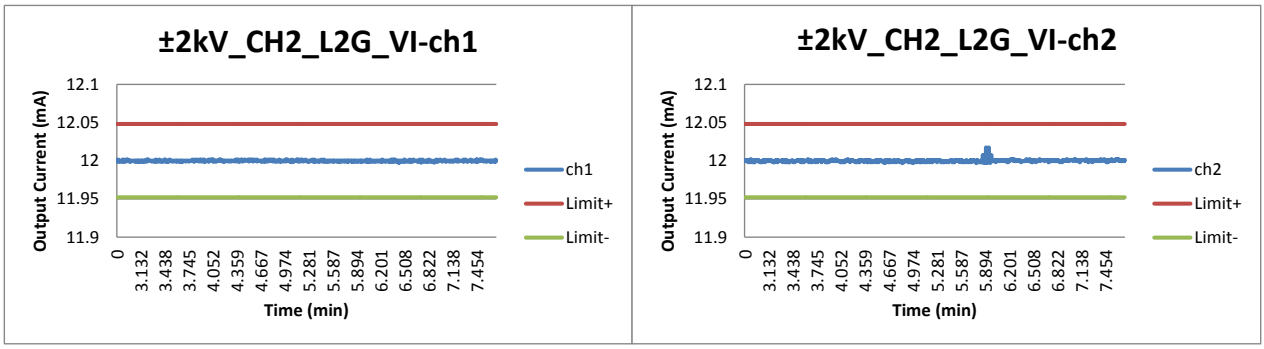

Figure 27: I_{OUT} +12 mA - ±2 kV Surge - Line-to-Ground Applied to CH2 Output

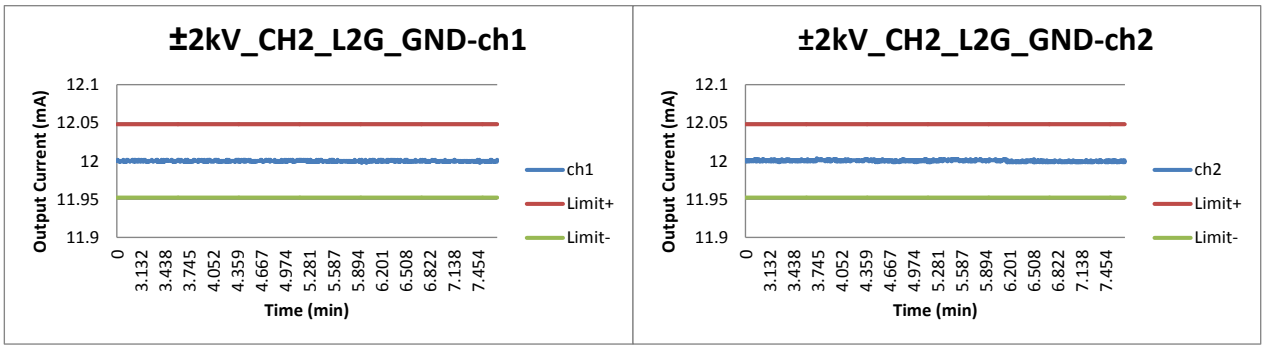

Figure 28: I_{OUT} +12 mA - ±2 kV Surge - Line-to-Ground Applied to CH2 GND

7.4.2 *V_{OUT} Surge Results*

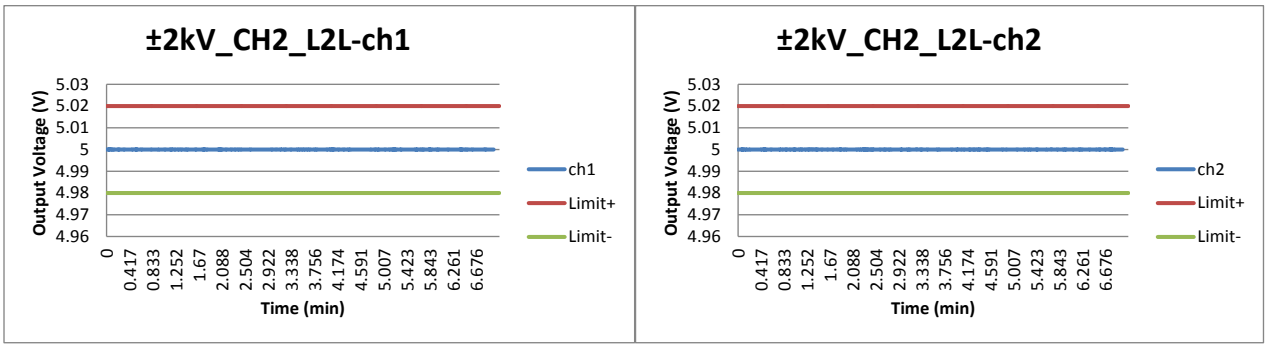

Figure 29: V_{OUT} +5 V - ±2 kV Surge - Line-to-Line Applied between CH2 Output and GND

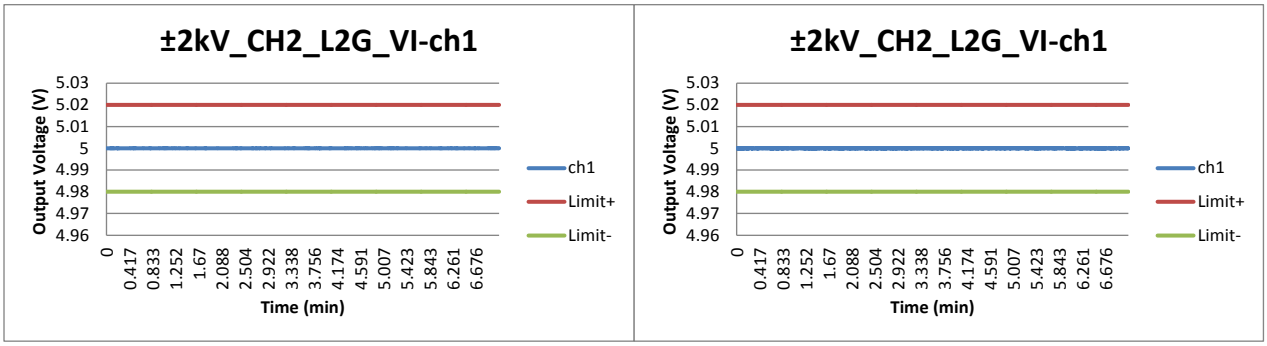

Figure 30: V_{OUT} +5 V - ±2 kV Surge - Line-to-Ground Applied to CH2 Output

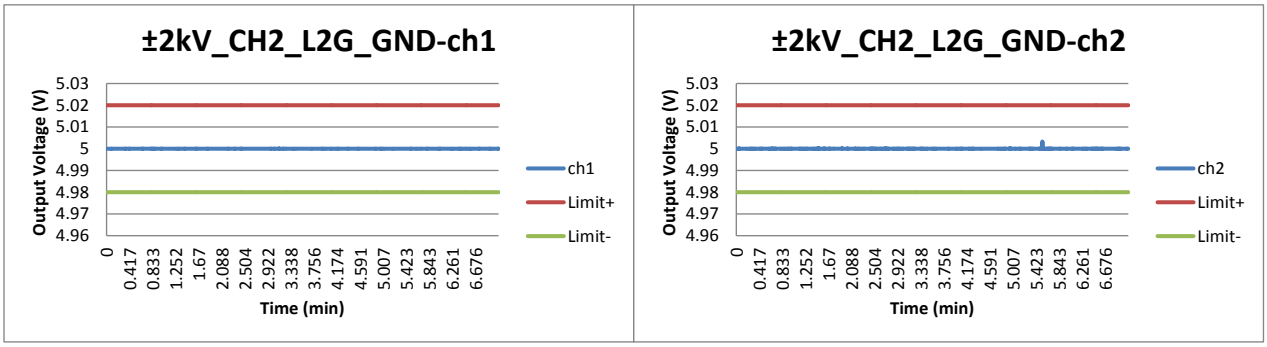

Figure 31: V_{OUT} +5 V - ±2 kV Surge - Line-to-Ground Applied to CH2 GND

7.5 IEC61000-4-6: CI (Conducted Immunity)

The conducted immunity tests caused deviation in both the voltage and current outputs. The I_{OUT} deviations were outside of the 0.1% FSR range resulting in a class B rating whereas the V_{OUT} results remained within the 0.1% output tolerance. The results are summarized in Table 11. Figure 32 and Figure 33 show the behavior of the outputs during exposure to the CI test. A list of the test frequencies versus the test time can be seen in Table 20.

Table 11. IEC61000-4-6 Results

	Result	Class
Current (0-24mA)	Pass	B
Voltage (±10 V)	Pass	A

7.5.1 I_{OUT} CI Results

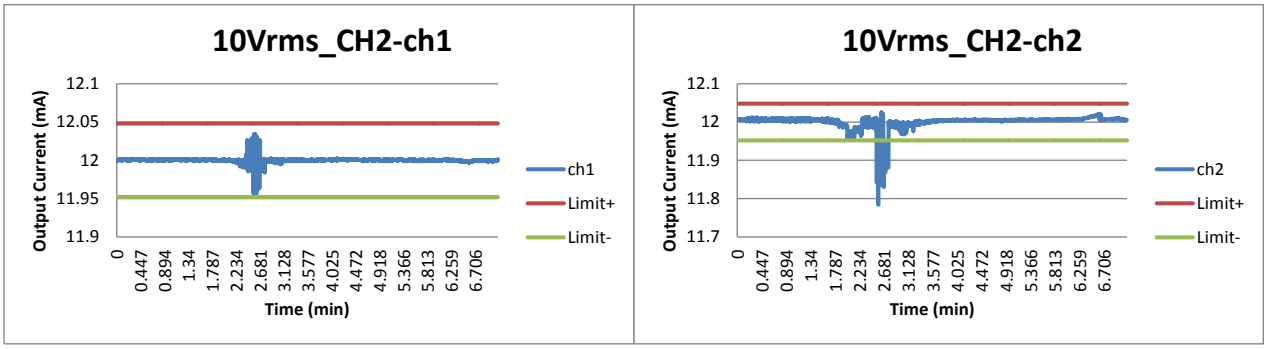

Figure 32: I_{OUT} 12 mA – 10 Vrms CI Applied to CH2

7.5.2 V_{OUT} CI Results

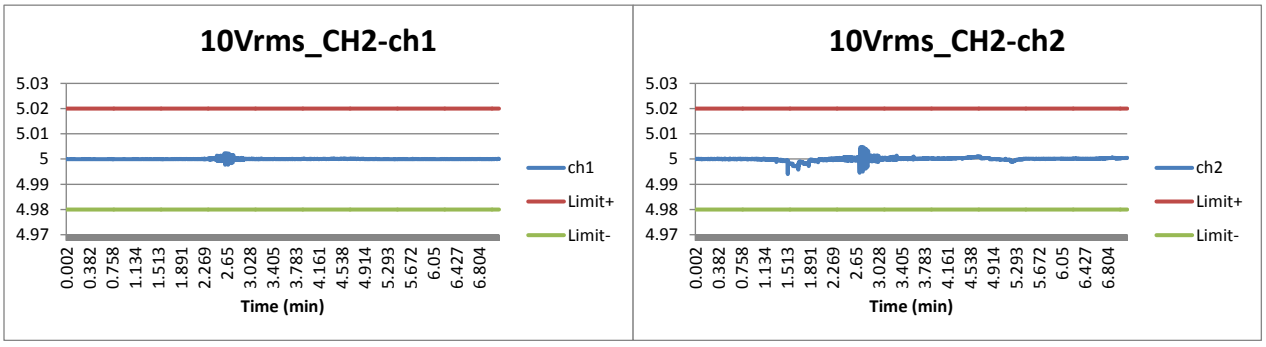

Figure 33: V_{OUT} 5 V – 10 Vrms CI Applied to CH2

8 Modifications

While simply changing the V_{DAC} output range can change the output span to different common industrial output ranges, the resulting loss of resolution is commonly not acceptable. Therefore, hardware modifications should be made to achieve other V_{OUT} and I_{OUT} ranges. Single-ended V_{OUT} and I_{OUT} ranges can be achieved by connecting the R_{SET} resistor to GND instead of +2.5 V. Table 12 displays values for V_{REF}, R_G, and R_{SET} for common industrial output ranges.

Table 12. V_{REF}, R_{SET}, and R_G Values for Common Industrial Output Ranges

I_{OUT}	V_{REF}	R_{SET}	V_{OUT}	R_G
±25 mA	2.5 V	976 Ω	±10 V	8.06 kΩ
			±5 V	4.02 kΩ
±24 mA	2.5 V	1.2 kΩ	±10 V	8.25 kΩ
			±5 V	4.22 kΩ
±20 mA	2.5 V	1.02 kΩ	±10 V	9.76 kΩ
			±5 V	4.87 kΩ
0-25 mA	0 V	1.98 kΩ	0-10 V	8.20 kΩ
			0-5 V	4.02 kΩ
0-24 mA	0 V	2.05 kΩ	0-10 V	8.25 kΩ
			0-5 V	4.12 kΩ
0-20 mA	0 V	2.43 kΩ	0-10 V	9.76 kΩ
			0-5 V	4.87 kΩ

The DAC8563 has 12 and 14-bit equivalents, the DAC8163 and DAC7563, which can be directly substituted for the DAC8563 in lower accuracy systems. The output channel count could be increased to four channels using the four-channel DAC8565 or reduced to one channel using the single-channel DAC8560. The DAC8552 could also be used as a 16-bit option but would require an external reference voltage.

The XTR300 is the only integrated solution available from Texas Instruments that can create a sourcing and sinking current output. A discrete solution could be designed to create the same bipolar current output but it would be more complex and likely less accurate than using the XTR300.

For applications that do not require both sourcing and sinking current, the DAC8760 devices can be substituted for the DAC8563 and XTR300 to create the desired voltage and current outputs. Also, solutions could be created using a DAC and the XTR111 current driver.

The output protection circuit was specifically designed to protect the outputs of the XTR300 powered from bipolar 15 V supplies. Modifying the power supply voltages used in this design may require the selection of different components, such as higher or lower breakdown voltage TVS diodes. Discrete solutions that use multiple integrated circuits may also need to choose different protection components for appropriate protection.

9 About the Authors

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

Janet Sun is an analog field application engineer in Beijing, China supporting industrial and other performance analog customers. She completed work on this system as well as several others during a 6-month rotation working with the precision amplifier team in Dallas.

10 Acknowledgements & References

The authors wish to acknowledge NTS (National Technical Systems) in Plano, TX for their assistance performing the electromagnetic compatibility tests.

1. *Kevin Duke, Collin Wells, "Single-Channel Industrial Voltage and Current Output Driver, Isolated, EMC/EMI Tested", TIPD153*

2. *Collin Wells, Reza Abdullah, "Creating a Combined Voltage and Current Output with the DACx760" SBAA199, July 2014.*

3. *IEC Publication 61000-4-2 "Electromagnetic Compatibility (EMC) – Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test," International Electrotechnical Commission, 2008.*

4. *IEC Publication 61000-4-3 "Electromagnetic Compatibility (EMC) – Part 4-3: Testing and Measurement Techniques – Radiated, Radio-Frequency, Electromagnetic Field Immunity Test," International Electrotechnical Commission, 2006.*

5. *IEC Publication 61000-4-4 "Electromagnetic Compatibility (EMC) – Part 4-4: Testing and Measurement Techniques – Electrical Fast Transient/Burst Immunity Test," International Electrotechnical Commission, 2012.*

6. *IEC Publication 61000-4-5 "Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test," International Electrotechnical Commission, 2012.*

7. *IEC Publication 61000-4-6 "Electromagnetic Compatibility (EMC) – Part 4-6: Testing and Measurement Techniques – Immunity to Conducted Disturbances, Induced by Radio-Frequency Fields," International Electrotechnical Commission, 2008.*

8. *H. Ott, Electromagnetic Compatibility. John Wiley & Sons Inc., 2009.*

Appendix A.

A.1 Electrical Schematic

The Altium electrical schematic for this design can be seen in Figure 34.

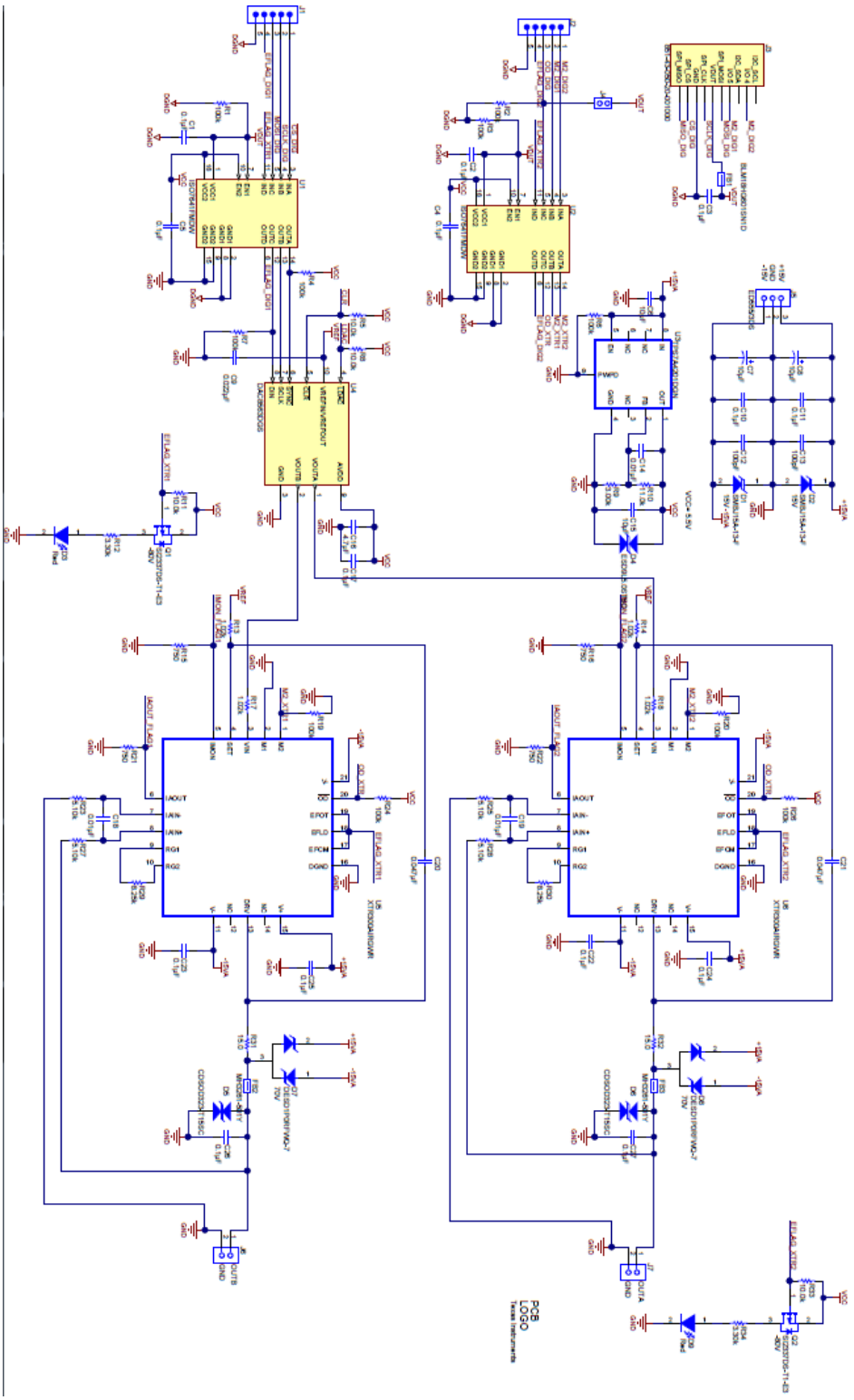

Figure 34: Altium Schematic

A.2 Bill of Materials

The bill of materials for this circuit can be seen in Figure 35.

Item #	Quantity	Designator	Value	Description	Manufacturer	Part Number
1	12	C1, C2, C3, C4, C5, C10, C11, C17, C22, C23, C24, C25	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H104KA93D
2	1	C6	10uF	CAP, CERM, 10uF, 50V, +/-10%, X7R, 1210	MuRata	GRM32ER71H106KA12L
3	2	C7, C8	10uF	CAP, TANT, 10uF, 50V, +/-10%, 0.8 ohm, 7343-43 SMD	Vishay-Sprague	293D106X9050E2TE3
4	1	C9	0.022uF	CAP, CERM, 0.022uF, 16V, +/-10%, X7R, 0603	Kemet	C0603C223K4RACTU
5	2	C12, C13	100pF	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A101JAT2A
6	3	C14, C18, C19	0.01uF	CAP, CERM, 0.01uF, 50V, +/-5%, X7R, 0603	Kemet	C0603C103J5RACTU
7	1	C15	10uF	CAP, CERM, 10uF, 16V, +/-10%, X7R, 1206	MuRata	GRM31CR71C106KAC7L
8	1	C16	4.7uF	CAP, CERM, 4.7uF, 16V, +/-10%, X7R, 1206	TDK	C3216X7R1C475K
9	2	C20, C21	0.047uF	CAP, CERM, 0.047uF, 50V, +/-10%, X7R, 0603	TDK	C1608X7R1H473K
10	2	C26, C27	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	Kemet	C0603C104K5RACTU
11	2	D1, D2		Diode, TVS, Uni, 15V, 600W, SMB	Diodes Inc.	SMBJ15A-13-F
12	2	D3, D9		LED, Red, SMD	Lite-On	LTST-C170KRKT
13	1	D4		TVS ESD PROT ULT LOW CAP SOD-923	ON Semiconductor	ESD9L5.0ST5G
14	2	D5, D6		DIODE TVS ARRAY 15V SOD323	Bourns	CDSOD323-T15SC
15	2	D7, D8		Diode, TVS, Uni, 70V, W, SOT-323	Diodes Inc.	DESD1P0RFWQ-7
16	1	FB1		FERRITE CHIP 600 OHM 200MA 0603	MuRata	BLM18HG601SN1D
17	2	FB2, FB3		BEAD FERRITE 500 OHM 3.0A 3216	Bourns Inc.	MH3261-501Y
18	2	J1, J2		CONN HEADER 5POS .100" T/H GLD	Samtec, Inc.	TSW-105-07-G-S
19	1	J3		CONN SOCKET 50PIN .050 R/A SNGL	Mill-Max Manufacturing Corp.	851-43-050-20-001000
20	1	J4		CONN HEADER 2POS .050 T/H GOLD"	Samtec	TMS-102-02-G-S
21	1	J5		TERMINAL BLOCK 3.5MM 3POS PCB	On Shore Technology Inc	ED555/3DS
22	2	J6, J7		TERMINAL BLOCK 3.5MM 2POS PCB	On Shore Technology Inc	ED555/2DS
23	2	Q1, Q2		MOSFET, P-CH, -80V, -1.2A, SOT-23	Vishay-Siliconix	SI2337DS-T1-E3
24	10	R1, R2, R3, R4, R6, R7, R19, R20, R24, R26	100k	RES, 100k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603100KFKEA
25	4	R5, R8, R11, R33	10.0k	RES, 10.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA
26	1	R9	3.00k	RES, 3.00k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-073KL
27	1	R10	11.0k	RES, 11.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060311K0FKEA
28	2	R12, R34	3.30k	RES, 3.30k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-073K3L
29	4	R13, R14, R17, R18	1.02k	RES, 1.02k ohm, 0.1%, 0.1W, 0603	Yageo America	RT0603BRD071K02L
30	4	R15, R16, R21, R22	750	RES, 750 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603750RFKEA
31	4	R23, R25, R27, R28	5.10k	RES, 5.10k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-075K1L
32	2	R29, R30	8.25k	RES, 8.25k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-8251-B-T5
33	2	R31, R32	15	RES, 15.0 ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW080515R0FKEA
34	2	U1, U2		IC DGTL ISO 4CH LOGIC 16SOIC	Texas Instruments	ISO7641FMDW
35	1	U3		IC, 28-V Input Voltage, 50-mA Voltage Regulator	Texas Instruments	TPS7A4201DGN
36	1	U4		IC DAC 16BIT SRL DUAL 10MSOP	Texas Instruments	DAC8563SDGS
37	2	U5, U6		IC, Industrial Analog Current/Voltage Output Driver	Texas Instruments	XTR300AIRGWR

Figure 35: Bill of Materials

A.3 Circuit Performance Calculations with Maximum Values

A.3.1 Maximum I_{OUT} Accuracy Calculations

Table 13: Maximum DAC8563 Performance Specifications

Output Range	DAC8563 Specification	Maximum Value
Current (±24 mA)	Offset (mV)	±4
	DNL (LSB)	±1
	INL (LSB)	±12
	Gain error (%FSR)	±0.15
	V_{REF} Accuracy (mV)	±5

The maximum total unadjusted error, TUE, of DAC8563 can be calculated as shown in Equation 17.

$$I_{TUE\_DAC}(\%FSR) = \left(\sqrt{\left(\frac{4mV}{4.896V}\right)^2 + \left(\frac{12}{2^{16}}\right)^2 + \left(\frac{0.15}{100}\right)^2 + \left(\frac{5mV}{2.5V}\right)^2} \right) \times 100 = 0.2637\%FSR \quad (17)$$

Applying a two-point calibration to the design will remove the effects of gain and offset errors leaving only the linearity errors of the DAC8563 as shown in Equation 18:

$$I_{CAL\_DAC}(\%FSR) = \left(\sqrt{\left(\frac{12}{2^{16}}\right)^2} \right) \times 100 = 0.01837\%FSR \quad (18)$$

The XTR300 performance specifications in I_{OUT} mode, including the effects of R_{SET}, are displayed in Table 14.

Table 14: Typical XTR300 Circuit I_{OUT} Performance Specifications

Output Range	XTR300 Specification	Maximum Value
Current (±24 mA)	Offset (mV)	±1.8
	Nonlinearity (%FSR)	±0.1
	Gain Error (%FSR)	±0.12
	V_{REF} Accuracy (mV)	±5
	R_{SET} Tolerance (%)	±0.1

Using these specifications and the DAC8563 input voltage range, the TUE of XTR300 can be calculated as shown in Equation 19.

$$I_{TUE\_XTR}(\%FSR) = \left(\sqrt{\left(\frac{1.8mV}{4.896V}\right)^2 + \left(\frac{0.1}{100}\right)^2 + \left(\frac{0.12}{100}\right)^2 + \left(\frac{5mV}{4.896V}\right)^2 + \left(\frac{0.1}{100}\right)^2} \right) \times 100 = 0.2149\% \quad (19)$$

Applying a two-point calibration to the design will remove the effects of gain and offset errors leaving only the linearity errors of the XTR300 as shown in Equation 20:

$$I_{CAL\_XTR}(\%FSR) = \left(\sqrt{\left(\frac{0.1}{100}\right)^2} \right) \times 100 = 0.1\%FSR \quad (20)$$

Since the DAC error and the XTR error are uncorrelated, a probable maximum full system TUE for ±24mA outputs can be calculated by taking the root of the sum of squares (RSS) of the individual maximum errors from the DAC8563 and XTR300, as shown in Equation 21.

$$I_{TUE\_TOTAL}(\%FSR) = \sqrt{I_{TUE\_DAC}(\%FSR)^2 + I_{TUE\_XTR}(\%FSR)^2} = \sqrt{(0.2637\%)^2 + (0.2149\%)^2} = 0.3401\% \quad (21)$$

The final maximum calibrated results are shown in Equation 22.

$$I_{CAL\_TOTAL}(\%FSR) = \sqrt{I_{CAL\_DAC}(\%FSR)^2 + I_{CAL\_XTR}(\%FSR)^2} = \left(\sqrt{(0.01837)^2 + (0.1)^2}\right) = 0.1017\%FSR \quad (22)$$

A.3.2 Maximum V_{OUT} Accuracy Calculations

The same performance specifications apply for the DAC8563 in V_{OUT} mode as they did in I_{OUT} mode. However, the DAC output voltage has a span of 4.945 V for a ±10 V output resulting in a slightly lower error as shown in Equation 23:

$$V_{TUE\_DAC}(\%FSR) = \left(\sqrt{\left(\frac{1mV}{4.945V}\right)^2 + \left(\frac{4}{2^{16}}\right)^2 + (0.0001)^2 + \left(\frac{0.1mV}{2.5V}\right)^2}\right) \times 100 = 0.02634\%FSR \quad (23)$$

The maximum XTR300 performance specifications in V_{OUT} mode, including the effects of R_{SET} and R_G, are displayed in Table 15.

Table 15: Maximum XTR300 Circuit V_{OUT} Performance Specifications

Output Range	XTR300 Specification	Typical Value
Voltage (±10 V)	Offset (mV)	±1.8
	Nonlinearity (%FSR)	±0.1
	Gain error (%FSR)	±0.1
	V_{REF} Accuracy (mV)	±5
	R_{SET} Tolerance (%)	±0.1
	R_G Tolerance (%)	±0.1

The TUE of XTR300 in V_{OUT} mode is calculated in Equation 24.

$$V_{TUE\_XTR}(\%FSR) = \left(\sqrt{\left(\frac{1.8mV}{4.945V}\right)^2 + \left(\frac{0.1}{100}\right)^2 + \left(\frac{0.1}{100}\right)^2 + \left(\frac{5mV}{4.945V}\right)^2 + \left(\frac{0.1}{100}\right)^2 + \left(\frac{0.1}{100}\right)^2}\right) \times 100 = 0.227\%FSR \quad (24)$$

A two-point calibration will reduce the V_{OUT} errors to the linearity error of the XTR300 as shown in Equation 25.

$$V_{CAL\_XTR}(\%FSR) = \left(\sqrt{\left(\frac{0.1}{100}\right)^2}\right) \times 100 = 0.1\%FSR \quad (25)$$

The V_{OUT} circuit maximum TUE is calculated in Equation 26 using the DAC8563 and XTR300 maximum TUE results.

$$V_{TUE\_TOTAL}(\%FSR) = \sqrt{V_{TUE\_DAC}(\%FSR)^2 + V_{TUE\_XTR}(\%FSR)^2} = \sqrt{(0.2634\%)^2 + (0.227\%)^2} = 0.3477\%FSR \quad (26)$$

The final calibrated results for V_{OUT} are shown in Equation 27.

$$V_{CAL\_TOTAL}(\%FSR) = \sqrt{V_{CAL\_DAC}(\%FSR)^2 + V_{CAL\_XTR}(\%FSR)^2} = \left(\sqrt{(0.01831)^2 + (0.1)^2}\right) = 0.1017\%FSR \quad (27)$$

A.4 DAC8563 Performance Results

The performance results for both DAC8563 outputs were also captured using 8.5 digit multi-meters. The DAC8563 output voltages can be seen in Figure 36.

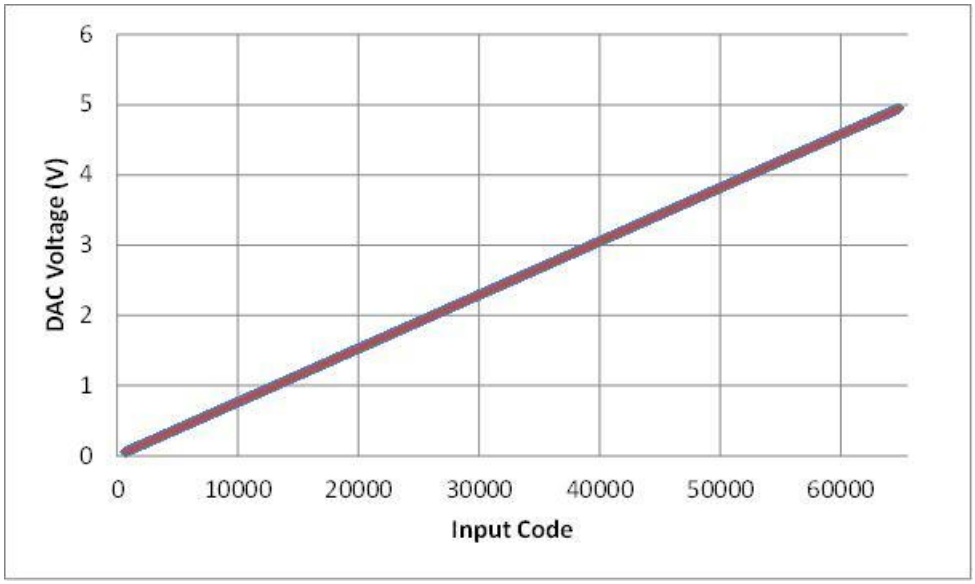

Figure 36: DAC8563 Output Voltage vs Input Code for CH1 (red) and CH2 (blue)

The DAC8563 output voltage error has been plotted in Figure 37. The highest measured output error is 1.25 mV or 0.025% FSR for the 5 V output span.

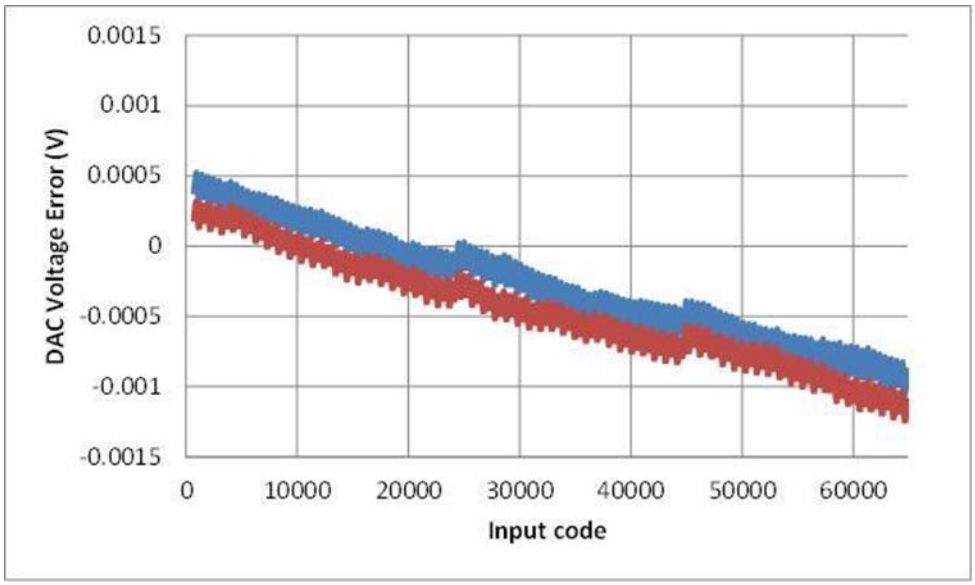

Figure 37: DAC8563 Output Voltage Error vs. Input Code for CH1 (red) and CH2 (blue)

Applying a two-point calibration removes the gain and offset errors leaving only the linearity of the DAC8563 as shown in Figure 38. The calibrated error is less than 150 µV or 0.003% FSR.

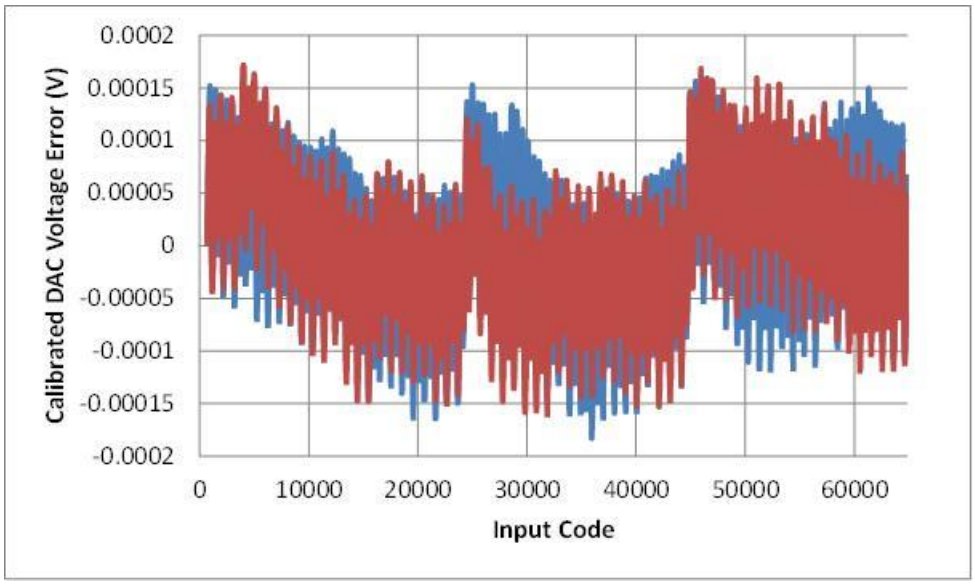

Figure 38: Calibrated DAC8563 Output Voltage Error vs. Input Code for CH1 (red) and CH2 (blue)

The differential non-linearity (DNL) results can be seen in Figure 39. The results are < 1LSB as stated in the datasheet specification.

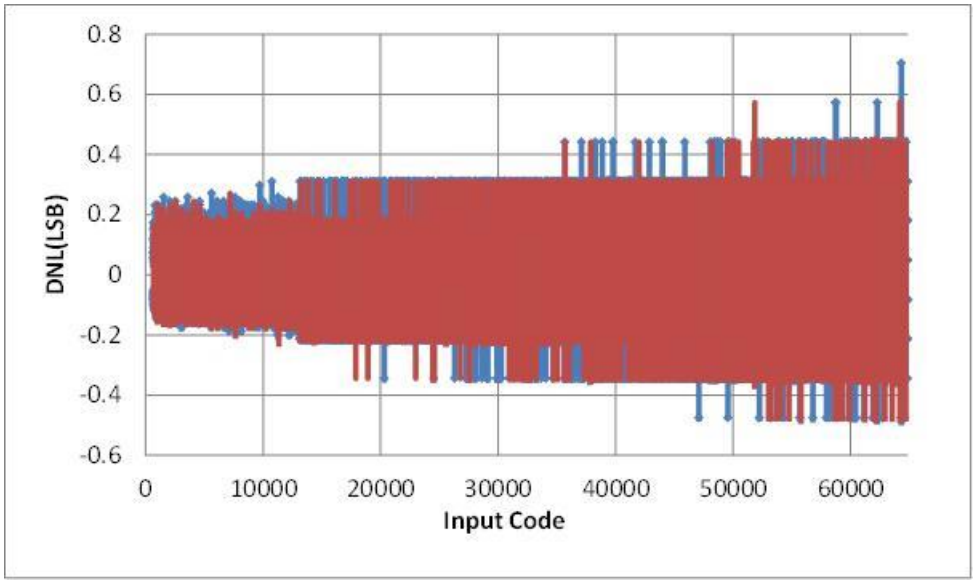

Figure 39: DAC8563 DNL Results for CH1 (red) and CH2 (blue)

The integral non-linearity (INL) results for the DAC8563 are shown in Figure 40. The INL is less than the typical value of ±4 LSB.

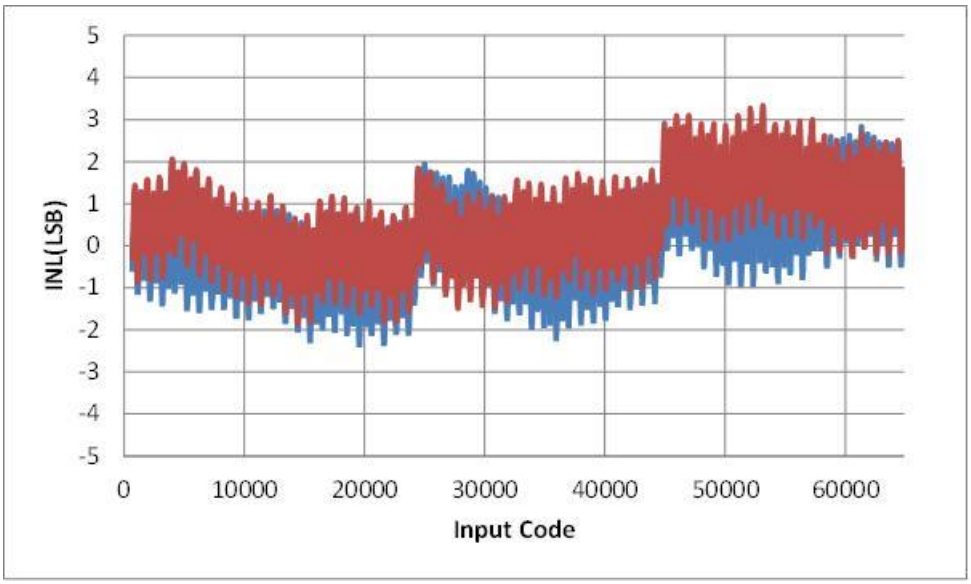

Figure 40: DAC8563 INL Results for CH1 (red) and CH2 (blue)

The measured DAC8563 results have been compared to the calculated results from Section 4.1 in Table 16. Note that the gain error has combined the gain error of the DAC8563 and the gain error from the V_{REF} voltage inaccuracy.

Table 16: Comparison of Measured and Calculated DAC8563 Performance

Output Range	DAC8563 Specification	Typical Value	Measured Results
Current (±24 mA)	Offset (mV)	±1	±0.003
	DNL (LSB)	±0.2	±0.4
	INL (LSB)	±4	±3
	Gain error (%FSR)	±0.0102	±0.03
	Calculated TUE (%FSR)	0.0239	0.0253
	Calibrated Error (%FSR)	0.0061	0.003

The gain error was likely a little higher than the calculated value because the V_{REF} voltage error was a little higher than the typical 0.1 mV value used in the calculations.

A.5 XTR300 ±24 mA Output Results

Once calculated, the errors from the DAC8563 can be removed from the final output errors leaving only the errors of the XTR300. The measurement results of the XTR300 outputs versus the DAC8563 input voltages are shown in Figure 41.

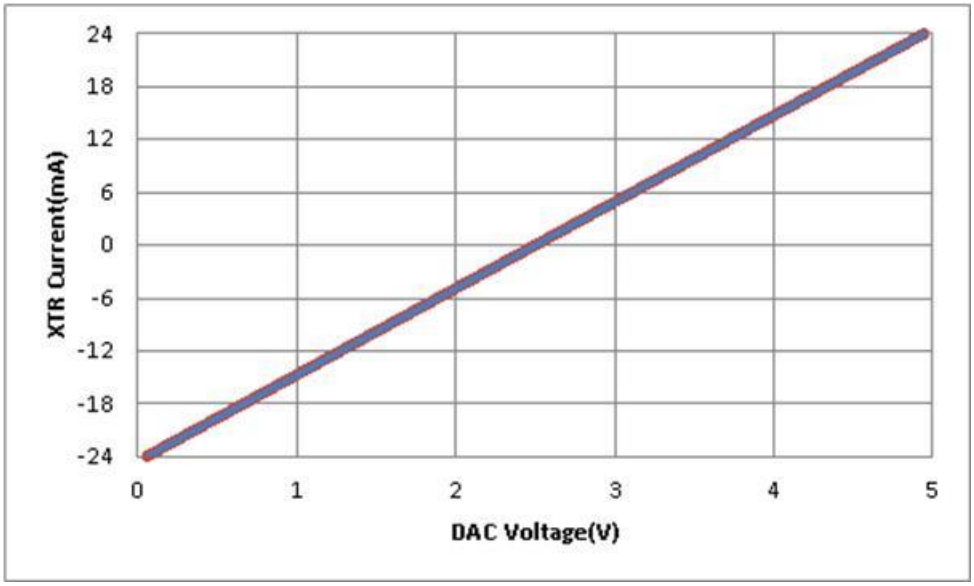

Figure 41: XTR300 Output Current vs. Input Voltage for CH1 (red) and CH2 (blue)

The output current error of the XTR300 outputs has been plotted in Figure 42. The worst error is around 12.5 µA or 0.026% FSR for the ±24 mA output span.

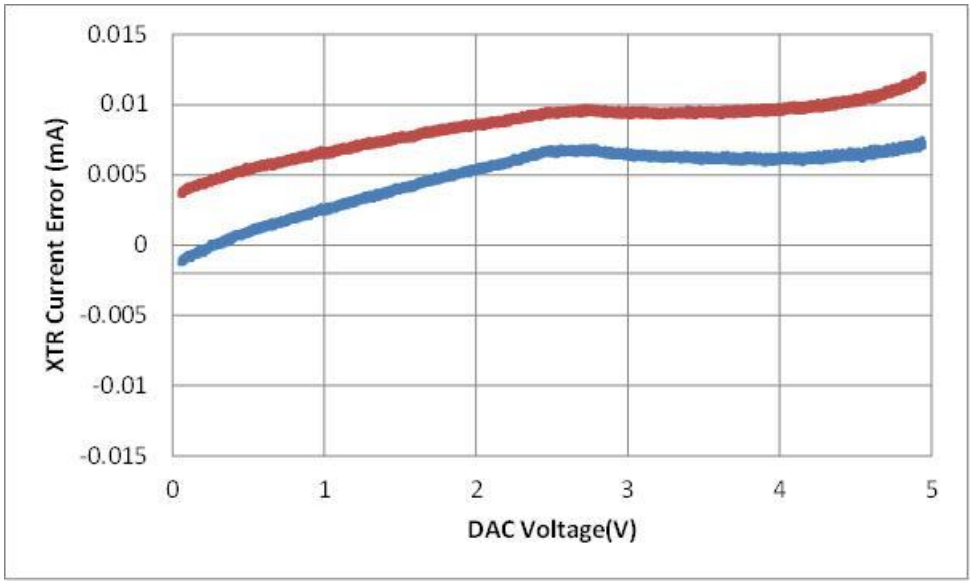

Figure 42: XTR300 Output Current Error vs. Input Voltage for CH1 (red) and CH2 (blue)

Applying a two-point gain and offset calibration to the results produces the final results reduces the error to the linearity errors of the XTR300 as shown in Figure 43. After calibration the worst error is 3 µA or 0.00625% FSR.

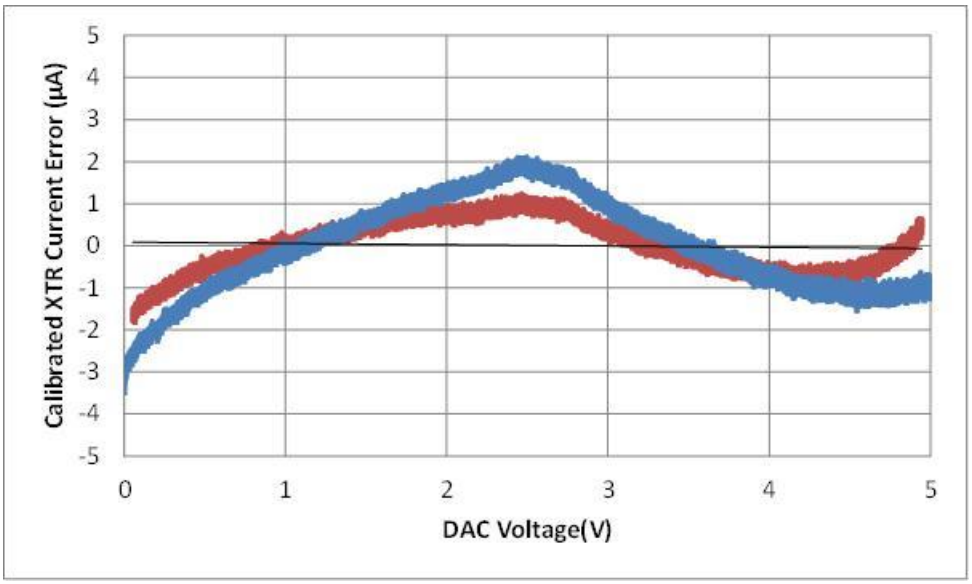

Figure 43: Calibrated XTR300 Output Current Error vs. Input Voltage for CH1 (red) and CH2 (blue)

The measured XTR300 results in I_{OUT} mode have been compared to the calculated results from Section 4.1 in Table 17. Note that the offset value includes the offset of the XTR300 and the V_{REF} inaccuracy and has been converted to output current. Also note that the gain error includes the gain error of the XTR300 and the gain error from the R_{SET} resistor.

Table 17: Comparison of Measured and Calculated XTR300 Circuit I_{OUT} Performance

XTR300 Specification	Typical Value	Measured Results
Offset (uA)	±4	10
Gain Error (%FSR)	±0.108	0.018
TUE (%FSR)	±0.1085	0.026
Calibrated Error (%FSR)	±0.01	0.00625

The measured offset current was likely higher than the calculation because the V_{REF} voltage error was higher than the typical value of 0.1 mV, correlating to the higher DAC8563 gain error reported in Appendix A.4. The measured gain error was less than calculated because the R_{SET} error was less than the specified maximum tolerance of 0.1%.

A.6 XTR300 ±10 V Output Results

The measurement results for the XTR300 in voltage mode can be seen in Figure 44.

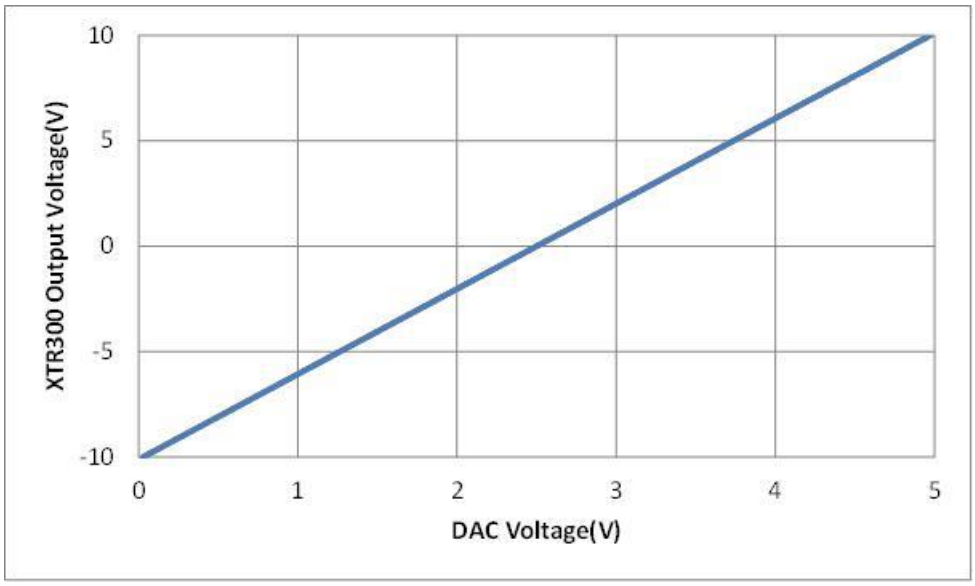

Figure 44: XTR300 Output Voltage vs. Input Voltage for CH1 (red) and CH2 (blue)

The output voltage error of the XTR300 outputs has been plotted in Figure 45. The worst error is around 3.5 mV or 0.0175% FSR for the ±10 V output span.

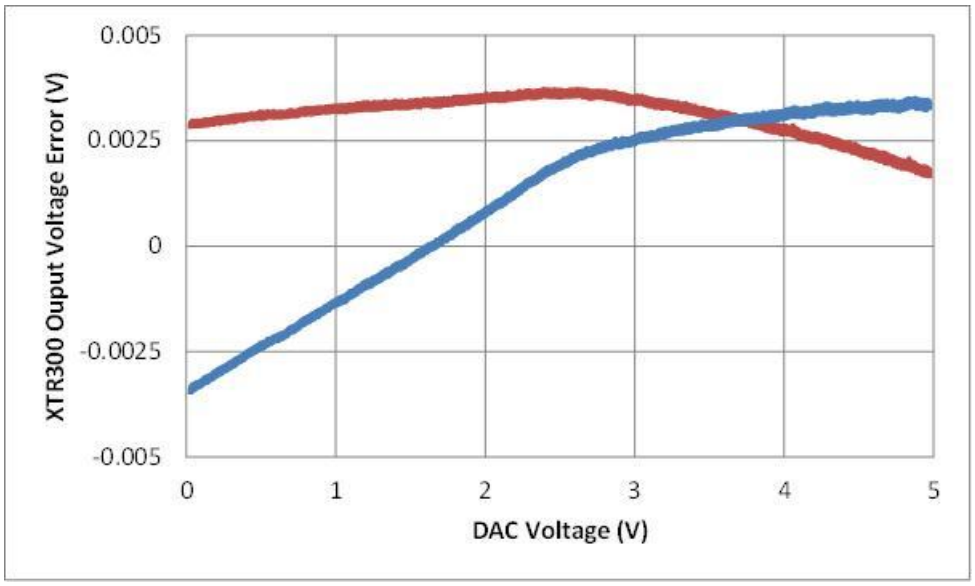

Figure 45: XTR300 Output Voltage Error vs. Input Voltage for CH1 (red) and CH2 (blue)

The results after a two-point gain and offset calibration can be seen in Figure 46. The worst calibrated error is about 1.4 mV or 0.007% FSR.

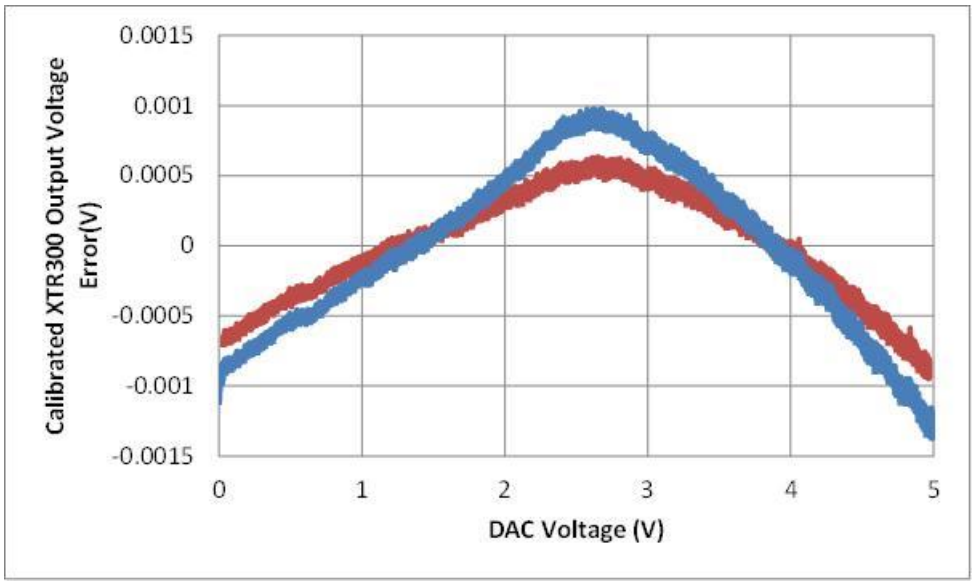

Figure 46: Calibrated XTR300 Output Voltage Error vs. Input Voltage for CH1 (red) and CH2 (blue)

The measured XTR300 results in V_{OUT} mode have been compared to the calculated results from Section 4.2 in Table 17. Note that the offset voltage value includes the offset of the XTR300 and the V_{REF} inaccuracy and has been converted to output voltage. Also note that the gain error includes the gain error of the XTR300 and the gain errors from the R_{SET} and R_G resistors.

Table 18: Comparison of Measured and Calculated XTR300 Circuit V_{OUT} Performance

XTR300 Specification	Typical Value	Measured Results
Offset (mV)	±1.65	±3
Gain Error (%FSR)	±0.1469	0.03
TUE (%FSR)	±0.1494	±0.0175
Calibrated Error (%FSR)	±0.01	±0.007

The measured offset current was likely higher than the calculation because the V_{REF} voltage error was higher than the typical value of 0.1 mV, correlating to the higher DAC8563 gain error reported in Appendix A.4. The measured gain errors were less than calculated because the R_{SET} and R_G errors were less than the specified maximum tolerances of 0.1%.

A.7 IEC61000-4-3: Radiated Immunity - Test Frequency versus Test Time

Table 19 lists the frequencies associated with the test times displayed in Figure 20 through Figure 23.

Table 19: IEC61000-4-3: Radiated Immunity - Test Time vs. Frequency

Time (min : sec)	Frequency (MHz)	Time (min : sec)	Frequency (MHz)	Time (min : sec)	Frequency (MHz)
0	80	4:30	175.58	9:16	443
30	81.6	4:50	190	9:32	461
1:00	91	5:00	197.9	9:50	489
1:24	96.6	5:29	210	10:06	514
1:34	100.5	5:50	222.9	10:20	540.5
1:52	104.65	6:06	239	10:36	579.5
2:06	109.99	6:20	248	11:02	621.2
2:22	115.6	6:37	264	11:17	646.5
2:32	120.3	6:58	280	11:37	700
2:49	126.4	7:01	294	12:00	758
3:00	131.57	7:32	319	12:23	756.9
3:14	136.9	7:49	340	12:40	862
3:40	1445.33	8:11	355	14:30	906.7
3:50	155.82	8:34	389	14:42	962
4:10	163.7	8:57	413	15.00	1000

A.8 IEC61000-4-6: Conducted Immunity - Test Frequency versus Test Time

Table 20 lists the frequencies associated with the test times displayed in Figure 32 and Figure 33.

Table 20: IEC61000-4-6: Conducted Immunity - Test Time vs. Frequency

Time (min : sec)	Frequency (MHz)	Time (min : sec)	Frequency (MHz)	Time (min : sec)	Frequency (MHz)
0	0.150	2:31	1.287	4:49	11.035
0:14	0.175	2:36	1.5	4:53	12.865
0:28	0.204	2:49	1.749	5:02	15
0:42	0.238	2:56	2.039	5:08	17.489
0:54	0.277	3:38	2.377	5:13	20.39
1:05	0.323	3:47	2.772	5:21	23.773
1:16	0.377	3:57	3.232	5:32	27.718
1:27	0.439	4:03	3.768	5:51	32.317
1:38	0.512	4:07	4.393	6:18	37.678
1:47	0.597	4:13	5.122	6:32	43.93
2:00	0.696	4:22	5.972	6:35	51.218
2:05	0.812	4:28	6.962	6:52	59.716
2:17	0.946	4:34	8.118	7:08	69.624
2:21	1.104	4:41	9.464	7:26	80

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