

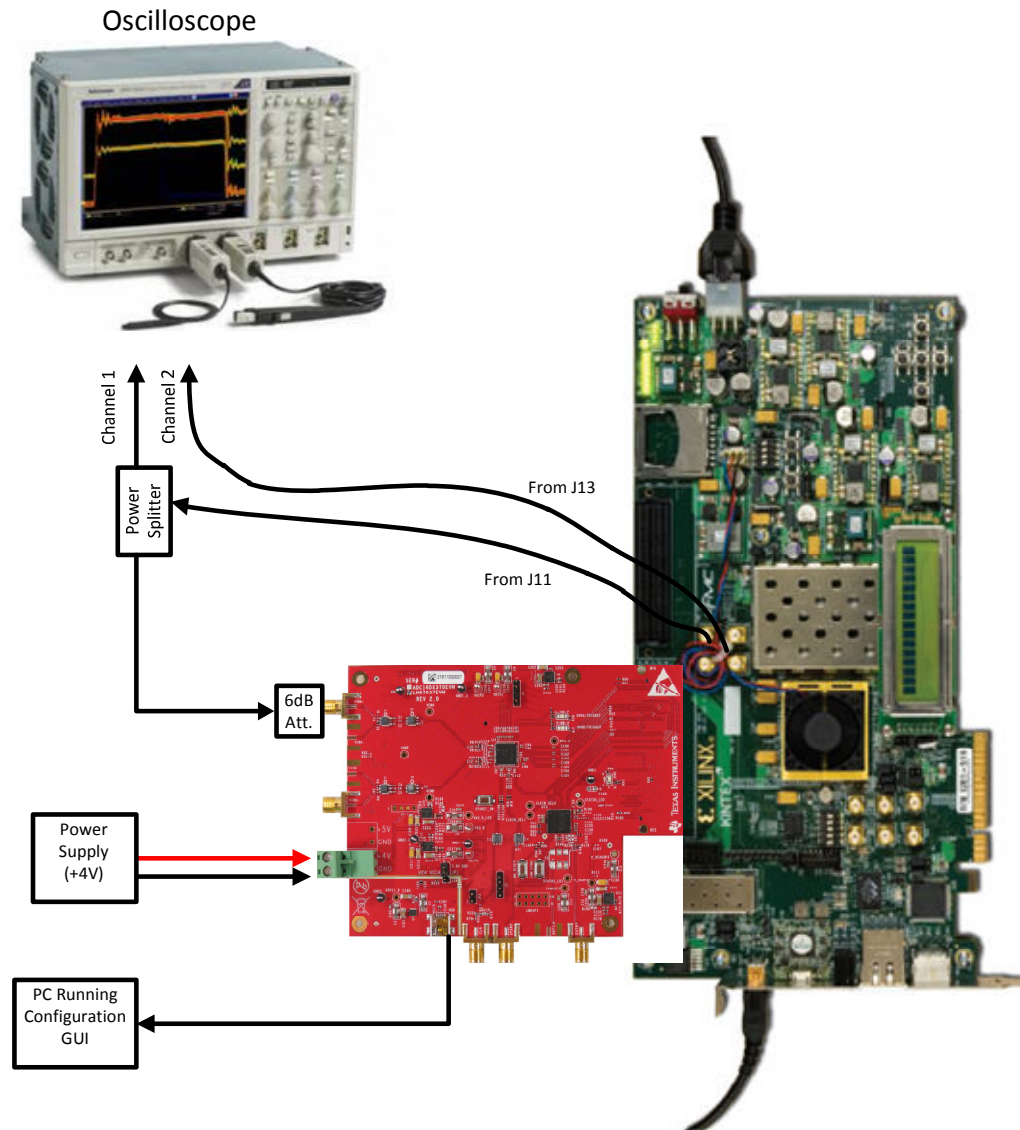
LM97937/ADC16DX370 + Kintex 7 JESD204B Link Latency Measurement Report

2/10/2014

Summary

- Demonstrated deterministic latency and measured the latency of the JESD204B interface between the LM97937 and Kintex 7
- LM97937EVM + KC705 (Xilinx Kintex7 Reference Board)
- Deterministic Latency Demonstrated
 - Latency measured to be 139.9 frame clock cycles
 - Latency Calculated to be 138.9 frame clock cycles
 - Accuracy limited by transmissions line delays, baluns used in the signal path as well as small delays in the FPGA

Hardware Bench Setup



Hardware Bench Setup

- LM97937EVM connects to KC705 on HPC FMC connector
- LM97937EVM is modified from the default configuration
 - ADC CLKIN (368.64MHz) and SYSREF (11.52MHz) driven by LMK04828, LVPECL
 - FPGA driven by LMK04828 such that DEVCLKB=92.16MHz, DEVCLKA=184.32MHz, and SYSREF = 5.76MHz
 - LMK04828 driven by 61.44MHz XO and PLL2 enabled
 - Both SYSREF outputs delayed ~1ns from LMK synchronized rising edges using LMK SDCLK analog delays
 - LMK04828 registers programmed for the above conditions
- FPGA generates a coherent 5.76MHz square wave output from J11 and that is input into Ch.A of LM97937EVM and split off to oscilloscope
- ADC Ch.A MSB is output on J13 and routed to O-scope
- Routings from J11 and J13 and splitting of signal are length minimized and matched as close as possible between channels
- LM97937 configured for L=2 lane/ch., offset binary format

Firmware

- Developed in Xilinx Vivado v2013.4
- Firmware targeted to Kintex 7, XC7325TFFG900
- Design utilizes the JESD204 IP Core v5.1 and is based on the example project provided with the IP Core.
- Some of the required changes to the example project included:
 - Changing GTX so that refclk is 185MHz and lane rate is 3.7Gb/s
 - Updating gblclk input path to accommodate 92.5MHz as JESD204 core operating clock (samples SYSREF)
 - Ensure that the gblclk and sysref differential input clock buffers have 100 ohm input terminations
 - Routing JESD core output bits (corresponding to sample MSBs) directly to SMA output J13. The MSBs of the 4 different samples available in each 92.5MHz clock cycles are selectable using the DIP switches.
 - Modifying AXI files to set default JESD settings as L=4, K=32, F=1, RX Buffer Delay = 4 (making RBD=28), SYSREF always, SCR off

Experiment

- Monitor the alignment of the pulse trains coming from J11 and J13 and verify that they are:
 - Deterministic and do not change skew each time the system is powered up
 - Skewed by the appropriate amount as calculated

Calculated Latency

- For this experiment the following apply
 - All units in Frame clock cycles
 - $t_{RX_LMFC} = 28$
 - $t_{RX_DESER} = 92 \pm 2$
 - $t_{TX_LMFC} = 3.5$
 - $t_{TX_SER} = 6 \pm 1$
 - $t_{LANE} = \pm 1$
 - $K = 32$
 - $RBD=28$ ($RX_BUFFER_DELAY=4$)

Calculated Latency

- Use equations 4 & 5 to verify the n value with release time margin

$$((n-1) \times K + RBD) \times T_{\text{frame}} \leq n \times K \times T_{\text{frame}} < t_{\text{TX_SER}} + t_{\text{LANE}} + t_{\text{RX_DESER}} + (t_{\text{TX_LMFC}} - t_{\text{RX_LMFC}})$$

$$t_{\text{TX_SER}} + t_{\text{LANE}} + t_{\text{RX_DESER}} + (t_{\text{TX_LMFC}} - t_{\text{RX_LMFC}}) < (n \times K + RBD) \times T_{\text{frame}} \leq (n+1) \times T_{\text{frame}}$$

- Try n = 2
- Equation 4: $((2-1) \times 32 + 28) \leq 2 \times 32 < 6 \pm 1 \pm 1 + 92 \pm 2 + (6 - 28)$
 - $60 \leq 64 < 76 \pm 4$
 - OK (8 cycles margin)
- Equation 5: $6 \pm 1 \pm 1 + 92 \pm 2 + (6 - 28) < (2 \times 32 + 28) \leq 3 \times 32$
 - $76 \pm 4 < 92 < 96$
 - OK (12 cycle margin)

Calculated Latency

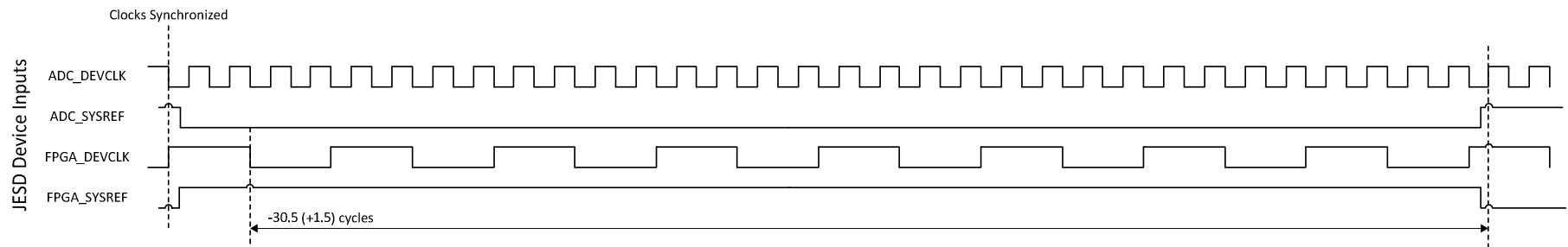
- Per the application note, the latency is calculated from equation 10

$$t_{\text{LINK_LAT_ABS}} = (n \times K + \text{RBD}) \times T_{\text{frame}} + (t_{\text{RX_LMFC}} - t_{\text{TX_LMFC}})$$

- $t_{\text{RX_LMFC}} = 28$, $t_{\text{TX_LMFC}} = 3.5$, $n = 2$, $K = 32$, $\text{RBD} = 28$
 - $t_{\text{LINK_LAT_ABS}}/T_{\text{FRAME}} = 116.5$
 - Add ADC core latency (+12.5, ADC16DX370) \rightarrow 119 clock cycles
- Additional system and experiment dependent details impact latency
 - Skew between moments that SYSREF event is sampled at ADC and FPGA
 - Skew of routing DEVCLK/SYSREF to ADC and FPGA
 - Transmission line skew of routing of output from FPGA board to O-scope
 - Additional processing delays at the back-end of the receiver

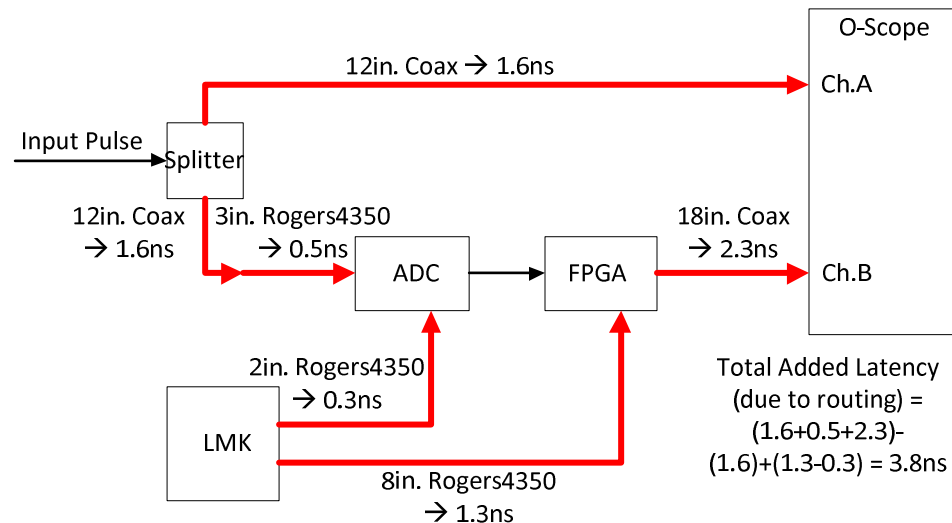
Calculated Latency

- The alignment of the RX and TX LMFCs is influenced by the alignment of the DEVCLKs and SYSREFs to the ADC and FPGA
- The DEVCLK and SYSREF routing from the LMK to the ADC is inverted on the EVM compared to the routing to the FPGA
 - SYSREF is set to $F_s/64$ so the SYSREF inversion to the ADC does not matter
- The FPGA samples on the falling edge of SYSREF @92.5MHz
- ADC samples SYSREF on the rising edge of DEVCLK
- The ADC samples SYSREF high 1.5 cycles before the FPGA



Calculated Latency

- Some latency in the measurement is due to signal routing
- 2.8ns added due to input signal and MSB routing to O-scope
- 1ns added due to DEVCLK/SYSREF routing to ADC and FPGA
- Total Added Latency = 3.8ns (1.4 cycles)
- Accuracy of these calculations expected to be no better than +/-1 frame

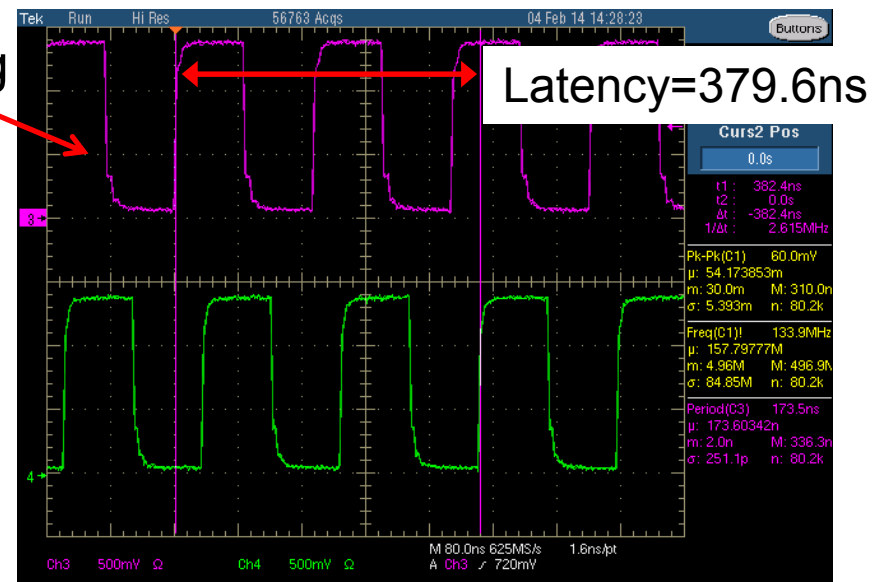
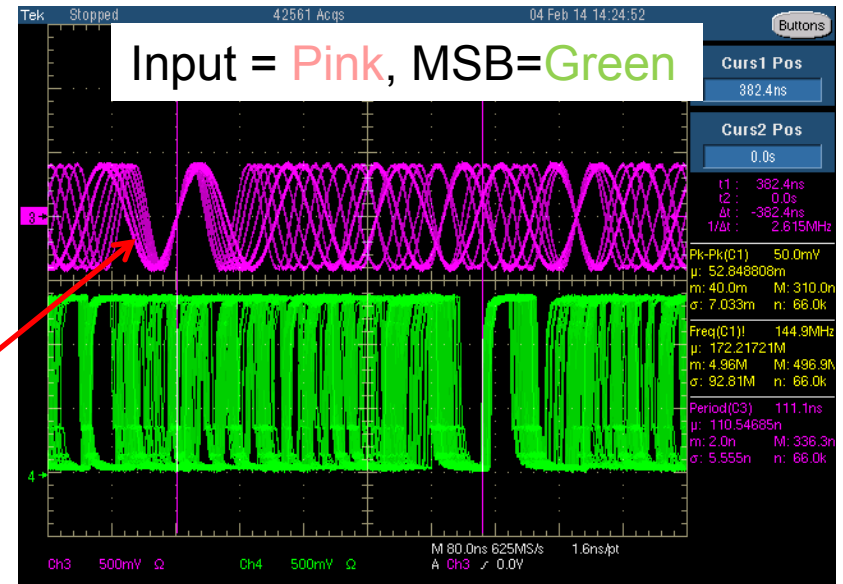


Calculated Latency

- Latency calculated from Eq. 10 plus ADC core latency = 119 clock cycles
- The following also extend the latency
 - DEVCLK and output routing skew = +1.4
 - SYSREF sampling skew = +1.5
 - Additional RX processing = +7
- Total Calculated Latency = $119 + 1.4 + 1.5 + 7 = \mathbf{138.9 \text{ cycles}}$
- Missing 1.0 cycles in total latency calculation compared to measured

Measured Results

- Oscilloscope measures time between rising edge input into ADC and MSB output transition from 0 to 1
- Input a sinusoid into ADC first and sweep the frequency to determine correct latency edge
- Input a pulse train with a period that is an integer multiple of the sampling period for accurate measurement
- Measured latency = 379.6ns (139.9 frame clock cycles)
- System power cycled multiple times and latency remains constant



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