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TI Precision Designs: Verified Design

Single Supply Single-Ended Input to Differential Output

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Circuit Description

This single ended input to differential output circuit converts a single ended input of +0.1V to +2.4V into a differential output of ± 2.3V on a single +2.7V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, Vout+. The second amplifier inverts the input and adds a reference voltage to generate Vout-. Both Vout+ and Vout- range from 0.1V to 2.4V. The difference, Vdiff, is the difference between Vout+ and Vout-. This makes the differential output voltage range +2.3V

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
OPA333	Product Folder

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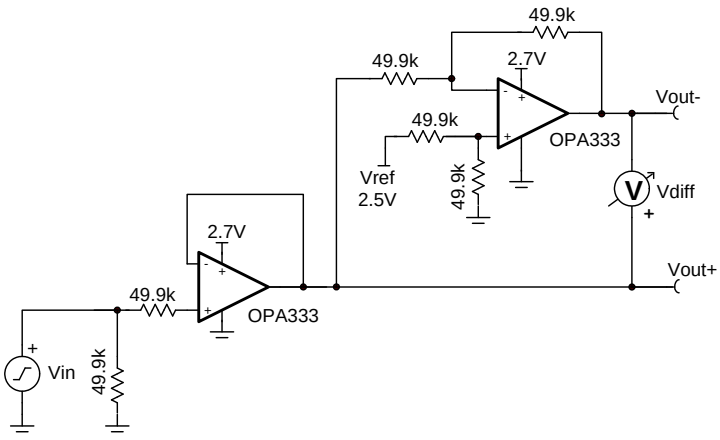


1 Design Summary

The design requirements are as follows:

- Supply Voltage: 2.7V
- Reference Voltage: 2.5V
- Input: 0.1V - 2.4V
- Output Differential: ±2.3V
- Output Common Mode Voltage: +1.25V
- Small Signal Bandwidth: 100kHz
- Low Power: 100µA

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Test Condition	Goal	Hand Calculation	Simulated	Measured
Uncalibrated Error for Vdiff (%FSR)	0.1 < Vin < 2.4V	±0.1%	-	-0.2%	0.07%
Calibrated Error for Vdiff (%FSR)	0.1 < Vin < 2.4V	±0.01%	-	-	0.002%
Total Current	Vcc = 2.7V	100µA	84.1µA	68.3µA	68.5µA
Bandwidth	Vcc = 2.7V	100kHz	200kHz	300kHz	300kHz
Noise	Total Integrated	100 µV rms	-	67.4µV rms	-

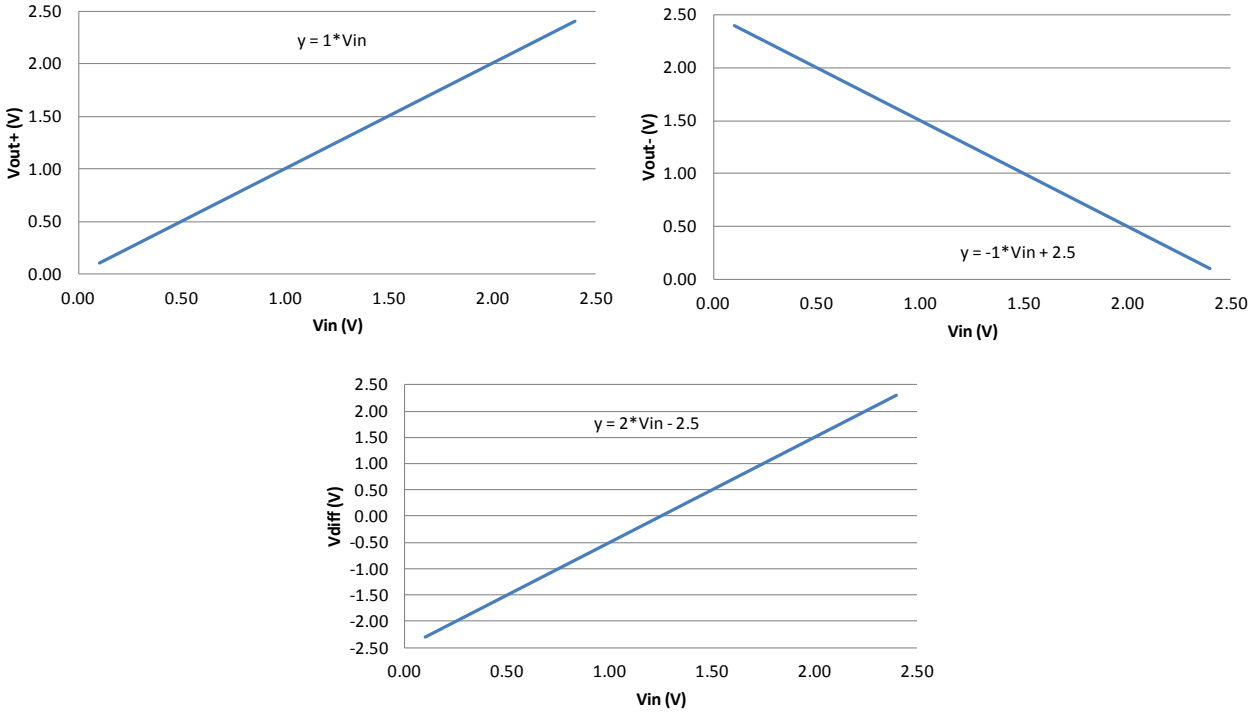


Figure 1: Measured Transfer Function for Vout+, Vout-, and Vdiff

2 Theory of Operation

Figure 2 illustrates the detailed schematic.

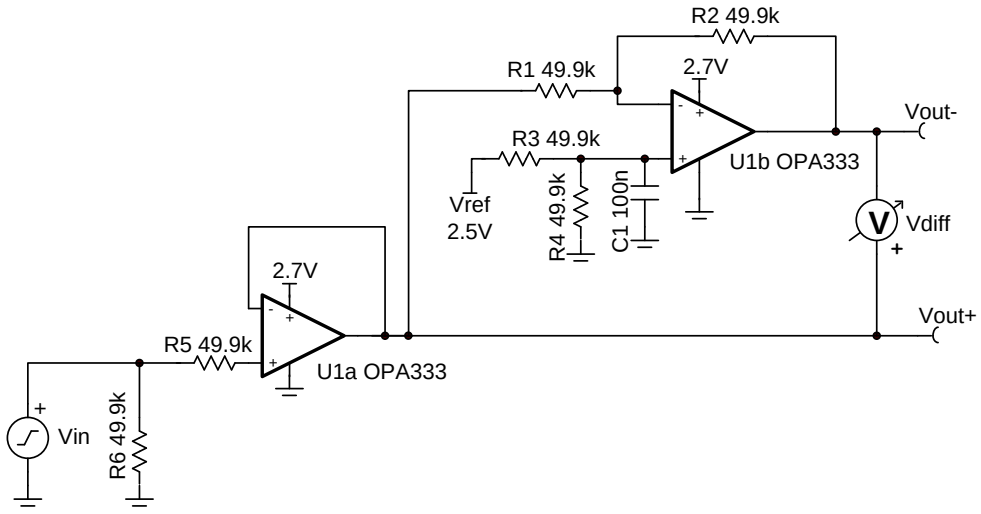


Figure 2: Detailed Schematic

2.1 Design Overview

The circuit takes a single ended input signal, Vin, and generates two output signals, Vout+ and Vout- using two amplifiers and a reference voltage, Vref. The differential output signal, Vdiff, is the difference between the two single-ended output signals. Vout+ is the output of the first amplifier and is a buffered version of the input signal, Vin; see Equation (1). Vout- is the output of the second amplifier which uses Vref to add an offset voltage to Vin and feedback to add inverting gain. The transfer function for Vout- is Equation (2).

$$V_{out+} = V_{in} \tag{1}$$

$$V_{out-} = V_{ref} * \left(\frac{R4}{R3 + R4}\right) * \left(1 + \frac{R2}{R1}\right) - V_{in} * \frac{R2}{R1} \tag{2}$$

Vdiff is the differential output voltage between Vout+ and Vout-. The transfer function for Vdiff is shown in Equation (3). By applying the conditions that R1 = R2 and R3 = R4 the transfer function is simplified into Equation (6). Using this configuration the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the Vref. The differential output range is twice the Vref. Furthermore, the common mode voltage will at one half of Vref; see Equation (7).

$$V_{diff} = V_{out+} - V_{out-} = V_{in} * \left(1 + \frac{R2}{R1}\right) - V_{ref} * \left(\frac{R4}{R3 + R4}\right) * \left(1 + \frac{R2}{R1}\right) \tag{3}$$

$$V_{out+} = V_{in} \tag{4}$$

$$V_{out-} = V_{ref} - V_{in} \tag{5}$$

$$V_{diff} = 2 * V_{in} - V_{ref} \tag{6}$$

$$V_{cm} = \frac{V_{out+} + V_{out-}}{2} = \frac{1}{2}V_{ref} \tag{7}$$

3 Component Selection

This section will cover the reasoning behind the selected component values.

3.1 Amplifier Selection

In this design our goal is to achieve good dc accuracy and low noise while maintaining low power. Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations will determine the linearity. In general an amplifier with rail-to-rail input and output swing is required. Low input offset voltage and offset drift are also key considerations for dc accuracy. Bandwidth is not a key concern for this design; however, in section 7.1 we will discuss circuit modifications that allow for a higher bandwidth design.

The OPA333 meets all of the key considerations for this circuit. The OPA333 is a high-precision CMOS op amp with 5µV offset, 0.05µV/°C drift, and 55nV/rtHz output noise. The OPA333 uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. It is optimized for low-voltage, single supply operation with an output swing to within 50 mV of the positive rail Additionally, the quiescent current is typically 25µA, allowing for low power operation. The typical unity gain bandwidth for the OPA333 is approximately 350kHz, which is above our design requirement. While this is a relatively low bandwidth, the key concern for designing this circuit was low power. In general, increasing bandwidth on an op amp will increase the quiescent current and power used by the amplifier.

3.2 Passive Component Selection

Because the transfer function of Vout- is heavily reliant on resistors R1, R2, R3, and R4, resistors with low tolerances should be used to maximize performance and minimize error. To fit the design requirement of low power, we also selected the resistance to minimize the op amp load current. However, the resistance cannot be too high, or noise from the resistor will be too large. For this design, resistors with resistance values of 49.9k and tolerances of 0.1% were used to fit these criteria. Using these resistances, the maximum current drawn by the circuit is 84.1µA (see Equations (8) and (9)). This current is a combination of the quiescent current, the output of U1b, and the reference current.

$$I_{max} = \frac{V_{out\_max} - 0.5 * Vref}{R2} + \frac{Vref}{R3 + R4} + 2 * I_Q \quad (8)$$

Where

- I_{max} is the maximum current drawn by the entire circuit
- V_{out_max} is the maximum output at Vout-
- I_Q is the typical quiescent current of the amplifier

$$I_{max} = \frac{(2.5V) - 0.5 * (2.5V)}{49.9k\Omega} + \frac{2.5V}{49.9k\Omega + 49.9k\Omega} + 2 * (17\mu A) = 84.1\mu A \quad (9)$$

From Figure 3, the noise spectral density of the resistors is less than 28.7nV/rtHz. Figure 3.3 shows that the noise of the OPA333 is approximately 55nV/rtHz. For low noise design it is recommended that the amplifier noise is larger than the resistor noise. The op amp is generally the most expensive part, and it would be counter-intuitive to purchase a low noise amplifier only to have more noise from the resistors. The resistor noise is lower than the amplifier noise which confirms our selection is correct (i.e. 28.7nV/rtHz < 55nV/rtHz).

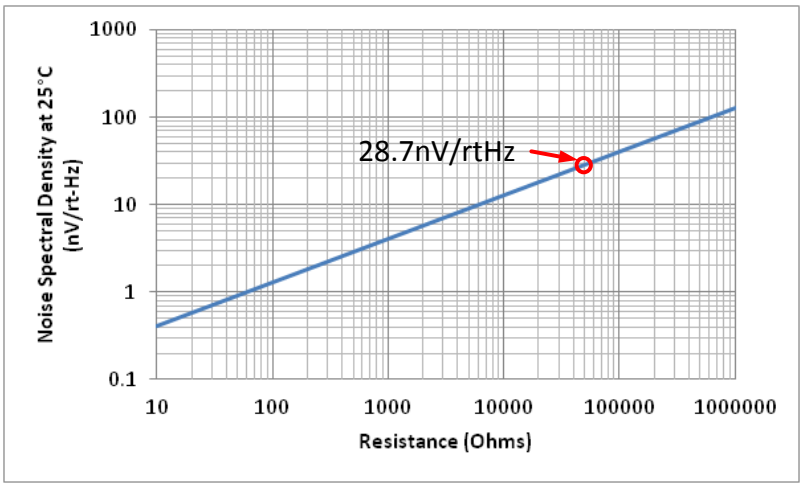


Figure 3: Noise Spectral Density vs. Resistance

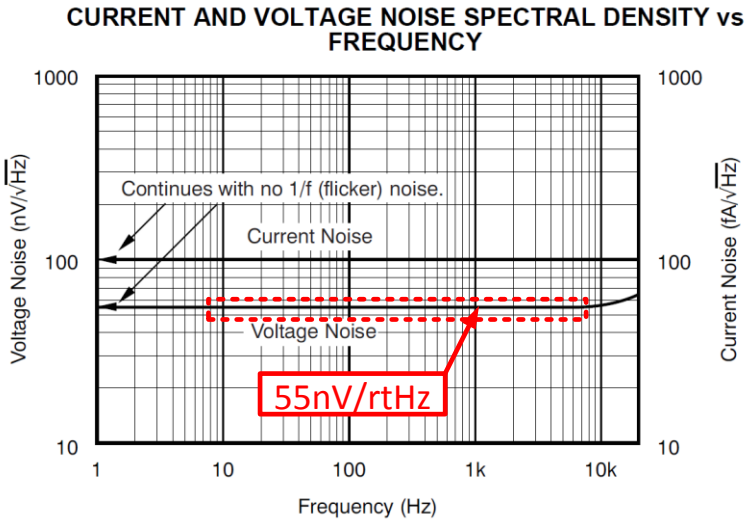


Figure 4: Noise Spectral Density for OPA333

The resistor R5 protects the input of the amplifier by limiting the current in case transient input voltages exceed the supply voltage of the amplifier. According to the absolute maximum device ratings for the amplifier, the input current must be less than 10mA. The example in Figure 5 shows that the current would be limited to 0.53mA for a 30V transient. Equation (10) and (11) show the calculation for a 30V transient. Note, for negative transients V_{supply} is zero. Equations (12) and (13) show the maximum transient for this configuration. Note that the transient protection in this example is beyond what is generally needed, however, the resistance is consistent with other resistors in the circuit to simplify the BOM. Furthermore, the noise contribution and offset current effects introduced by R5 will not create any significant errors.

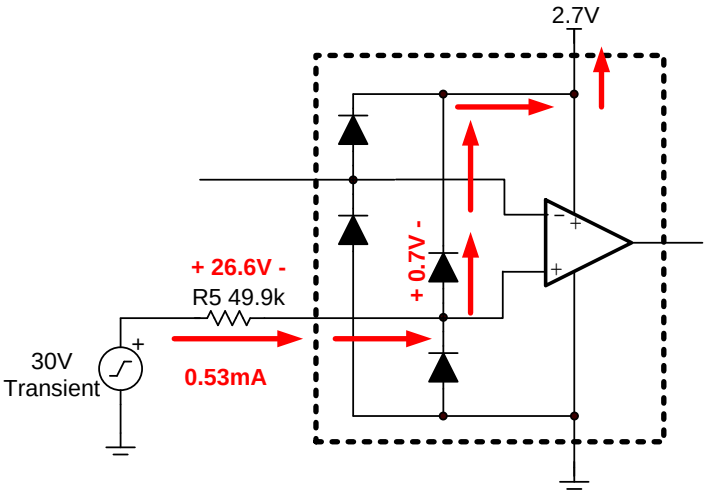


Figure 5: Protection Resistor

$$I_{in} = \frac{V_{in} - V_{diode} - V_{supply}}{R_{lim}} \quad \textbf{(10)}$$

$$I_{in} = \frac{30V - 0.7V - 2.7V}{49.9k\Omega} = 0.53mA \quad \textbf{(11)}$$

$$V_{in} = I_{in} * R_{lim} + V_{diode} + V_{supply} \quad \textbf{(12)}$$

$$V_{in} = (10mA) * (49.9k\Omega) + 0.7V + 2.7V = 502.4V \quad \textbf{(13)}$$

The remaining components, R6 and C1, ensure accuracy. Resistor R6 prevents floating inputs. For convenience, R6 is set to have a resistance of 49.9kΩ. Resistors R5 and R6 do not have to have 0.1% tolerances because they do not affect the transfer function. The capacitor, C1 is a filter capacitor.

4 Simulation

Figure 6 gives the TINA SPICE schematic used for the simulations in this section.

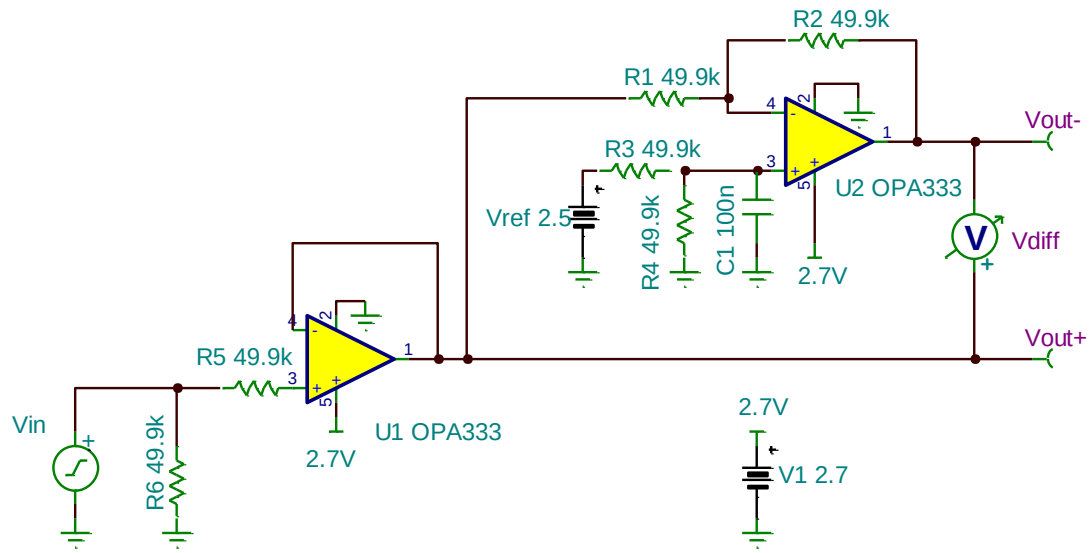


Figure 6: TINA SPICE Simulation Schematic

4.1 Transfer Function (dc)

The plots in Figure 7 were created by sweeping the dc voltage from 0.1V to 2.4V. Note that the input is restricted by 0.1V to maintain linearity of the OPA333 by keeping its outputs at least 100mV away from either power supply rail.

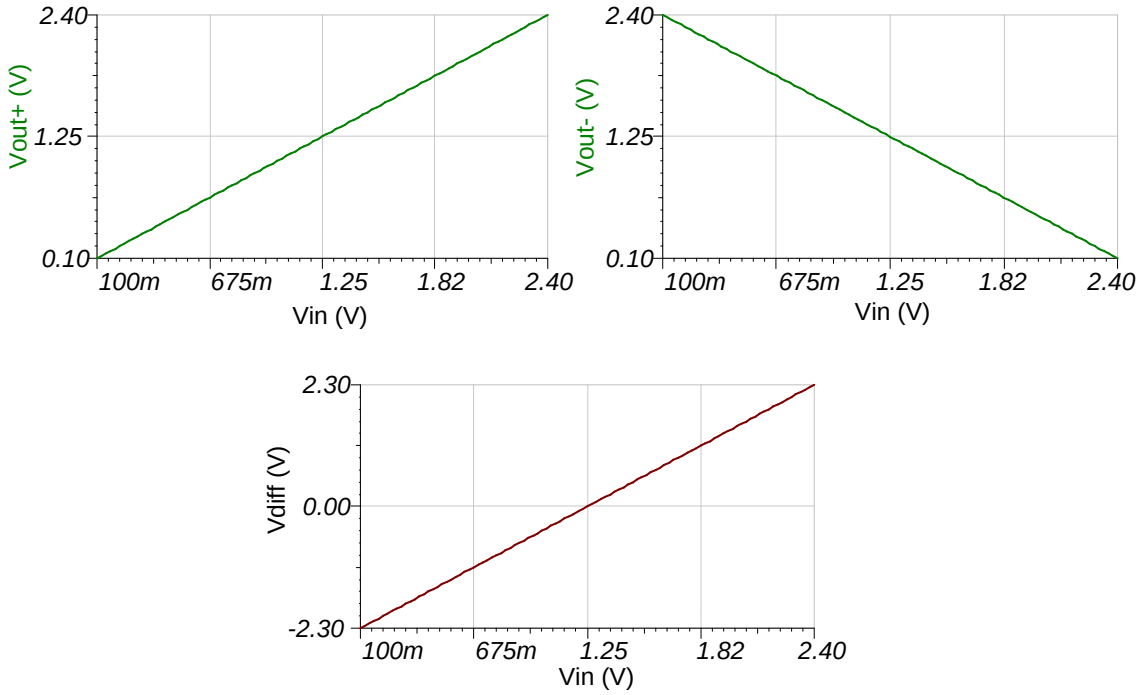


Figure 7: Simulated dc Transfer Function

The error plots in Figure 8 were generated using a Monte Carlo Analysis where the input (Vin) was swept from 0V to 2.5V to show total error. The error was measured as a percentage of the full scale range (%FSR). The different slopes are caused by the statistical variation of the resistance due to tolerance. In this case, the tolerance of each resistor is set to 0.1%. Notice that at the ends of the input range the error increases. This is because of output swing limitations on the OPA333. Also the open loop gain (Aol) decreases when the output is less than 100mV from the power supply rails (see Figure 9).

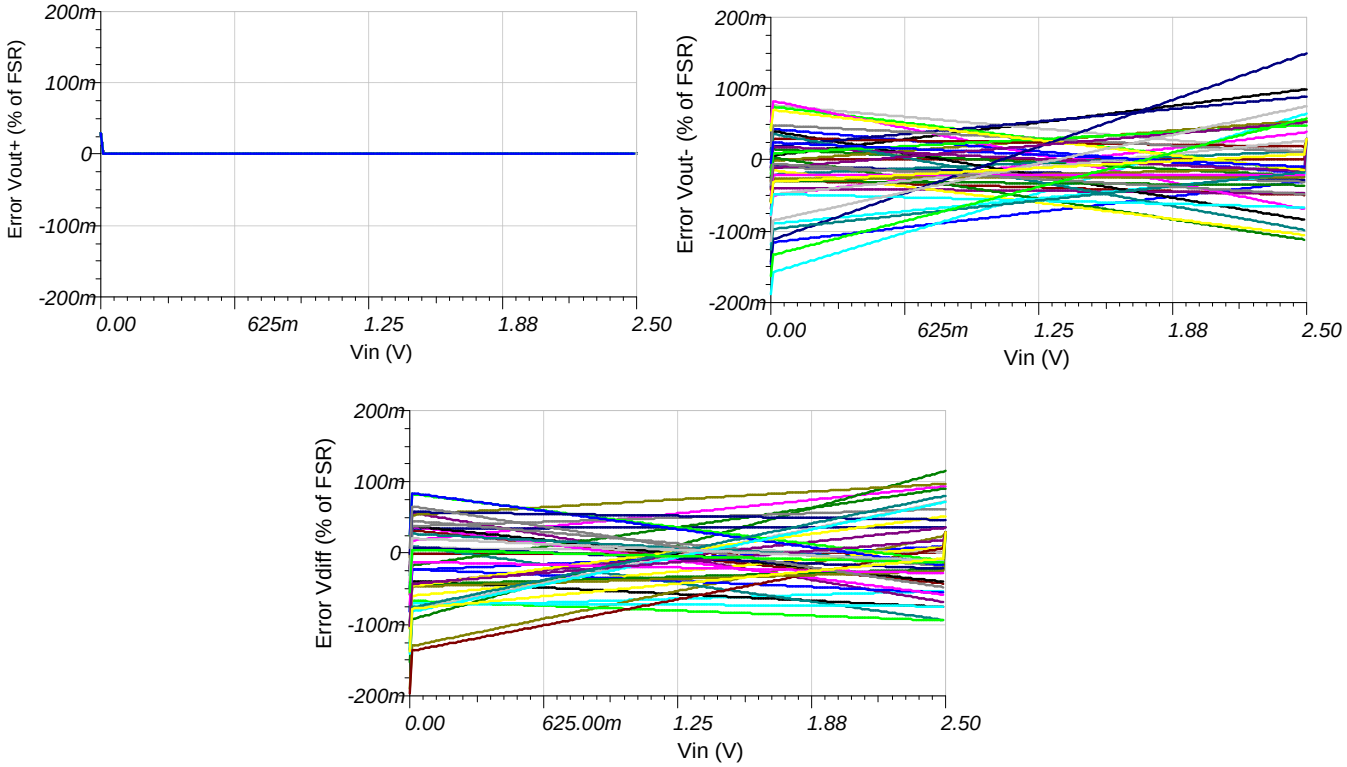


Figure 8: Monte Carlo Error Analysis of dc Transfer Function

OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	(V–) + 100mV < V_O < (V+) – 100mV, R_L = 10kΩ	106	130		dB

Figure 9: Excerpt from OPA333 Data Sheet

The noise analysis in Figure 10 shows the varying noise of Vdiff across different values of resistances due to the tolerance. By inspection, the thickness of the line is not large, suggesting that noise does not vary greatly with our chosen tolerances. The Figure 11 is the integral of Figure 10 and represents the total noise. Overall, the total noise is approximately 67.4μV rms or 404μVpp.

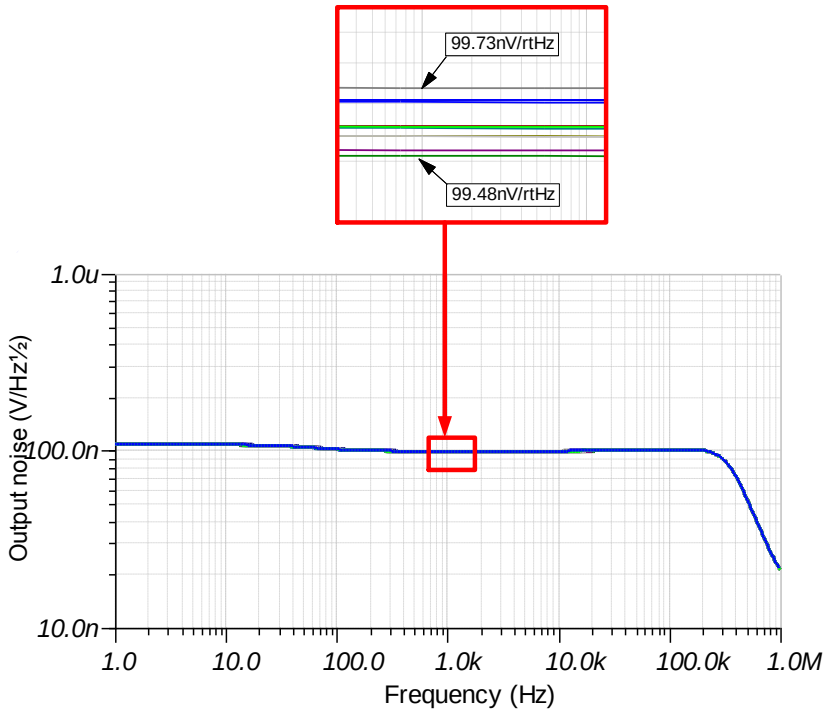


Figure 10: Noise Spectral Density Out (Monte Carlo Analysis)

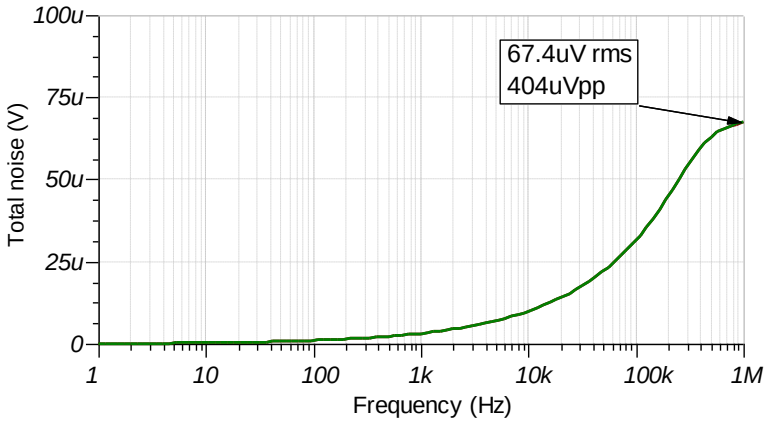


Figure 11: Total Integrated Noise Output (V rms)

4.2 Bandwidth

Figure 12 is the Aol curve taken from the OPA333 data sheet. The bandwidth of the buffer configuration, where gain (G_n) is equal to one, of the OPA333 is the point where the Aol curve equals 0dB. Consistent with the data sheet table, this appears to be approximately 350kHz. The second op amp is in noise gain configuration of 2 (6dB). Noise gain is the non-inverting gain of an op amp configuration. When using an Aol curve, noise gain must always be used. The bandwidth for $G_n = 2$ appears to be approximately 200kHz. These should be consistent with the results of the small signal input found in section 6.3.

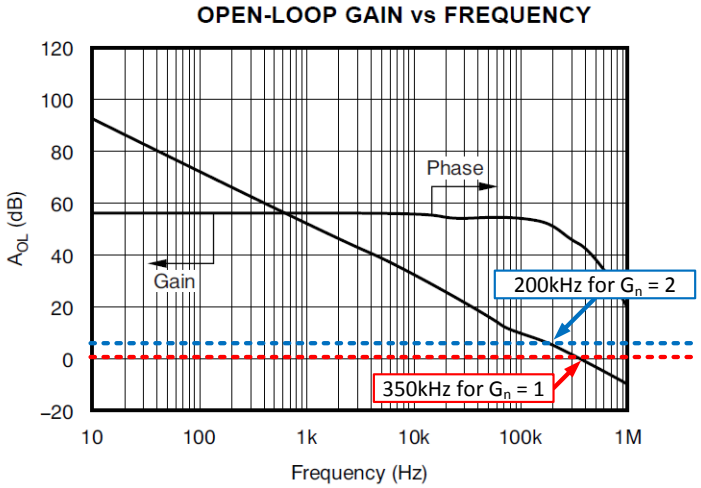


Figure 12: Estimating Bandwidth for OPA333 Using the Aol Curve

Figure 13 shows the simulated bandwidth limitations for each output. Vout+ has a wider bandwidth than Vout- because the noise gain is lower for Vout+ ($G_n = 1$ for Vout+ and $G_n = 2$ for Vout-). Notice that the simulated results differ from the calculated results (compare Figure 12 and Figure 13). The differences between simulated and calculated results occur because the model only approximates the data sheet and secondary effects, such as gain peaking, may affect results.

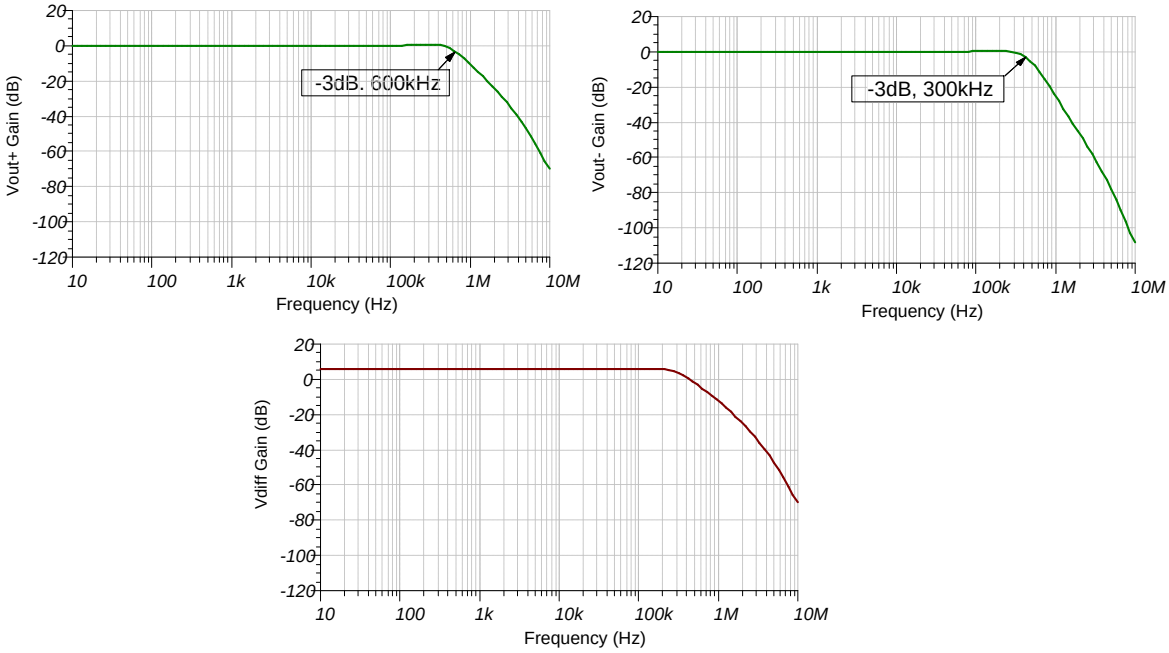


Figure 13: Simulated Bandwidth limits

4.3 Large Signal Step Response

A step input wave from 0.1V to 2.4V was applied to measure the settling time to an accuracy of 0.1%. From Figure 4.10, the approximate settling time is 17.8µs for 0.1% tolerance.

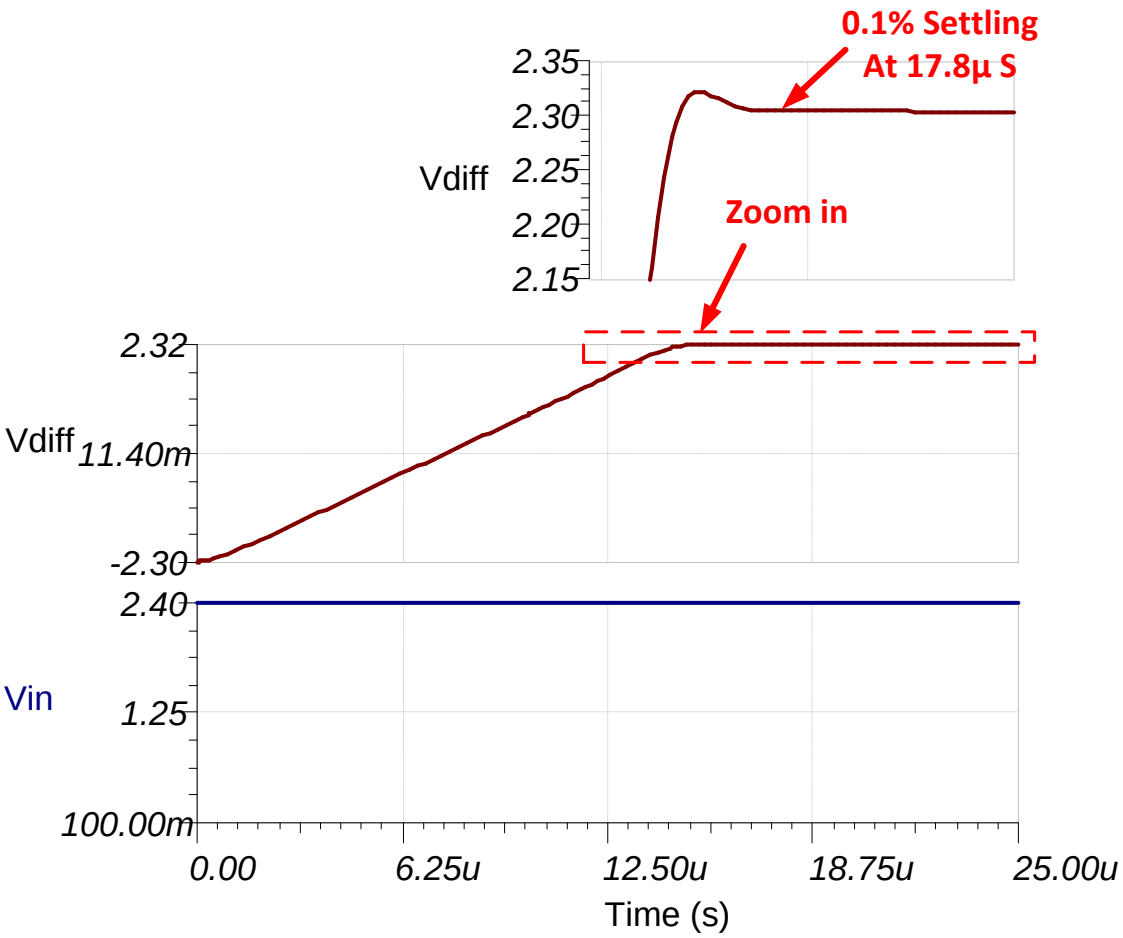


Figure 14: 0.1% Settling Time (Vin = 0.1V to 2.4V)

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The general guidelines for precision PCB layout were used on this design. For example, trace lengths are kept to minimum length especially input signals.

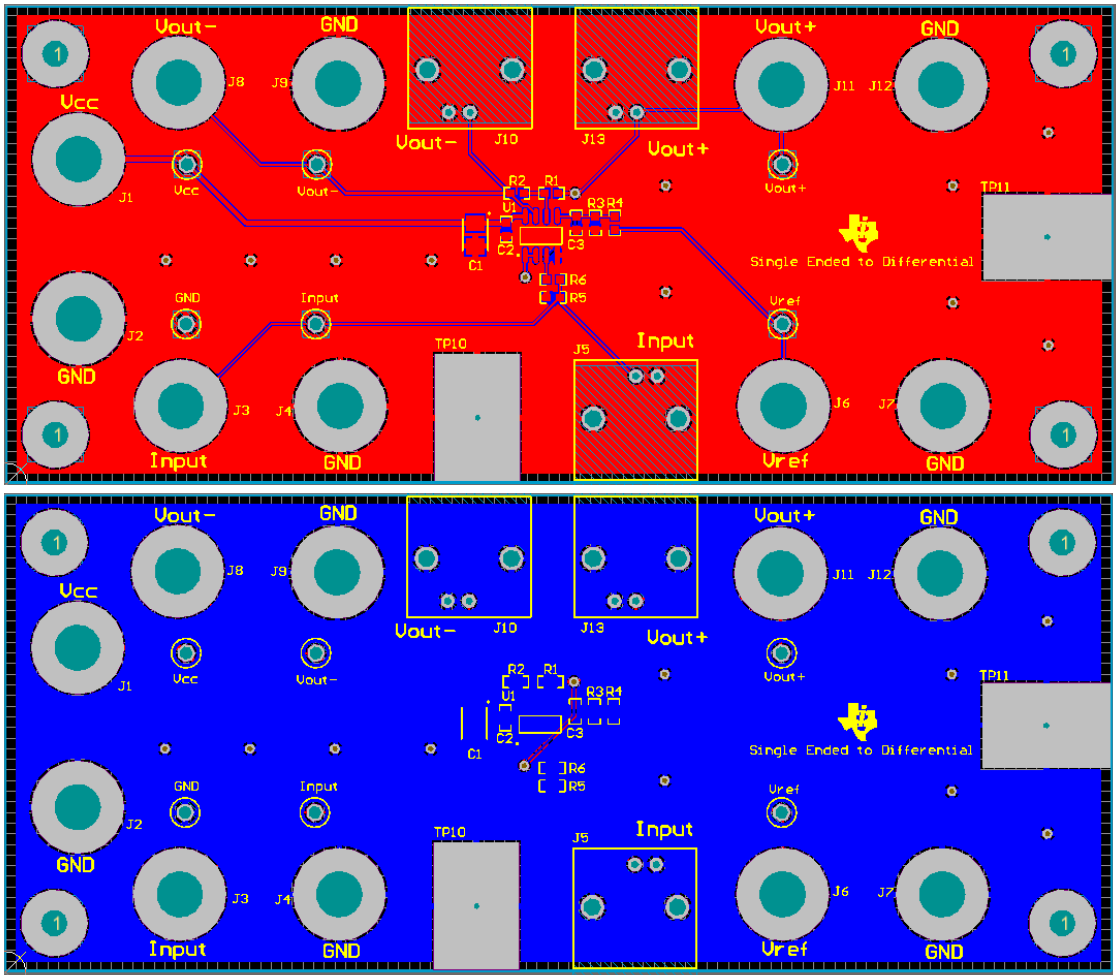


Figure 15: Altium PCB Top Layout (top) and Bottom Layout (bottom)

6 Verification & Measured Performance

6.1 Transfer Function (dc)

The measured transfer functions in Figure 16 were generated by sweeping the input voltage from 0.1V to 2.4V. The full input range is actually 0V to 2.5V, but it is restricted by 0.1V to maintain optimal linearity. A two point calibration was used to optimize the accuracy of the system (see Appendix B). The results in this section are all measured post calibration.

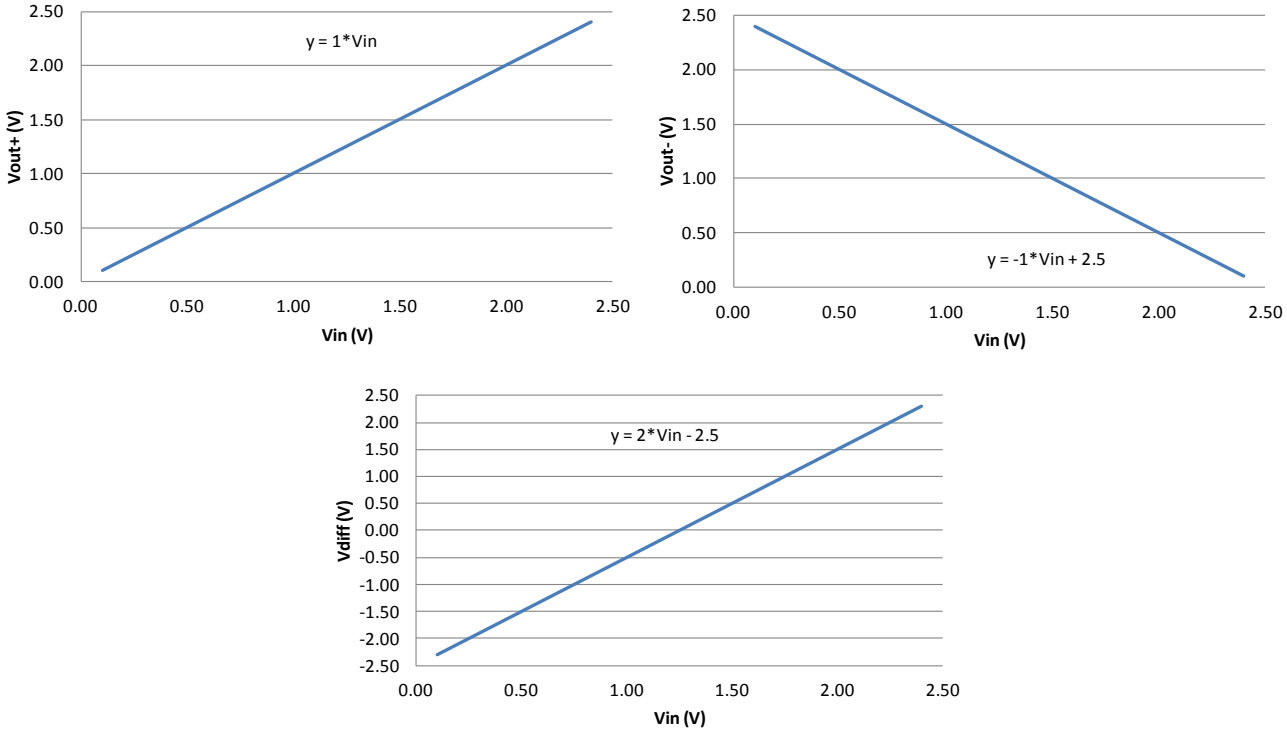


Figure 16: Measured dc Transfer Function (post calibration)

Figure 17 shows the post calibration error. The major sources of error in this circuit are resistor tolerance, and offset voltage. Calibration eliminates these errors. The error remaining after calibration is from noise, temperature drift, common mode rejection, and other non-repeatability errors. Overall, the errors are very small: 0.000222%, -0.00161%, and 0.00164% for Vout+, Vout-, and Vdiff respectively. These errors are voltage differences in the tens of microvolts.

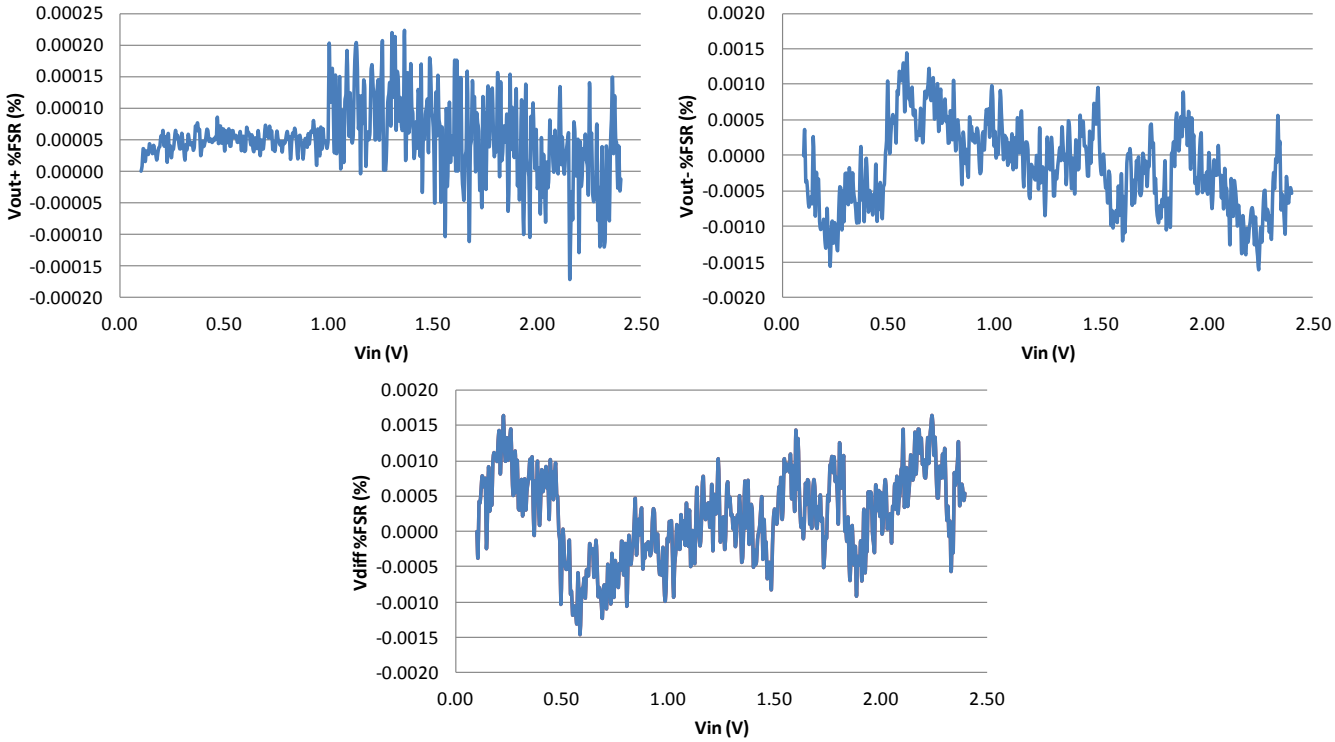


Figure 17: Measured Error as % FSR (Post Calibration)

Figure 18 illustrates error as a % of FSR for entire input range (0V < Vin < 2.5V). Notice that the errors increase dramatically as the input approaches either end of its range. This is why the input range is restricted to 0.1V < Vin <2.4V during calibration to optimize accuracy.

This non-linearity is the result of the output swing limitations of the OPA333 (see section 4.1). Overall, the errors for Vout+, Vout-, and Vdiff are 0.0207%, 0.0438% and -0.0457% respectively. These are errors of millivolts, two orders of magnitude larger than the errors in the linear region, showing non-linearity near 0V and 2.5V.

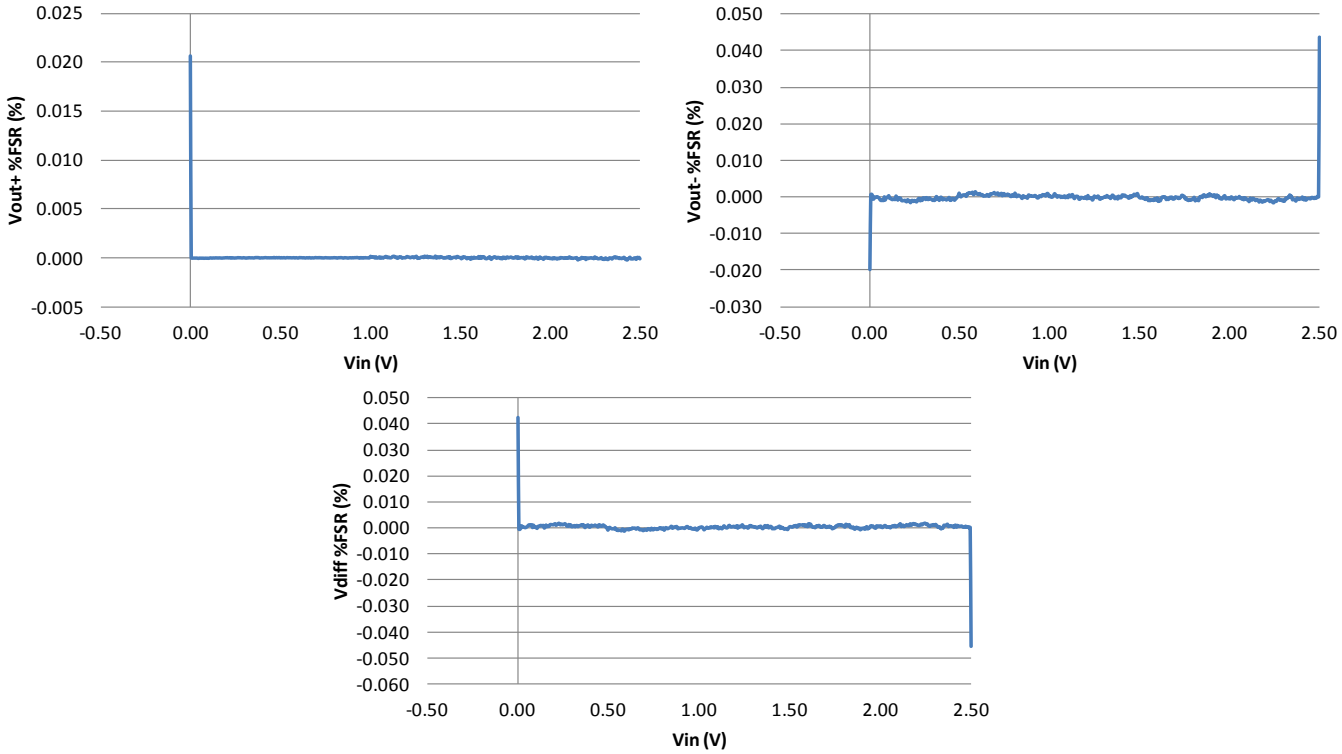


Figure 18: Error as % FSR Including Non-linear Region

6.2 Slew Induced Distortion (THD+N)

When applying sinusoidal waveforms to this circuit, it is possible to cause slew induced distortion. Slew induced distortion occurs when the rise time of the sine wave exceeds the amplifiers slew rate. Both the frequency and amplitude of the input signal affect the rise time and are factors in determining if slew induced distortion is an issue. The relationship between slew rate limit, frequency, and peak output signal is given in Equation (14).

$$SR \geq 2\pi f V_{pk} \tag{14}$$

Where

- **SR** is the minimum amplifier slew rate required to avoid slew induced distortion
- **f** is the frequency of the input signal
- $\mathbf{V_{pk}}$ is the peak voltage of the output signal

Equation (14) can be rearranged into Equation (15) to find the full power bandwidth, f_{FB}.

$$f_{FB} = \frac{SR}{2\pi V_{pk}} \tag{15}$$

Where

- $\mathbf{f_{FB}}$ is the full power bandwidth. This is the maximum frequency that can be applied without slew induced distortion.

The full power bandwidth can also be seen as a maximum output frequency that can be achieved without having slew induced distortion. For a full-scale input signal, the full power bandwidth is calculated below.

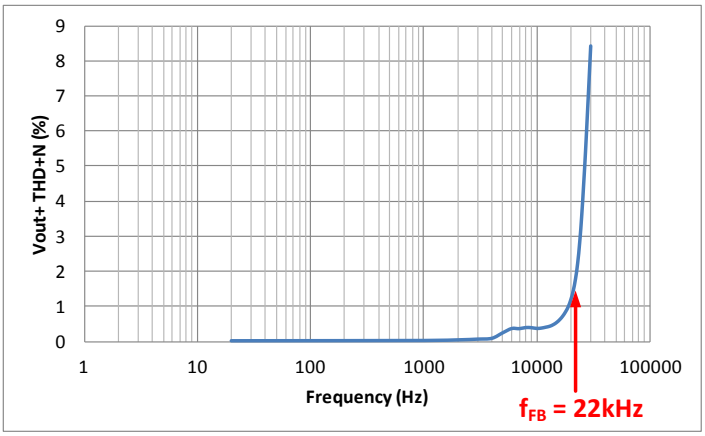
$$f_{FB} = \frac{0.16V/\mu s}{2\pi(1.15V)} \approx 22kHz \tag{16}$$

Where

- **SR** is 0.16V/µs for the OPA333 (found in the data sheet)
- $\mathbf{V_{pk}}$ is the peak amplitude. For a sine wave, this is half the peak-to-peak amplitude. In this case, the peak amplitude is 1.15V (i.e. half of 2.3V)

The data in Figure 19 was generated by sweeping frequency from 20Hz to 30kHz and measuring the total harmonic distortion and noise (THD+N) with automated test equipment optimized for measuring THD+N. The objective is to show that distortion will dramatically increase as we approach the slew induced distortion frequency limit (f_{FB} = 22kHz).

THD+N approaches 0.1% at approximately 3kHz for Vout- and 4kHz for Vout+. THD+N of 0.1% is sometimes thought of as the maximum distortion allowable for reasonable performance. As a rule of thumb, the full power bandwidth should be a decade less than the frequency calculated by the slew rate to ensure minimal distortion.



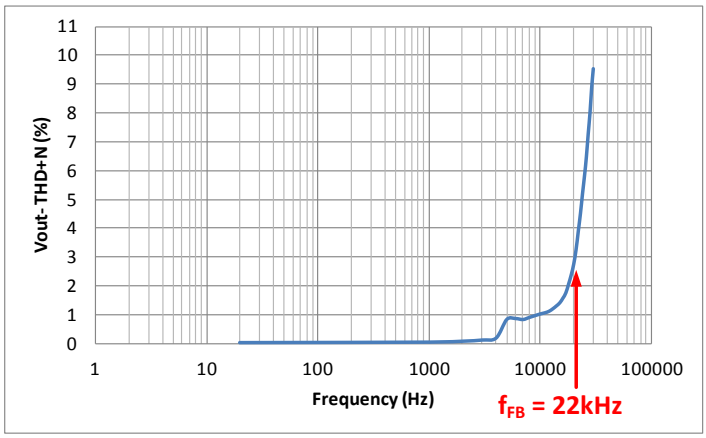


Figure 19: THD+N for Both Outputs

6.3 Bandwidth

The small signal response data was generated by using a function generator to generate a sine wave of amplitude 10Vpp and an offset of 1.25V for the input. The small signal was offset such that the signal was entirely in the linear operating region. Using the same bandwidth calculation as above, the bandwidth is calculated below.

$$f_{FB} = \frac{0.16\text{V}/\mu\text{s}}{2\pi(5\text{mV})} \approx 5\text{MHz} \quad \textbf{(17)}$$

However, the bandwidth of the OPA333 is shown in Section 4.2 to be 350kHZ for the first op amp and 200kHz for the second op amp. Since these limits are lower, they will control the bandwidth.

The data for Vout+ in Figure 20 was calculated by plotting the ratio of the peak-to-peak value of Vout+ to Vin in decibels verses the frequency. The formula to calculate the gain in decibels is Equation (18).

$$\text{Gain(db)} = 20 * \log {}^{V_{out+}}/_{V_{in}} \quad \textbf{(18)}$$

The data for Vout- in Figure 20 was calculated in a similar manner. However, the ratio was of the peak-to-peak value of Vout- to Vout+, as shown in Equation (19).

$$f_{FB} = \frac{0.16\text{V}/\mu\text{s}}{2\pi(5\text{mV})} \approx 5\text{MHz} \quad \textbf{(19)}$$

The ratio is Vout- to Vout+ because the input to the second op amp is Vout+.

The measured -3dB frequencies for Vout+ and Vout- are 600kHz and 300kHz respectively. The bandwidth of the circuit is therefore 300kHz. This is higher than the calculated bandwidth due to effects of peaking near unity gain

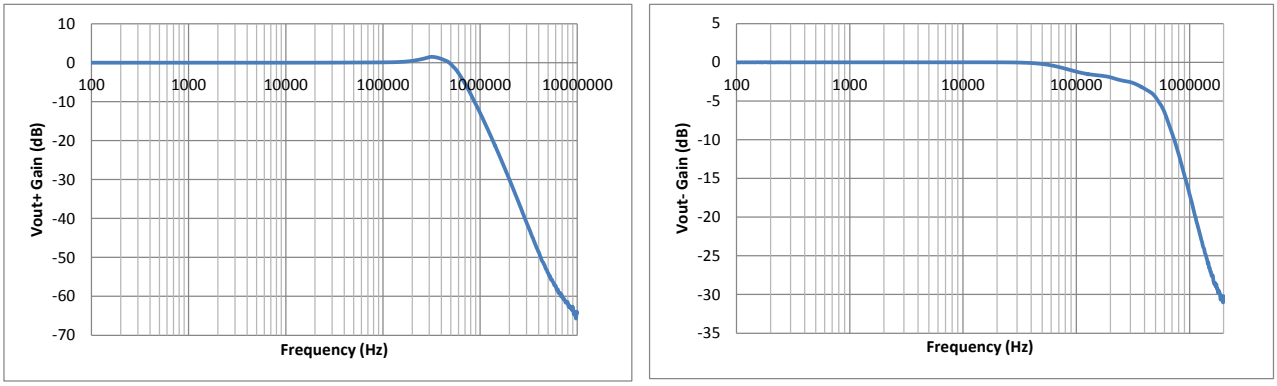


Figure 20: Bode Plots for Vout+ and Vout-

6.4 Large Signal Step Response

The large signal step response was generated with a function generator creating a square wave with frequency 1kHz, amplitude of 2.3Vpp, and offset of 1.25V. The results are shown in Figure 21.

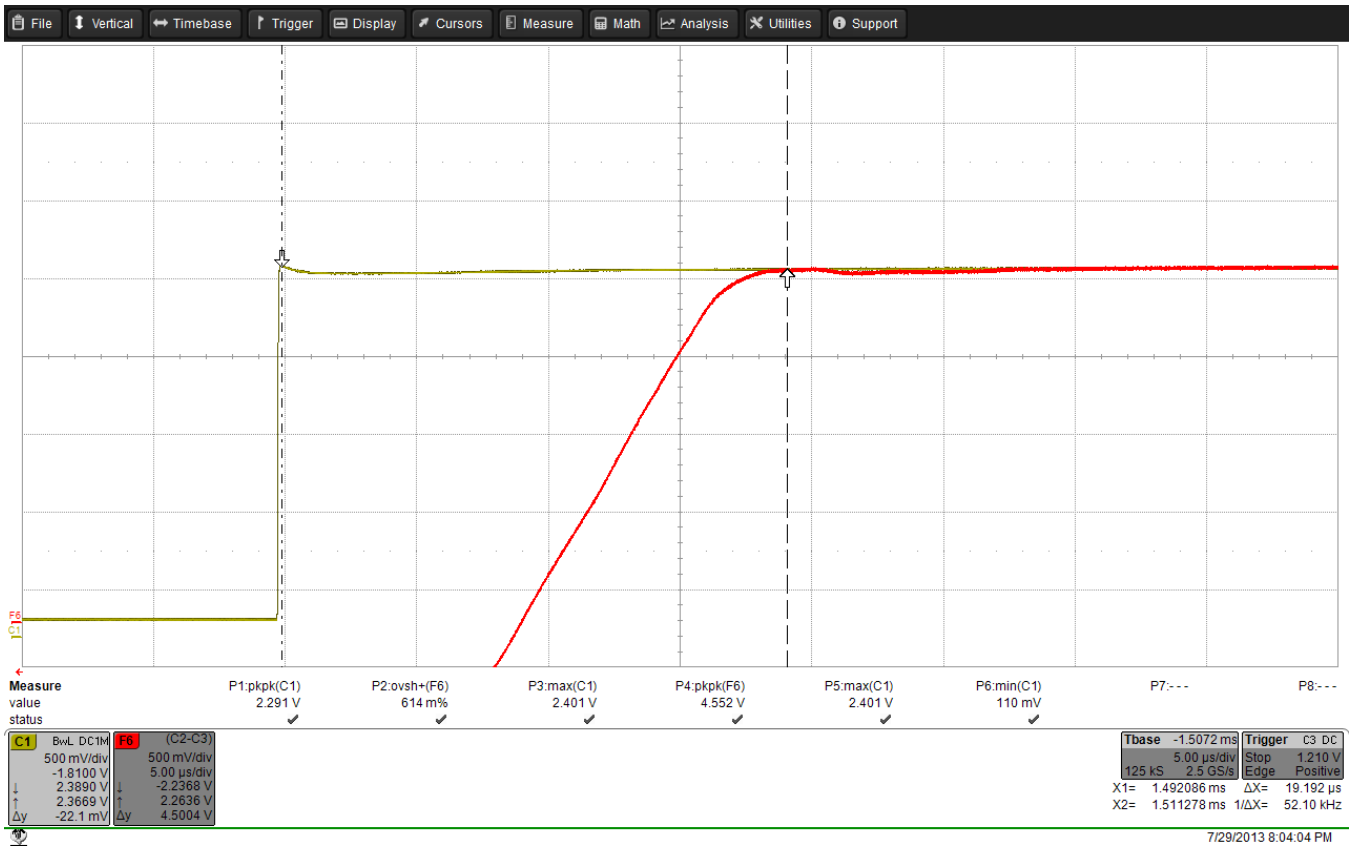


Figure 21: Large Signal Step Response of Vdiff

The settling time to 0.1% tolerance could not be measured. The measured settling time to 1% was approximately 20µs.

7 Modifications

7.1 Increasing Bandwidth

To increase bandwidth, a different amplifier must be chosen. The tradeoff with increasing bandwidth is increasing the power dissipated by the circuit. In general, amplifiers with wider bandwidth consume more power. In general, amplifiers with lower noise will consume more power. Smaller resistances must then be used (see Figure 3). This further decreases noise and increases power. Table 2 lists possible alternative amplifiers with their respective maximum specifications.

Table 2: Alternative Amplifiers

	OPA314	OPA376	OPA374	OPA320
Bandwidth (MHz)	3	5.5	6.5	20
Noise at 1kHz (nV/rtHz)	14	7.5	15	7
Offset Voltage (µV)	2500	25	5000	150
Offset Drift (µV/°C)	1	2	3	1.5
Quiescent Current (µA)	210	950	750	1600

7.2 Changing Input and Output Range

Another modification to the circuit is changing the input range and output differential range (see Figure 22). Both changes can be implemented by adding a gain in the first stage. This also changes the common mode voltage of the outputs. Initially, the common mode is 1.25V. The new common mode voltage will depend on the resistances chosen and may possibly not be constant. To make the common mode voltage constant, R2 must equal R1 (see Equation (23)). This also makes Vout+ and Vout- symmetric about the common mode. The new transfer functions and the common mode voltage are shown as Equations (20), (21), (22), and (23) with R2 = R1.

$$V_{out+} = \left(1 + \frac{R8}{R7}\right) * V_{in} \quad \textbf{(20)}$$

$$V_{out-} = 2 * V_{ref} * \left(\frac{\mathrm{R4}}{R3 + R4}\right) * - \left(1 + \frac{R8}{R7}\right) * V_{in} \quad \textbf{(21)}$$

$$V_{diff} = 2 * \left(1 + \frac{R8}{R7}\right) * V_{in} - 2 * V_{ref} * \left(\frac{\mathrm{R4}}{R3 + R4}\right) \quad \textbf{(22)}$$

$$\mathrm{V_{cm}} = \frac{1}{2} * \left(\left(\frac{\mathrm{R4}}{R3+R4}\right) * \left(1+\frac{\mathrm{R2}}{\mathrm{R1}}\right) * \mathrm{V_{ref}} + \left(1 - \frac{\mathrm{R2}}{\mathrm{R1}}\right) * V_{out+}\right) = \left(\frac{\mathrm{R4}}{R3+R4}\right) \mathrm{V_{ref}} \quad \textbf{(23)}$$

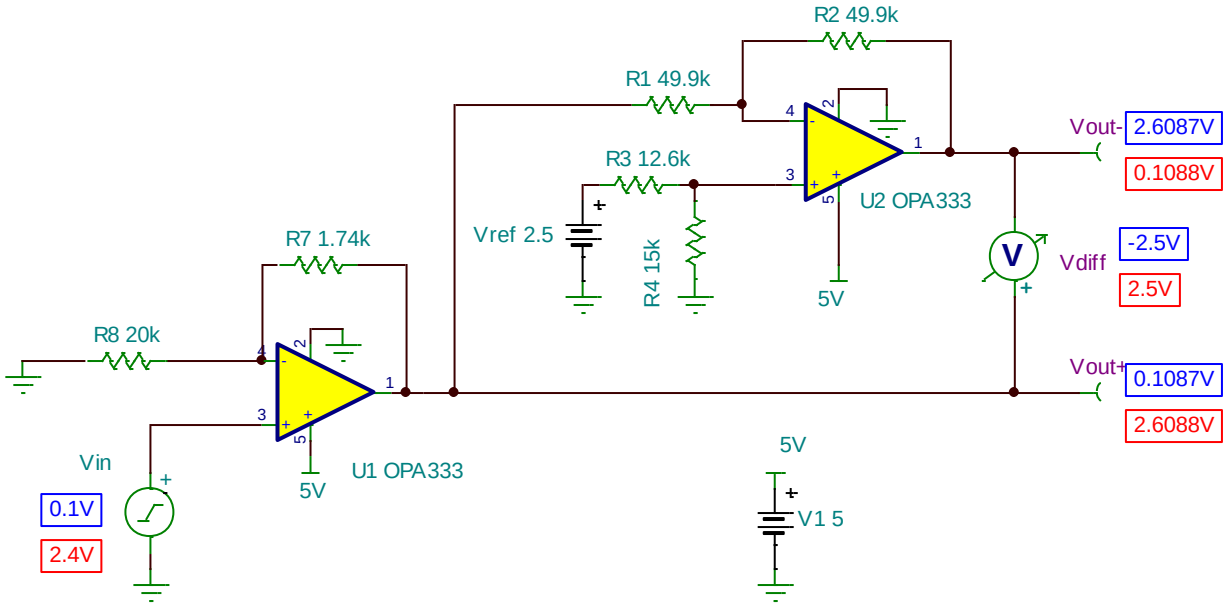


Figure 22: Modified Circuit

To explain the process, consider an example with an input range of 0.1V to 2.4V to and output differential range of ±2.5V and a reference of 2.5V. Because R1 = R2, we know that both Vout+ and Vout- must have full scale ranges of 2.5V. The input full scale range is 2.3V (i.e. 2.4V – 0.1V). The gain of the first amplifier must scale the full scale input range to the full scale output range (i.e. gain is equal to 2.5V/2.3V). Therefore, the relationship between R8 and R7, which controls the gain of the first amplifier, is defined (see Equation (24)). Note that if the gain is too large, the output swing of Vout+ may be in the non-linear region of the amplifier. In this example, 0.1087V < Vout+ < 2.6088V. The maximum output is less than 100mV away from the power supply, so the power supply must be changed to maintain linearity. The circuit was modified to use a 5V power supply

$$\frac{R8}{R7} = \frac{2.5V}{2.3V} - 1 = 0.0870 \quad \textbf{(24)}$$

This gain defines the output range of Vout+, which also defines the output range of Vout- (see Table 3 or Figure 22: Modified CircuitFigure 22).

Table 3: Voltage Range for Vin and all Outputs

	Vin (V)	Vout+ (V)	Vdiff V (V)	Vout- (V)
Minimum Voltage	0.1	0.10870	-2.5	2.60870
Maximum Voltage	2.4	2.60880	2.5	0.10880

Both outputs are symmetric about some common mode, so the common mode is the midpoint of the either output range. Using this information and Equation (23), we can determine the relationship of R3 and R4 (see Equation (25)).

$$\frac{R4}{R3} = \frac{0.5 * (2.60870V + 0.10880V)}{2.5V - 0.5 * (2.60870V + 0.10880V)} = 1.1906 \quad \textbf{(25)}$$

The resistances chosen need to fulfill the ratios, follow the guidelines set in section 3.2, and be consistent with standard resistances. Figure 23 displays the simulated transfer functions of the designed circuit.

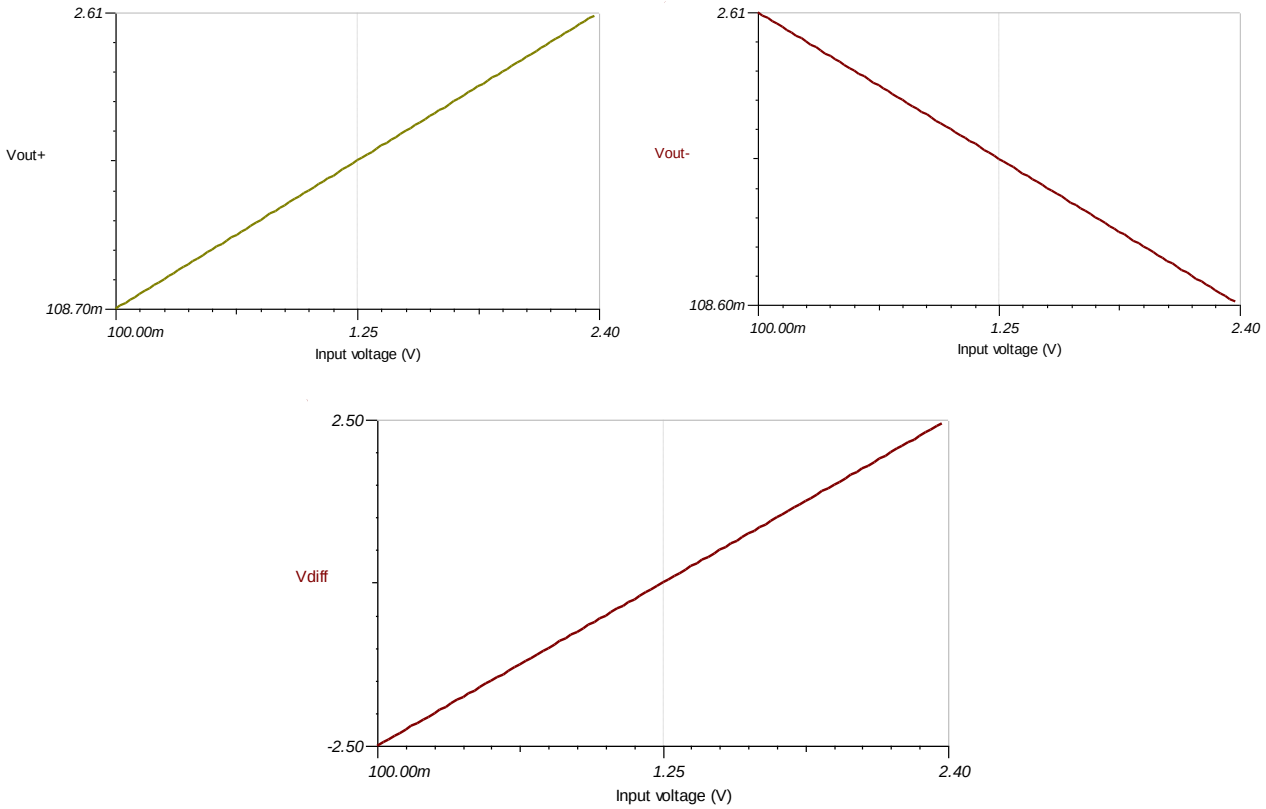


Figure 23: Simulated Transfer Functions for Modified Circuit

8 About the Author

Thanh-Phong Nguyen was an intern for the Precisions Linear group at Texas Instruments. He currently is an undergraduate student pursuing a B.S. in Electrical Engineering at the Georgia Institute of Technology.

9 Acknowledgements & References

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2. *J. Vega. (2013, August 7). Harmonic Distortion: Part I – Understanding Harmonic Distortion Vs. Frequency Measurements in Op Amps. Available: http://www.en-genius.net/site/zones/acquisitionZone/technical_notes/acqt_013012*

Appendix A.

A.1 Electrical Schematic

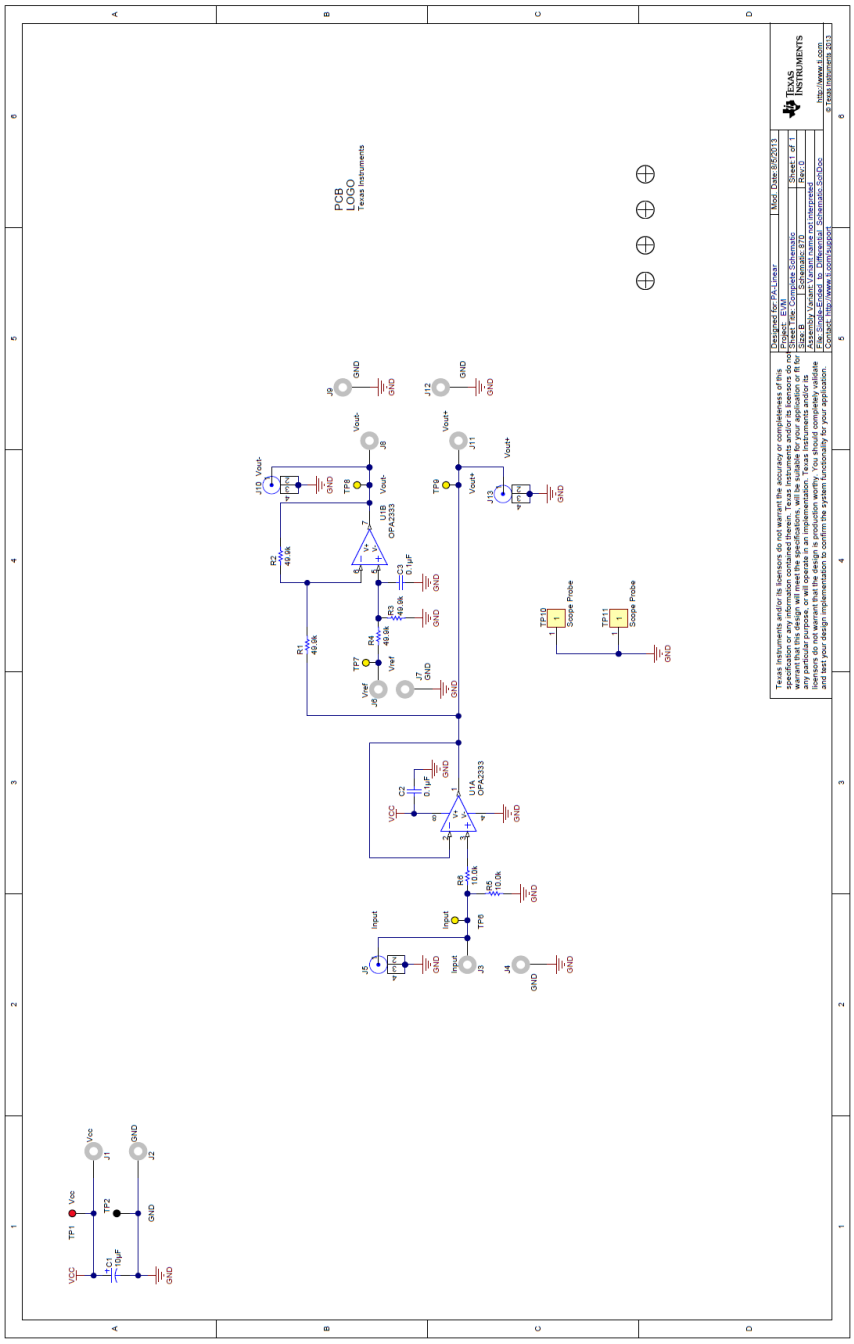

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Item	Qty	Value	Designator	Description	Manufacturer	Manufacturer Part #	Supplier Part #
1	1	10uF	C1	CAP, TANT, 10uF, 20V, 20%, 1 ohm, 3528-21 SMD	AVX	TPSB106M020R1000	478-4087-1-ND
2	2	0.1uF	C2, C3	CAP, CERM, 0.1uF, 50V, 10%, X7R, 0603	MuRata	GRM188R71H104KA93D	490-1519-1-ND
3	10		J1, J2, J3, J4, J6, J7, J8, J9, J11, J12	JACK NON-INSULATED .218" Keystone"	575-4	575-4K-ND	
4	5		J2, J4, J7, J9, J12	JACK NON-INSULATED .218" Keystone"	575-4	575-4K-ND	
5	3		J5, J10, J13	BNC Connector	TE Connectivity	1-1478032-0	A97560-ND
6	6	49.9k	R1, R2, R3, R4, R5, R6	RES, 49.9k ohm, 0.1%, 0.1W, 0603	Panasonic	ERA-3AEB4992V	P49.9KDBCT-ND
7	1	Vcc	TP1	Test Point, TH, Compact, Red	Keystone	5005	5005K-ND
8	1	Black	TP2	Test Point, TH, Compact, Black	Keystone	5006	5006K-ND
9	4	Yellow	TP6, TP7, TP8, TP9	Test Point, TH, Compact, Yellow	Keystone	5009	5009K-ND
10	1	LF353M	U1	1.8V, 17µA, microPower, Precision, Zero Drift CMOS Op Amp	Texas Instruments	OPA2333AID	296-19543-5-ND
11	4		U90, U91, U92, U93	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	H542-ND

Figure A-2: Bill of Materials

Appendix B.

B.1 Calibration

Due to amplifier offset voltage and resistor tolerance, the data will have an offset and a gain error. Figure 24 illustrates this point with great exaggeration. One source of gain error is due to the tolerances of the resistors. This was simulated in the Monte Carlo analysis in section 4.1. Another source of gain error is limitations of Aol; it is not infinite nor constant. The offset is due to uncertainties in the reference voltage, Vref. Calibration will remove these uncertainties.

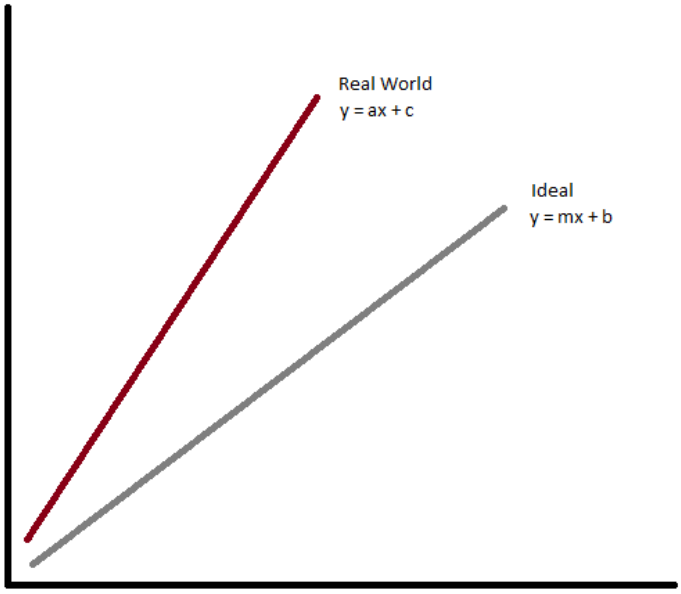

Figure 24: Measured Data with Offset and Gain Error

To calibrate the data, we assume the data is linear. We assume that there is a gain error, G_{error}, and an offset, V_{offset}. In other words, Equation (26) mathematically defines the relationship between the ideal voltage reading and the measured one.

$$V_{measured} = G_{error} * V_{ideal} + V_{offset} \quad (26)$$

Assuming good linearity, G_{error} and V_{offset} should be constant for all measured values. To find these constants, the maximum and the minimum of the linear range will only be considered. Therefore, we will have a system of two equations with two unknowns: Equations (27) and (28).

$$V_{measured\_max} = G_{error} * V_{ideal,\_max} + V_{offset} \quad (27)$$

$$V_{measured\_min} = G_{error} * V_{ideal\_min} + V_{offset} \quad (28)$$

Solving Equations (27) and (28) for G_{error} and V_{offset} yields Equations (29) and (30).

$$G_{error} = \frac{V_{measured\_max} - V_{measured,\_min}}{V_{ideal\_max} - V_{ideal\_min}} \quad (29)$$

$$V_{offset} = \frac{V_{measured\_min} * V_{ideal\_max} - V_{measured\_max} * V_{ideal\_min}}{V_{ideal\_max} - V_{ideal\_min}} \quad (30)$$

In Figure 25, the uncalibrated data for Vout+ is displayed. The red squares indicate the endpoints of the linear range.

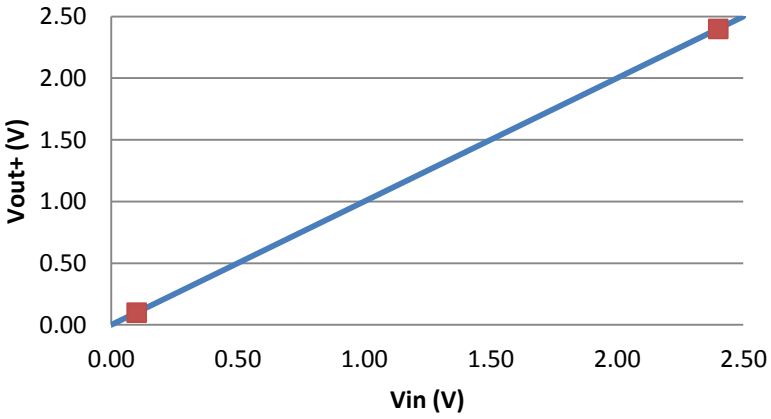

Figure 25: Uncalibrated Vout+ Data

The maximum Vout+ in the linear range is 2.39973V and the minimum is 0.10017V. The values of the ideal Vout+ are 2.39978V and 0.10017V respectively. Using Equations (29) and (30), we can find the offset and gain error.

$$G_{error} = \frac{2.39973V - 0.10017V}{2.39978V - 0.10017V} = 0.999980\ V/V \quad (31)$$

$$V_{offset} = \frac{(0.10017V) * (2.39978V) - (2.39973V) * (0.10017V)}{(2.39978V) - (0.10017V)} = 1.68 \times 10^{-6}\ V \quad (32)$$

This procedure must be repeated for all 3 outputs. The gain errors and offsets for the measured data are summarized in Table 4.

Table 4: Calculated Gain Error and Offset Voltage

Reading	Gain Error (V/V)	Offset (V)
Vout+	0.999980	1.68e-6
Vout-	0.999995	-1.20e-3
Vdiff	0.99999	1.18e-3

To calibrate the data, the offset is subtracted, and the gain error is divided out for all measured values, as shown in Equation (33).

$$V_{calibrated} = \frac{V_{measured} - V_{offset}}{G_{error}} \quad (33)$$

The calibrated error is shown in section 6.1.

Even with calibration, there will be errors in the output due to inherent op amp errors such as input offset voltage, offset drift, and noise. The error in %FSR is defined in Equation (34). In error analysis, error in %FSR will be used to avoid complications near an ideal value of 0V.

$$\%FSR_{error} = \frac{V_{measured} - V_{ideal}}{|Measurement\ Range|} \quad (34)$$

The measurement range is 4.6V for Vout+, Vout-, and Vdiff to allow for comparison.

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