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TI Designs – Precision: Verified Design

36 V, 1 A SPI Controlled Power Supply with Integrated Current Shunt

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Circuit Description

Simple power supplies are often required when constructing test hardware. This version offers 16-bits of programmable accuracy using a Serial Peripheral Interface protocol while providing a maximum voltage of 36 V with a maximum current load of 1 A. This supply can also interface with a simple SAR or Δ-Σ analog to digital converter (ADC) for continuous output current monitoring.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
DAC8871	Product Folder
OPA140	Product Folder
LF411A	Product Folder
OPA549	Product Folder
INA146	Product Folder
REF102	Product Folder
OPA2277	Product Folder

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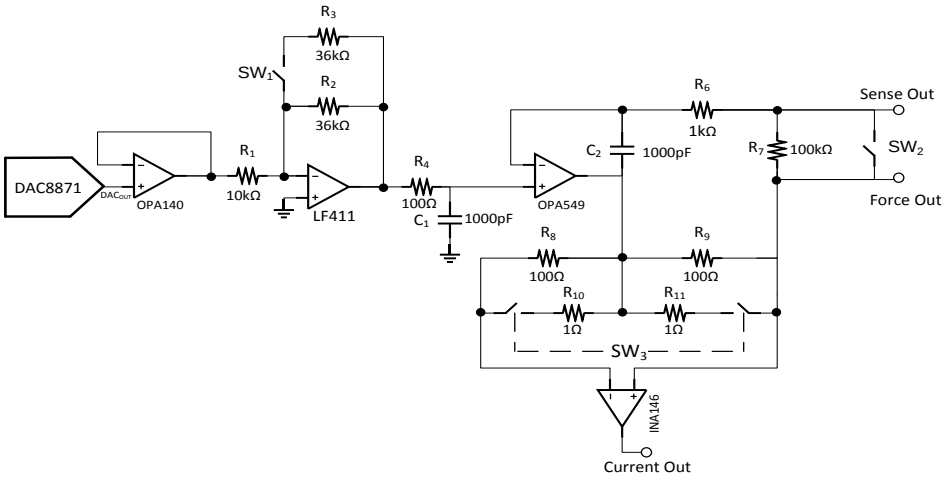

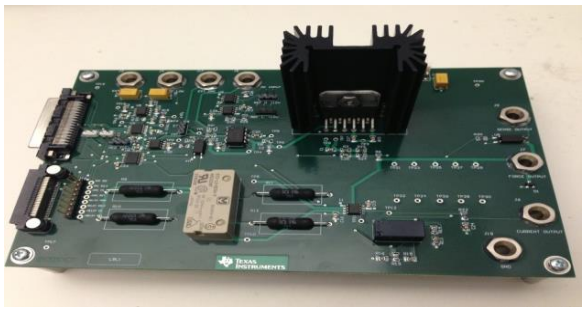

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1 Design Summary

The design requirements are as follows:

- Supply voltage for amplifying and power stages of 43 V dc. The negative supply requires -3 V dc and the positive supply requires 40 V dc
- Supply Current Limit of 1A @ 40 V
- Supply voltage for other components: -15 V to 15 V dc
- Input: Two 3-wire Serial-Peripheral Interfaces (SPIs) for DAC and Relay configuration control
- Current Monitor Output: Scaled to ±1 V to easily fit inside a typical precision analog-to-digital (ADC) range

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	INA146 Gain (V/V)	Current Shunt (Ω)	Goal	Simulated	Measured
V_{OUT} Gain Error (%FSR)	1 or 100	1 or 100	0.1%	-0.006716	-0.079
V_{OUT} Load Regulation (µV/mA)	1	1	50	-0.016680	2.92
		100	50	-1.088813	2.61
	100	1	50	-0.013118	2.45
		100	50	-1.088727	N/A
V_{OUT} Offset (mV)	1 or 100	1 or 100	50	4.2205615	8.2301825
INA Gain Error (%FSR)	1	1	1	-1.998930	1.001730
		100	1	-2.007920	-0.030363
	100	1	1	-1.988344	1.003658
		100	1	-1.997240	-0.141955
INA CMRR (dB)	1	1	70	68.999155	92.278229
		100	70	69.008537	89.456711
	100	1	70	69.091690	92.317234
		100	70	69.101018	89.538604

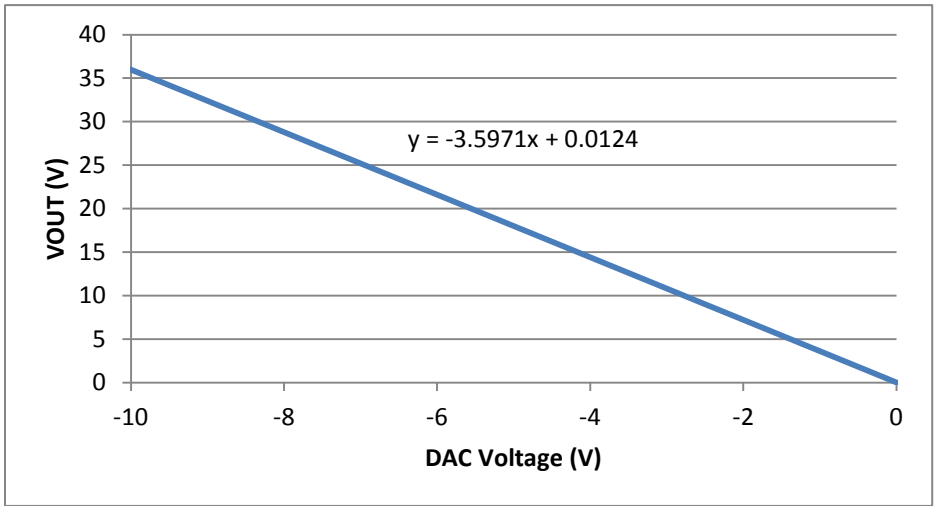

Figure 1: Measured Transfer Function

2 Theory of Operation

A schematic for the circuit is shown in Figure 2.

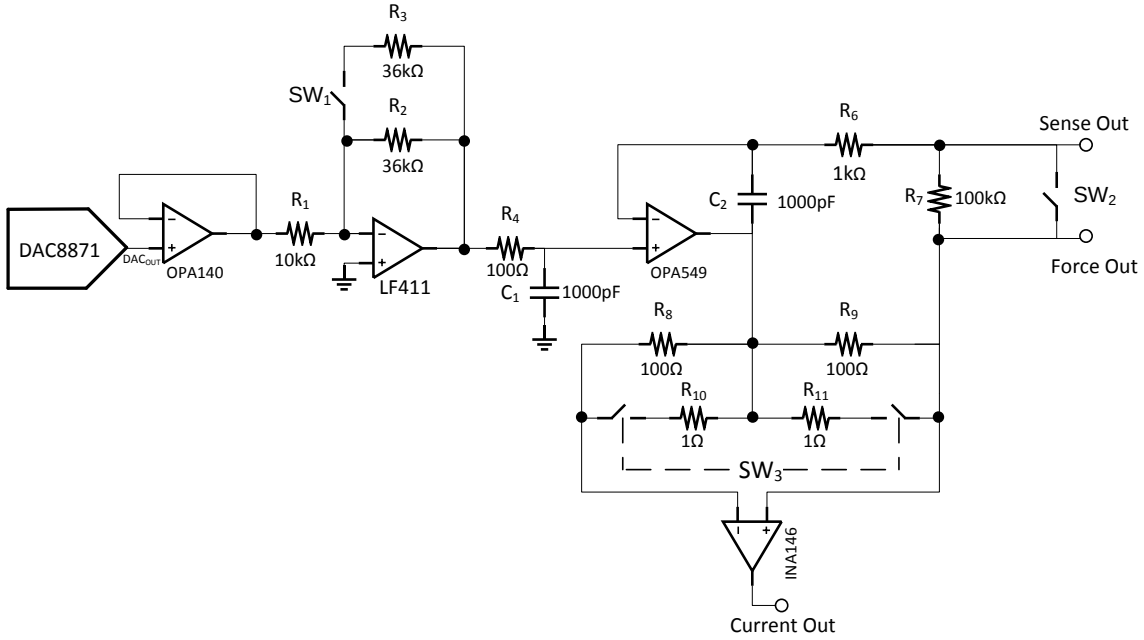

Figure 2: Simplified Schematic

2.1 DAC Reference Buffer Design

A DAC8871 (U_3) is used to provide the control voltage for the power supply. Using a SPI bus the user communicates to the DAC to program the new voltage at the DAC output. This voltage is amplified in later stages to the desired levels. The range of voltage the DAC can output is determined by the voltages at its reference pins. For example, if the V_{REFH} pin is connected to 10 V and the V_{REFL} pin was connected to 0 V the DAC would have a range of 0 to 10 V. The design contains an on board voltage reference that sets V_{REFH} to 10 V and V_{REFL} to -10 V shown in Figure 3. There is also a secondary option for the user to choose external reference voltages via the J_{13} and J_{14} jumpers.

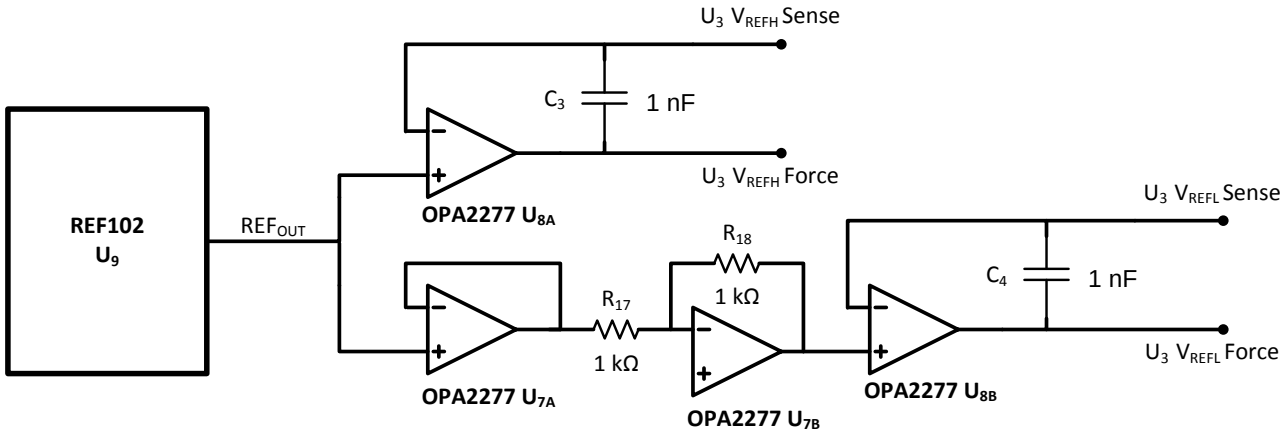

Figure 3: DAC Voltage Reference

To create the DAC references first we need a stable voltage source. The REF102 (U_9) produces a stable voltage of 10 V. All that is missing is a -10 V reference. To create the low voltage reference (V_{REFL}) the REF102 10 V output is inverted using an op amp (U_{7B}) with an inverting configuration of -1 and then buffered (U_{8B}) to prevent interaction between the DAC8871 R-2R ladder and the OPA2277 feedback network. The buffer U_{7A} between the inverting amplifier and U_9 prevents R_{17} from loading the output of U_9 and causing the voltage to drop.

2.2 DAC Output Buffer Design

The DAC8871 architecture is a R-2R back-DAC. A consequence of the back-DAC architecture is that the DAC output impedance (Z_O) is always approximately 6.25 kΩ. This is listed in the product datasheet specification table. Any load the DAC drives must take this constant large Z_O into account as it will be a large source of error in any design. By buffering the DAC output with an OPA140 (U_{10}) we significantly limit the contribution of Z_O to the overall error in the design. Without the buffer the DAC output voltage would be divided between the Z_O and R_1, preventing the DAC from reaching its full output range. The OPA140 is a JFET input op amp has a maximum 10 pA bias current at room temperature. Its contribution to the error is

$$Verror = Zo \times I_{BIAS} \times G = 6.25k\Omega \times 10pA \times 1 = 62.5nV$$

And far below the threshold of the DAC's least significant bit (LSB)

$$LSB = \frac{V_{REFH} - V_{REFL}}{2^N} = \frac{10V - (-10V)}{2^{16}} = 305\mu V$$

2.3 Buffer and Power Amplifier Design

The output of the DAC8871 needs to be amplified to achieve the desired voltage range of 0 – 36 V. The LF411A (U_2) is chosen for its high voltage power rail compliance that is necessary to achieve the 36V output with a 40 V supply. The DAC output range spans ±10 V so U_2 is configured in a gain of -3.6 V/V to meet the specification. This configuration gives a possible ±36 V of span at the output of U_2. Our initial design only calls for a 0 – 36 V span. This is compensated by losing 1-bit of precision in the DAC range, effectively rendering our DAC as a 15-bit DAC and not a 16-bit DAC. It will be seen in the Modifications section that we can recover this resolution with a minor change to the DAC voltage reference.

The LF411A inverting configuration was chosen to keep the input common mode fixed at ground (GND) and reduce the common mode error in the design. However, the negative gain means the DAC must be configured to output a negative voltage.

$$V_{OUT} = -\frac{R_{FEEDBACK}}{R_{IN}} V_{IN} \quad (1)$$

R_2 (or $R_2||R_3$ for bipolar operation) is the feedback resistor, R_1 is the input resistor, and the buffered DAC voltage from the OPA140 is V_{IN}.

The OPA549 (O_1) power amplifier is used to buffer the LF411A output to increase the output current drive to meet the design specifications of 1 A. A Kelvin connection is provided to allow for remote sensing at the load power amplifier's load. R_7 prevents the amplifier from railing when the Kelvin connection is not being utilized.

2.4 Output Current Sense Design

In conjunction with the shunt resistors (R_8 – R_{11}) the INA146 (I_1) acts as a high side current shunt monitor as shown in Figure 4. The shunt resistor converts the load current into a voltage that is amplified by the INA146. The INA146 is a two op-amp instrumentation amplifier as opposed to the more common 3 op-amp configuration. There is a 0.1 V/V resistive divider at each input and the current shunt R_9 or R_{11} is in series with the divider on the non-inverting input. In order to balance the bias current offset generated by the shunt a matching resistor R_8 or R_{10} is added in series with the inverting input. If these resistors were not present the INA would see an unbalanced resistance and the resulting bias current would cause the common mode rejection to decrease. When SW_3 is closed the shunt voltage is equal to the shunt current, otherwise it's 100 times the shunt current. The shunt voltage is amplified by the INA146 where it is scaled to match a ±1V ADC range.

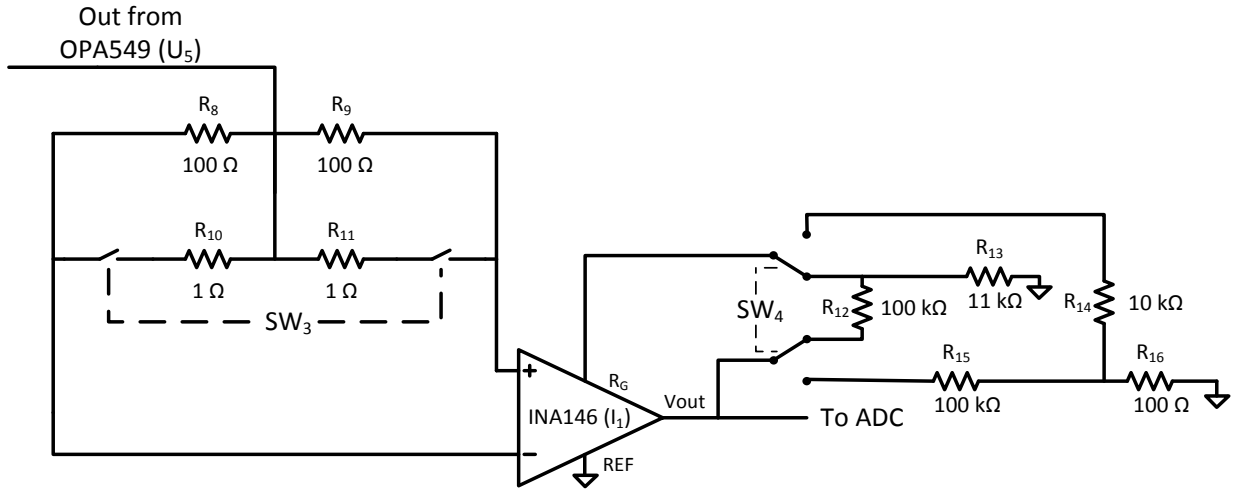

Figure 4: INA Gain Settings

When SW_4 is in the reset position (as shown in Figure 4) the gain of the INA146 is 1 V/V. In the second position it is 100 V/V. The voltage output from the INA146 is 1, 100, or 10000 times the shunt current depending on the shunt resistor used and INA gain settings. This voltage can easily be read by an ADC and used to monitor the current draw from the power supply.

Table 2: INA Gain Configurations

SW_3 Setting	SW_4 Setting	Shunt Resistor (Ω)	INA Gain (V/V)	Total Gain (V/V)
Open	Reset	100	1	100
	Set	100	100	10000
Closed	Reset	1	1	1
	Set	1	100	100

3 Component Selection

3.1 Passive Component Selection

The amplification portion of this circuit is used to gain the voltage from the DAC to the desired range. Equation 2 shows how the output voltage of the op amp relates to the input voltage.

In the power supply circuit R_1 is the input resistor and R_2 is the feedback resistor. The max VOUT for the circuit is 36 V and VIN, the voltage coming from the DAC, was chosen to be a maximum of 10 V. This information is used to calculate the ratio of the feedback resistors to the input resistor in the power supply circuit. It is shown explicitly in the following equations:

$$36V = \frac{R_2}{R_1} 10V \quad (2)$$

$$R_2 = 3.6 * R_1 \quad (3)$$

Using standard resistor values the easiest way to get these ratios is to use a 10kΩ resistor for R_1 and 36kΩ resistors for R_2.

R_4 and C_1 are used as a low pass filter to attenuate high frequency noise. Equation 3 shows the formula to find cutoff frequency:

$$f_{CUTOFF} = \frac{1}{2 * \pi * R * C} \quad (4)$$

We selected a cutoff frequency of 1.5 MHz and a resistance of 100Ω. The equation was solved for capacitance. This resulted in the following:

$$1.5MHz = \frac{1}{2 * \pi * 100\Omega * C} \quad (5)$$

$$C = 1000\,pF \quad (6)$$

R_6 was chosen as 1kΩ to be able to provide adequate protection from feedback current should the outputs ever short circuit. As an example Equation 7 shows what the device would be current limited to in the worst case scenario of a 36 V input while the output is shorted.

$$I_{IN} = \frac{V_{OUT}}{R_6} = \frac{36V}{1000\Omega} = 36mA \quad (7)$$

R_7 was chosen to be 100kΩ so that when SW_2 is closed for the Kelvin connection all the current would flow through the force/sense lines. R_7 also ensures that the OPA549 does not run open loop when the Kelvin lines are open.

Since the shunt resistors R_8 through R_{11} make a voltage proportional to the current based on their value they were selected to be either 1Ω or 100Ω for simple software calculations. Special consideration for these resistors was necessary, however, since they could potentially have 1 amp of current through them. For that reason 3 W power resistors are selected.

R_{12} through R_{16} were selected to give the INA146 a 1 V/V and 100 V/V gain configurations. Their values are specified by the INA146's datasheet (see page 8 of the INA146 datasheet).

R_{17} and R_{18} were used to create an inverting op-amp with a gain of -1. The value of 1 kΩ was a tradeoff between noise and power dissipation.

C_3 and C_4 serve provide high frequency compensation for the V_{REF} buffers to ensure stability.

3.2 DAC Selection

In order to achieve the maximum voltage of 36 V in the chosen circuit configuration, a DAC capable of producing -10 V is required. There are a number of options to achieve negative voltage outputs using back-DAC architectures. The DAC8871 is chosen because it is a native high voltage DAC capable of accepting 39.6 V between V_{REFH} and V_{REFL}. This makes DAC8871 very flexible to meet the specifications of this unipolar design to output +10 V while being adaptable for other configurations discussed in the Modifications section

Briefly mentioned in 2.3, this 16-bit DAC is only being used as a 15-bit DAC. This is because the output of the DAC8871 is gained by -3.6 V/V in the U_2 stage. The DAC8871 output requirements are only -10V to 0V but the output can span -10 V to 10 V. This means that half the DAC's code span from 0x8000 to 0xFFFF is not utilized for the unipolar design. This trade off was made in order to allow for the bipolar options discussed later.

3.3 DAC Reference Selection

A voltage reference was needed to produce a very stable value of 10 V. The only two references capable of producing such a voltage are the REF5010 and the REF102. Of the two devices REF102 was ultimately chosen because it has lower noise of 5 µVPP, a lower drift of 2.5 ppm/○C, and a better initial accuracy of ±2.5 mV.

3.4 Reference Buffer Selection

The reference buffers need to be precision amplifiers with low offset voltage and low offset drift along with low voltage noise and be stable at unity gain. The OPA2277 is an excellent choice with 12 nV/√Hz at 10 Hz, a maximum 25 µV of dc offset and a maximum offset drift of 0.25 µV/C. Even with the large heat sink required in the design the power op amp will create a change in the ambient temperature so searching for a very low offset drift coefficient is important to maintain accuracy as the output power increases.

3.5 DAC Buffer Selection

For the DAC buffer an op amp that is stable at unity gain is required. A JFET op amp is desired because they have a high output impedance and low voltage noise density. The OPA140 meets both these features as well as having low offset voltage and low bias current.

3.6 Amplifier Selection

The amplification section of the power supply requires a precision op amp capable of handling rail-to-rail voltage difference of 44 V. This component must have a low offset to meet the low offset specifications. The LF411A meets these requirements with a maximum of 500 µV offset, no more than 10 µV/C of offset drift. Also, this stage also must remain low noise because the input of the final stage sees the root sum of squares of the DAC8871, OPA140, and LF411A noise gained by -3.6 V/V. The LF411A has a typical voltage noise of 25 nV/√Hz.

3.7 Power Amplifier Selection

Since the LF411A cannot sustain an output current of 1 A, it is necessary to have a buffer amplifier capable of sourcing that current for an extended period of time. Rail-to-rail swing is also a careful consideration for this output power stage because the closer the power stage can swing to the rails the less head room the power rails must provide. Of the op amps available the OPA549 was the best fit.

The OPA549 specifications are good enough for this design: 500 µV max offset, 20 µV/C offset drift, 9V/µs slew rate, and 70 nV/√Hz noise. The OPA549 is capable of sustaining 1 A indefinitely while used in conjunction with the Thermalloy 6399B heat sink (which is recommended in the data sheet).

3.8 Instrumentation Amplifier Selection

The INA146 was chosen as the instrumentation for the power supply because it was the only instrumentation amplifier capable of working in the bi-polar case (which is discussed more in depth in the modification section).

The INA146, however, does present its own difficulties since it is composed of two op amps as opposed to the more common three op amp configuration. The inputs have an input resistor divider and higher bias current than a 3-amp INA. This meant that it would have a poor CMRR unless compensated for. This problem was overcome by having pairs of shunt resistors and arranging them in the way shown in Figure 2 (see Figure 7 on page 11 of the INA146 datasheet).

3.9 Relay Driver Selection

To make using the switches easier it was decided to use a relay driver in the power supply circuit. The relay driver needs a minimum of 6 channels. The TLP9202 (U_6) was chosen because it has 8 channels and a built in 5 V LDO for powering the relays, thus eliminating the need for another component.

3.10 Protection Diode Selection

There is also a protection diode (D_1) in the design. This diode connects between the negative power rail and the output providing low side protection to the output of the design should there be a short below the power rail. A fast switching BAS116 diode is used to clamp to the negative rail.

4 Simulation

Figure 5 shows the TINA-TI™ schematic used to simulate the circuit.

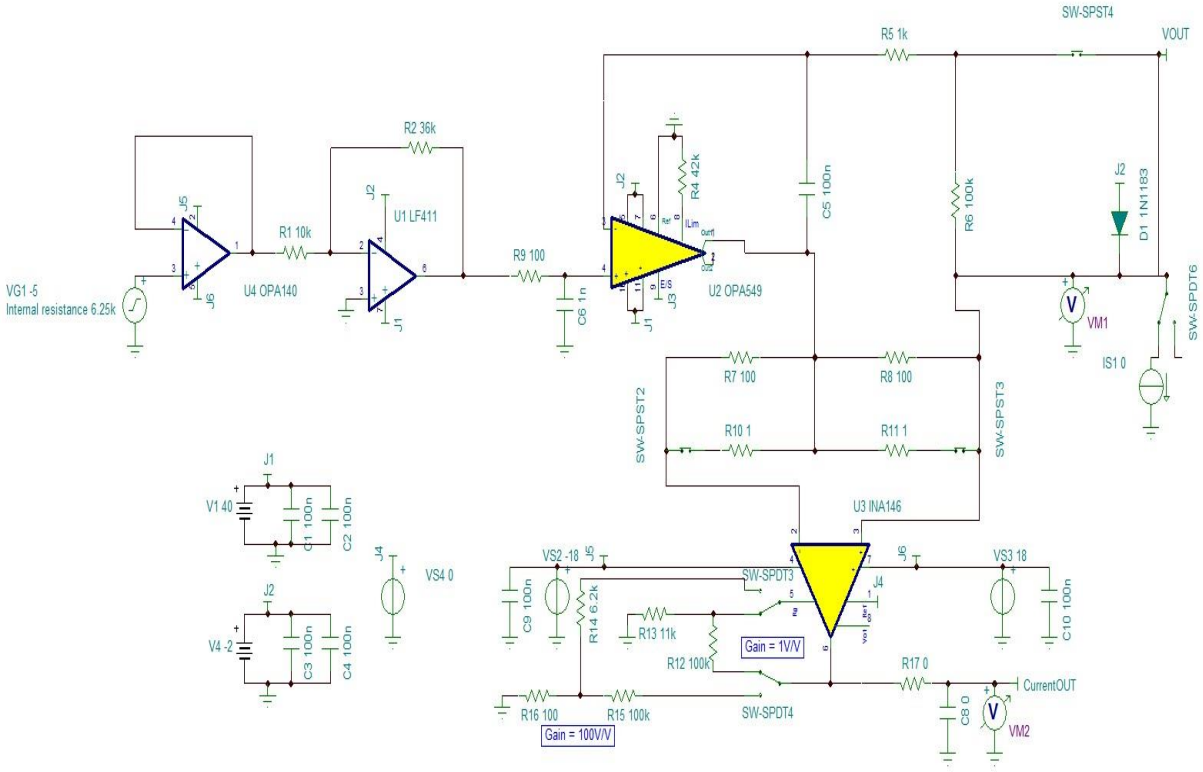

Figure 5: TINA-TI™ Schematic

Since TINA-TI™ does not have a model for the DAC8871, the circuit only consists of the portion of the power supply after the DAC buffer. In the simulation VS1 is used to represent the DAC8871 output voltage. The equivalent output impedance is added to the source for better simulation accuracy.

4.1 Transfer Function

The result of the transfer function is shown in Figure 6.

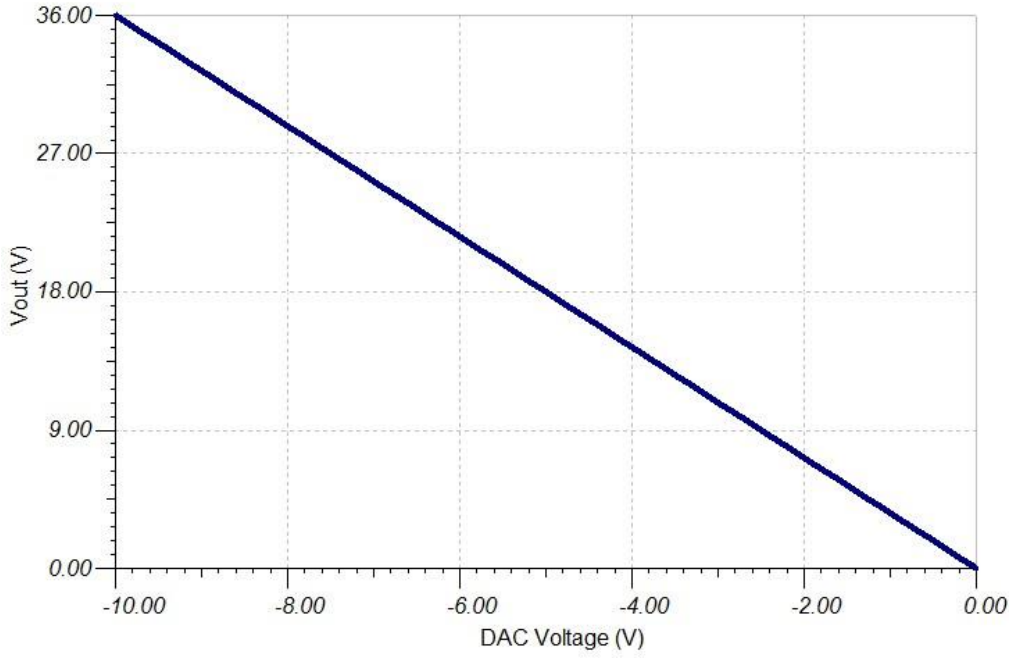

Figure 6: Transfer Function

4.2 V_{OUT} Gain Error

To calculate gain error, measurements were taken at the voltage output of the power supply while there was no current load. This data was then exported into a spreadsheet and the gain error was calculated using Equation 8.

$$\%FSR = \frac{\left(V_{OUT(MAX)} - V_{OUT(MIN)}\right) - G_{IDEAL} * \left(V_{IN(MAX)} - V_{IN(MIN)}\right)}{G_{IDEAL} * \left(V_{IN(MAX)} - V_{IN(MIN)}\right)} * 100\,\% \quad (8)$$

The gain error was calculated for each shunt resistor and INA gain setting and results can be seen in Table 3: Simulated VOUT Gain Error.

Table 3: Simulated VOUT Gain Error

INA Gain (V/V)	Shunt Resistor (Ω)	Gain Error (%FSR)
1 or 100	1 or 100	-0.006716

4.3 V_{OUT} Offset

The offset of the power supply output is simply the simulated output when the input voltage was 0 V. It was measured for each shunt resistor and INA gain settings and the results can be seen in Table 4: Simulated VOUT Offset.

Table 4: Simulated VOUT Offset

INA Gain (V/V)	Shunt Resistor (Ω)	V_{OUT} Offset (mV)
1 or 100	1 or 100	4.2205615

4.4 V_{OUT} Load Regulation

For calculating the load regulation, the input voltage was made constant so that the output would ideally be 18 V. Then the current load on the power supply was swept from -1 A to 1 A, -10 mA to 10 mA, or -100 µA to 100 µA depending on the shunt resistor and INA gain settings. Figure 7 through Figure 10 are graphical representations of the simulated data.

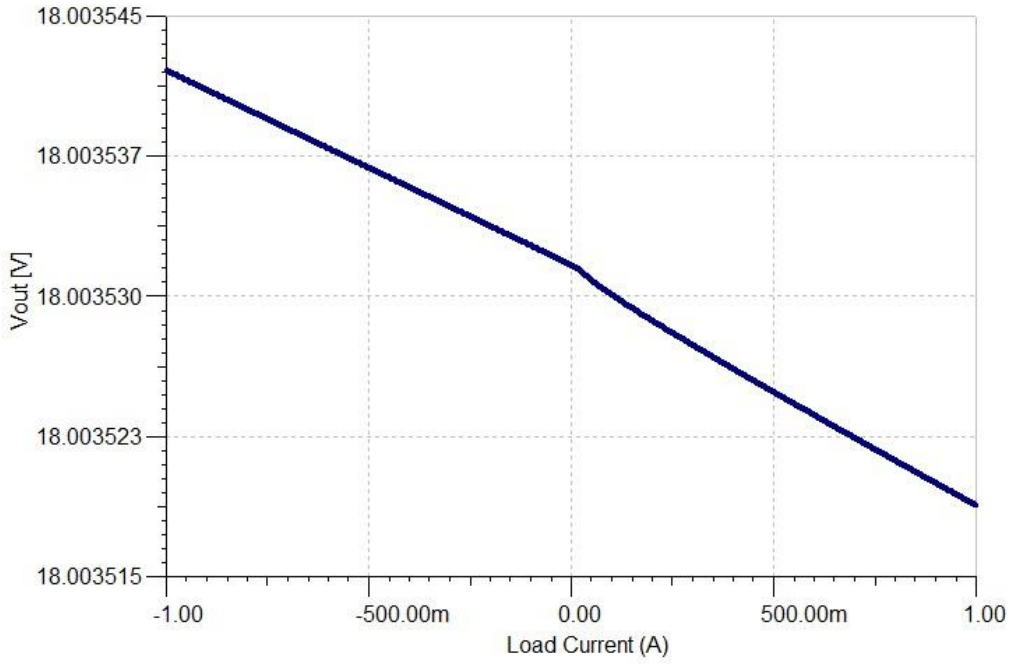

Figure 7: Load Regulation 1 V/V, 1 Ω

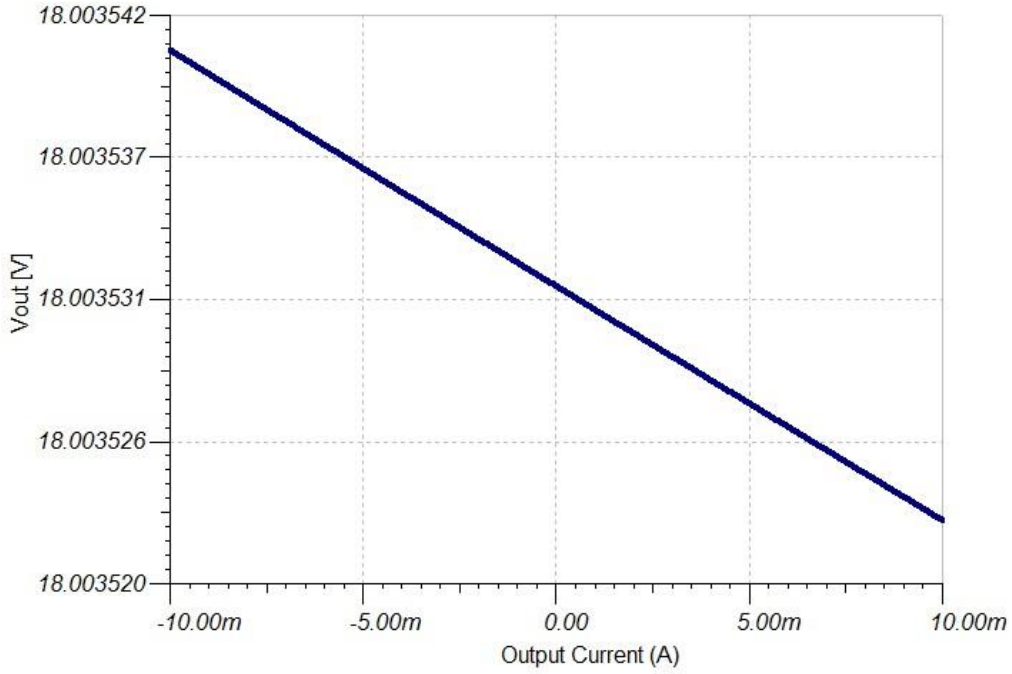

Figure 8: Load Regulation 1 V/V, 100 Ω

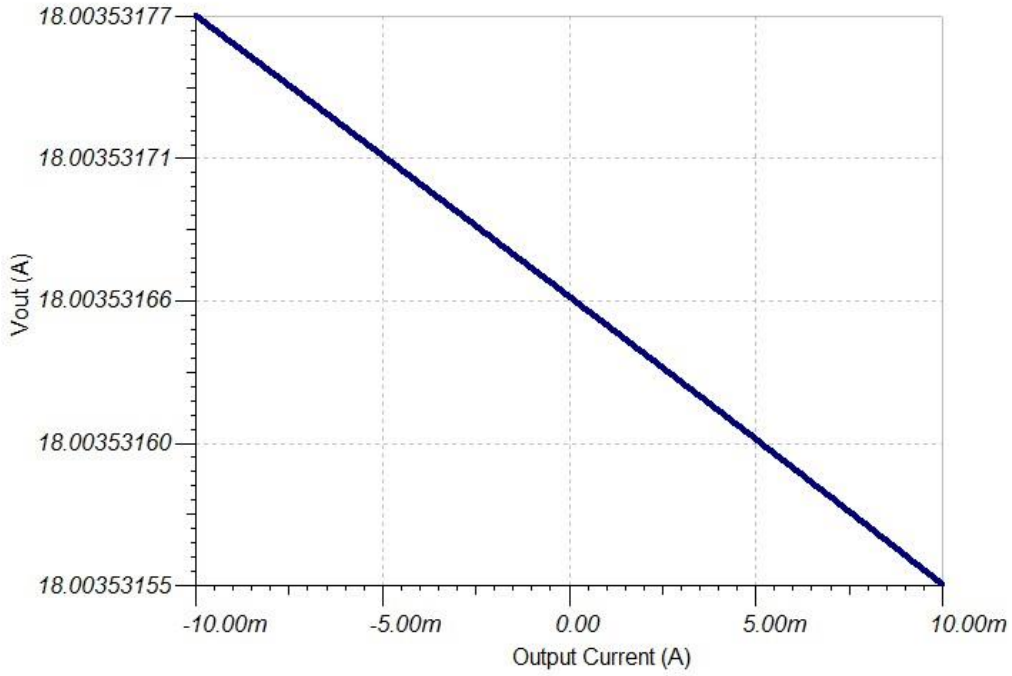

Figure 9: Load Regulation 100 V/V, 1 Ω

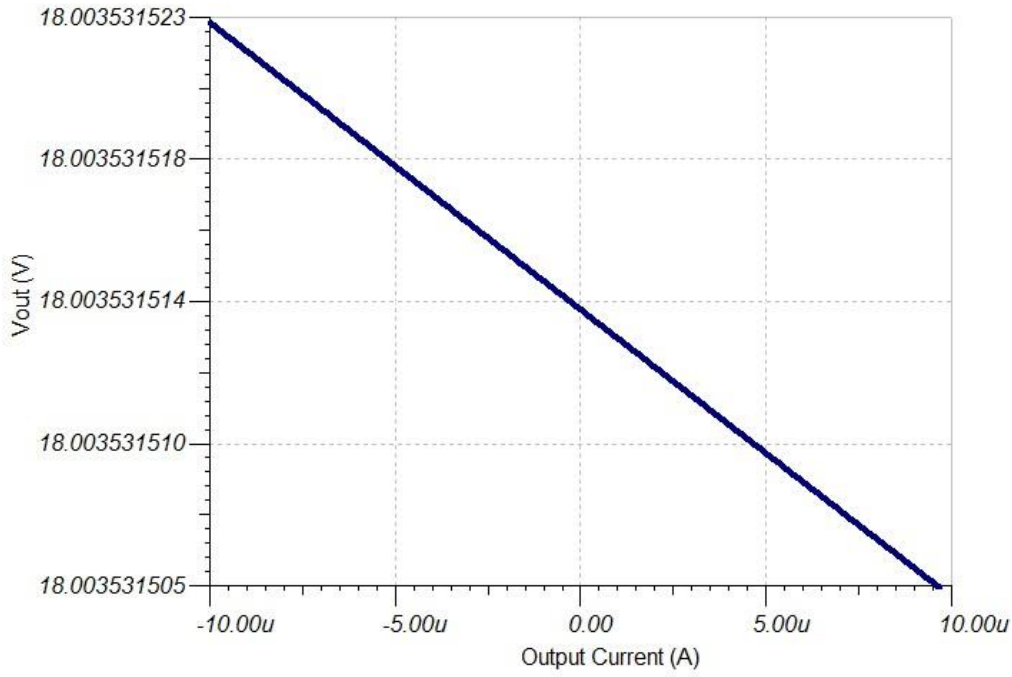

Figure 10: Load Regulation 100 V/V, 100 Ω

After simulations, the load regulation was calculated using Equation 9.

$$\text{Load Regulation } (\mu V / A) = \frac{V_{OUT(MAX)} - V_{OUT(MIN)}}{Current_{MAX} - Current_{MIN}} * 10^6 \quad (9)$$

The results of the calculation are listed in Table 5.

Table 5: Simulated Load Regulation

INA Gain (V/V)	Shunt Resistor (Ω)	V_{OUT} Load Regulation (µV/A)
1	1	-0.016680
	100	-1.088813
100	1	-0.013118
	100	-1.088727

4.5 INA Gain Error

For calculating this gain error simulations were taken at the current output of the power supply while there was no voltage output and the current was swept. Figure 11 through **Load Regulation 100 V/V, 100** Figure 13 are graphical representations of the data.

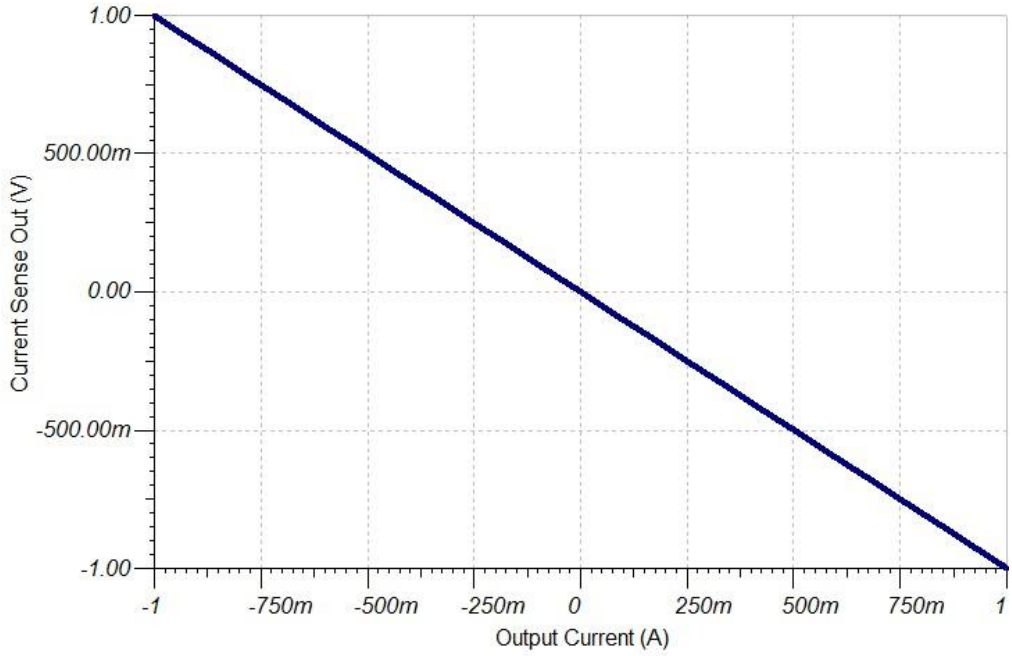

Figure 11: INA Output 1 V/V, 1 Ω

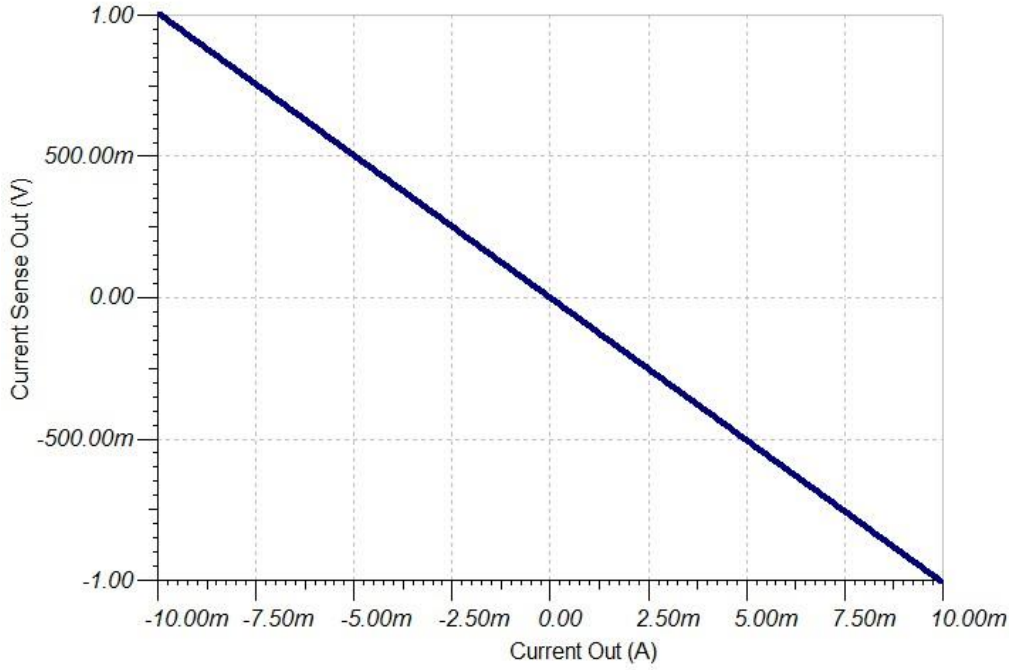

Figure 12: INA Output 1 V/V, 100 Ω

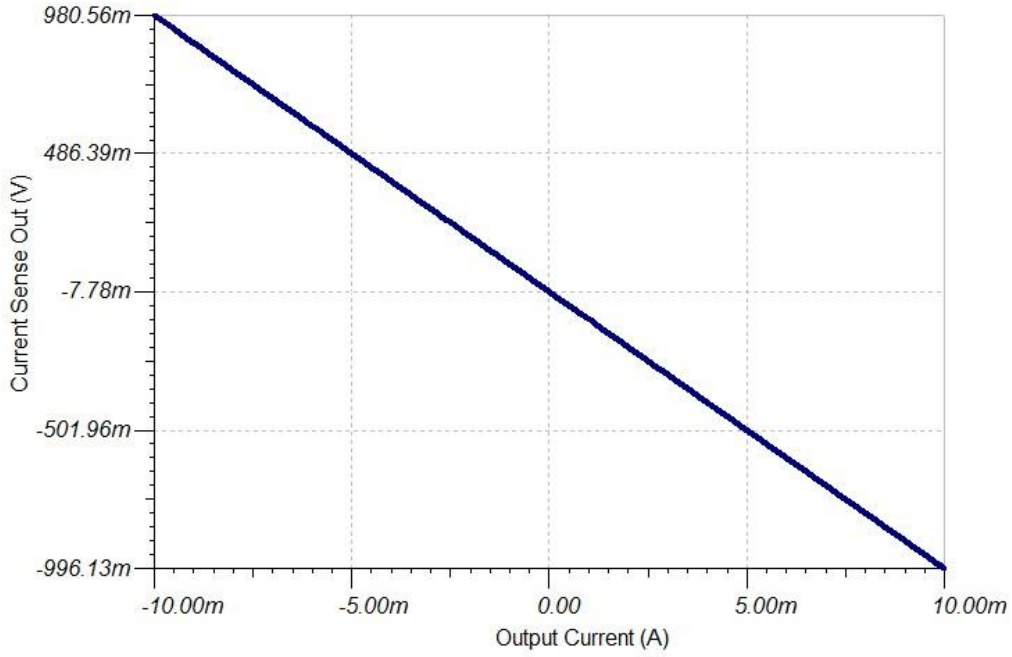

Figure 13: INA Output 100 V/V, 1 Ω

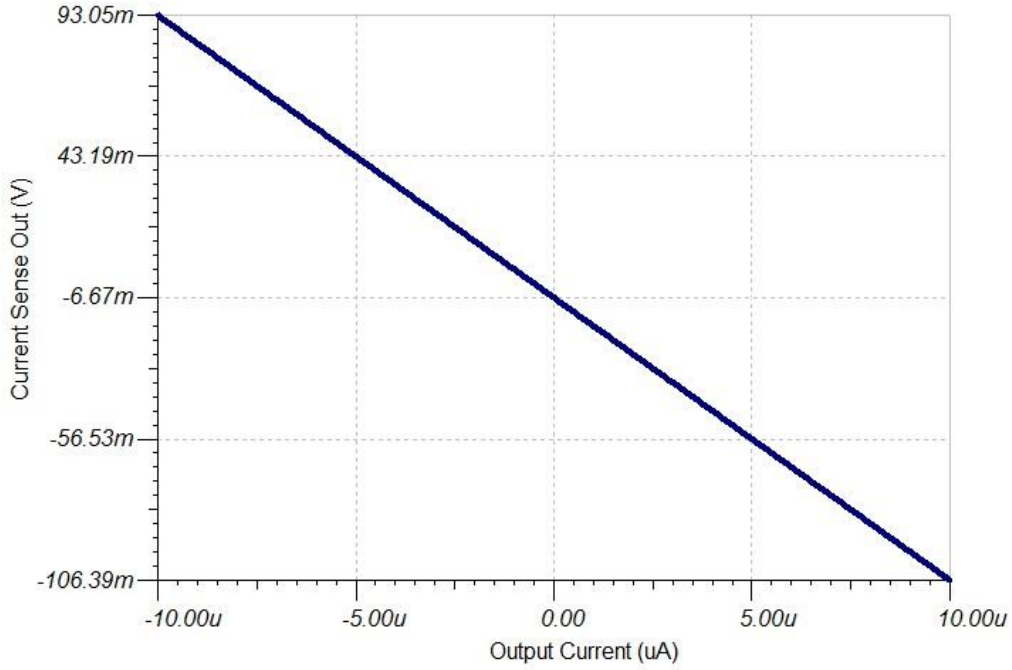

Figure 14: INA Output 100 V/V, 100 Ω

From the simulated data the gain error was then calculated with Equation 8, substituting V_{OUT} with Current Out and V_{IN} with Current Load. The results of the calculation are listed in Table 6.

Table 6: INA Gain Error

INA Gain (V/V)	Shunt Resistor (Ω)	INA Gain Error (%FSR)
1	1	-1.998930
	100	-2.007920
100	1	-1.988344
	100	-1.997240

4.6 INA CMRR

The simulations for the common-mode rejection ratio (CMRR) of the INA146 were taken at the current output while sweeping the power supply output from 0 V to 36 V with a current draw of zero amps. Figure 15 through Figure 18 represent a graphical representation of the data.

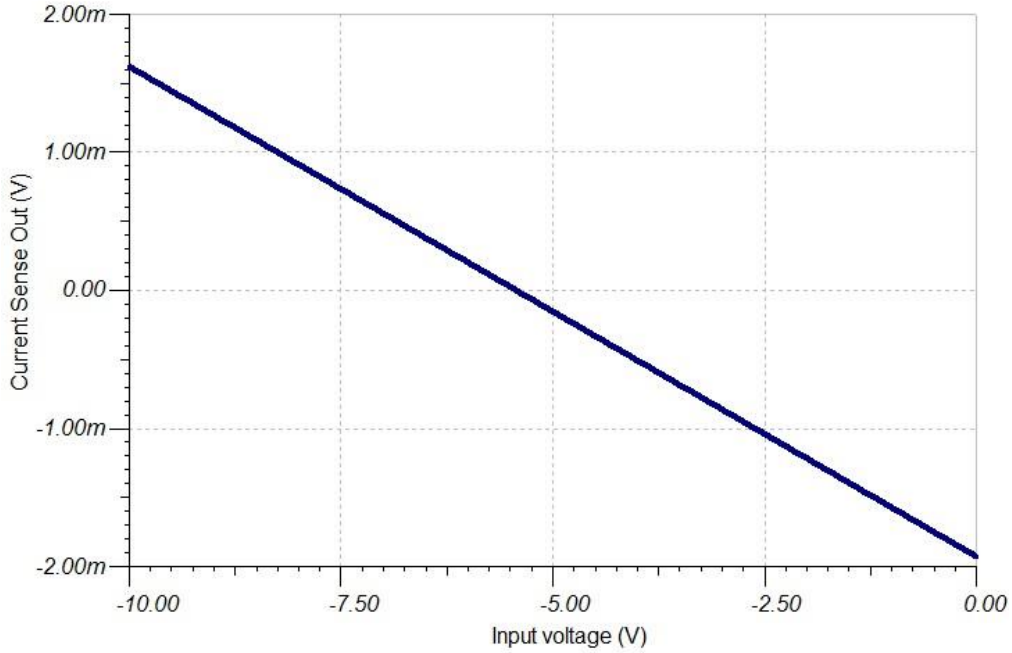

Figure 15: INA CMRR 1 V/V, 1 Ω

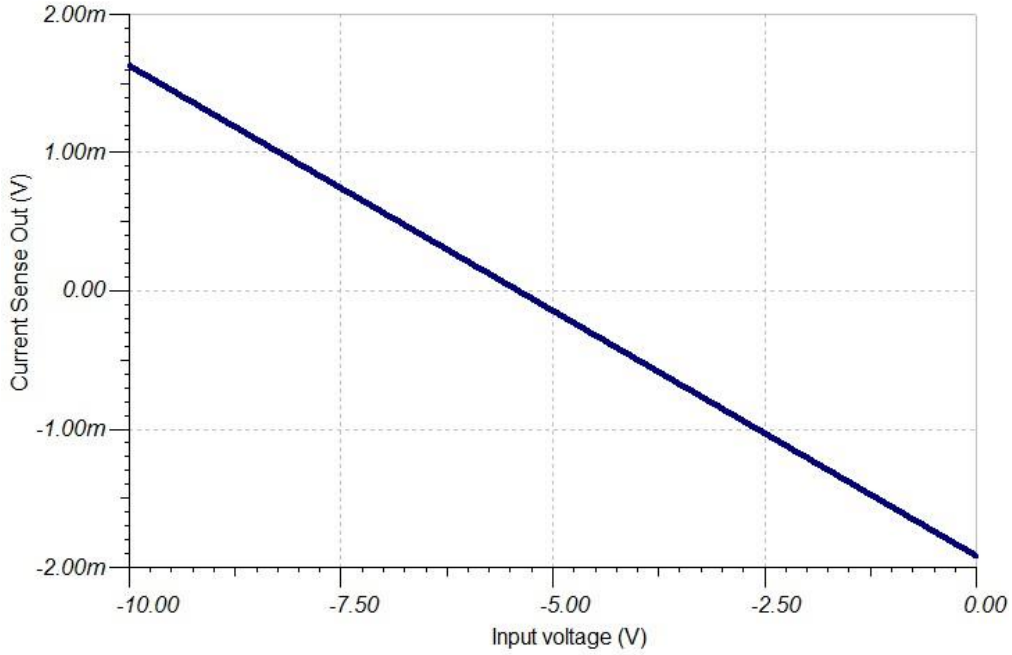

Figure 16: INA CMRR 1 V/V, 100 Ω

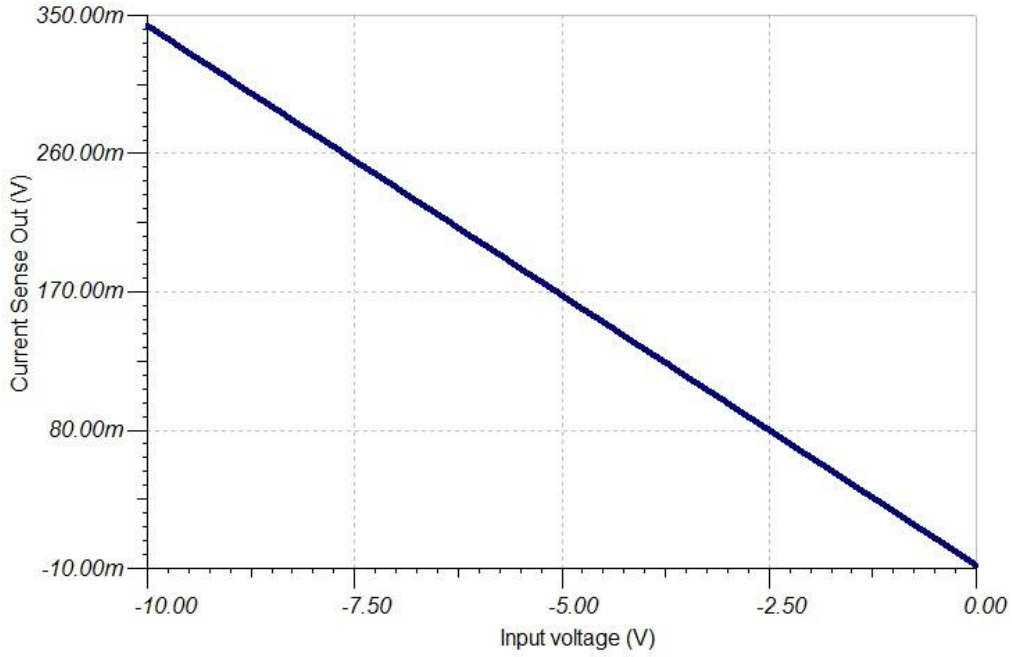

Figure 17: INA CMRR 100 V/V, 1 Ω

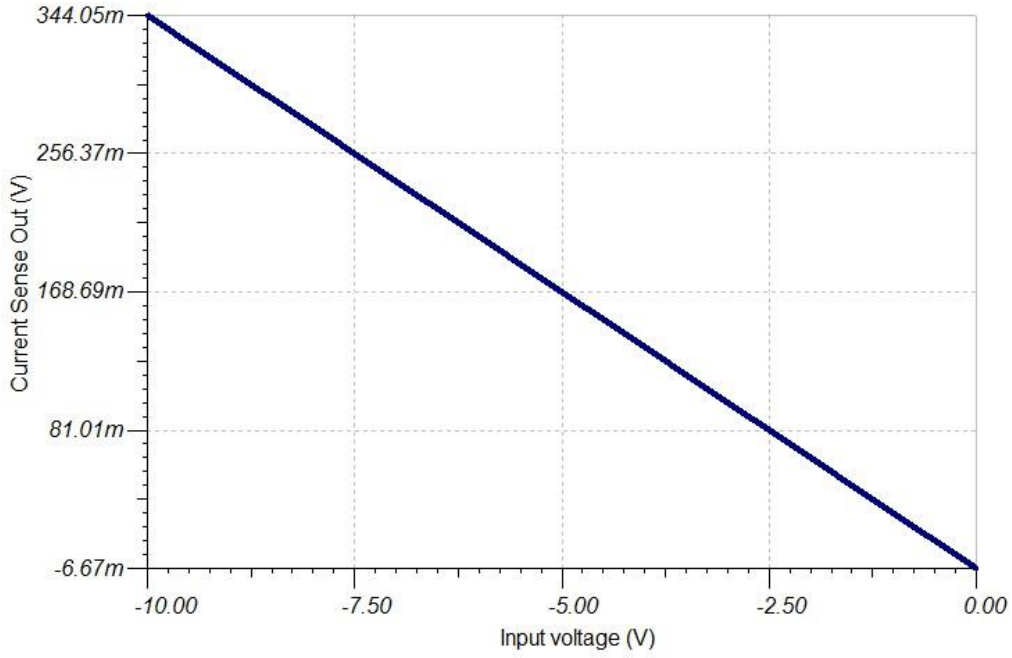

Figure 18: INA CMRR 100 V/V, 100 Ω

Because the CMRR used is input referred, two equations were necessary. Equation 10 was used to calculate the CMRR while the INA was in the 1 V/V setting and Equation 11 was used to calculate the CMRR when the INA was in the 100 V/V setting.

$$CMRR = -20 * \log_{10}\left(\frac{Current_{OUT(MAX)} - Current_{OUT(MIN)}}{V_{OUT(MAX)} - V_{OUT(MIN)}}\right) \quad (10)$$

$$CMRR = -20 * \frac{\log_{10}\left(\frac{Current_{OUT(MAX)} - Current_{OUT(MIN)}}{V_{OUT(MAX)} - V_{OUT(MIN)}}\right)}{100} \quad (11)$$

The results of the calculations are listed in Table 7.

Table 7: INA CMRR

INA Gain (V/V)	Shunt Resistor (Ω)	INA CMRR (dB)
1	1	68.999155
	100	69.008537
100	1	69.091690
	100	69.101018

4.7 Bandwidth

The bandwidth of the circuit was simulated by running an AC frequency sweep at the input of the OPA140. Figure 19 shows the bode plot of the AC sweep. The -3 dB point is at 728 kHz.

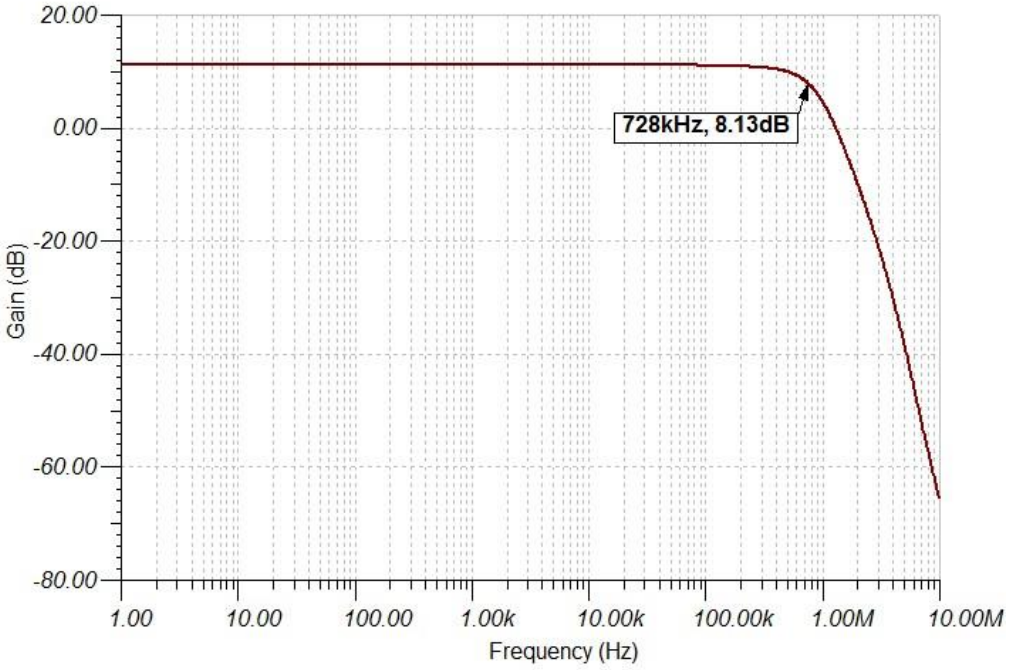

Figure 19: Simulated Bode Plot

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix.

5.1 PCB Layout

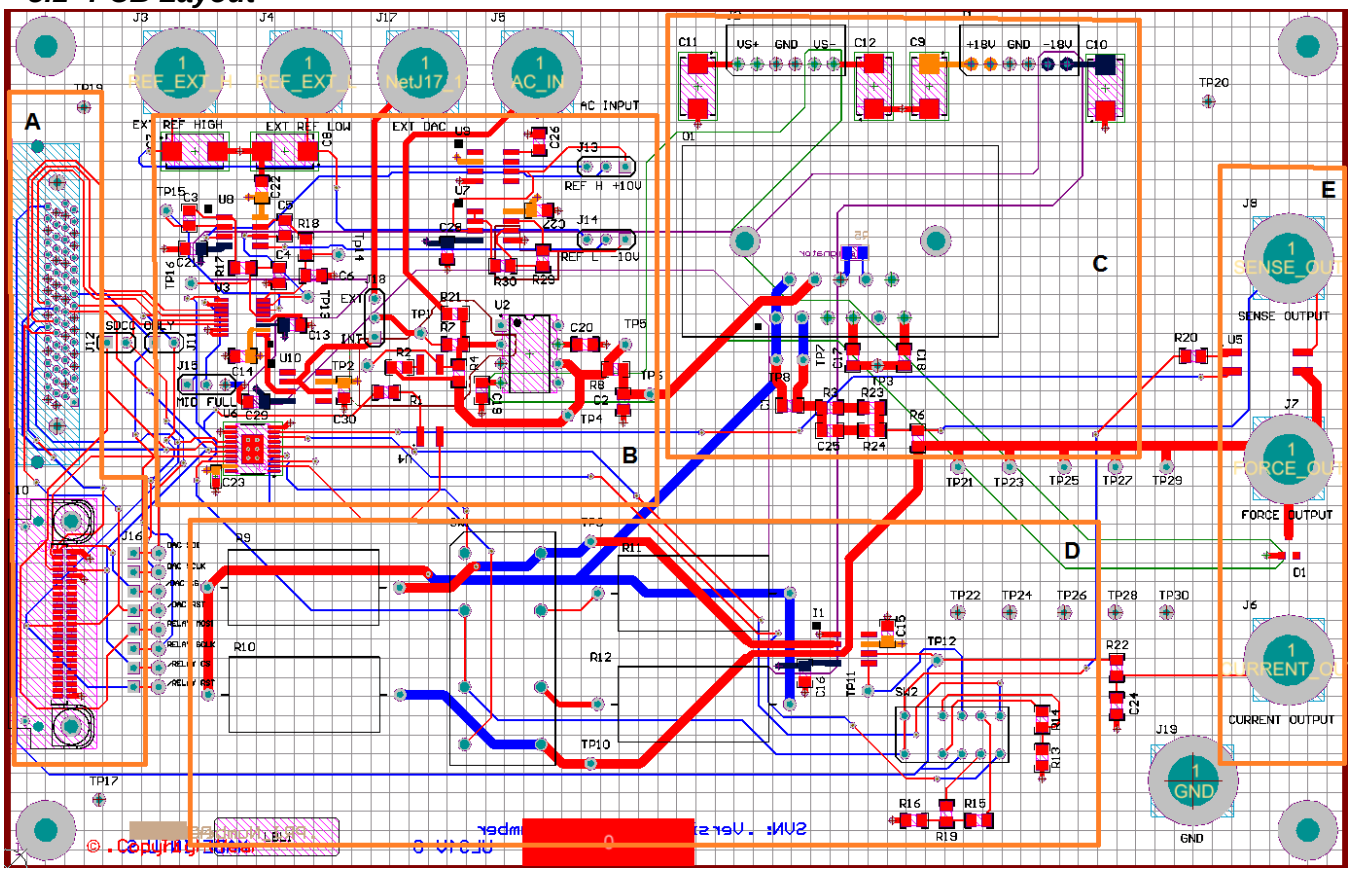

Figure 20: PCB Layout

The board is a six layer board made up of the top and bottom layer, two ground planes, and two power planes. The power planes are split planes with both a positive and negative voltage on them.

The Force Out traces are 50 mils wide because they have to potential to have 1 amp of current flowing through them. In order for the kelvin connection to be active U5 must be closed.

The layout of the circuit is as follows:

- Region A features a PXI connector, a serial data capture card (SDCC) connector (ERF8-025-01-L-D-RA-L-TR in the bill of materials), and a set of 100 mil spaced headers for connecting to the board if the user doesn't have the male version of the PXI or SDCC connector.
- Region B of the board contains the DAC and its references, the LF411A, and the relay driver.
- Region C has big block within it for the OPA549 and its heat sink. Above it are the power supply inputs for the circuit.
- Region D is the current shunt monitor and the relays to change its gain.
- Region E has the outputs of the circuit.

6 Verification & Measured Performance

The measured data was collected and the results were calculated using the same methods as the simulation section.

6.1 Transfer Function

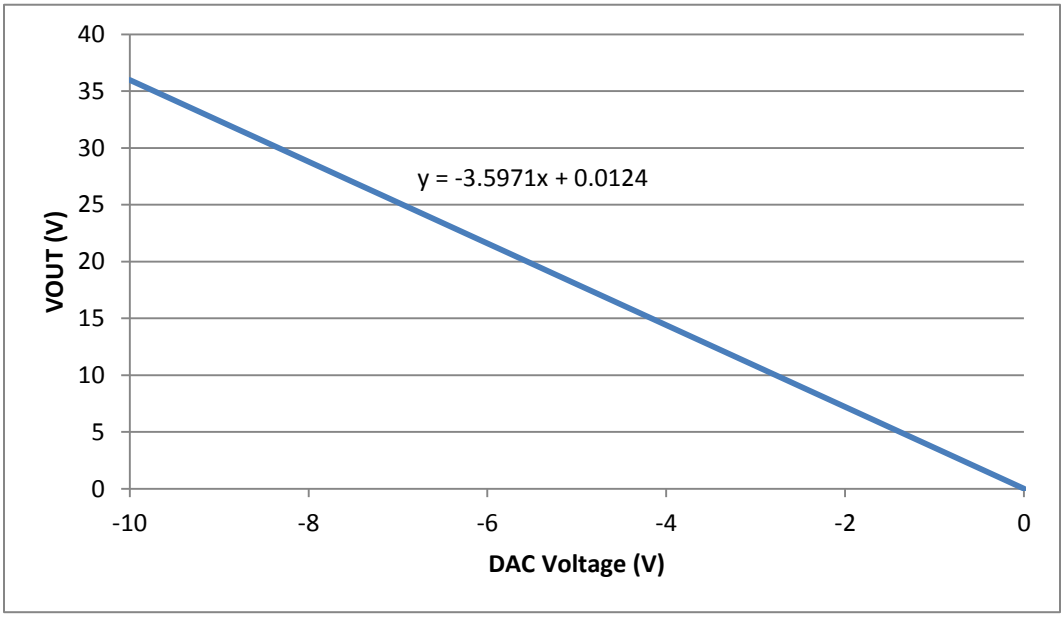

Figure 21: Measured Transfer Function

6.2 V_{OUT} Gain Error

Equation 8 shows the gain error calculation.

Table 8: Measured VOUT Gain Error

INA Gain (V/V)	Shunt Resistor (Ω)	V_{OUT} Gain Error (%FSR)
1 or 100	1 or 100	-0.07962175

6.3 V_{OUT} Offset

Table 9: Measured VOUT Offset

INA Gain (V/V)	Shunt Resistor (Ω)	V_{OUT} Offset (mV)
1 or 100	1 or 100	8.2301825

6.4 V_{OUT} Load Regulation

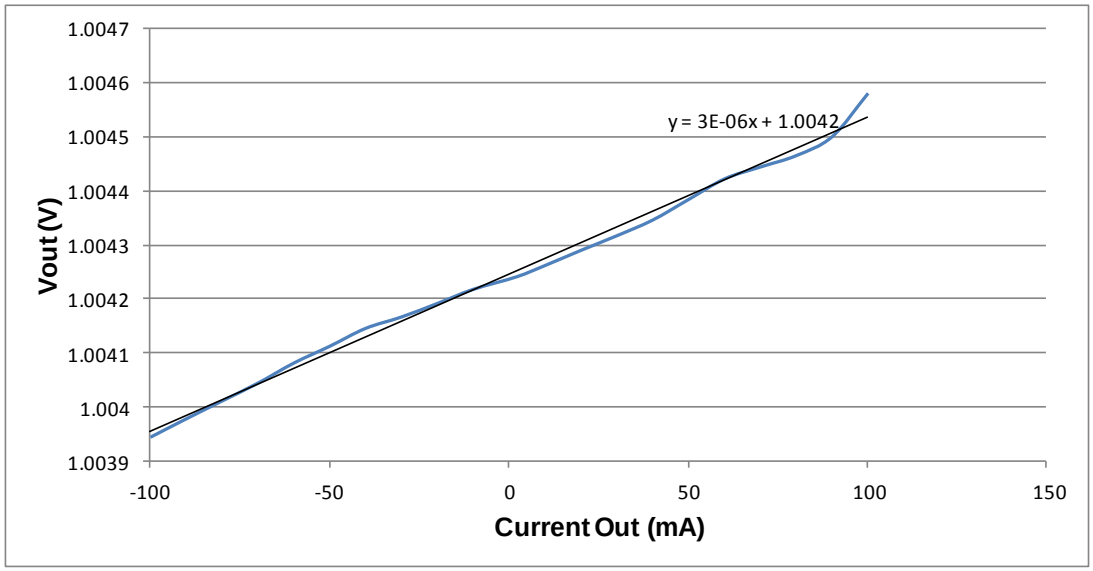

Figure 22: Load Regulation 1 V/V, 1 Ω

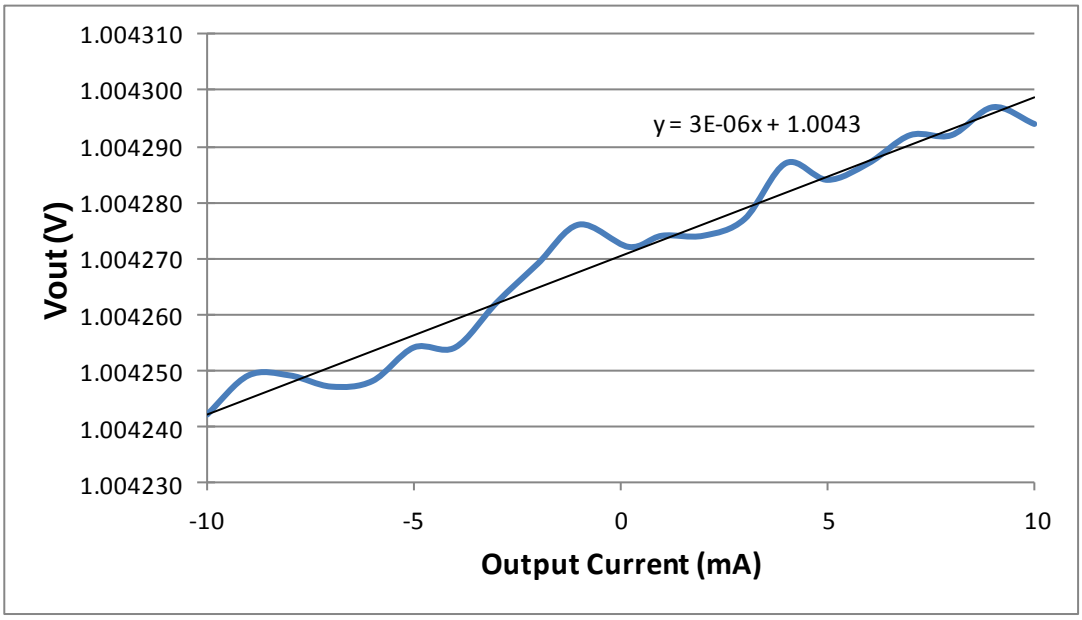

Figure 23: Load Regulation 1 V/V, 100 Ω

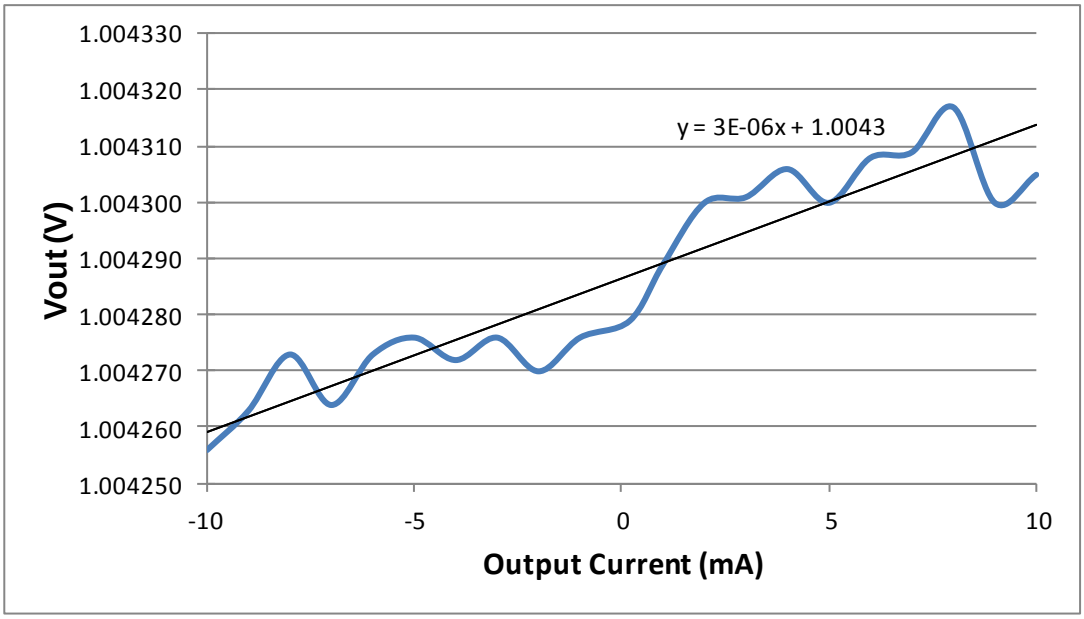

Figure 24: Load Regulation 100 V/V, 1 Ω

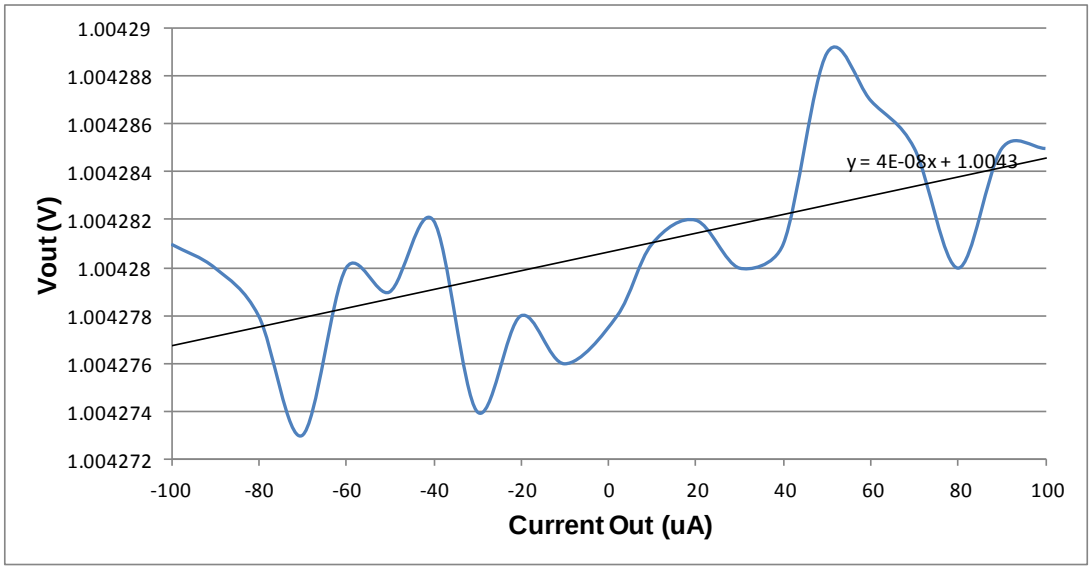

Figure 25: Load Regulation 100 V/V, 100 Ω

Equation 9 shows how the load regulation was calculated. The ability of the HP3458 meter to resolve the changes between each current decreased as the current range is decreased. The calculation for the ±100 µA range is omitted because the HP3458 could not resolve the correct value due to the noise of the system even with 100 power line cycles (PLC) of averaging.

Table 10: Measured VOUT Load Regulation

INA Gain (V/V)	Shunt Resistor (Ω)	V_{OUT} Load Regulation (µV/A)
1	1	2.92
	100	2.61
100	1	2.45
	100	N/A

6.5 INA Gain Error

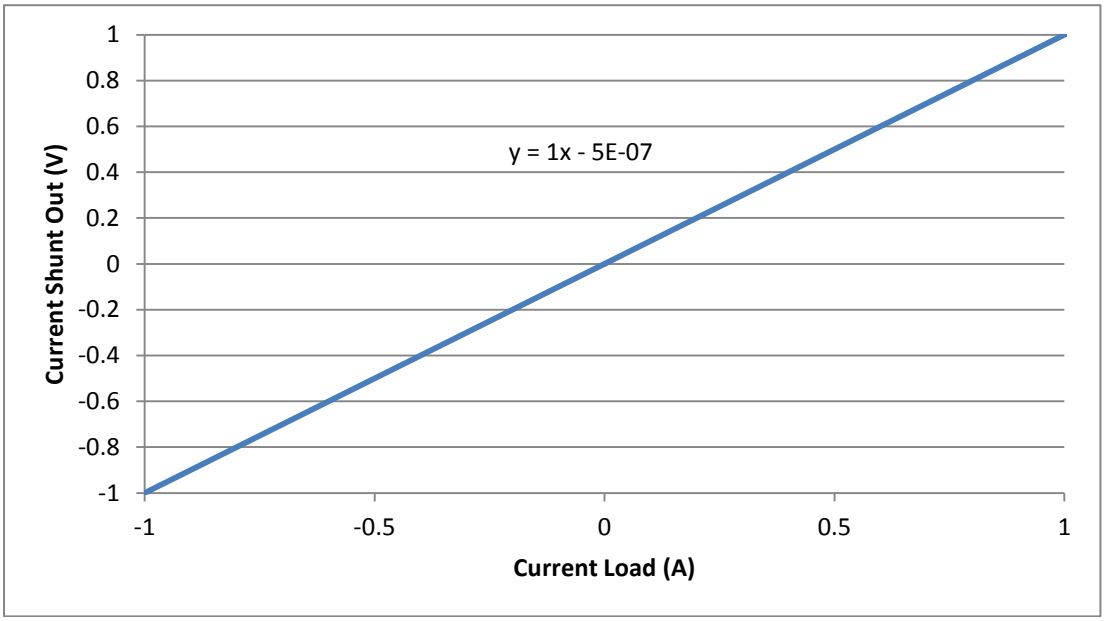

Figure 26: INA Output 1 V/V, 1 Ω

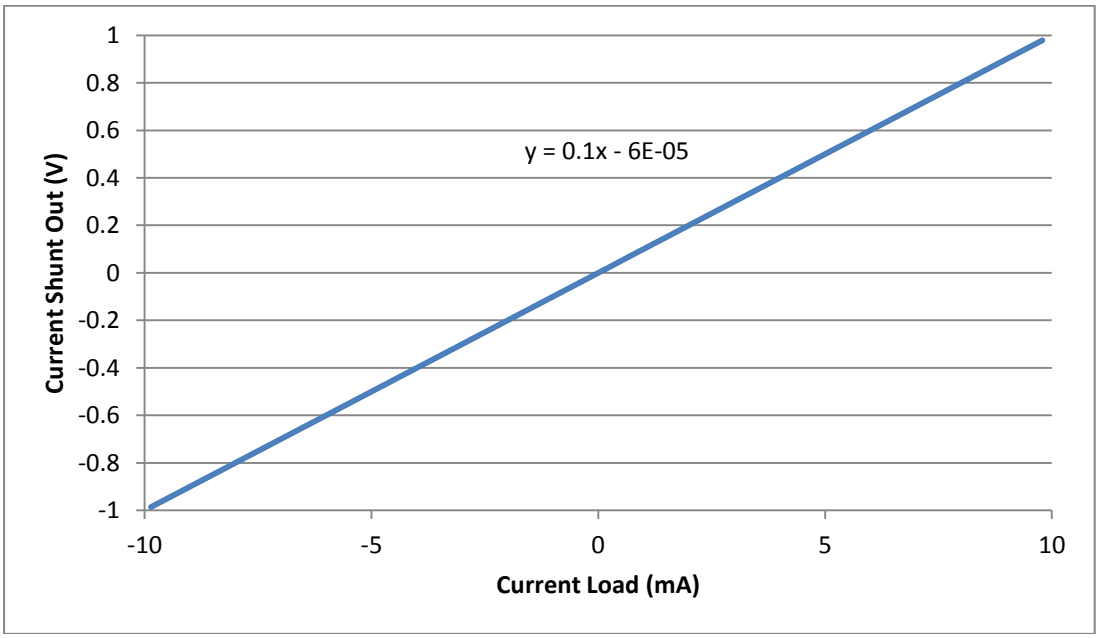

Figure 27: INA Output 1 V/V, 100 Ω

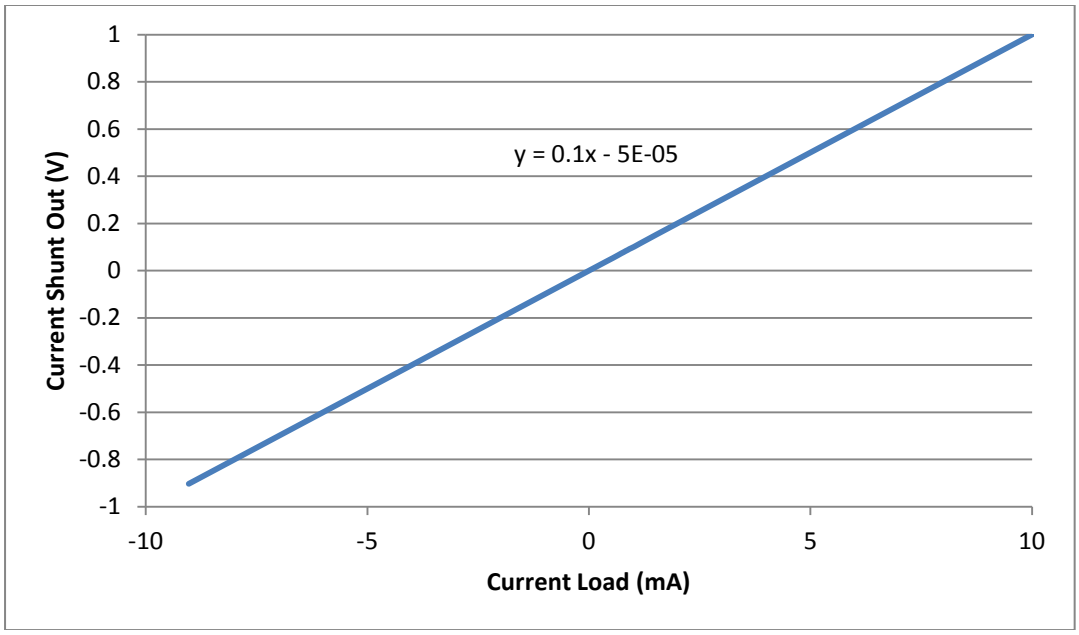

Figure 28: INA Output 100 V/V, 1 Ω

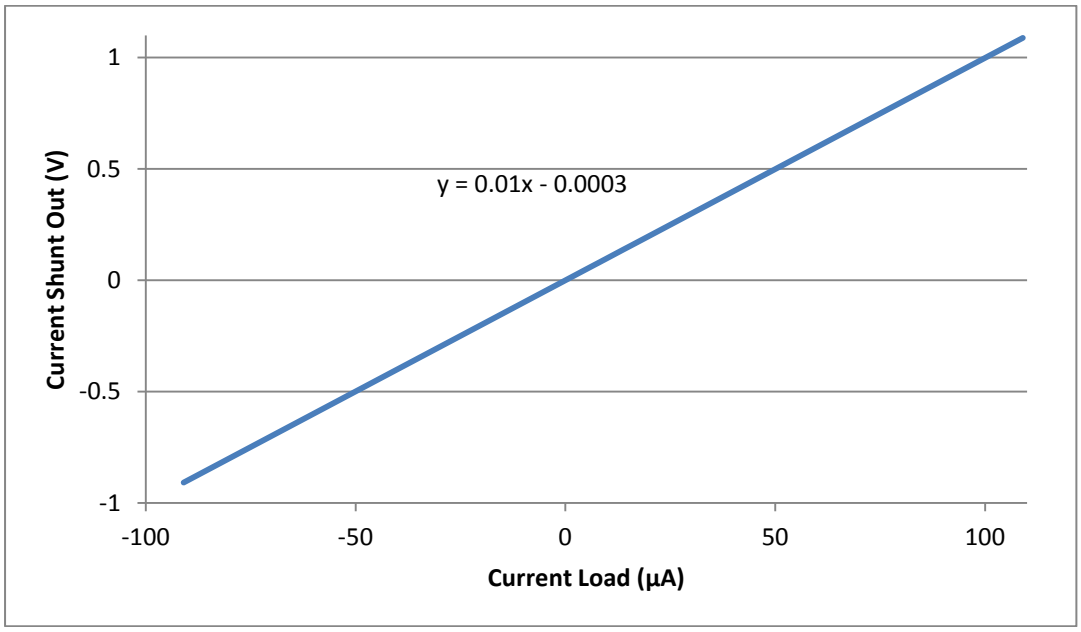

Figure 29: INA Output 100 V/V, 100 Ω

See Equation 8 to see how the gain error was calculated.

Table 11: Measured INA Gain Error

INA Gain (V/V)	Shunt Resistor (Ω)	INA Gain Error (%FSR)
1	1	1.001730
	100	-0.030363
100	1	1.003658
	100	-0.141955

6.6 INA CMRR

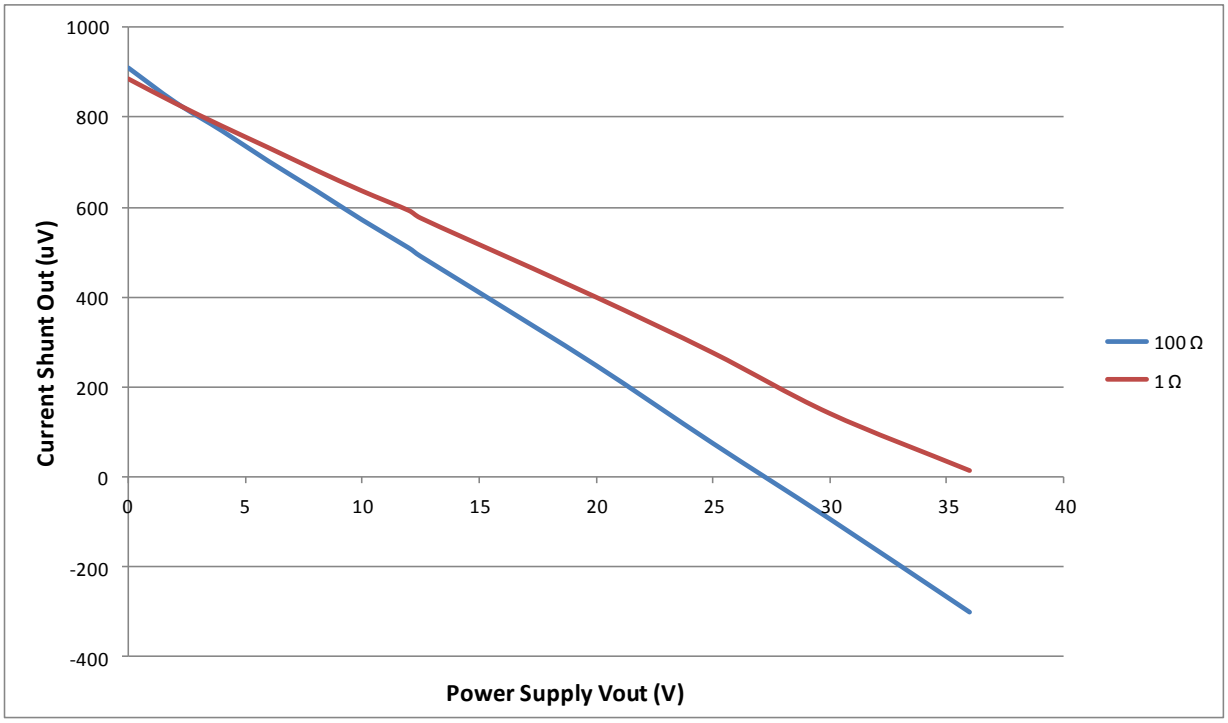

Figure 30: INA CMRR 1 V/V

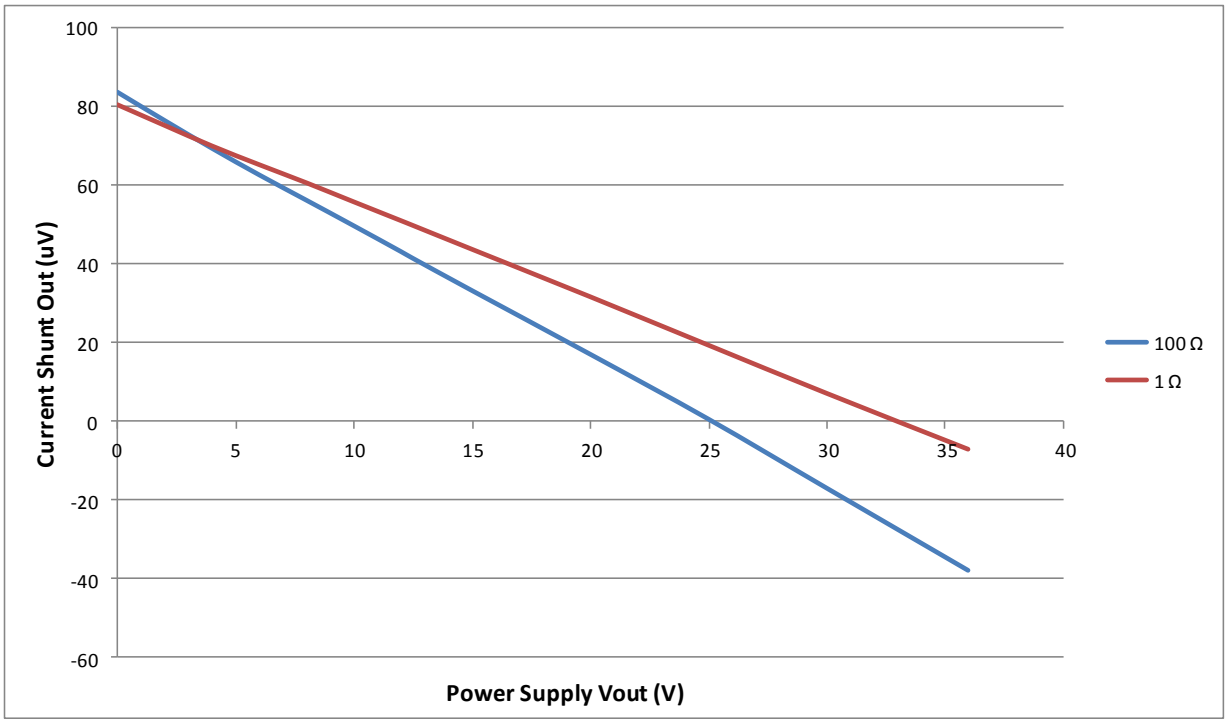

Figure 31: INA CMRR 100 V/V

See Equations 10 and 11 to see how the CMRR was calculated.

Table 12: Measured INA CMRR

INA Gain	Shunt Resistor	INA CMRR (dB)
1 V/V	1 Ω	92.278229
	100 Ω	89.456711
100 V/V	1 Ω	92.317234
	100 Ω	89.538604

6.7 Bandwidth

Figure 16 shows the measured bode plot of the circuit. The 3 dB point is at 500 kHz.

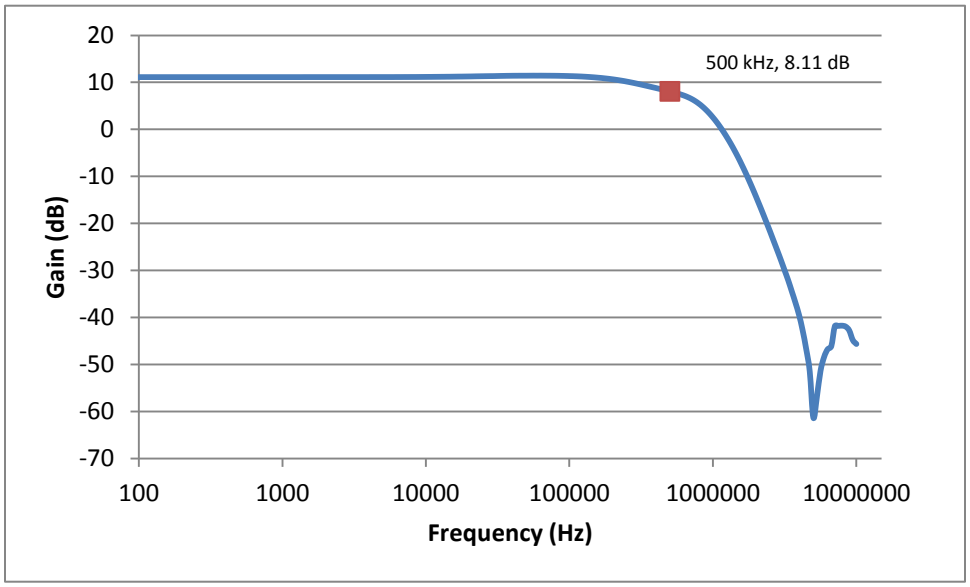

Figure 32: Bode Plot

7 Modifications

There are a number of modifications that can be applied to this circuit depending on the requirements of the user.

If the user requires a bipolar output, switching SW_1 to the closed position will change the gain of the LF411A from -3.6 V/V to -1.8 V/V. The DAC8871 is already set-up to span ±10 V because V_{REFH} is 10 V and V_{REFL} is -10 V. By changing the gain to -1.8 V/V the design will now have an output range of ±18 V with the same current load available.

The INA output can be modified to interface with an analog to digital converter (ADC) that has a 5 V unipolar supply. To make this change, connect I_1, pin 1 to 2.5 V instead of 0 V. This will bias the output of I_1 around 2.5 V while maintaining a voltage swing of ±1 V.

If the ±1 V swing is too small for the dynamic range of the user's ADC then changing the resistors to 5Ω and 500Ω pairs, the gain of the current shunt monitor would be increased from 1 or 100 V/V to 5 or 500 V/V. This would result in an INA output range of -5 V to 5 V. Similar changes can be made to match the input span of any ADC.

Another option to customize the output voltage would be to modify the V_{REFH} and V_{REFL} voltages. Remember, the DAC8871 will span any voltage applied to these pins up to a maximum difference of 39.6 V. Using a REF5050 to generate a 5 V reference instead of the REF102's 10 V would result in a ±5 V difference between V_{REFH} and V_{REFL}. This would result in a unipolar operation of 18 V and a bipolar operation of ±9 V.

8 About the Author

Adam Rozenberg is an undergraduate electrical engineering student at the University of Florida. He will be graduating with a BSEE in December 2013. Prior to interning with the High Performance Analog group in Texas Instruments he participated in medical and communications research.

Daniel Kimmitt is the Validation Manager in the Precision Digital to Analog Converters group. Prior to his current position he was a test engineer in the Linear Products group focusing on signal conditioning and temperature sensors. He joined TI in 2006 after receiving MSECE from the University of Florida in Gainesville, FL.

Bill Eisenhower is Test and Characterization Engineer in the Precision Digital to Analog Converters group. He joined TI in 2009 after completing his MSECE at the University of Illinois at Urbana-Champaign.

Appendix A.

A.1 Electrical Schematic

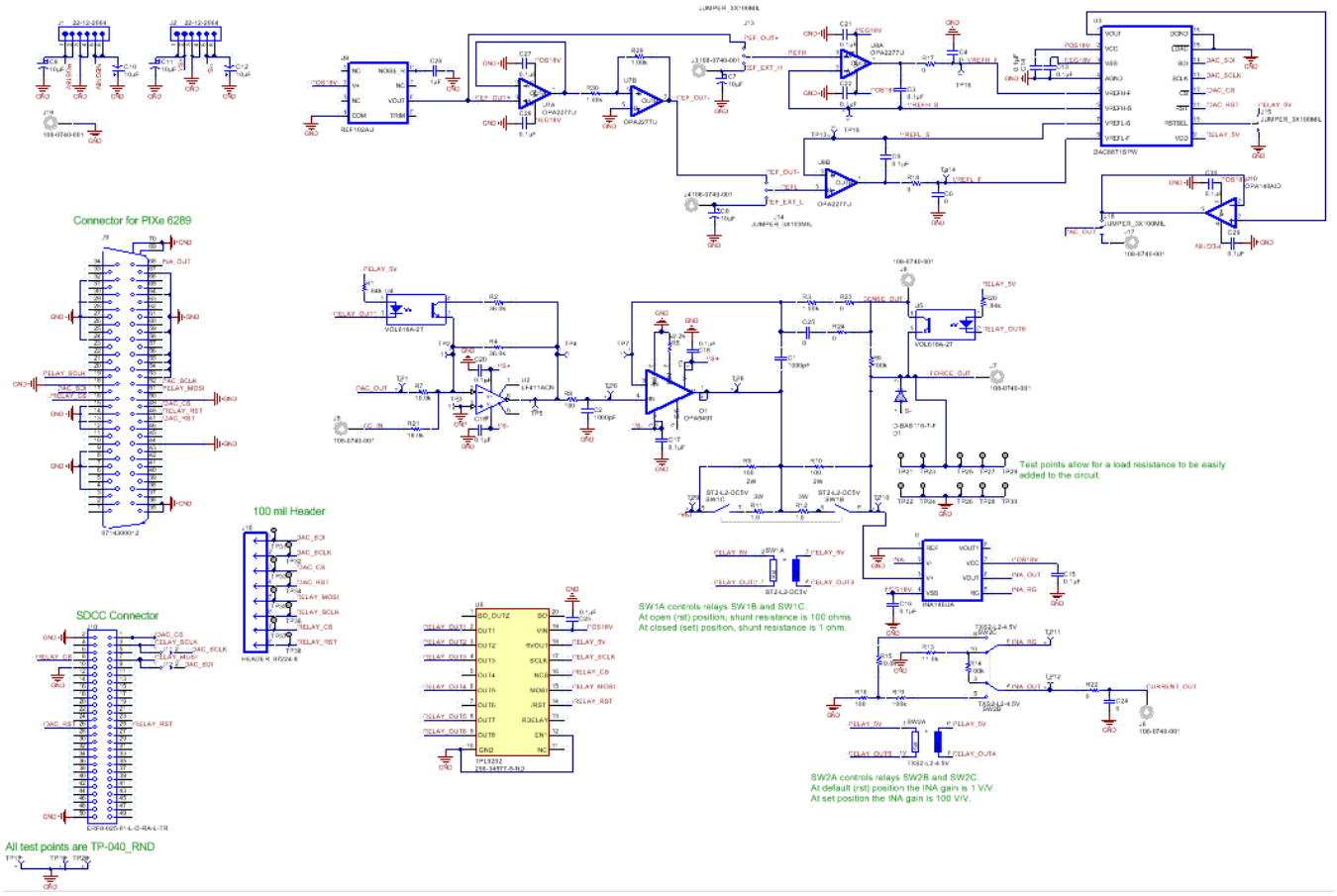

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Description	QTY	Ref Des	Manufacturer	Manufacturer Part Number
CAP, CERM, 1000pF, 50V, +/-1%, C0G/NP0, 0805	2	C1, C2	AVX Corporation	08055A102FAT2A
CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603	17	C3, C5, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C27, C28, C29, C30	AVX Corporation	06033C104JAT2A
Not Placed	4	C4, C6, C24, C25		
CAP, TA, 10uF, 50V, +/-10%, 0.4 ohm, SMD	6	C7, C8, C9, C10, C11, C12	AVX Corporation	TPSE106K050R0400
CAP, CERM, 1uF, 25V, +/-10%, X5R, 0805	1	C26	Murata Electronics	GRM216R61E105KA12D
Diode, Low Leakage, 215-mA, 85-V	1	D1	Diodes Inc.	BAS116-7-F
IC, High-Voltage, Programmable Gain difference Amp.	1	I1	Texas Instruments	INA146UA
2.54mm Pitch KK® Solid Header, Right Angle, with Friction Lock, 6 Circuits, 0.51µm Gold (Au) Plating	2	J1, J2	Molex Inc.	22-12-2064
Receptacle, D-Sub 68 Pos, R/A, TH	1	J9	Molex Inc.	0714300012
Receptacle, Micro High Speed Socket Strip, 0.8mm, 25x2, RA, SMT	1	J10	SAMTEC	ERF8-025-01-L-D-RA-L-TR
Header, Male 2-pin, 100mil spacing,	2	J11, J12	Sullins Connector Solutions	PEC02SAAN
Header, Male 3-pin, 100mil spacing,	4	J13, J14, J15, J18	Sullins Connector Solutions	PEC03SAAN
Header, 8-pin, 100mil spacing,	1	J16	TE Connectivity	87224-8
IC, High Voltage, high Currnet OpAmp	1	O1	Texas Instruments	OPA549T
RES, 1.82k ohm, 1%, 0.25W, 1206	2	R1, R20	Vishay Dale	CRCW12061K82FKEA
RES, 36.0k ohm, 0.1%, 0.125W, 0805	2	R2, R4	Susumu	RG2012P-363-B-T5
RES, 1.00k ohm, 0.5%, 0.1W, 0805	3	R3, R23, R24	Susumu	RR1220P-102-D
RES, 42.2k ohm, 0.1%, 0.125W, 0805	1	R5	Yageo	RT0805BRD0742K2L
RES, 100k ohm, 0.1%, 0.125W, 0805	3	R6, R14, R19	Susumu	RG2012P-104-B-T5
RES, 10.0k ohm, 0.1%, 0.125W, 0805	2	R7, R15	Susumu	RG2012P-103-B-T5
RES, 100 ohm, 0.1%, 0.125W, 0805	2	R8, R16	Susumu	RG2012P-101-B-T5
RES, 100 ohm, 1%, 3W, TH	2	R9, R10	Vishay Dale	CMF50100R00FHEB
RES, 1.0 ohm, 1%, 3W, TH	2	R11, R12	Vishay Dale	RS02B1R000FE70
RES, 11.0k ohm, 0.1%, 0.125W, 0805	1	R13	Susumu	RG2012P-113-B-T5
RES, 5.97k ohm, 0.1%, 0.125W, 0805	2	R17, R18,	Vishay Dale	RT0805BRD075K97L
RES, 18.0k ohm, 0.1%, 0.125W, 0805	1	R21	Susumu	RG2012P-183-B-T5
RES, 0 ohm, 5%, 0.125W, 0805	1	R17, R18, R22, R23, R24	Vishay Dale	CRCW08050000Z0EA
RES, 1.00k ohm, 0.1%, 0.125W, 0805	2	R29, R30	Susumu	RG2012P-102-B-T5
8A Polarized Relay	1	SW1	Panasonic Electric Works	ST2-L2-DC5V
Very High Sensitivity, 50 mW (nominal operating) Relay with LT style pin layout	1	SW2	Panasonic Electric Works	TXS2-L2-4.5V
Low Offset, Low Drift JFET Input Op Amp	1	U2	Texas Instruments	LF411AACN
IC, 16-bit Single Channel, ±18V o/p, Unbuffered, Serial Interface D-A Converter	1	U3	Texas Instruments	DAC8871SPW
OPTOCOUPLR PHOTOTRANS 125% 4LSOP	2	U4, U5		VOL618A-2T
8-Channel Relay Driver with Integrated 5-V LDO	1	U6	Texas Instruments	TPL9202
IC, High Precision Op Amp	2	U7, U8	Texas Instruments	OPA2277U
IC, 10V Precision Voltage Reference	1	U9	Texas Instruments	REF102AU
IC, High-Precision, Low-Noise, R-R Output, 11MHz JFET Op Amp	1	U10	Texas Instruments	OPA140AID

Figure A-2: Bill of Materials

Appendix B.

B.1 Thermal Images

WARNING: Avoid touching the OPA549 and shunt resistor during circuit operation. They can reach high temperatures.

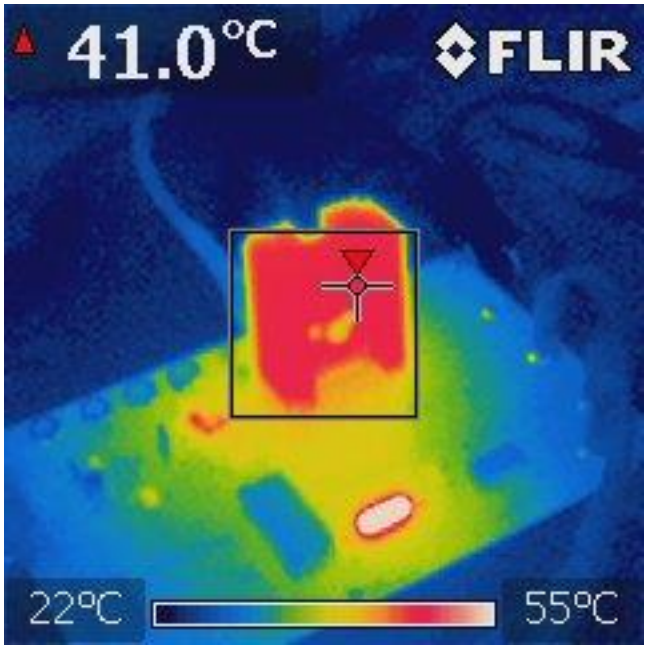

Figure B-1: OPA549 and its Heat Sink

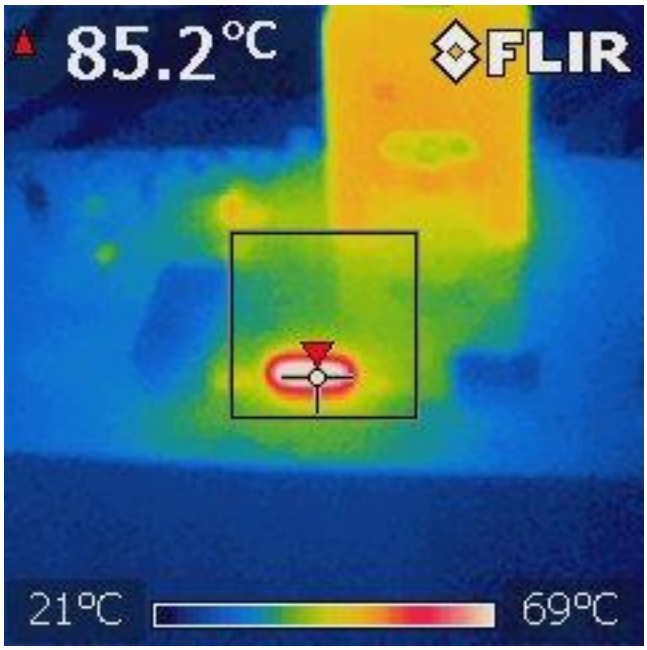

Figure B-1: Shunt Resistor R_{11}, 1 A load

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