

Class 6, PoE PD Active Clamp Forward Converter (15 V, 3.3 A) Reference Design



Description

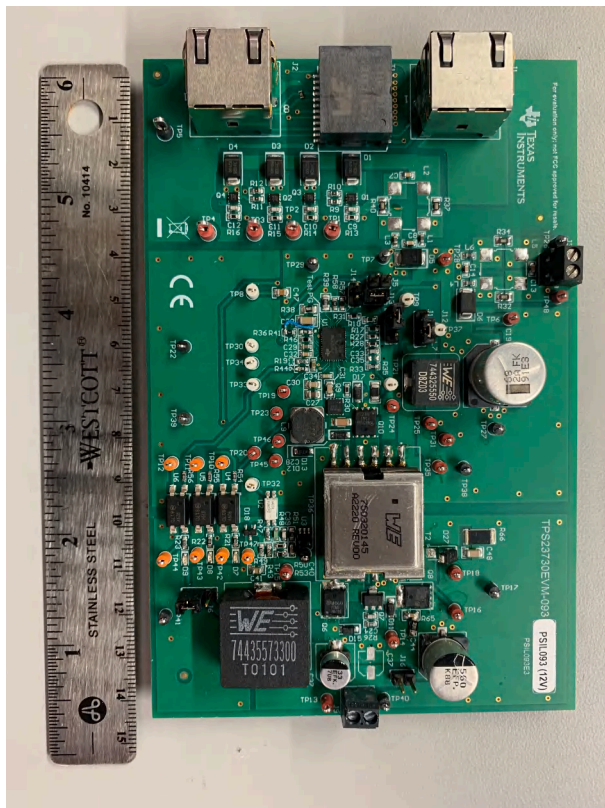
This reference design implements a Power-over-Ethernet (PoE) power device (PD) active clamp forward converter with 15-V and 3.3-A output. A TPS23730 PD with integrated pulse-width modulator (PWM) controller provides all the necessary functions to implement the PoE PD control and the PWM control for the active-clamp forward converter. This design uses secondary-side regulation (SSR) with an optocoupler feedback.

Features

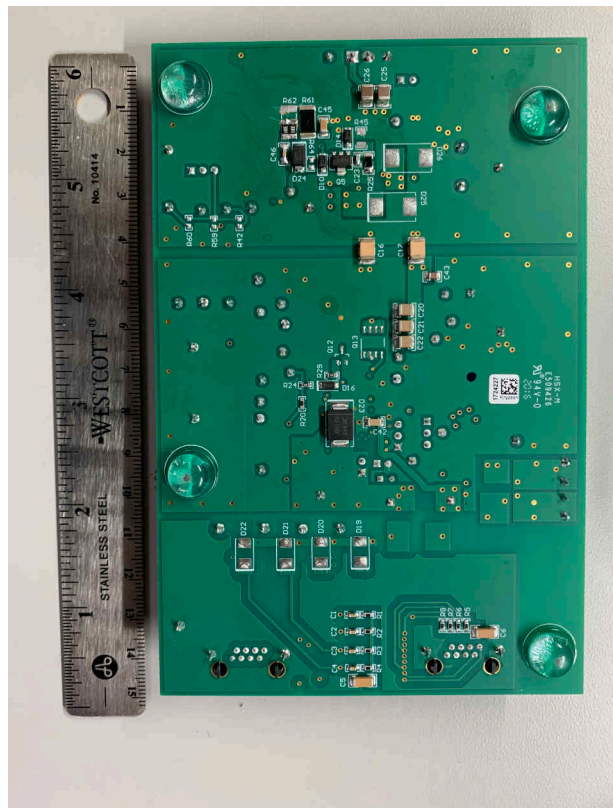
- IEEE802.3bt Type 3 compliant PoE PD
- Integrated PWM controller for flyback or active clamp forward configuration
- Frequency dithering for EMI reduction
- Soft-start control with advanced start-up and hiccup mode overload protection
- Soft-stop shutdown
- Optional adapter input

Applications

- IP network camera
- WLAN, Wi-Fi® access point
- Barcode reader



Top Photo



Bottom Photo

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input voltage	37 V–57 V (48-V nominal)
Output voltage	15 V
Output current	3.3 A
Nominal switching frequency	250 kHz

1.2 Required Equipment

- Type 3 or 4 PoE Power Source Equipment (PSE)
- Isolated DC power source, 0 V to 57 V, 2-A minimum
- 15-V, 3.3-A electronic load

1.3 Considerations

All measurements were taken under the following conditions:

- Approximately 25°C ambient
- 48-V input and 3.3-A load unless noted
- Using CAT5E 1-ft Ethernet cable

2 Testing and Results

2.1 Efficiency Graphs

Efficiency is shown in the following figure.

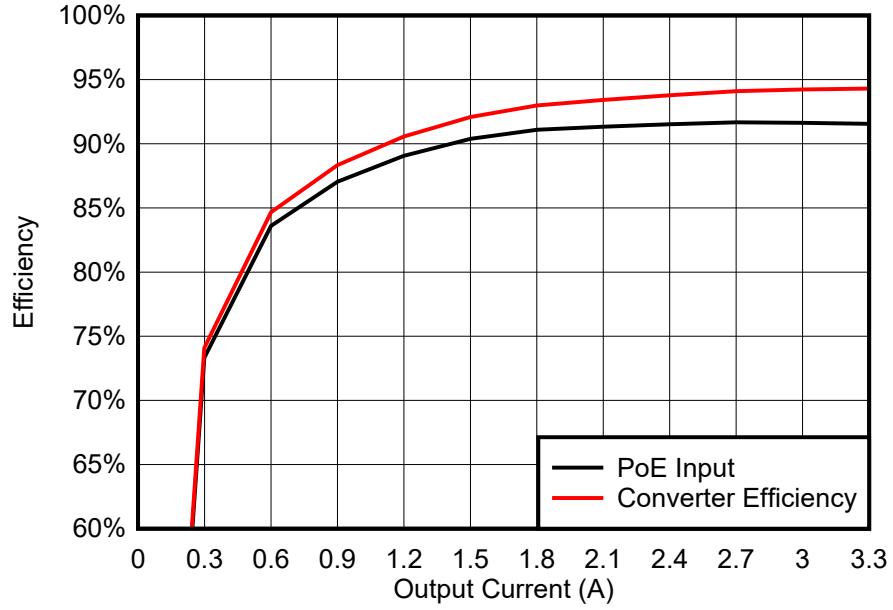


Figure 2-1. PMP23253 Rev. A Efficiency Graph, PoE Ideal Diode Bridge

2.2 Load Voltage Regulation

Load voltage regulation is shown in the following figure.

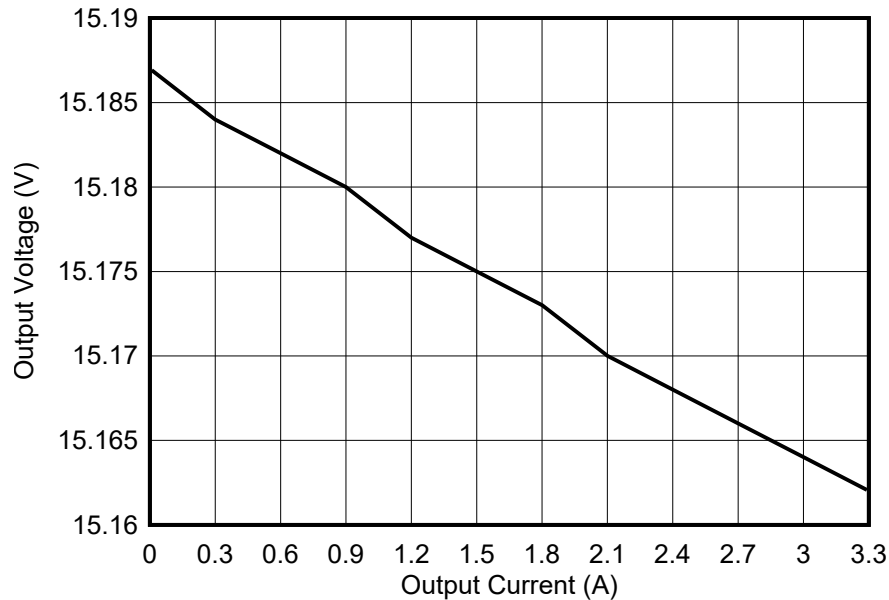


Figure 2-2. PMP23253 Rev. A, Load Voltage Regulation Curve

2.3 Efficiency Data

Efficiency data is shown in the following table.

Table 2-1. PMP23253 Efficiency Data

PoE Input Voltage (V)	PoE Input Current (A)	DC/DC Input Voltage (V)	Output Voltage (V)	Output Current (A)	PoE Efficiency	DC/DC Efficiency
48	0.034	47.619	15.187	0	0.0%	0.0%
48	0.129	47.499	15.184	0.299	73.3%	74.1%
48	0.227	47.397	15.182	0.6	83.6%	84.7%
48	0.327	47.299	15.18	0.9	87.0%	88.3%
48	0.426	47.205	15.177	1.2	89.1%	90.6%
48	0.525	47.112	15.175	1.501	90.4%	92.1%
48	0.625	47.02	15.173	1.801	91.1%	93.0%
48	0.727	46.931	15.17	2.101	91.3%	93.4%
48	0.829	46.844	15.168	2.401	91.5%	93.8%
48	0.931	46.762	15.166	2.701	91.7%	94.1%
48	1.035	46.675	15.164	3.002	91.6%	94.2%
48	1.139	46.594	15.162	3.301	91.5%	94.3%

2.4 Thermal Images

The thermal images are shown in the following figures.

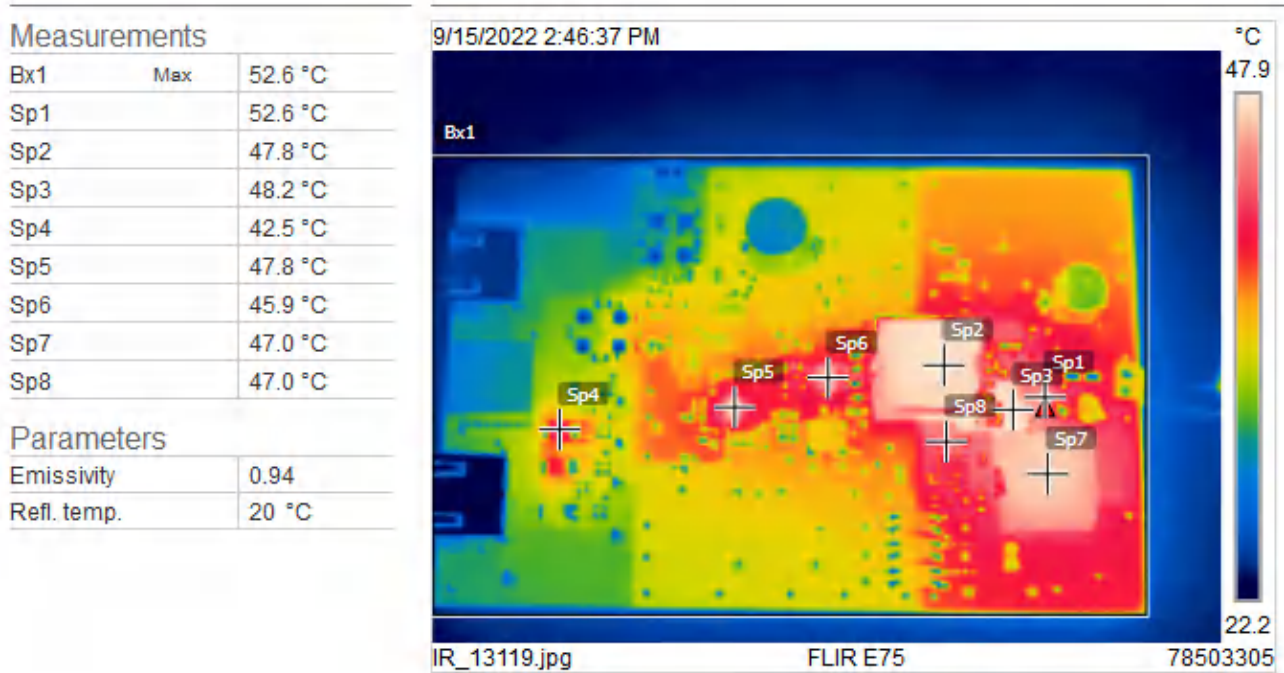


Figure 2-3. Top Thermal Image, 48-V Input, 3.3-A Load

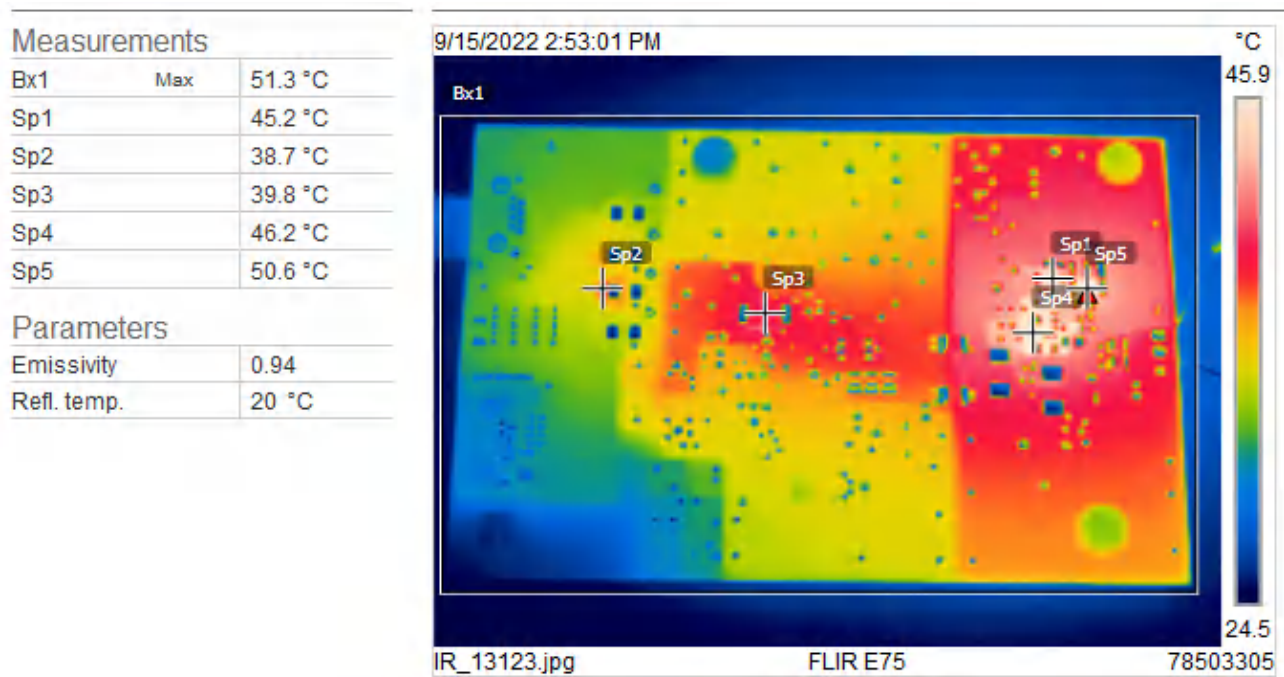


Figure 2-4. Bottom Thermal Image, 48-V Input, 3.3-A Load

2.5 Bode Plots

The PMP23253 bode plots are shown in the following figures.

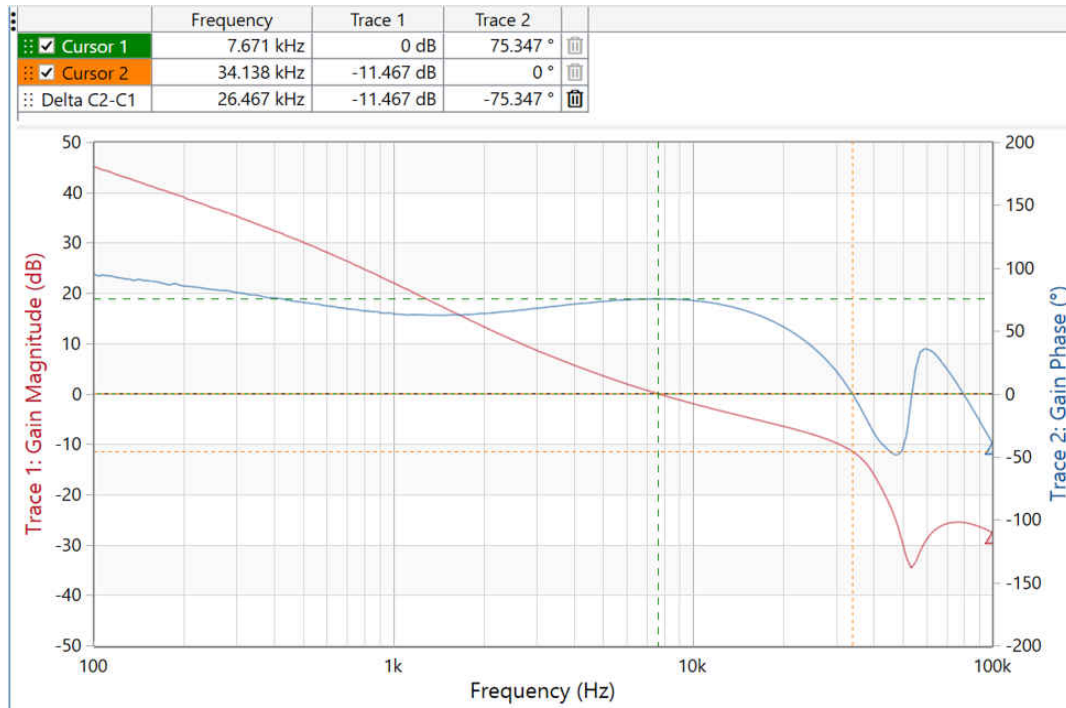


Figure 2-5. At 0-A Load Bandwidth = 7.7 kHz, Phase Margin = 75.3 Degrees, Gain Margin = 11.5 dB

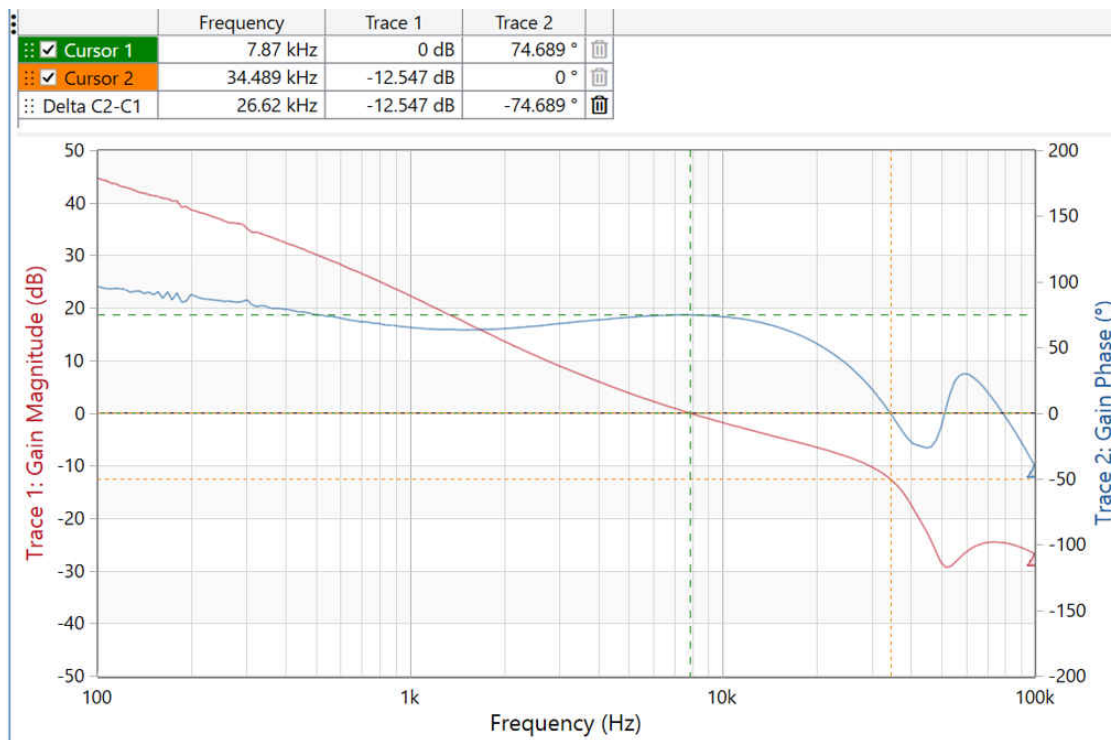


Figure 2-6. At 3.3-A Load Bandwidth = 7.9 kHz, Phase Margin = 74.7 Degrees, Gain Margin = 12.5 dB

3 Waveforms

3.1 Switching

Switching behavior is shown in the following figures.

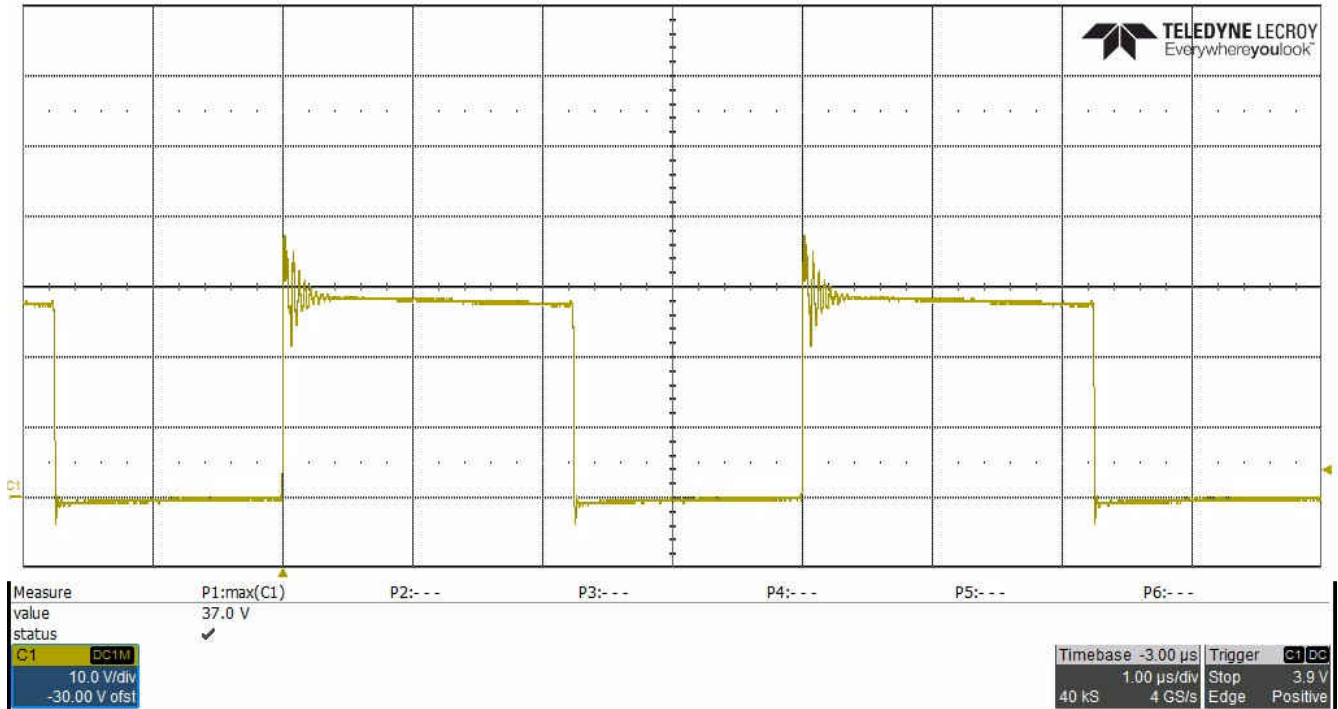


Figure 3-1. Voltage Drain-to-Source, Q6, 37-V Input, 3.3-A Load, Measured 37.0-V V_{peak}

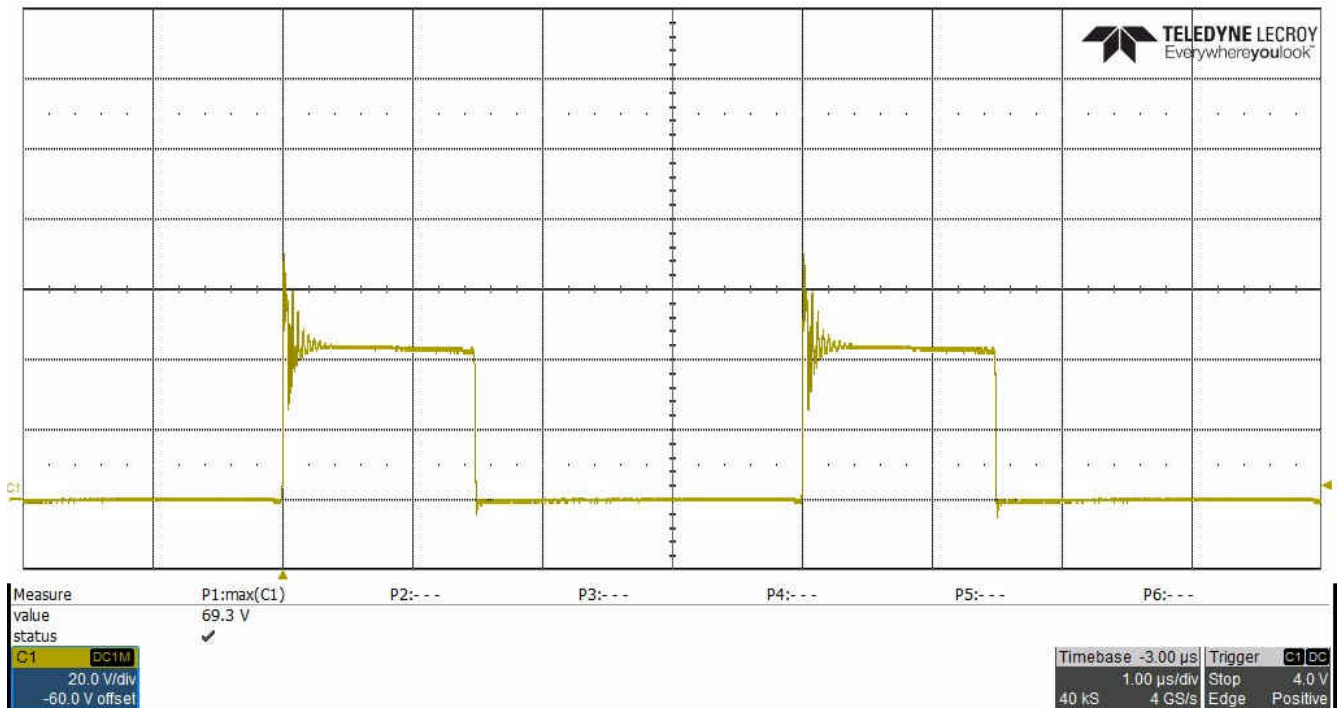


Figure 3-2. Voltage Drain-to-Source, Q6, 57-V Input, 3.3-A Load, Measured 69.3-V V_{peak}

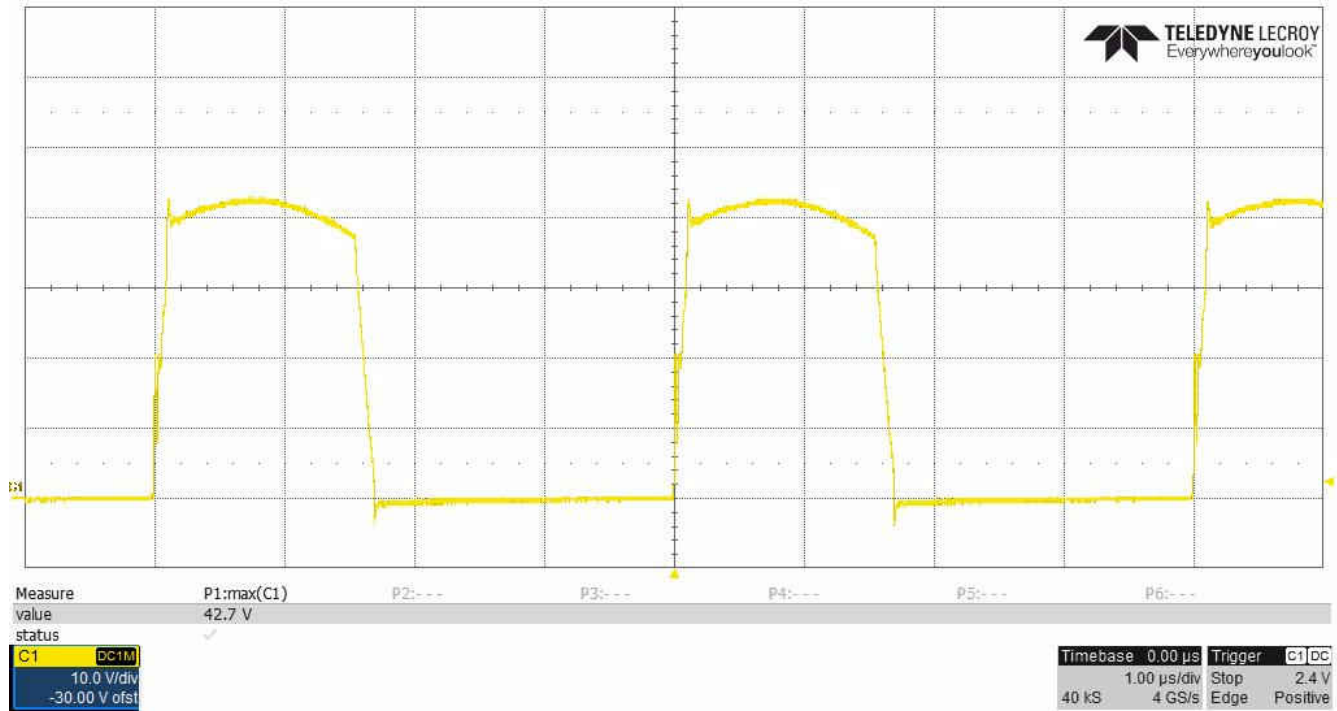


Figure 3-3. Voltage Drain-to-Source, Q8, 37-V Input, 3.3-A Load, Measured 42.7-V V_{peak}

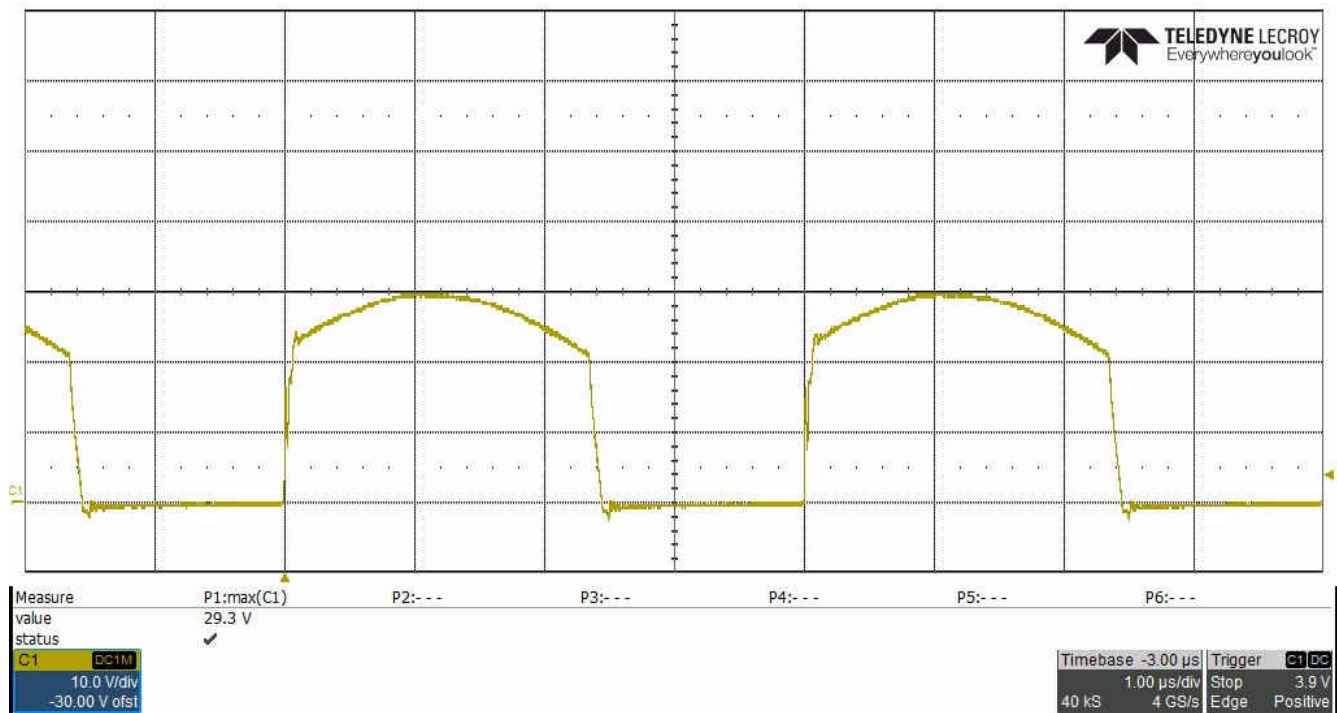


Figure 3-4. Voltage Drain-to-Source, Q8, 57-V Input, 3.3-A Load, Measured 29.3-V V_{peak}

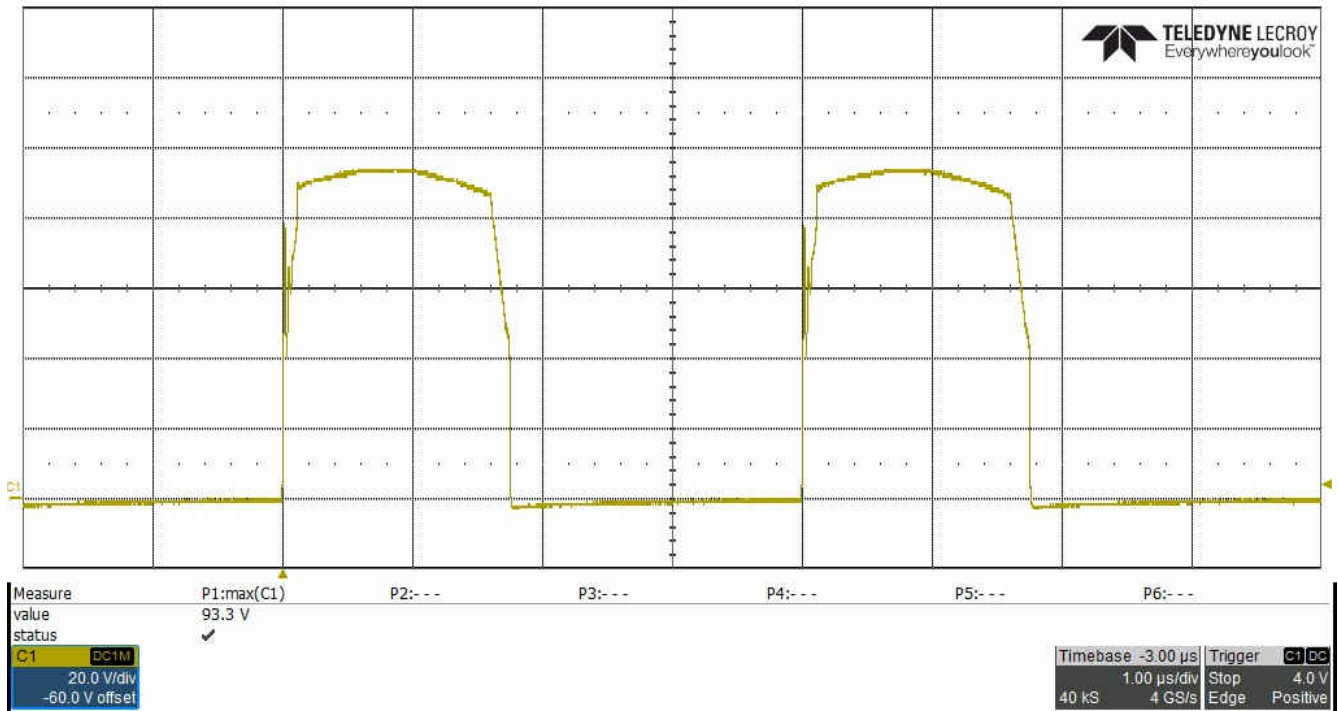


Figure 3-5. Voltage Drain-to-Source, Q10, 37-V Input, 3.3-A Load, Measured 93.3-V V_{peak}

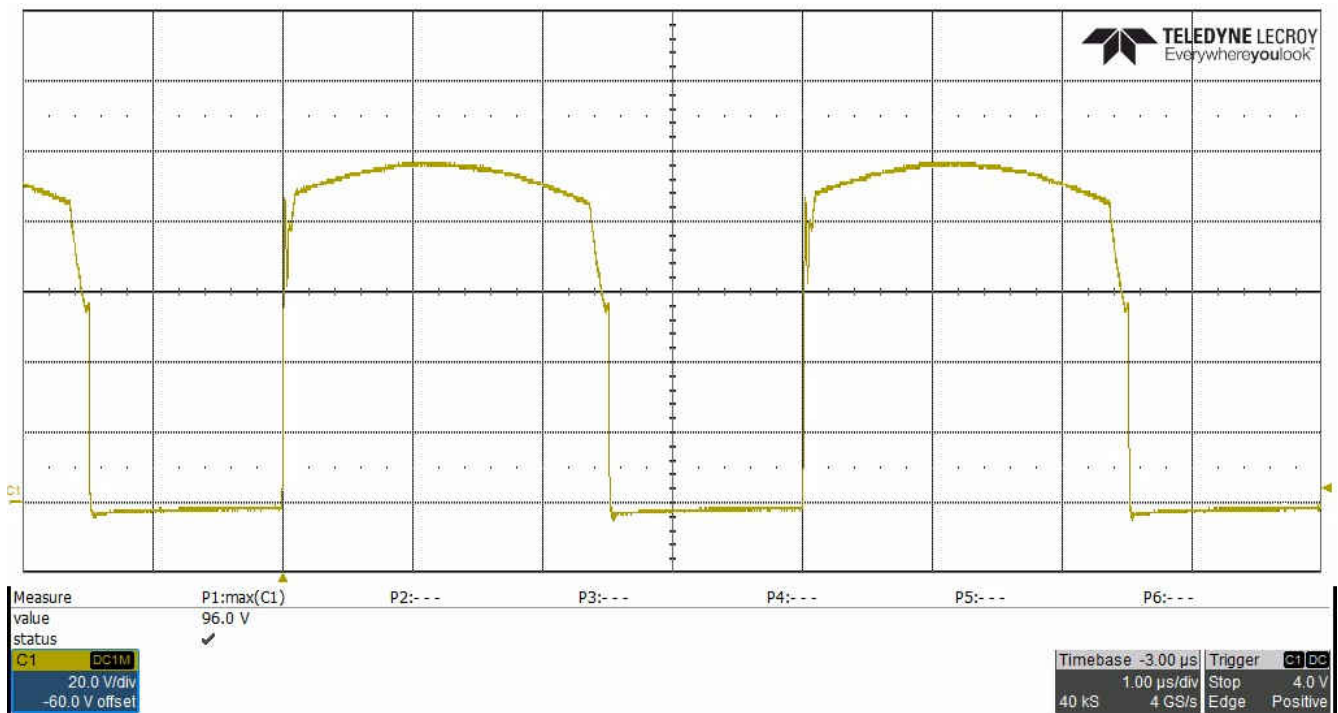


Figure 3-6. Voltage Drain-to-Source, Q10, 57-V Input, 3.3-A Load, Measured 96.0-V V_{peak}

3.2 Output Voltage Ripple

Voltage ripple waveforms are shown in the following figures.

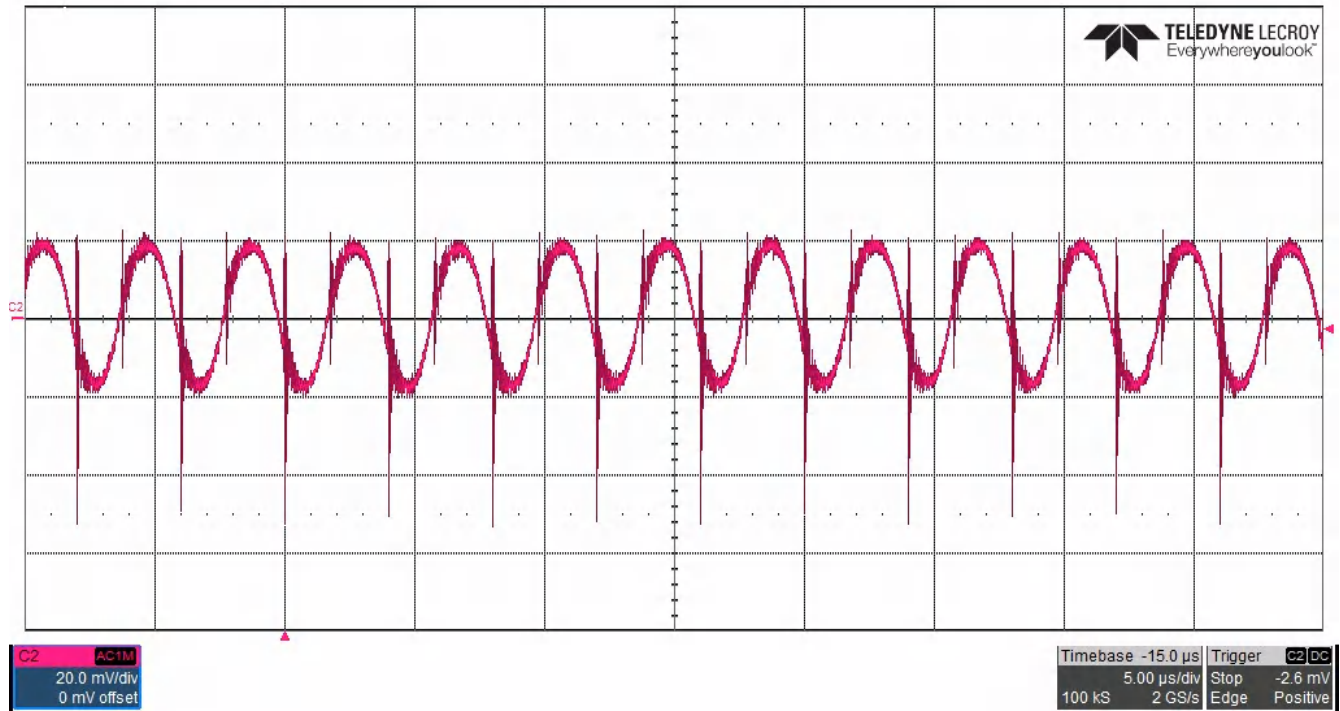


Figure 3-7. Output Voltage Ripple

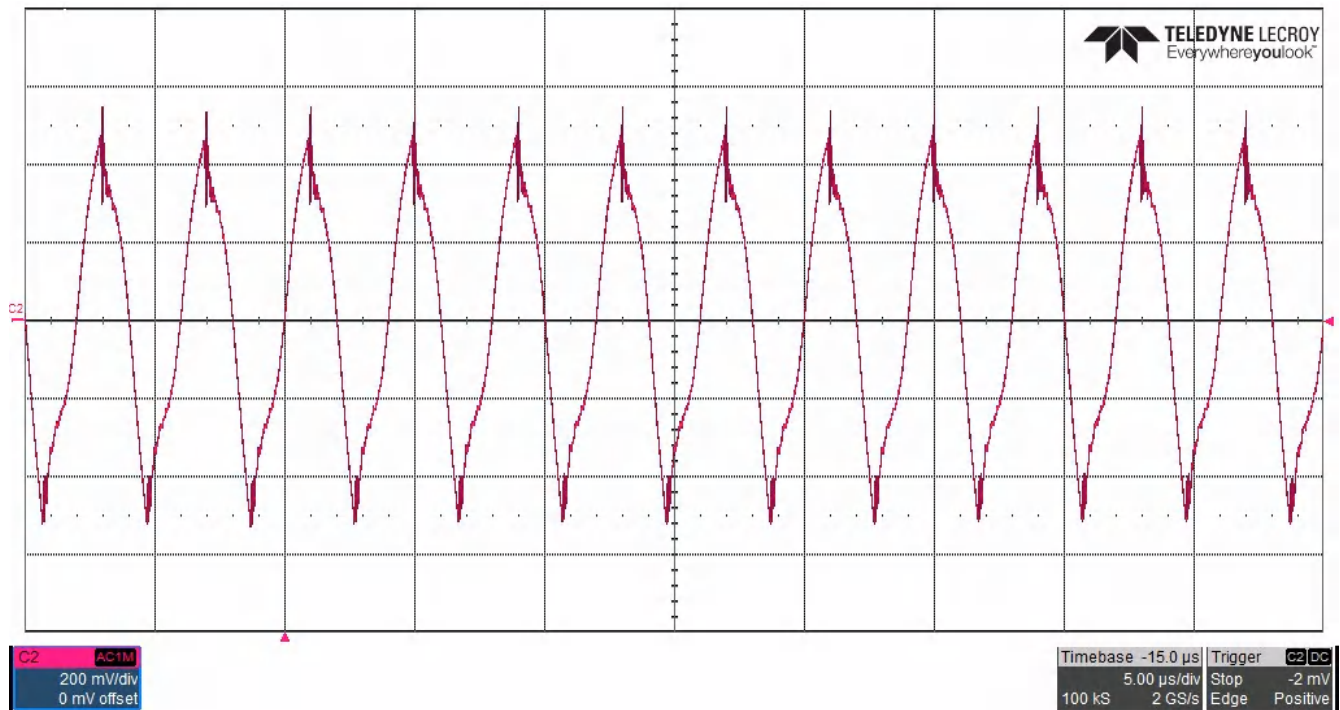


Figure 3-8. DC/DC Converter Input Voltage Ripple

3.3 Load Transients

Load transient response waveforms are shown in the following figures.

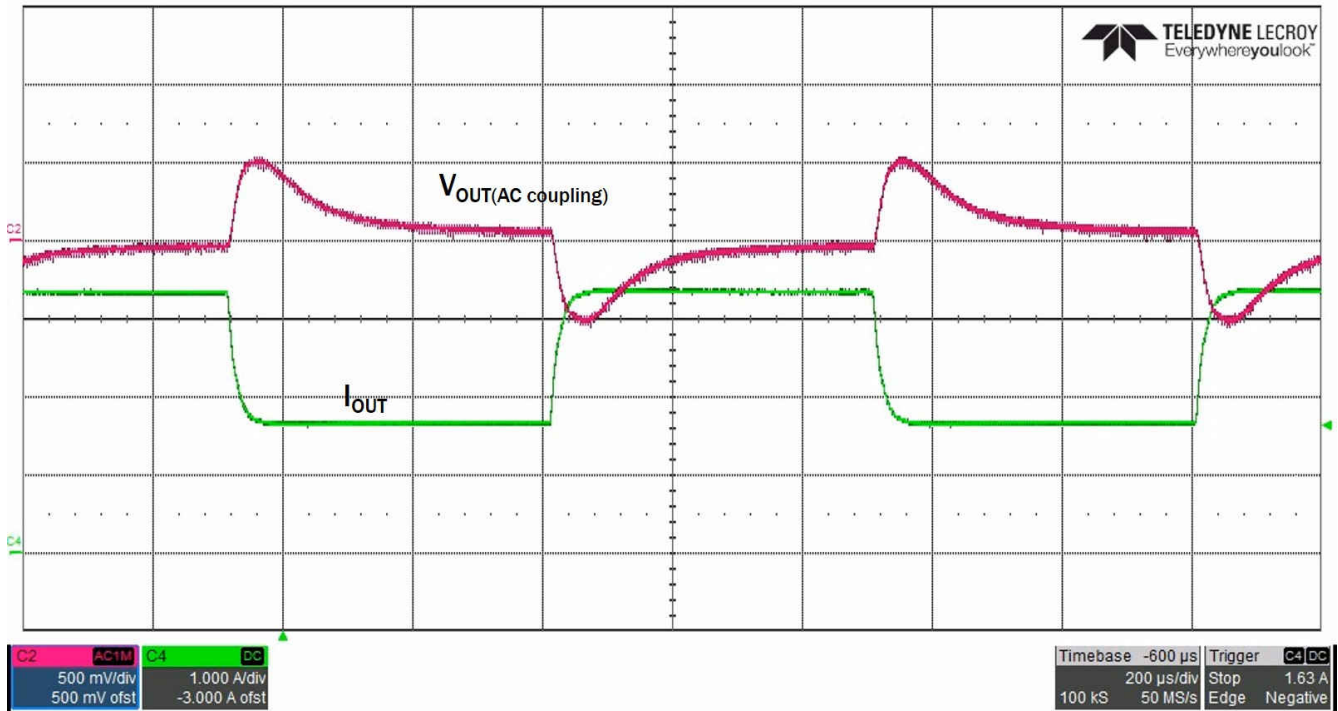


Figure 3-9. Output Load Step Response, 1.65-A to 3.30-A Load Step

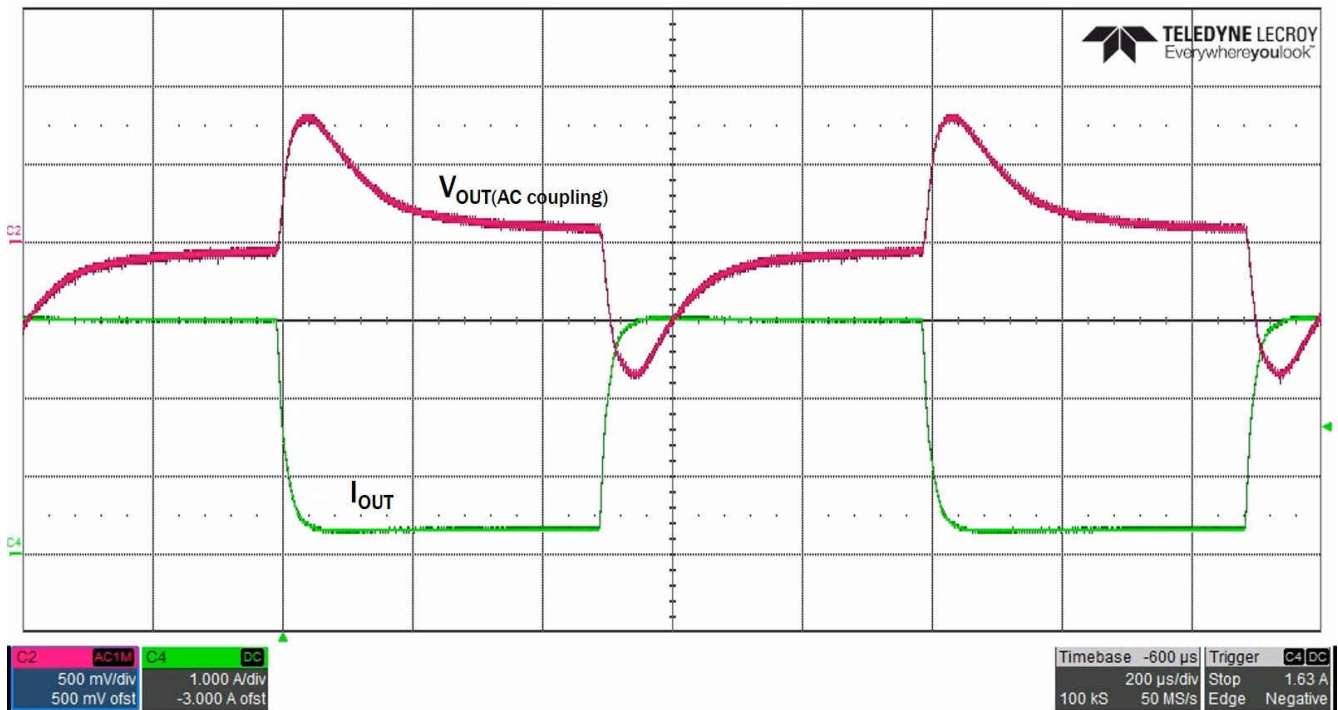


Figure 3-10. Output Load Step Response, 0.33-A to 2.97-A Load Step

3.4 Start-Up Sequence

Start-up behavior is shown in the following figures.

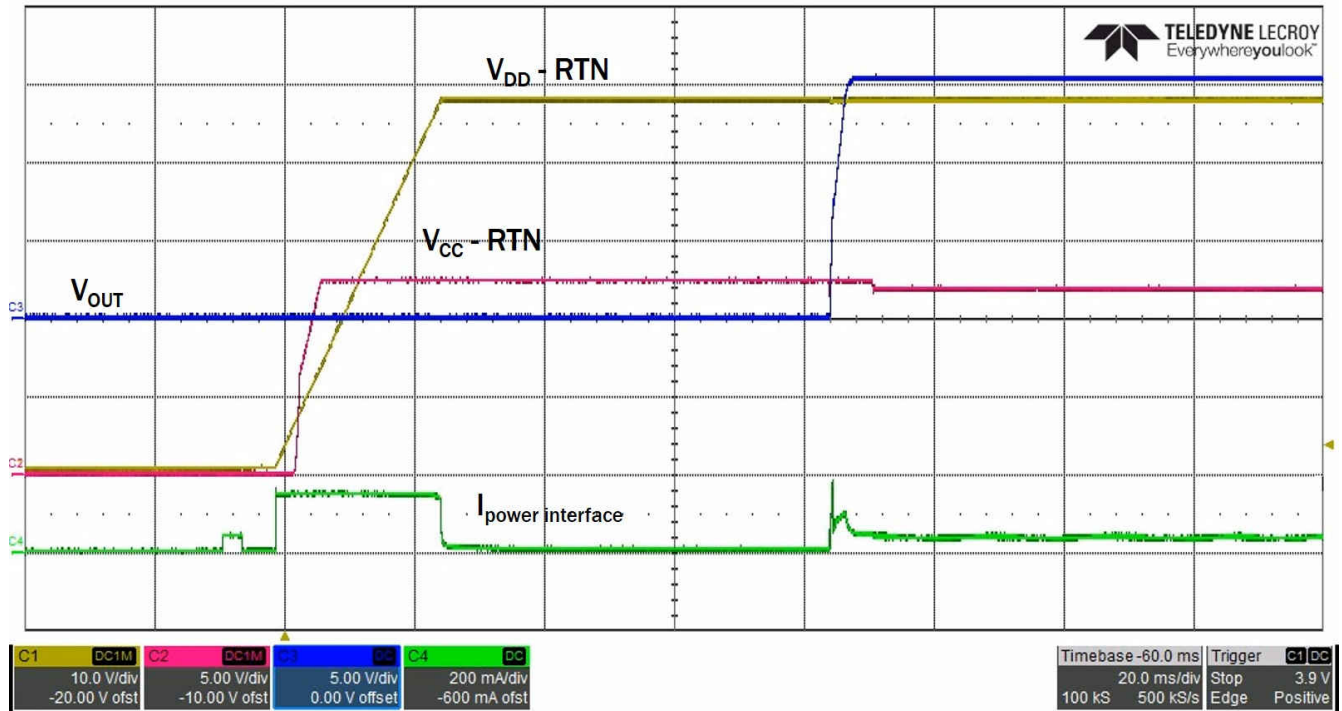


Figure 3-11. 0-A Load

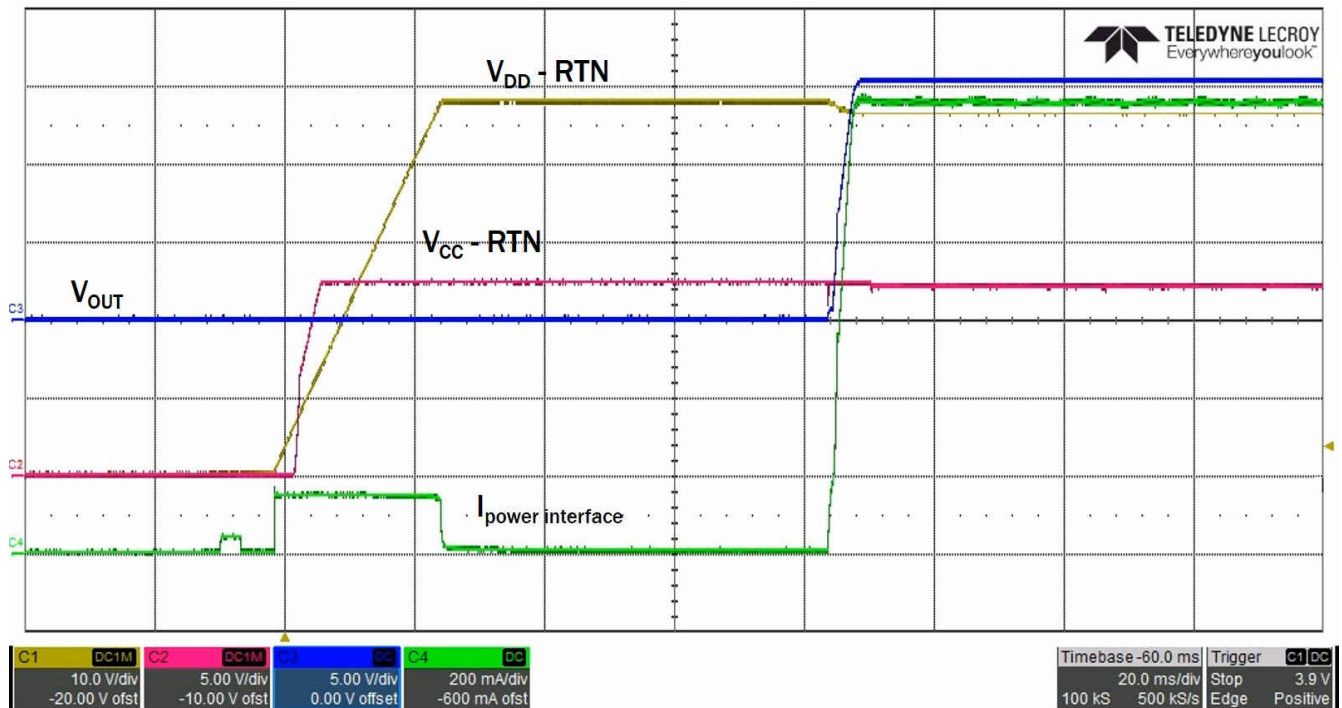


Figure 3-12. 3.3-A Load

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