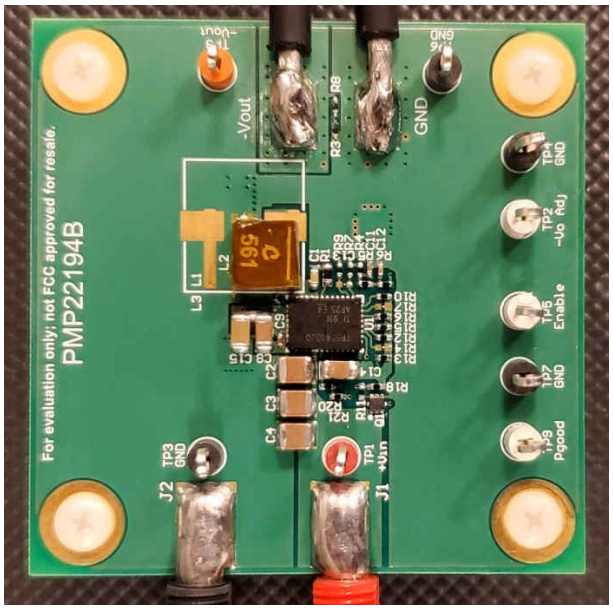
Test Report: PMP22194

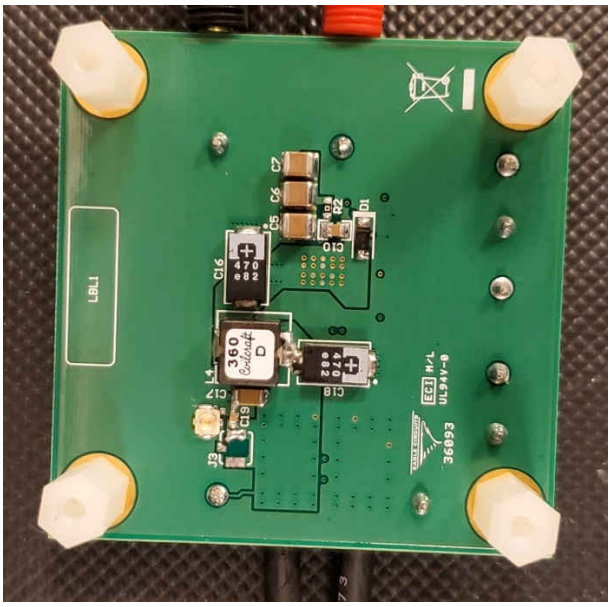
Synchronous Inverting Buck-Boost Converter Reference Design With Adjustable Negative Output Voltage

Description

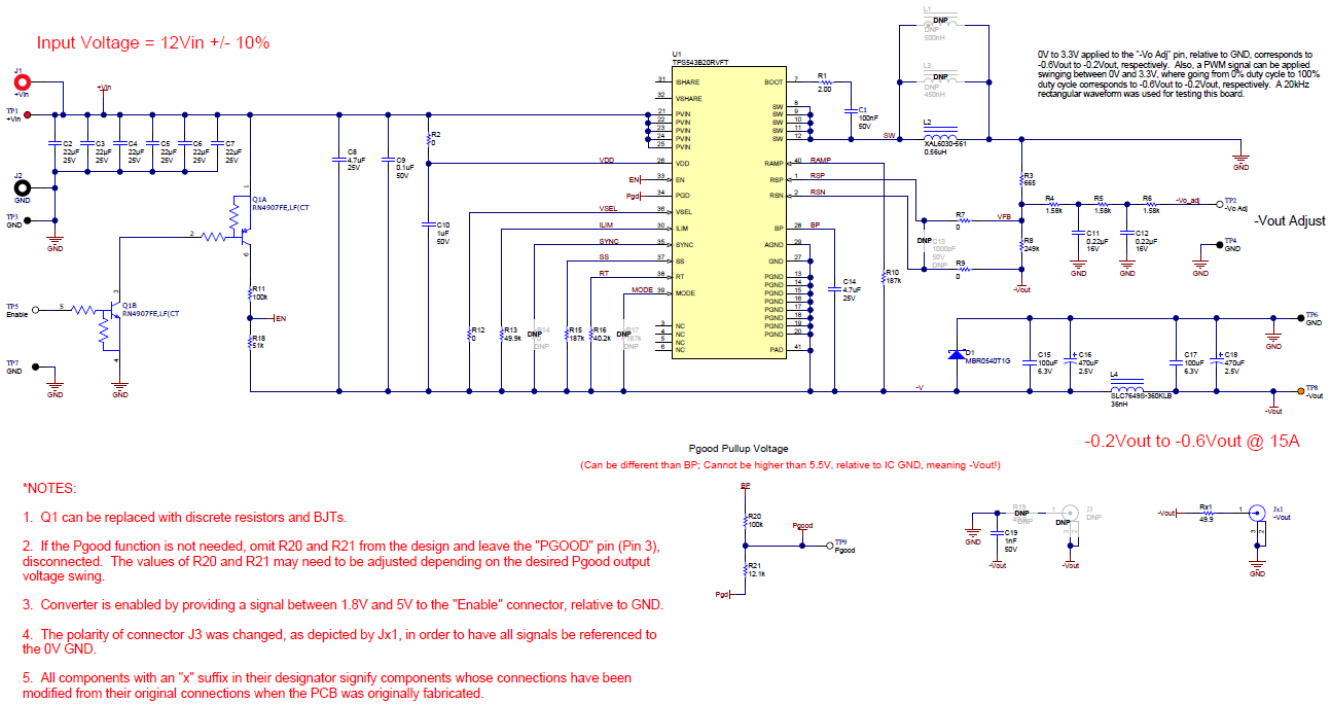
This reference design utilizes a synchronous buck regulator with internal top and bottom FETs, which is configured as a synchronous inverting buck-boost converter to provide an adjustable output of between –0.2 V and –0.6 V capable of delivering a maximum of 15 A of current to the load. The output voltage is adjusted by either providing a PWM signal or analog voltage signal to the –*Vout Adj* connector, referenced to GND. See the Board Schematic for details regarding voltages.



Top Side of PCB



Bottom Side of PCB



*NOTES:

1. Q1 can be replaced with discrete resistors and BJTs.
2. If the Pgood function is not needed, omit R20 and R21 from the design and leave the "PGOOD" pin (Pin 3), disconnected. The values of R20 and R21 may need to be adjusted depending on the desired Pgood output voltage swing.
3. Converter is enabled by providing a signal between 1.8V and 5V to the "Enable" connector, relative to GND.
4. The polarity of connector J3 was changed, as depicted by Jx1, in order to have all signals be referenced to the 0V GND.
5. All components with an "x" suffix in their designator signify components whose connections have been modified from their original connections when the PCB was originally fabricated.

Board Schematic

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
V_{IN}	12 VDC ±10%
V_{OUT}	–0.2 VDC to –0.6 VDC (adjustable)
I_{OUT}	15 A maximum
F_{SW}	500 kHz nominal

1.2 Required Equipment

- Power supplies (one to provide main converter power, the other to provide the enable signal)
- Electronic load (with very low operating voltage, that is, 0-V rated)
- Digital multimeters
- Oscilloscope
- Auxiliary power supply or function generator (for providing signal that controls the output voltage)

1.3 Considerations

The mating connector to J3 has an associated coax cable with a barrel connector at the other end that can be plugged into the oscilloscope. Since the barrel is connected to Earth GND via the oscilloscope, the J3 connector on the board was taken out and repositioned so that the GND connection gets connected to the GND barrel, as can be seen from the schematic. A 20-kHz pulse, with a LOW of 0 V and HIGH of 3.3 V, was used to provide an adjustable PWM signal to control the output voltage, referenced to GND. A 3.3-V signal voltage was used to enable the device via the *Enable* connector, referenced to GND.

The output ripple voltage was measured by another connector placed at the end of a blank copper clad board, to keep the measurement point away from the switch node. The original location, that is, where J3 is located, is too close to the switch node and so a lot of noise is being injected into the connector. The end of the copper clad board simply has a 100-µF and 1-nF capacitor close to the antenna connector where the measurement is made.

1.4 Dimensions

The Top Side and Bottom Side images present the top and bottom photos of the PMP21194 Rev B board. The board dimensions are 2.1 in × 2.1 in (53.3 mm × 53.3 mm). The actual solution size is approximately 0.98 in × 0.72 in (24.9 mm × 18.3 mm).

Figure 1-1 presents the top photo of the PMP21194 RevB board with an output extension board connected, to allow for a less noisy output voltage ripple measurement to be made. Since the original placement of the output voltage connector was very close to the switch node, a lot of noise was being injected into the connector which appeared as large, sharp spikes superimposed on the actual output ripple voltage. The addition of this copper clad board allowed for the point of measurement to be physically further from the noise source, that is, switch node.

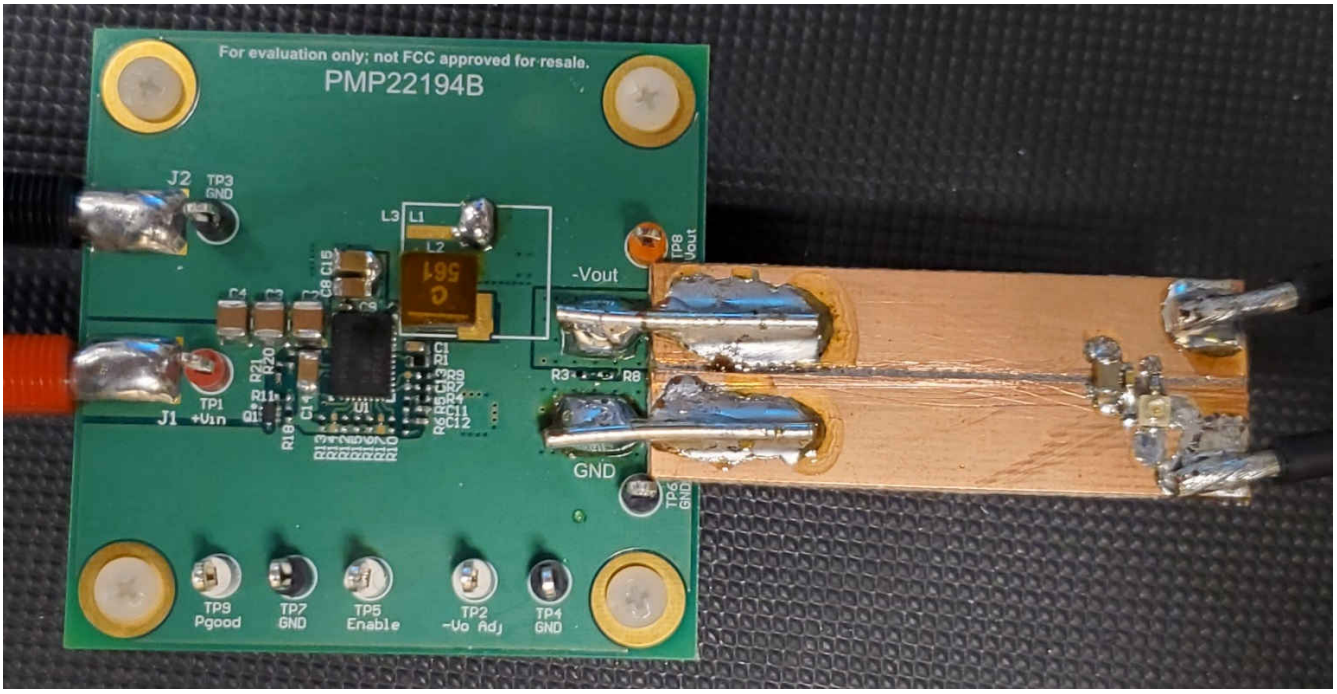


Figure 1-1. Top of PMP21194 Board (with extended output board to take output voltage ripple measurements away from the switch node, where noise is being coupled into the V_{OUT} connector, J3)

2 Testing and Results

2.1 Efficiency Graphs

The following figure shows the converter efficiency for a 12-V input with –0.2-V and –0.6-V outputs with the output being swept from 1.5 A to 15 A.

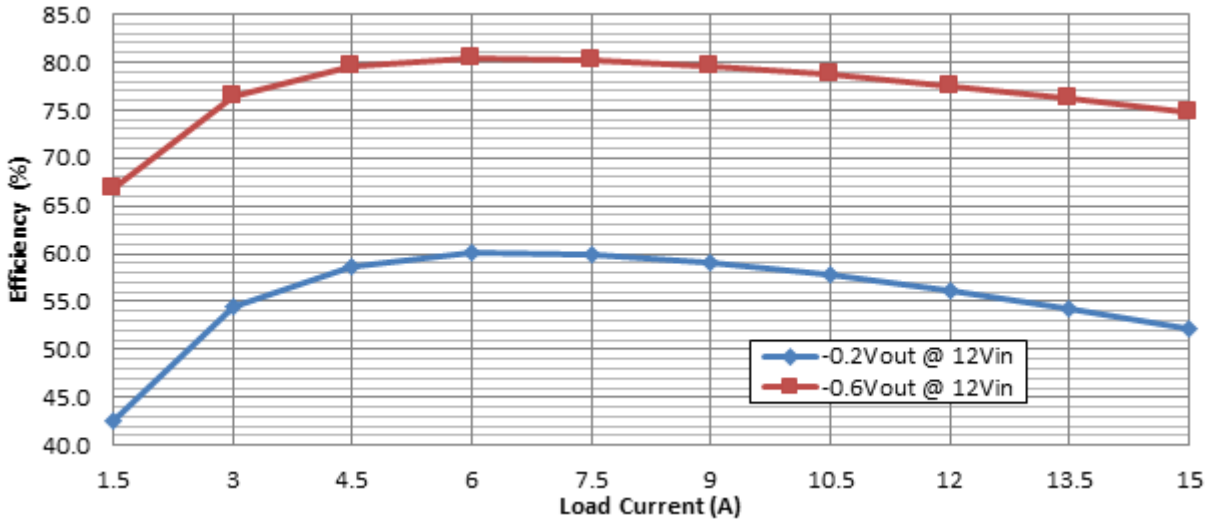


Figure 2-1. PMP22194 Rev B, Converter Efficiency 12-V Input, –0.2-V and –0.6-V Outputs

2.2 Efficiency Data

Table 2-1 and Table 2-2 show the efficiency data for –0.2-V and –0.6-V outputs with a 12-V input.

Table 2-1. Efficiency Data 12-V input, -0.2-V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
12	0.0238	–0.2002	0	0.2856	0.0000	0.2856	0.0
12	0.0587	–0.2001	1.5	0.7044	0.3002	0.4043	42.6
12	0.0918	–0.2001	3	1.1016	0.6003	0.5013	54.5
12	0.1277	–0.2001	4.5	1.5324	0.9005	0.6320	58.8
12	0.1667	–0.2001	6	2.0004	1.2006	0.7998	60.0
12	0.2089	–0.2001	7.5	2.5068	1.5008	1.0061	59.9
12	0.2540	–0.2002	9	3.0480	1.8018	1.2462	59.1
12	0.3032	–0.2002	10.5	3.6384	2.1021	1.5363	57.8
12	0.3571	–0.2002	12	4.2852	2.4024	1.8828	56.1
12	0.4157	–0.2003	13.5	4.9884	2.7041	2.2844	54.2
12	0.4795	–0.2004	15	5.7540	3.0060	2.7480	52.2

Table 2-2. Efficiency Data 12-V Input, –0.6-V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
12	0.0343	–0.5999	0	0.4116	0.0000	0.4116	0.0
12	0.1124	–0.5999	1.5	1.3488	0.8999	0.4490	66.7
12	0.1961	–0.5998	3	2.3532	1.7994	0.5538	76.5
12	0.2828	–0.5998	4.5	3.3936	2.6991	0.6945	79.5
12	0.3731	–0.5998	6	4.4772	3.5988	0.8784	80.4
12	0.4672	–0.5998	7.5	5.6064	4.4985	1.1079	80.2
12	0.565	–0.5999	9	6.7800	5.3991	1.3809	79.6
12	0.6663	–0.6	10.5	7.9956	6.3000	1.6956	78.8
12	0.7733	–0.6	12	9.2796	7.2000	2.0796	77.6
12	0.8856	–0.6	13.5	10.6272	8.1000	2.5272	76.2
12	1.0033	–0.6001	15	12.0396	9.0015	3.0381	74.8

2.3 Thermal Images

The thermal images in the following figures show operation at 12-V input and –0.2-V and –0.6-V outputs at 15-A load, with no airflow. Thermals images were taken of both the top and bottom side of the board and were captured after the board had reached thermal equilibrium.

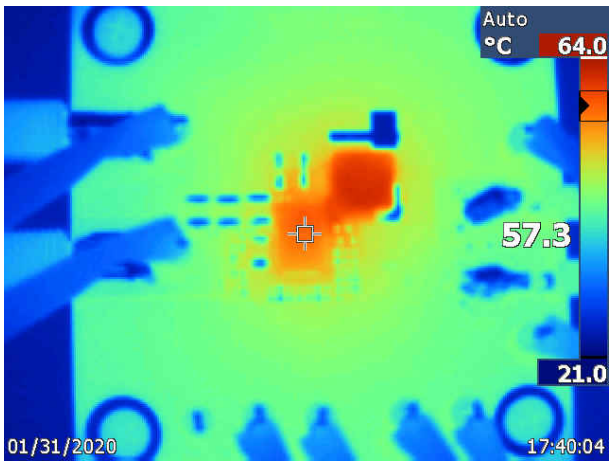


Figure 2-2. Thermal Image, Top Side of Board, 12-V Input, –0.2-V Output at 15-A Load

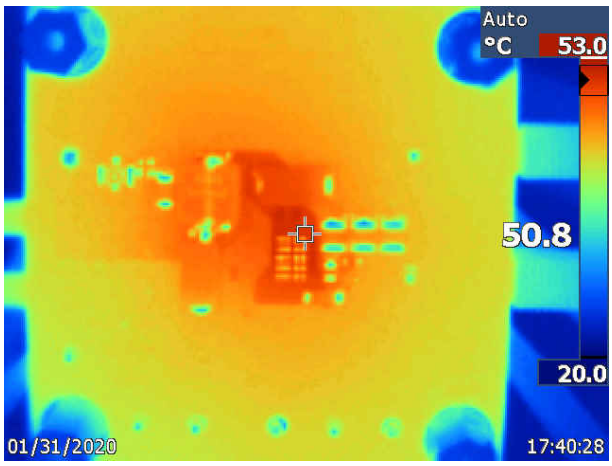


Figure 2-3. Thermal Image, Bottom Side of Board, 12-V Input, –0.2-V Output at 15-A Load

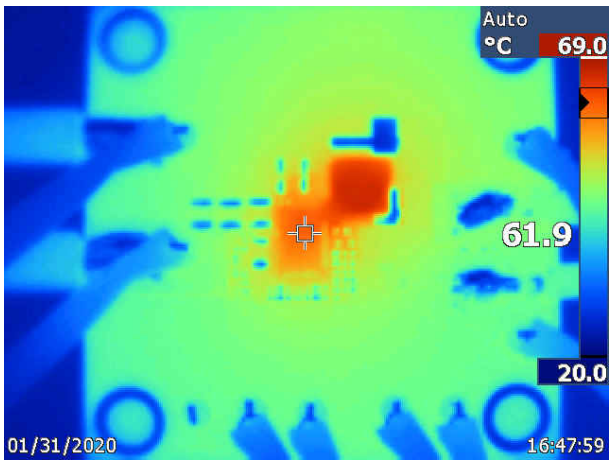


Figure 2-4. Thermal Image, Top Side of Board, 12-V Input, –0.6-V Output at 15-A Load

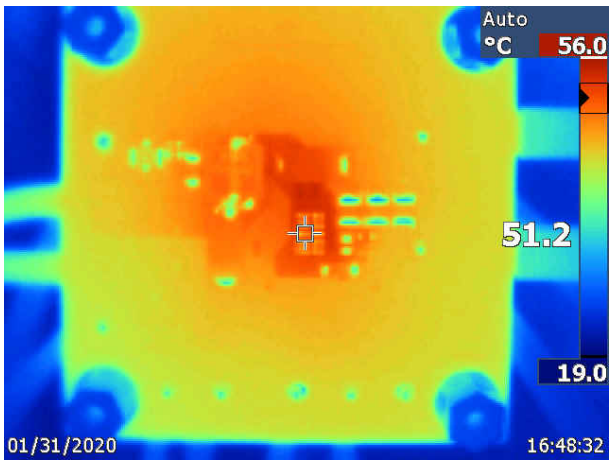


Figure 2-5. Thermal Image, Bottom Side of Board, 12-V Input, –0.6-V Output at 15-A Load

3 Waveforms

3.1 Switching

Figure 3-1 to Figure 3-4 show the switch node voltage of the converter at 12-V input and -0.2-V and -0.6-V output at no load and 15-A load conditions. Figure 3-1 illustrates that there are skipped pulses. This is due to the required ON-time pulses needing to be greater than the capable minimum ON-time of the regulator, which is 30 ns for the TPS543B20. This behavior tends to cease when the load is increased, which would require longer ON-time for regulation, due to the increase in duty cycle as power losses increase. The design should be evaluated for such behavior, especially for the boundary region of operation where the average switching frequency transitions from 500 kHz (with no pulse-skipping) to 250 kHz (that is, pulse-skipping; skipping every other pulse). The user needs to verify the operation and deem it acceptable under all their application scenarios, themselves.

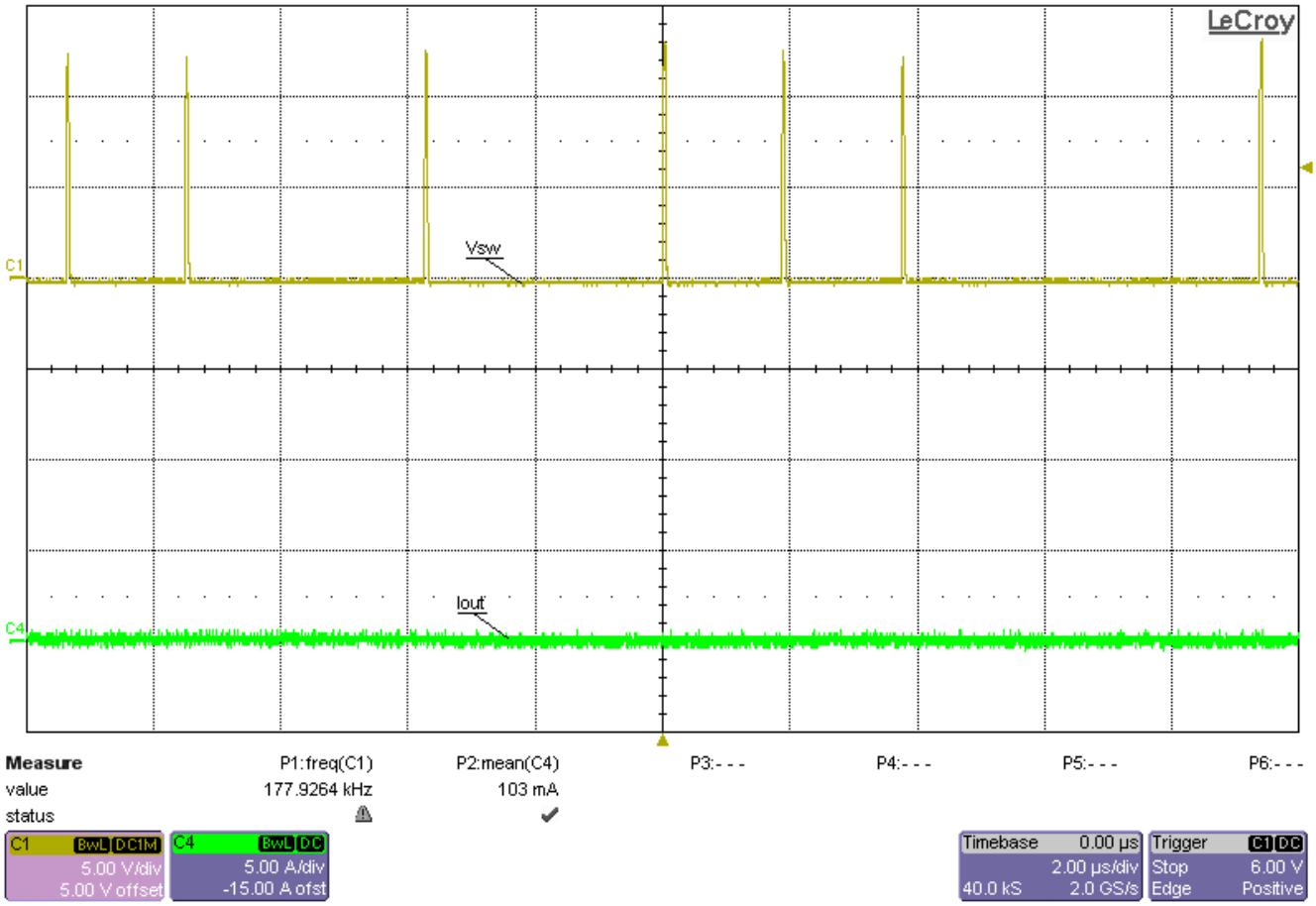


Figure 3-1. Switch Node Voltage, 12-V Input, –0.2-V Output, No Load

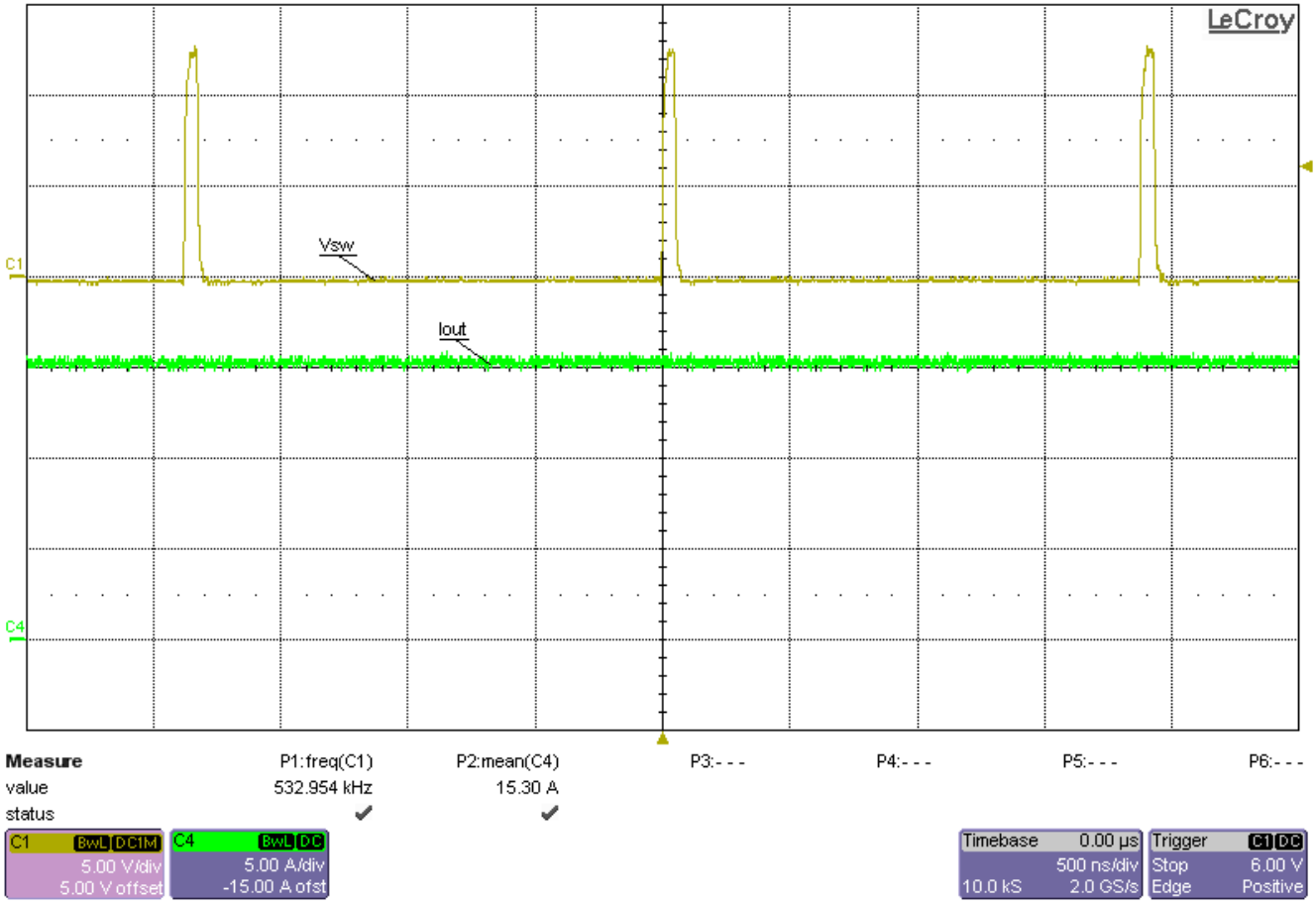


Figure 3-2. Switch Node Voltage, 12-V Input, –0.2-V Output, 15-A Load

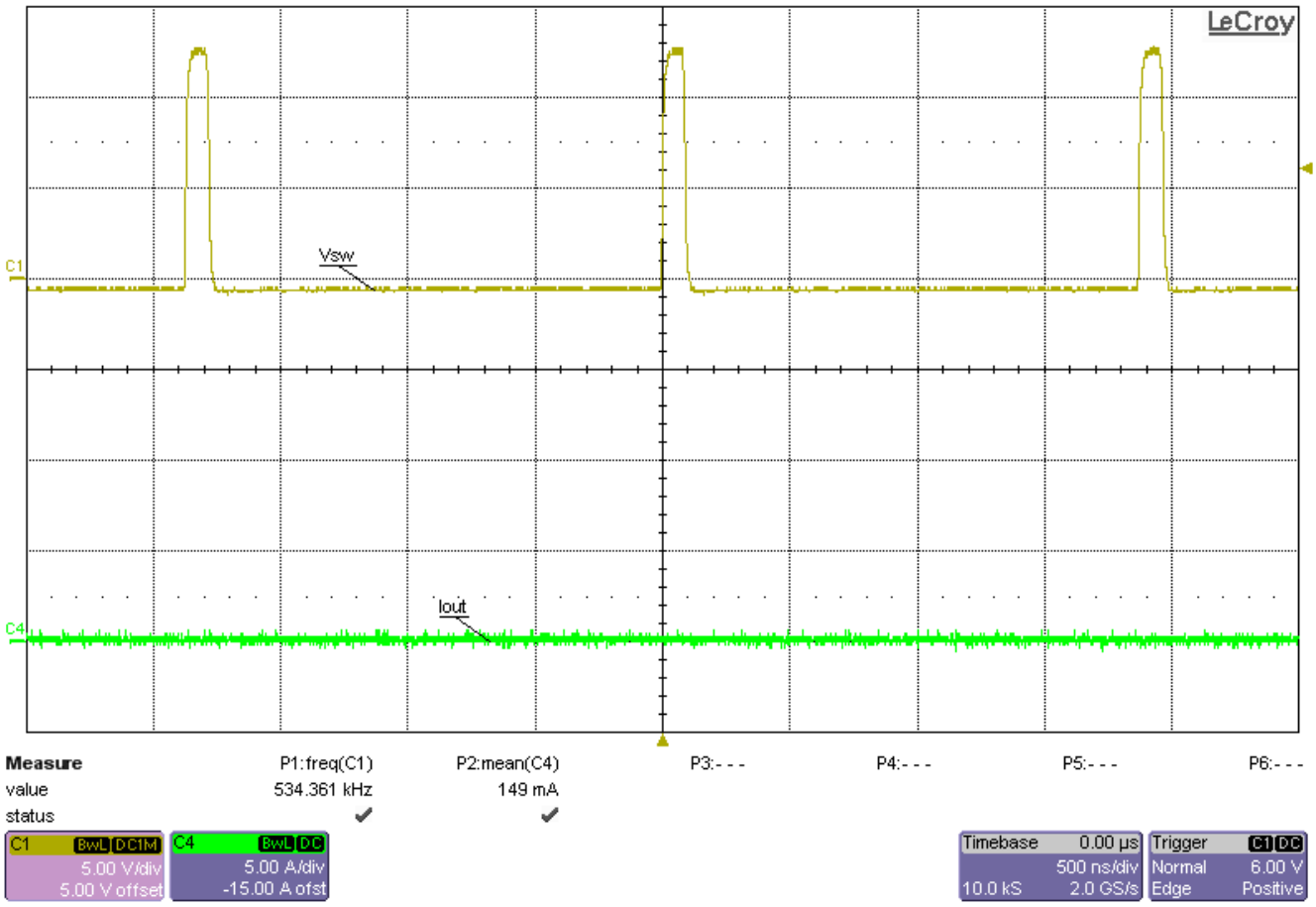


Figure 3-3. Switch Node Voltage, 12-V Input, –0.6-V Output, No Load

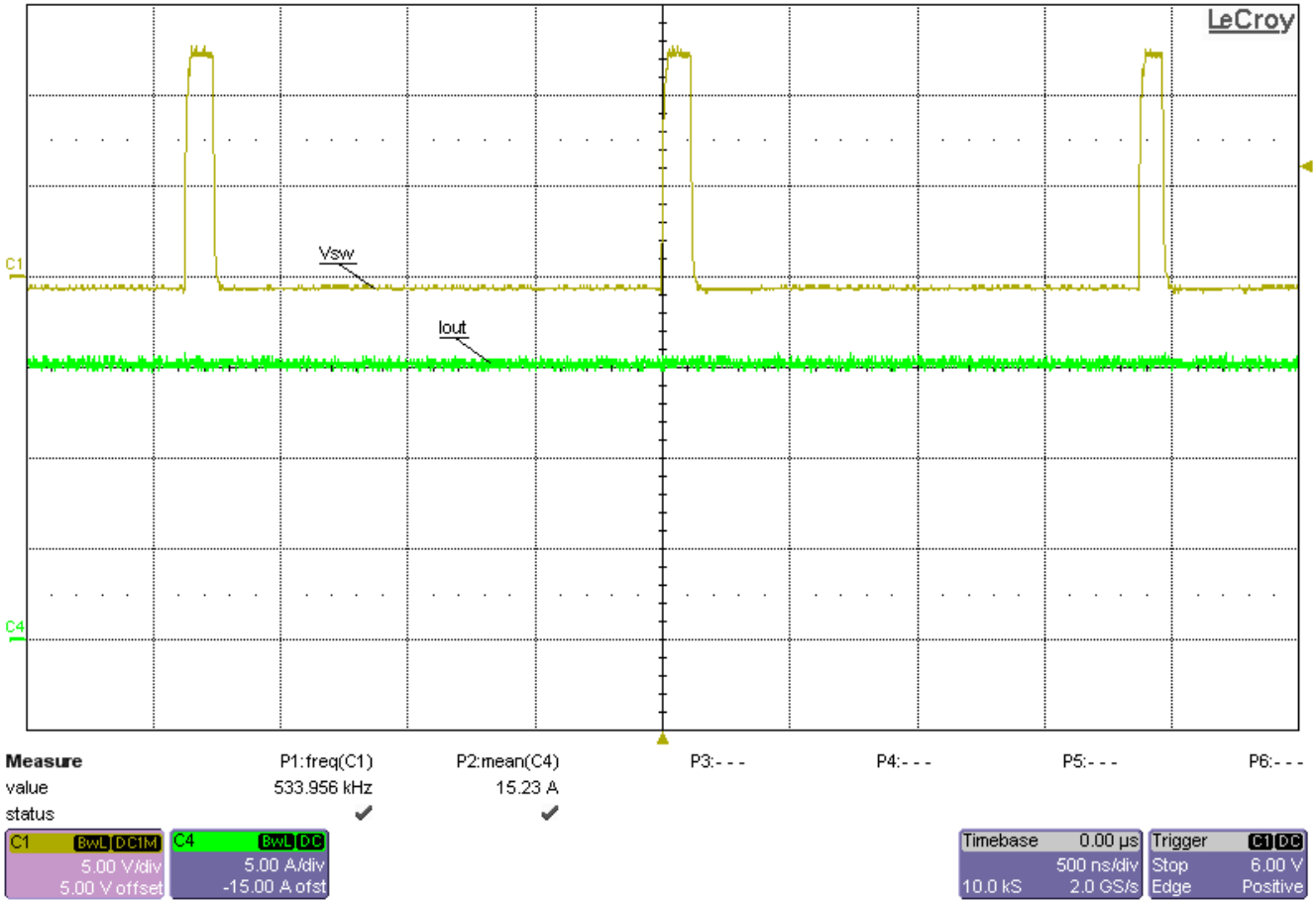


Figure 3-4. Switch Node Voltage, 12-V Input, –0.6-V Output, 15-A Load

3.2 Output Voltage Ripple

Figure 3-5 to Figure 3-8 show the output voltage ripple. The images are taken at 12-V input, –0.2-V and –0.6-V outputs both at no load and 15-A load conditions. The waveforms were captured with infinite persistence being enabled and measurements were made for the peak-to-peak, mean, and RMS values of the output voltage ripple.

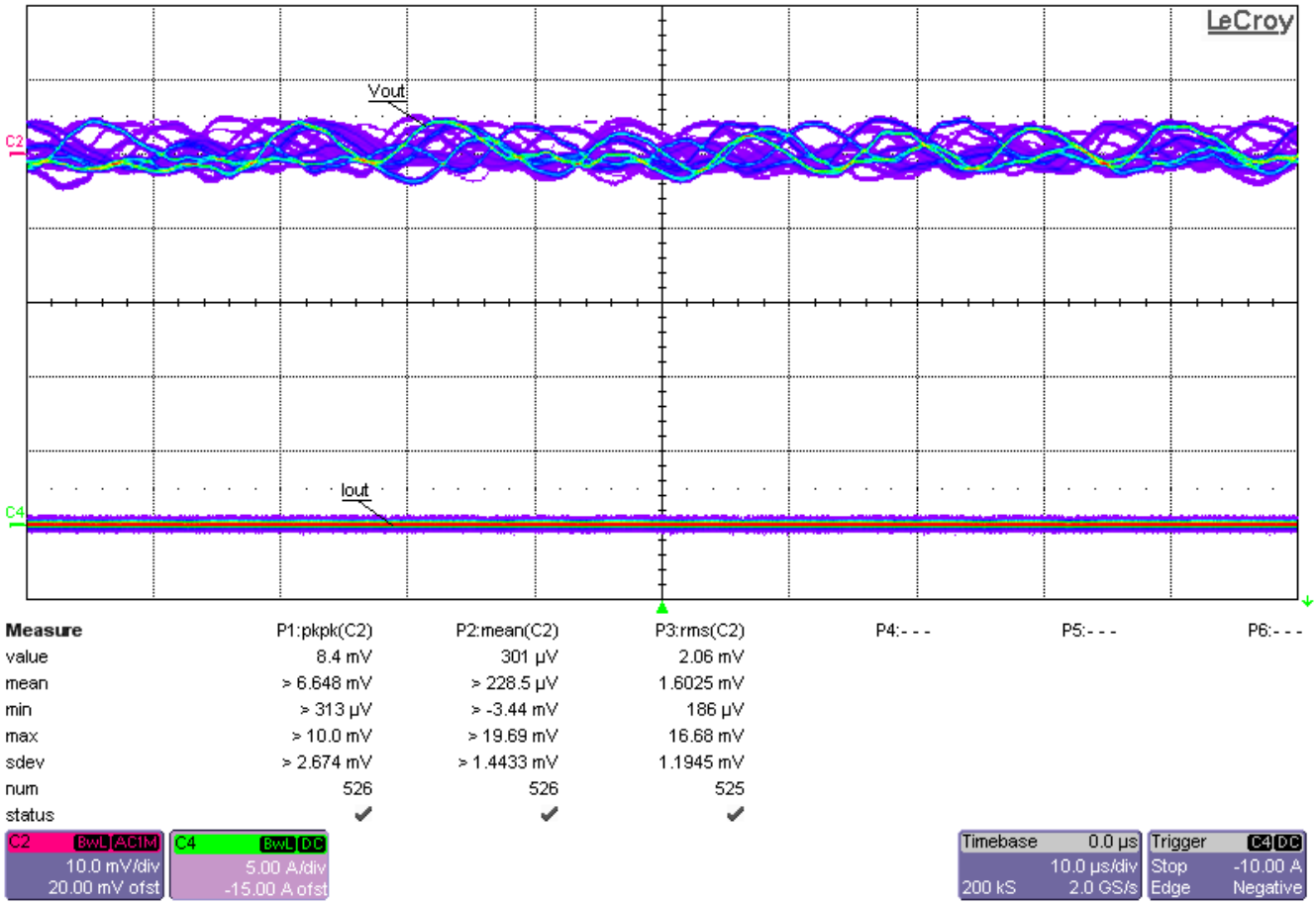


Figure 3-5. Output Voltage Ripple, 12-V Input, –0.2-V Output, No Load

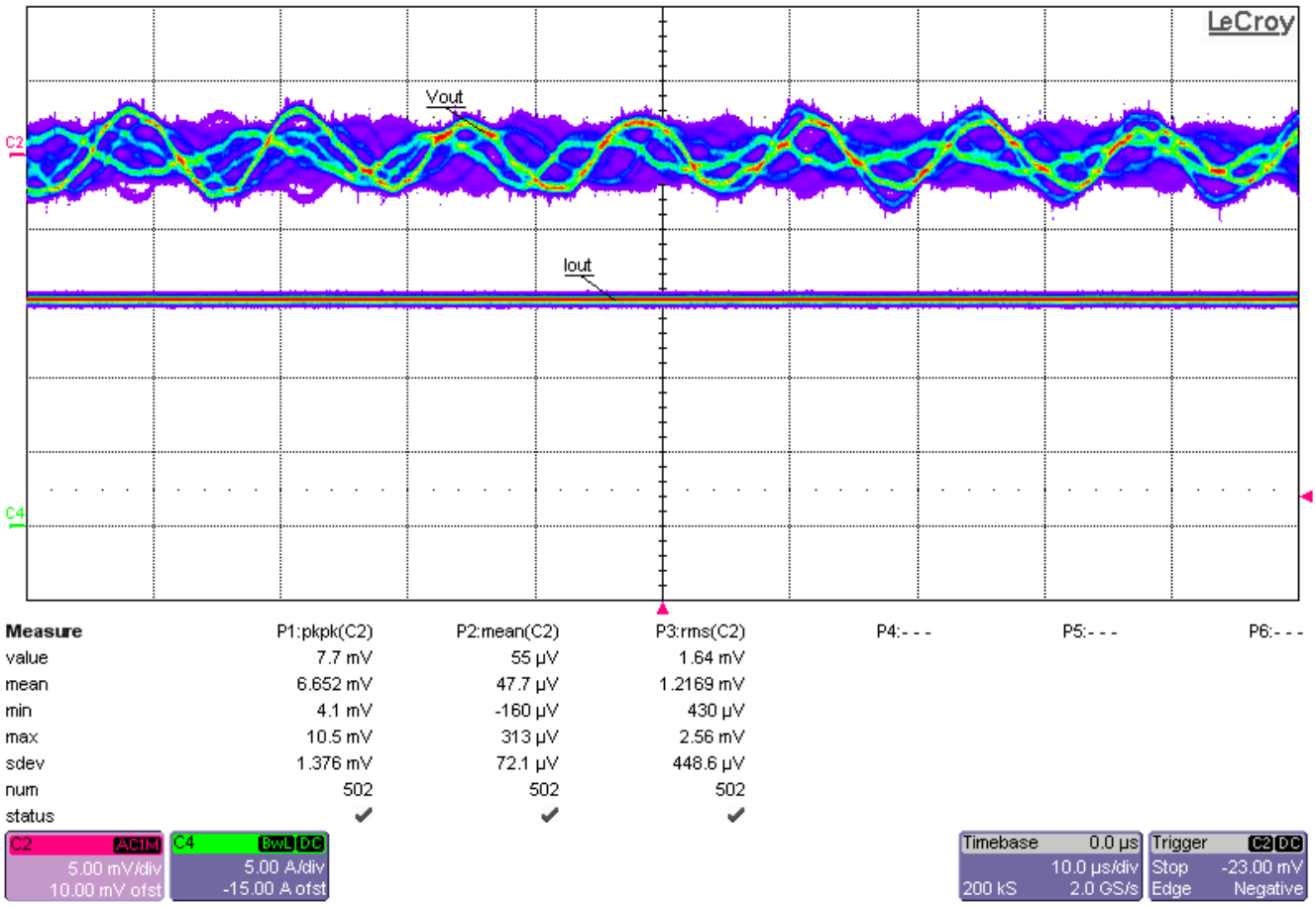


Figure 3-6. Output Voltage Ripple, 12-V Input, –0.2-V Output, 15-A Load

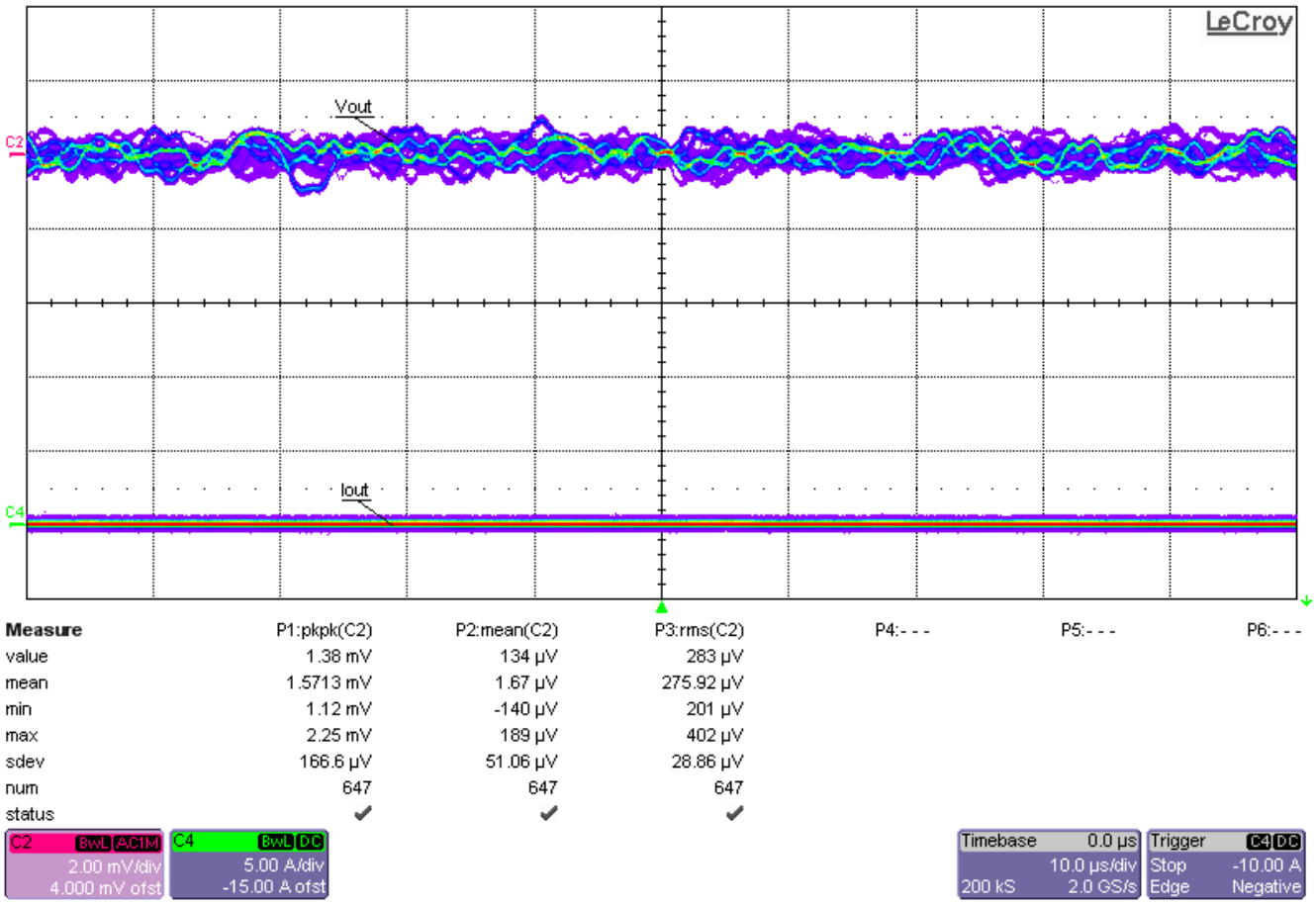


Figure 3-7. Output Voltage Ripple, 12-V Input, –0.6-V Output, No Load

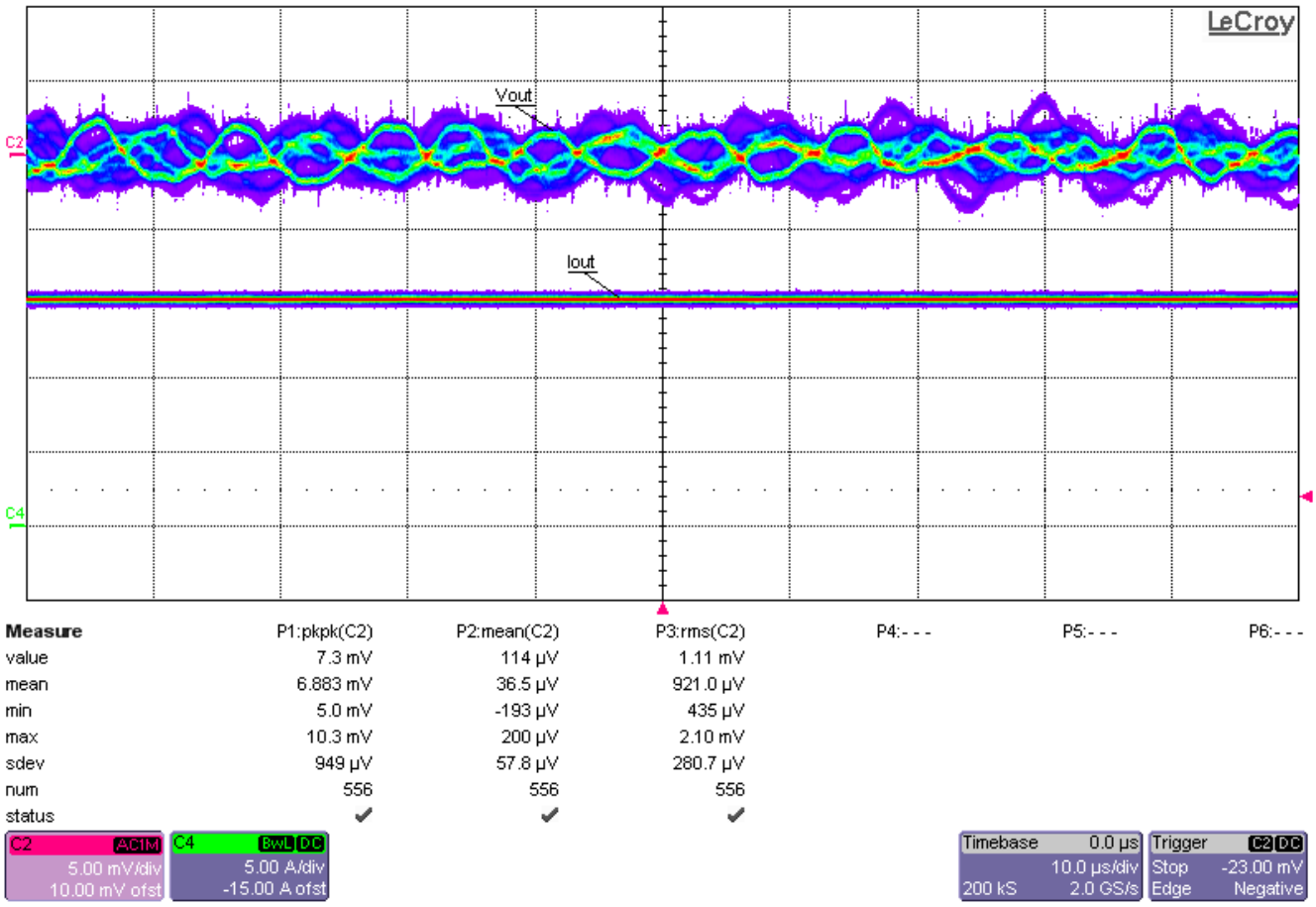


Figure 3-8. Output Voltage Ripple, 12-V Input, –0.6-V Output, 15-A Load

3.3 Load Transients

Figure 3-9 and Figure 3-10 show the load transient response of the converter at 12-V input and –0.2-V and –0.6-V outputs. The load is stepped from 50% to 100% of the load, corresponding to a 7.5-A to 15-A step.

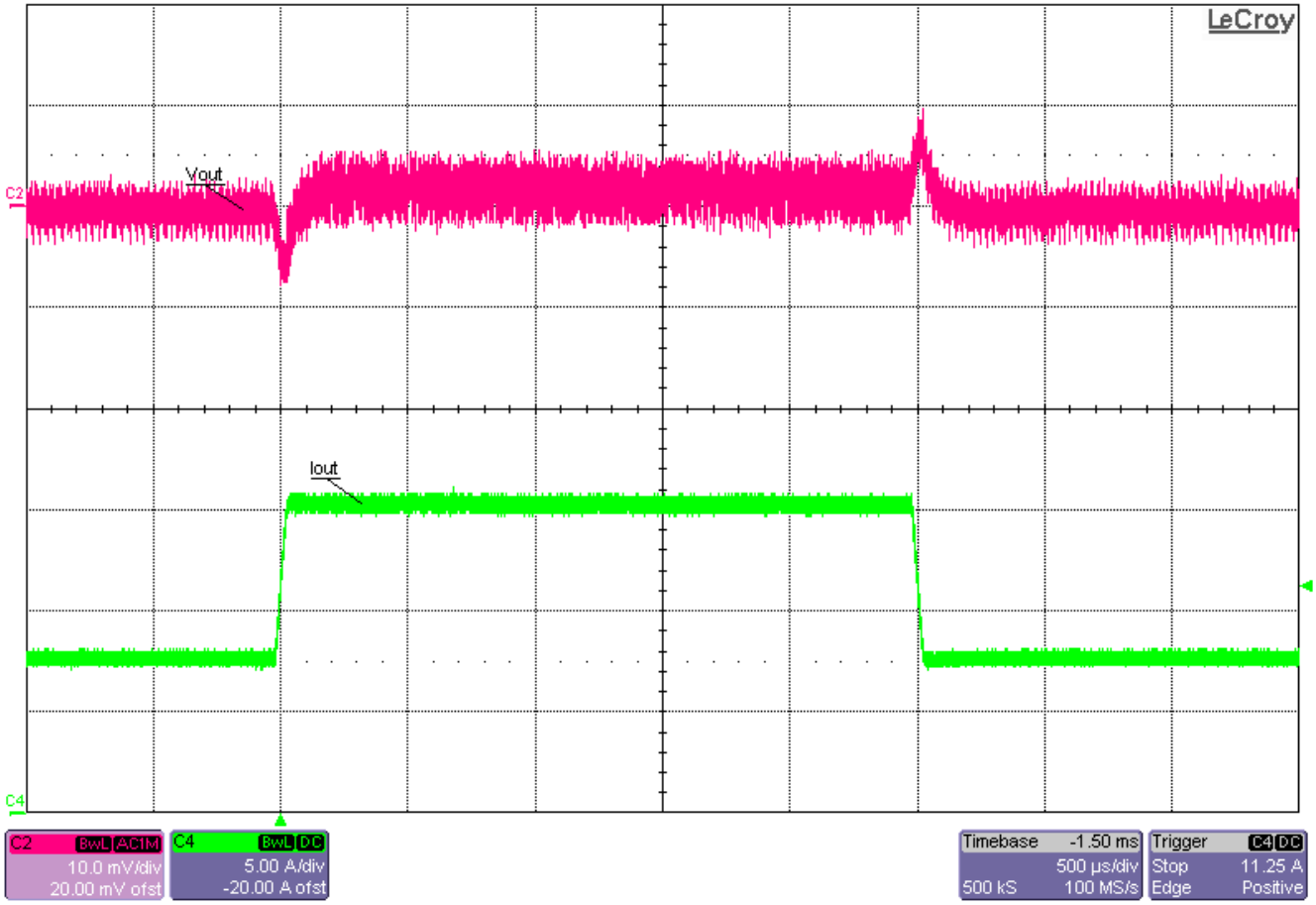


Figure 3-9. Load Transient Response, 12-V Input, –0.2-V Output, 7.5-A to 15-A Load Step

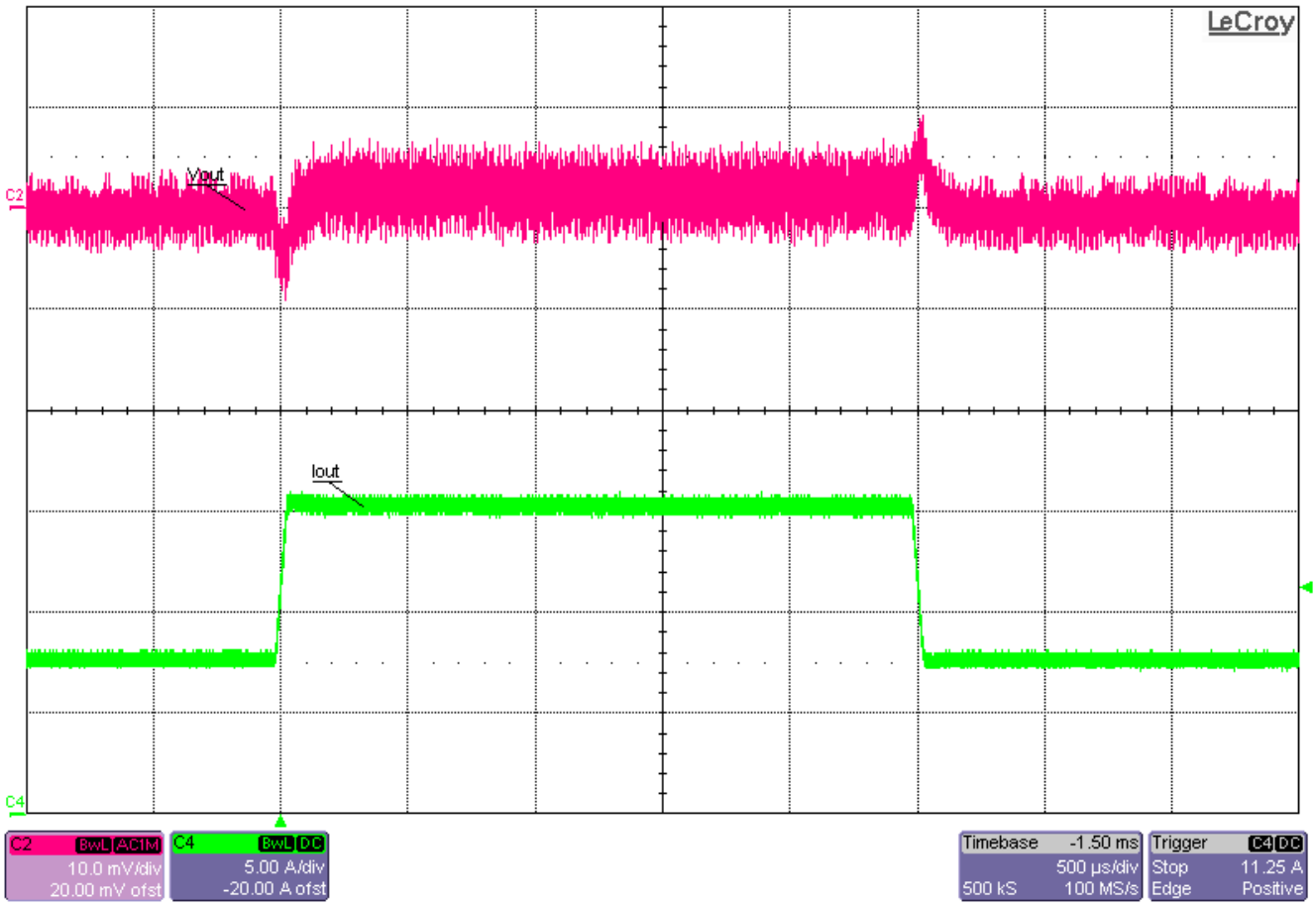


Figure 3-10. Load Transient Response, 12-V Input, –0.6-V Output, 7.5-A to 15-A Load Step

3.4 Start-up Sequence

Figure 3-11 to Figure 3-18 show the output voltage start-up waveforms at 12-V input and –0.2-V and –0.6-V output with the converter starting up into no load and into 15-A constant-current load using the electronic load. It can be seen that just before start-up, the output voltage actually reaches approximately +0.25 V. This is due to the bias currents passing through the regulator IC and onward through the clamping Schottky diode, D1. If this diode was not placed there, then the bias current would have passed through the body diode of the low-side FET of the regulator and generated an even higher voltage at the $-V_{OUT}$ connection. This inherent behavior is due to the inverting buck-boost topology and how the IC GND is actually floating initially, before regulation ensues. The two methods of enabling the converter have been captured: one where the input voltage is turned ON and the converter waits for the Enable signal to go HIGH; the other where the Enable signal is already set HIGH and the converter waits for the main power supply to be turned ON.

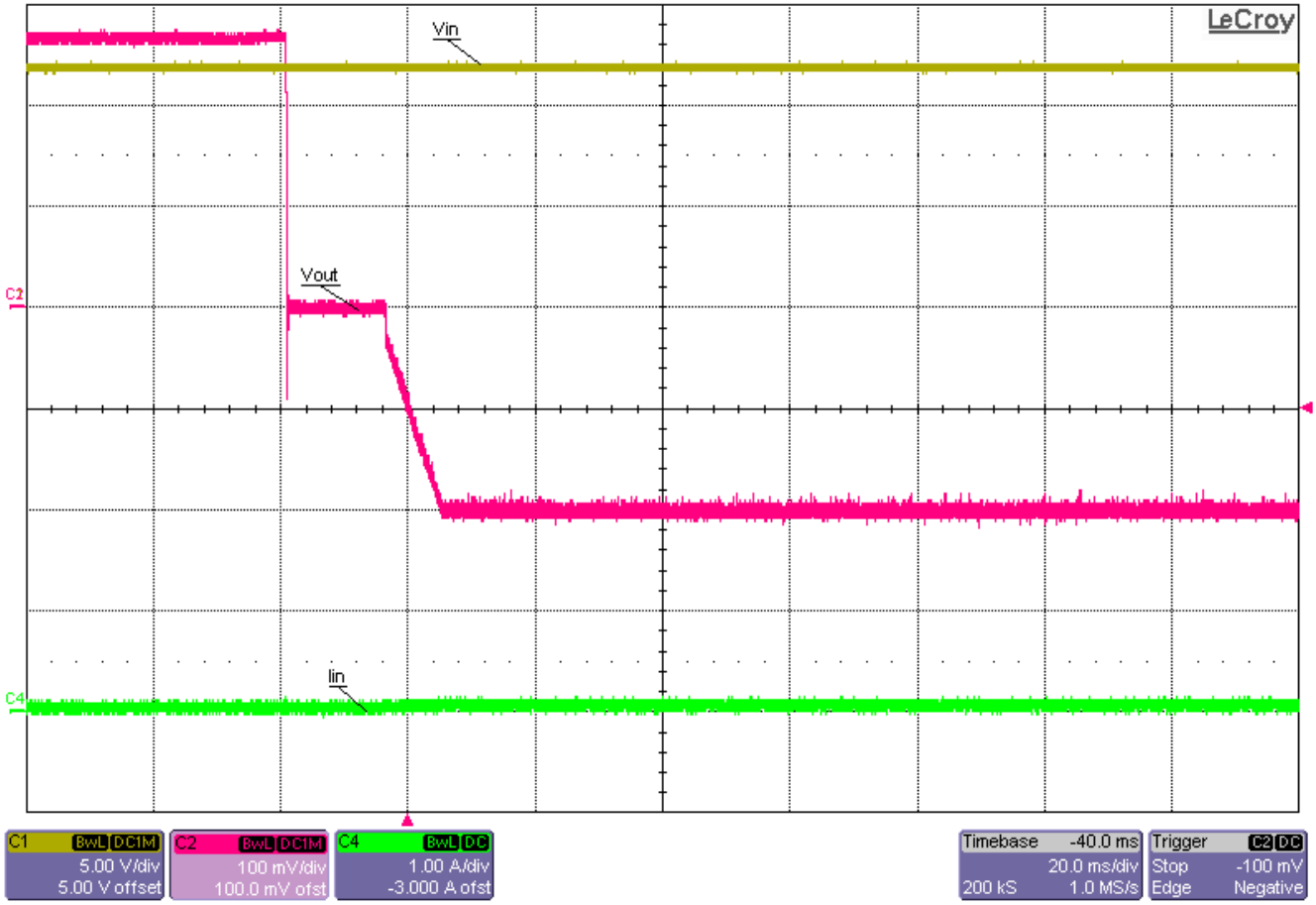


Figure 3-11. Start-up Into No Load, 12-V Input, –0.2-V Output, Start-up Initiated via the Enable Connection (Input Supply Already Turned ON)

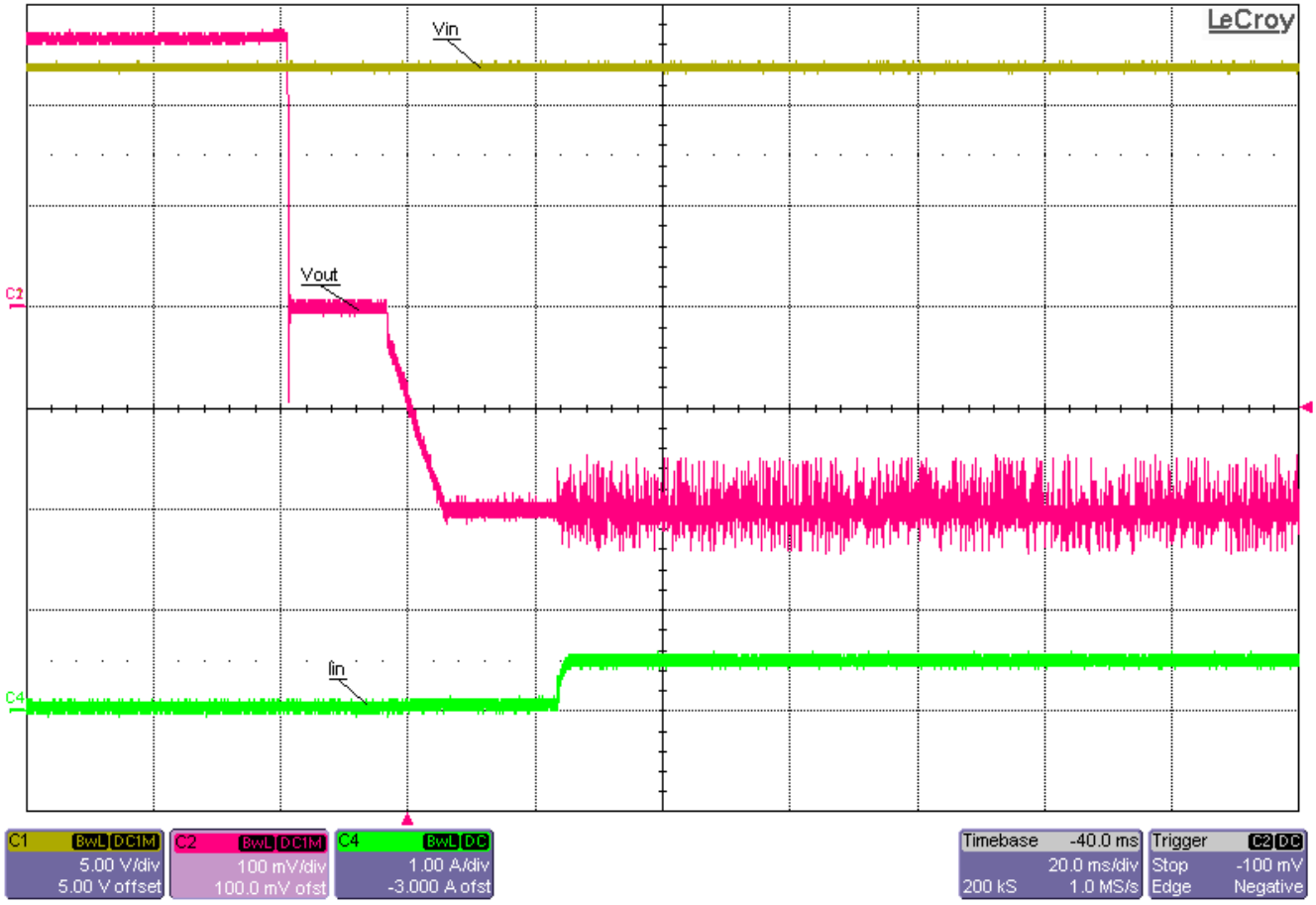


Figure 3-12. Start-up Into 15-A Constant-Current Load, 12-V Input, –0.2-V Output Start-up Initiated via the Enable Connection (Input Supply Already Turned ON)

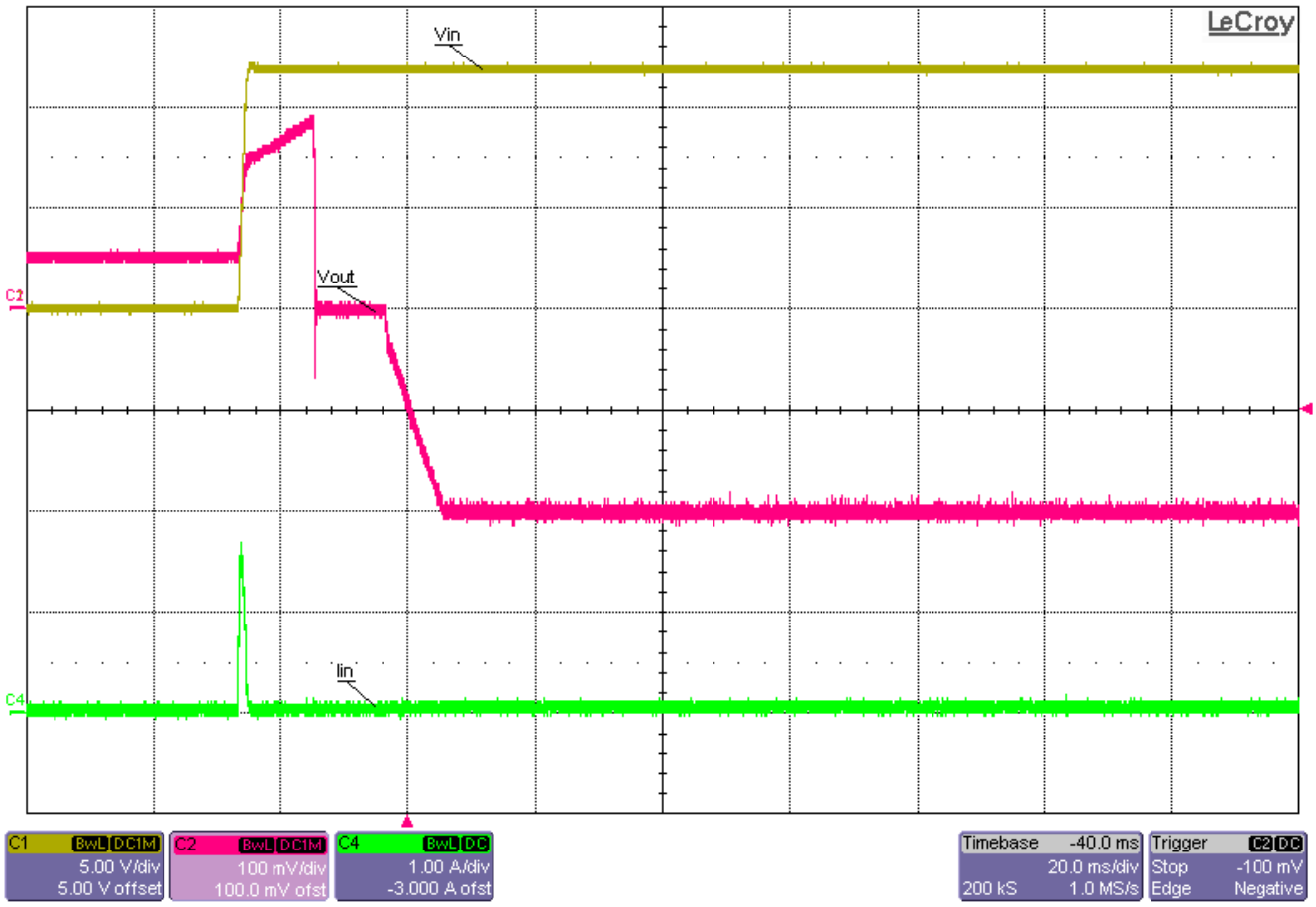


Figure 3-13. Start-up Into No Load, 12-V Input, –0.2-V Output, Start-up Initiated via Input Supply (Enable Signal Already Set High)

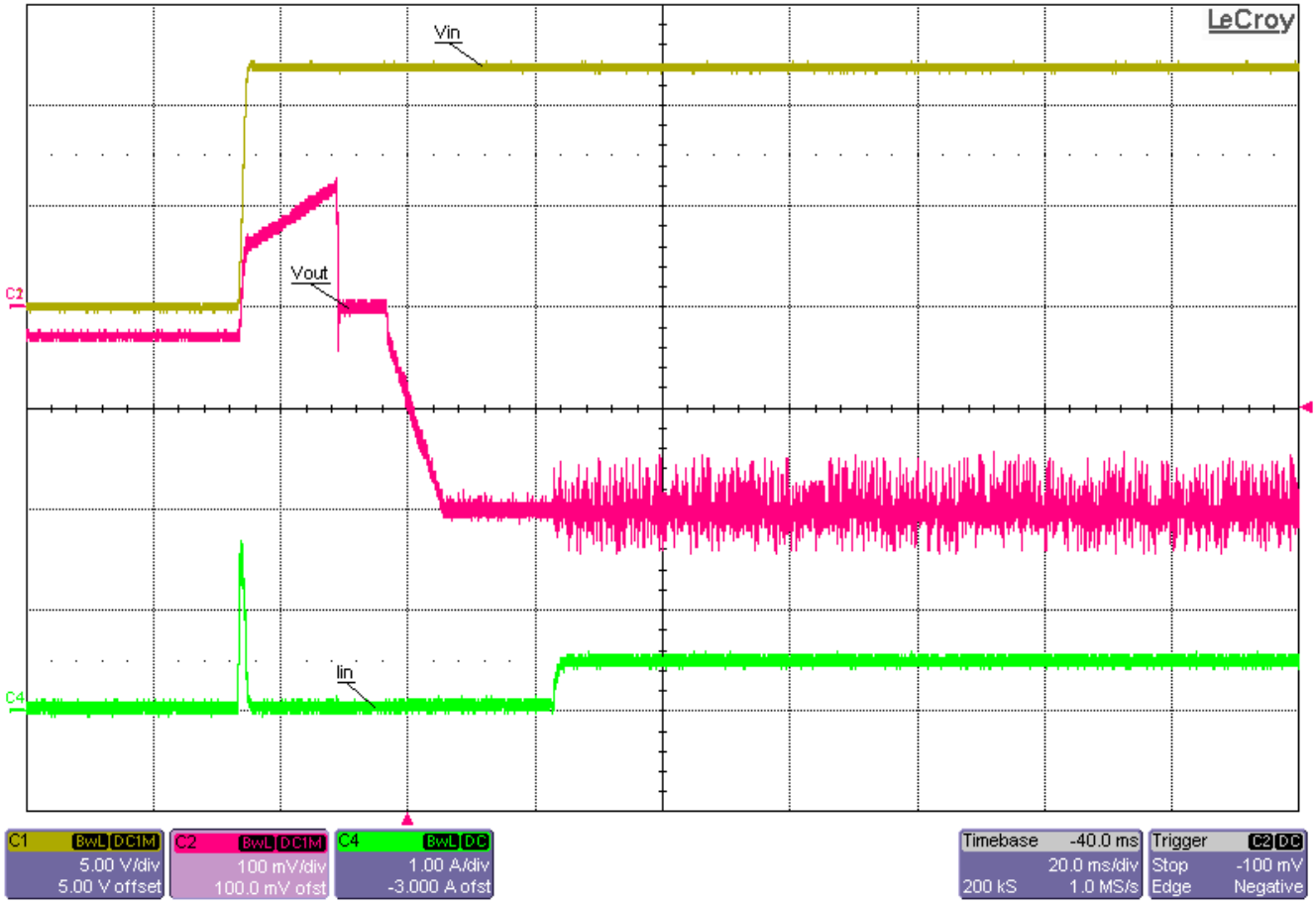


Figure 3-14. Start-up Into 15-A Constant-Current Load, 12-V Input, –0.2-V Output, Start-up Initiated via Input Supply (Enable Signal Already Set High)

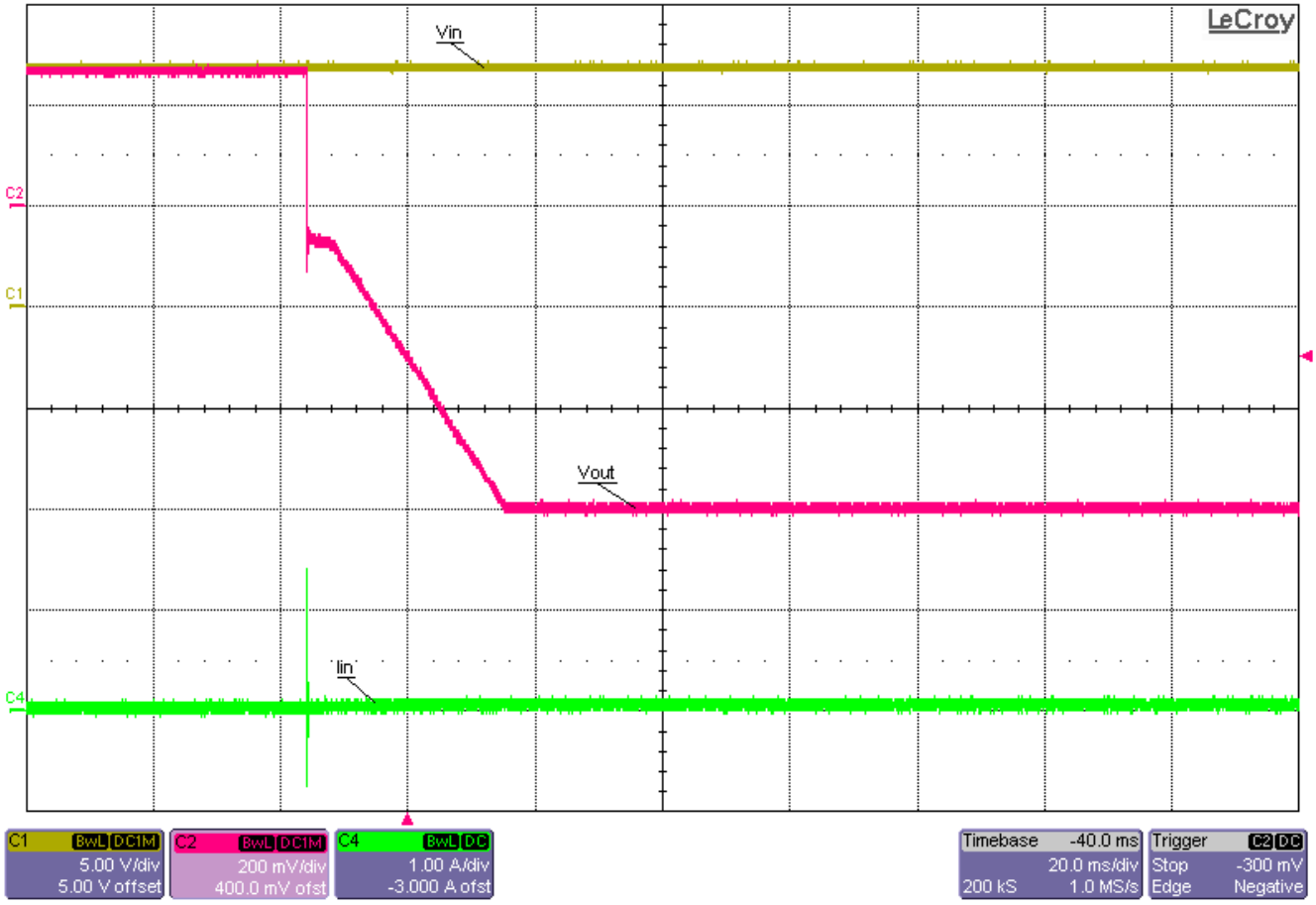


Figure 3-15. Start-up Into No Load, 12-V Input, –0.6-V Output, Start-up Initiated via the Enable Connection (Input Supply Already Turned ON)

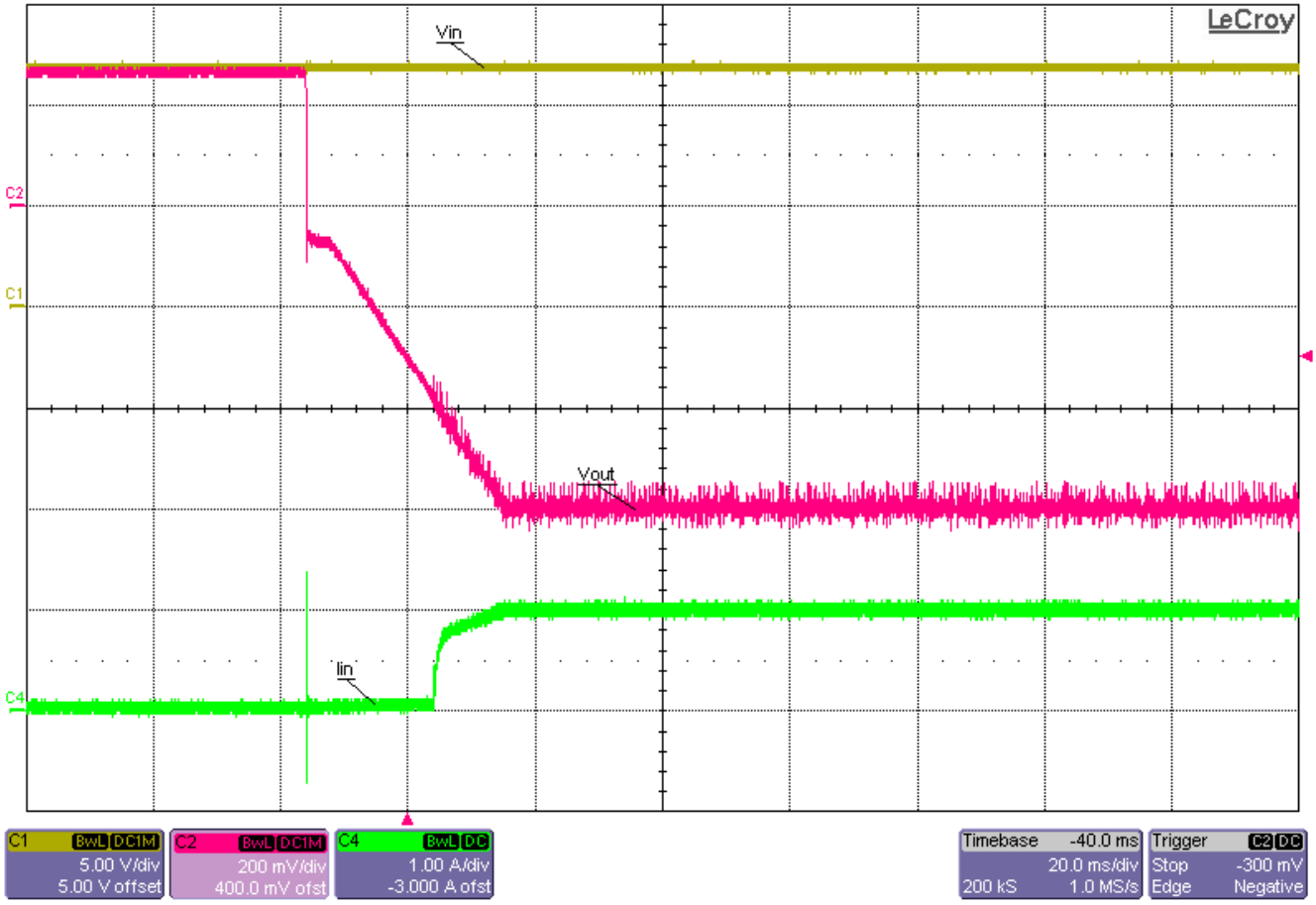


Figure 3-16. Start-up Into 15-A Constant-Current Load, 12-V Input, –0.6-V Output, Start-up Initiated via the Enable Connection (Input Supply Already Turned ON)

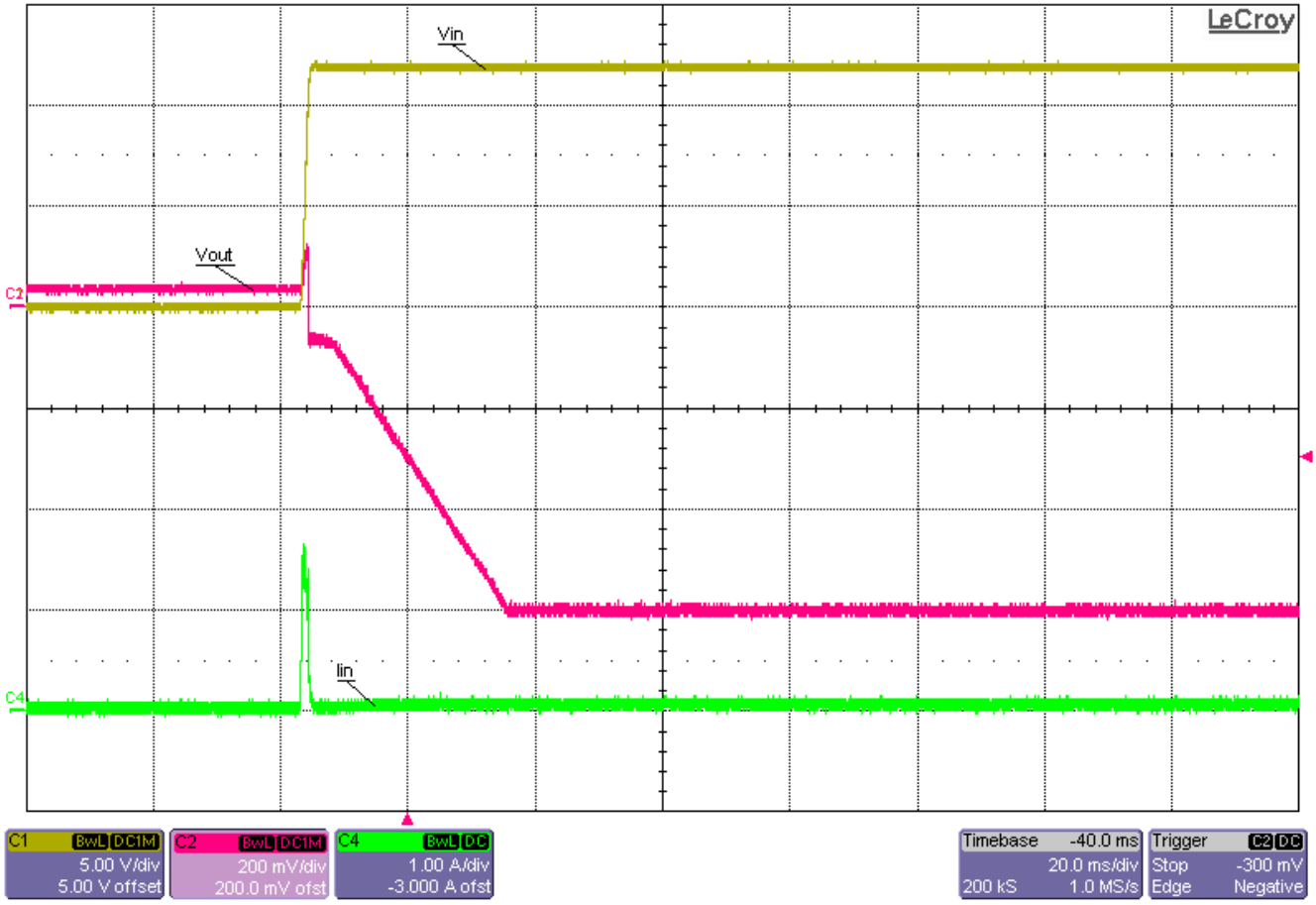


Figure 3-17. Start-up Into No Load, 12-V Input, –0.6-V Output, Start-up Initiated via Input Supply (Enable Signal Already Set High)

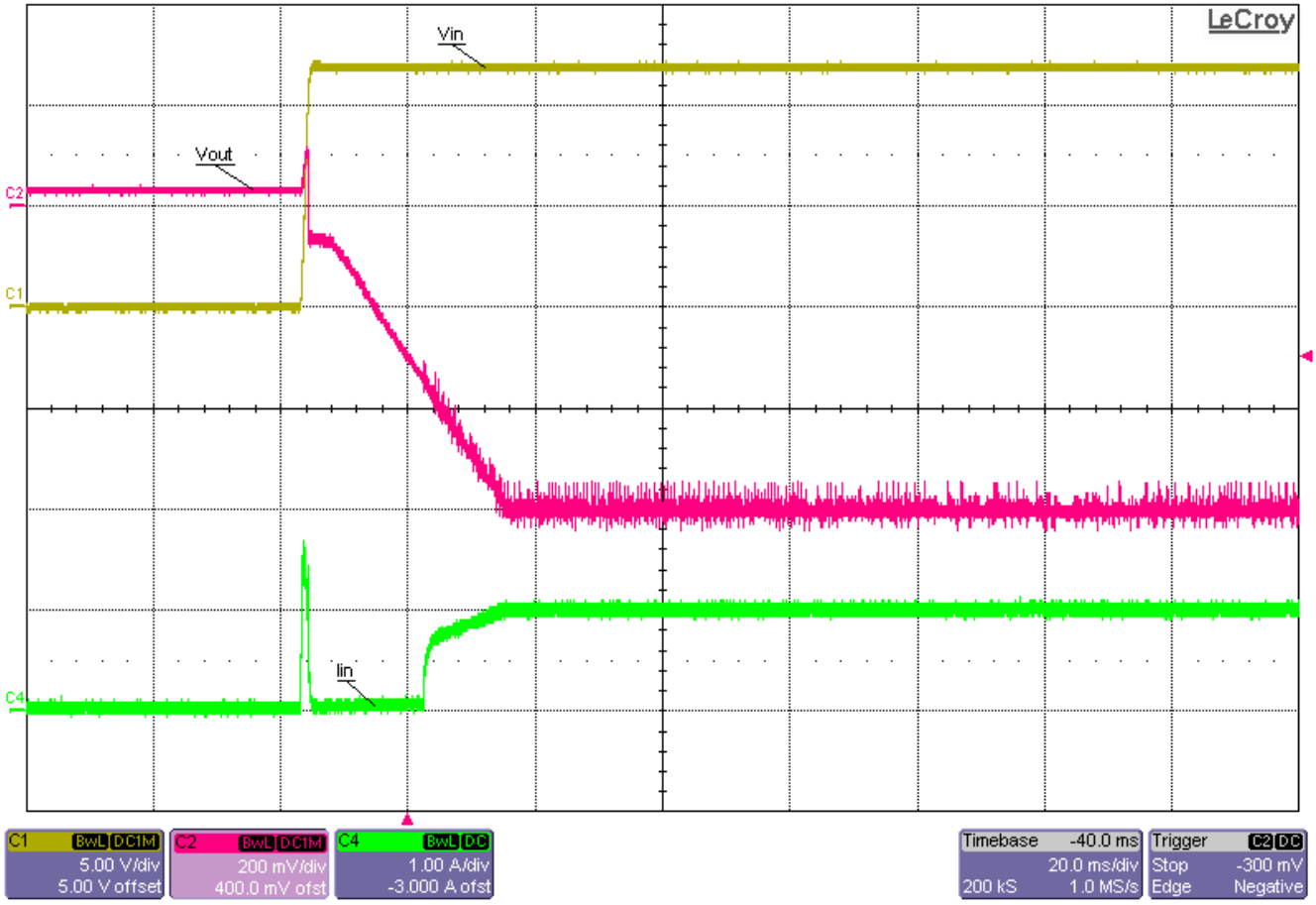


Figure 3-18. Start-up Into 15-A Constant-Current Load, 12-V Input, –0.6-V Output, Start-up Initiated via Input Supply (Enable Signal Already Set High)

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