Test Report: PMP22487

High-Voltage Buck Converter Reference Design for BMS Applications

Description

This non-isolated buck converter provides a fixed output of 14V at 130mA for BMS applications. It operates over an input voltage range of 18Vdc – 144Vdc after a startup greater than 23V. Operating in Discontinuous Conduction Mode (DCM), this converter utilizes the UCC28730 controller, which is referenced to the switch node. It offers high efficiency and low cost in a compact form factor.

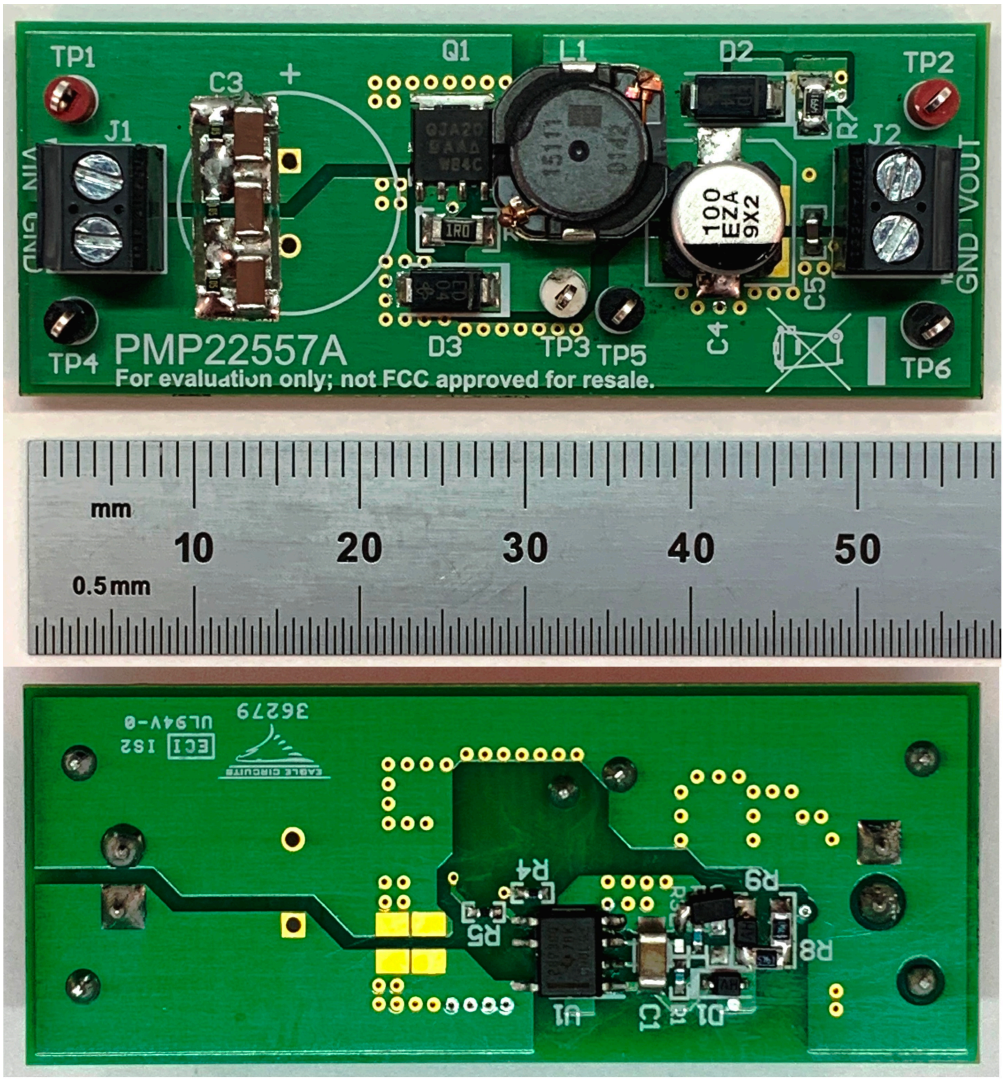

Figure 1-1. This figure shows the top of the board on the top, and the bottom of the board on the bottom.

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input voltage range	18 V–144 V, after > 23-V startup
Output voltage and current	14 V ±1 V, 130 mA maximum
Switching frequency	Variable, 83 KHz maximum
Isolation	No
Controller features	Valley switching, frequency dithering, 700-V startup switch, overcurrent and overvoltage protection

1.2 Required Equipment

- Resistive load (resistor decade box), 2 W minimum
- Power supply, adjustable, 0 V–150 V and 0.25 A minimum
- Oscilloscope and probes
- Digital multimeter

2 Testing and Results

2.1 Thermal Images

This thermal image shows the operating temperature of the **top** side of the board with 100 V_{DC} input and 14 V at 130-mA output at room temperature and no air flow.

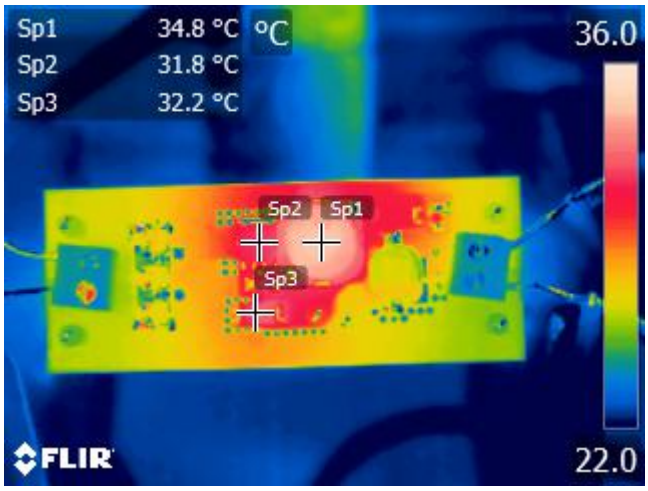

Figure 2-1. Top-Side Thermal Image, 100-V_{DC} Input, 14 V at 130-mA Output

This thermal image shows the operating temperature of the **bottom** side of the board with 100-V_{DC} input and 14 V at 130-mA output at room temperature and no air flow.

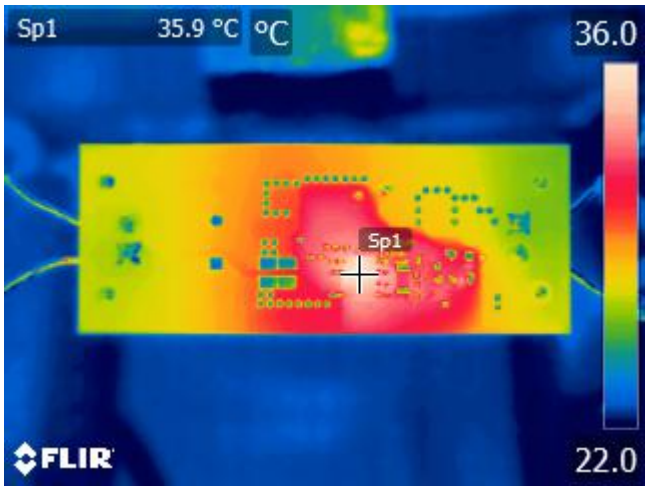

Figure 2-2. Bottom-Side Thermal Image, 100 V_{DC} Input, 14 V at 130-mA Output

This thermal image shows the operating temperature of the **top** side of the board with 30-V_{DC} input and 14 V at 130-mA output at room temperature and no air flow.

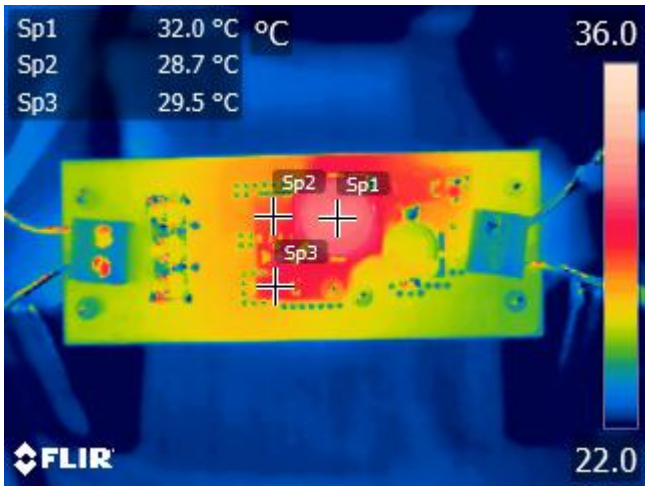

Figure 2-3. Top-Side Thermal Image, 30-V_{DC} Input, 14 V at 130-mA Output

This thermal image shows the operating temperature of the **bottom** side of the board with 30-V_{DC} input and 14 V at 130-mA output at room temperature and no air flow.

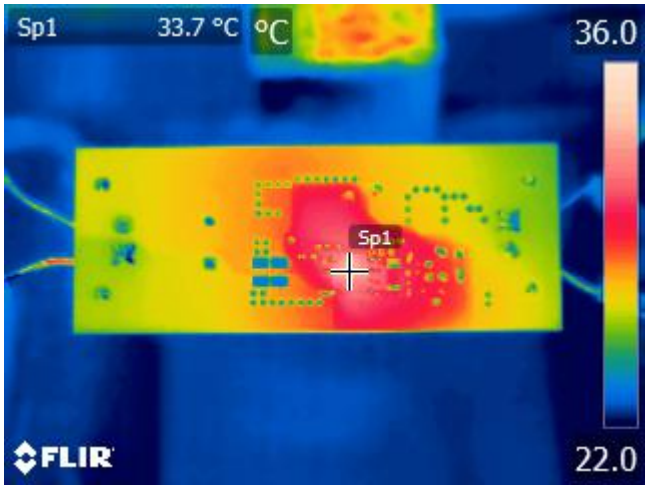

Figure 2-4. Bottom-Side Thermal Image, 30 V_{DC} Input, 14 V at 130-mA Output

2.2 Efficiency and Power Dissipation graphs

The following figure displays the efficiency and power dissipation of the converter at input voltages of 30 V_{DC}, 60 V_{DC}, 90 V_{DC} and 120 V_{DC}.

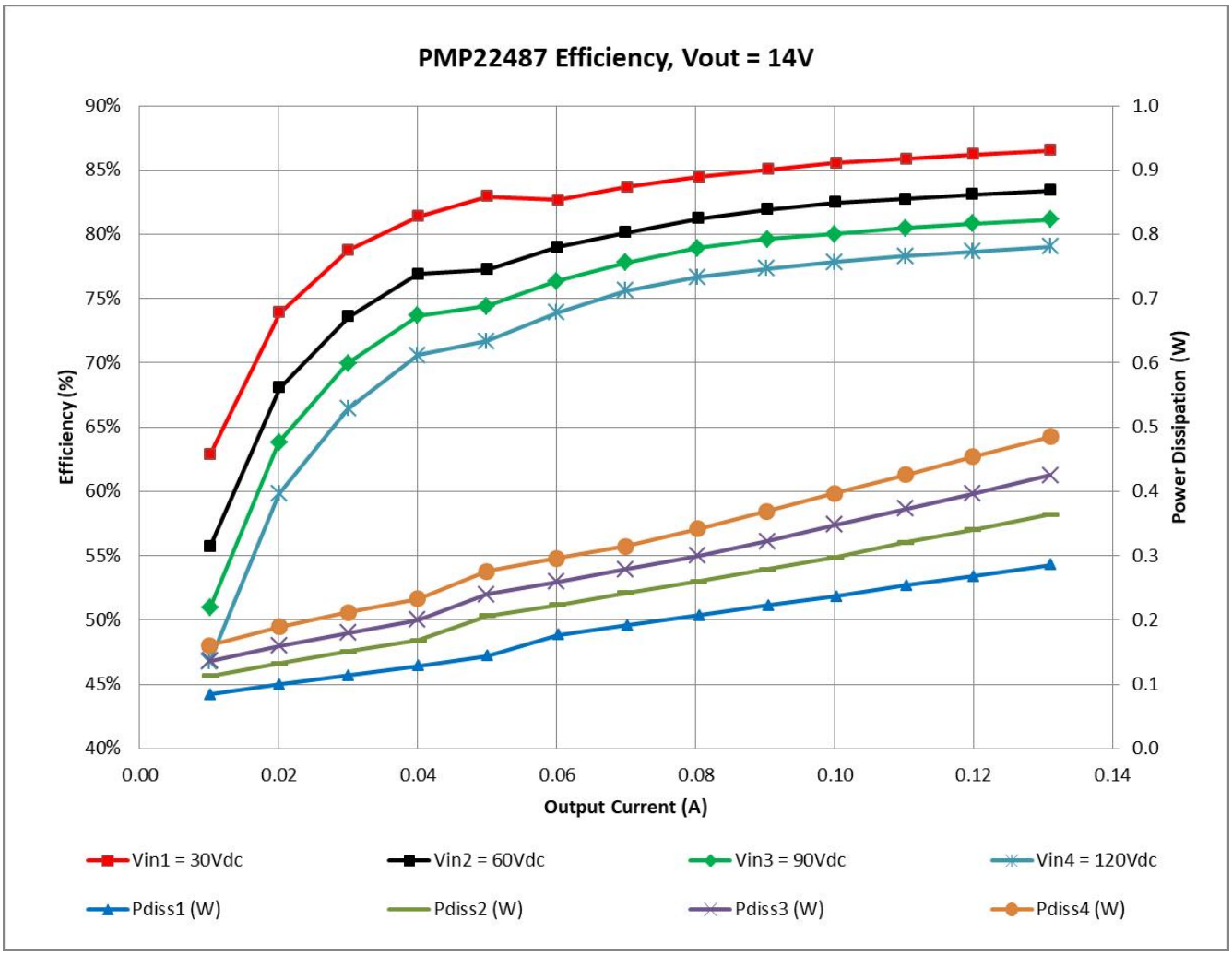

Figure 2-5. PMP22487 Efficiency, V_{OUT} = 14 V

2.3 Efficiency and Power Dissipation Data

Efficiency data is shown in the following table.

PMP22487 REVC						Efficiency (%)	Power Dissipation (W)
Vin	Iin	Vout	Iout	Pout	Pin	Vin1 = 30Vdc	Pdiss1 (W)
30.4600	0.0074	14.071	0.010110	0.142	0.226	62.9%	0.084
30.0970	0.0127	14.040	0.020110	0.282	0.382	73.9%	0.100
30.0870	0.0178	14.022	0.030060	0.422	0.535	78.8%	0.113
30.0290	0.0230	14.008	0.040080	0.561	0.690	81.4%	0.128
30.0190	0.0281	14.001	0.050000	0.700	0.844	82.9%	0.144
30.0570	0.0340	14.010	0.060200	0.843	1.020	82.7%	0.177
30.0470	0.0390	14.006	0.070100	0.982	1.173	83.7%	0.191
30.0367	0.0444	13.995	0.080500	1.127	1.334	84.5%	0.207
30.0269	0.0495	13.990	0.090400	1.265	1.487	85.0%	0.223
30.1160	0.0544	13.981	0.100200	1.401	1.638	85.5%	0.237
30.1060	0.0597	13.982	0.110300	1.542	1.796	85.9%	0.254
30.0480	0.0647	13.976	0.119900	1.676	1.944	86.2%	0.268
30.0370	0.0705	13.977	0.131100	1.832	2.118	86.5%	0.286
Vin	Iin	Vout	Iout	Pout	Pin	Vin2 = 60Vdc	Pdiss2 (W)
60.0800	0.0042	14.049	0.010100	0.142	0.255	55.7%	0.113
60.0270	0.0069	14.018	0.020080	0.281	0.414	68.1%	0.132
60.1270	0.0095	14.001	0.030020	0.420	0.571	73.6%	0.151
60.0170	0.0121	13.987	0.040020	0.560	0.728	76.9%	0.168
60.1650	0.0151	13.988	0.050000	0.699	0.905	77.2%	0.206
60.1120	0.0177	13.976	0.060100	0.840	1.063	79.0%	0.223
60.1070	0.0203	13.976	0.069900	0.977	1.219	80.1%	0.242
60.0440	0.0230	13.968	0.080400	1.123	1.383	81.2%	0.260
60.0970	0.0256	13.972	0.090300	1.262	1.540	81.9%	0.279
60.0340	0.0282	13.965	0.100100	1.398	1.695	82.5%	0.297
60.1350	0.0309	13.971	0.110200	1.540	1.861	82.7%	0.321
60.0820	0.0335	13.966	0.119800	1.673	2.013	83.1%	0.340
60.0180	0.0366	13.978	0.131100	1.833	2.197	83.4%	0.364

Figure 2-6. Efficiency data for Vin =30V, 60V

PMP22487 REVC						Efficiency (%)	Power Dissipation (W)
Vin	Iin	Vout	Iout1	Pout	Pin	Vin3 = 90Vdc	Pdiss3 (W)
90.1040	0.0031	14.026	0.010080	0.141	0.278	50.9%	0.136
90.1000	0.0049	14.014	0.020070	0.281	0.441	63.8%	0.159
90.0970	0.0067	13.995	0.030000	0.420	0.600	70.0%	0.180
90.0940	0.0084	13.982	0.040010	0.559	0.759	73.7%	0.200
90.0400	0.0104	13.977	0.049900	0.697	0.937	74.4%	0.240
90.1890	0.0122	13.967	0.060000	0.838	1.098	76.4%	0.260
90.0840	0.0139	13.968	0.069900	0.976	1.255	77.8%	0.279
90.0300	0.0158	13.962	0.080300	1.121	1.421	78.9%	0.300
90.0270	0.0176	13.967	0.090300	1.261	1.584	79.6%	0.322
90.0730	0.0194	13.962	0.100000	1.396	1.744	80.0%	0.348
90.0200	0.0212	13.968	0.110200	1.539	1.912	80.5%	0.373
90.1140	0.0230	13.964	0.119800	1.673	2.069	80.9%	0.396
90.0120	0.0251	13.976	0.131000	1.831	2.256	81.2%	0.425
Vin	Iin	Vout	Iout1	Pout	Pin	Vin4 = 120Vdc	Pdiss4 (W)
120.1880	0.0025	14.010	0.010070	0.141	0.302	46.8%	0.161
120.1860	0.0039	14.008	0.020060	0.281	0.470	59.8%	0.189
120.0850	0.0053	13.990	0.029990	0.420	0.632	66.4%	0.212
120.0820	0.0066	13.981	0.040010	0.559	0.793	70.6%	0.233
120.0800	0.0081	13.972	0.049900	0.697	0.973	71.7%	0.275
120.0770	0.0094	13.965	0.060000	0.838	1.134	73.9%	0.296
120.0750	0.0108	13.963	0.069900	0.976	1.291	75.6%	0.315
120.0720	0.0122	13.961	0.080300	1.121	1.462	76.7%	0.341
120.0170	0.0136	13.963	0.090200	1.259	1.629	77.3%	0.369
120.0140	0.0149	13.962	0.100000	1.396	1.794	77.8%	0.397
120.0640	0.0164	13.964	0.110200	1.539	1.965	78.3%	0.426
120.0610	0.0177	13.964	0.119800	1.673	2.127	78.7%	0.454
120.1070	0.0193	13.972	0.131000	1.830	2.316	79.0%	0.485

Figure 2-7. Efficiency data for Vin =90V, 120V

2.4 Voltage Regulation

The following graph displays the measured output voltage at input voltages of 18 V_{DC} and 144 V_{DC}.

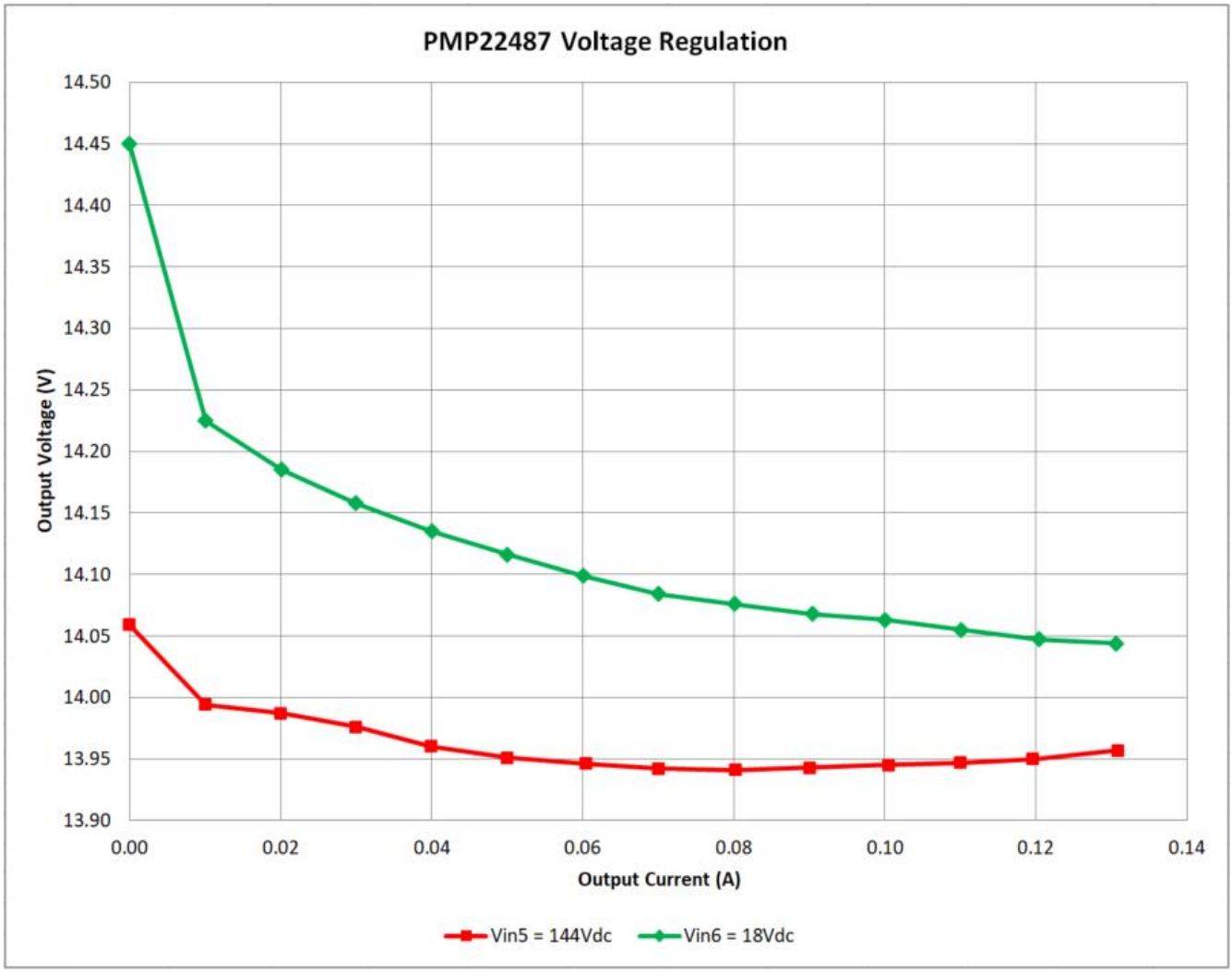

Figure 2-8. PMP22487 Voltage Regulation

3 Waveforms

3.1 Start-up

The following figure shows output voltage startup waveform (BLUE) after the application of 30-V input (YELLOW) with the 14-V output loaded to 130 mA.

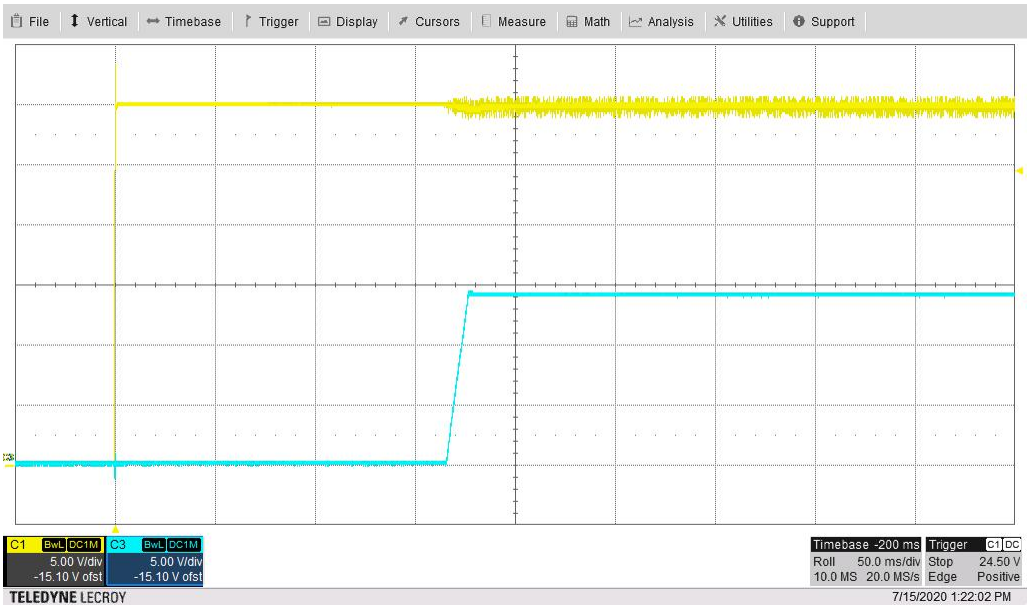

Figure 3-1. Output Voltage Start-up Waveform (V_{IN}: 5 V/div, V_{OUT}: 5 V/div, 50 ms/div)

The following figure shows the output voltage startup waveform (BLUE) after the application of 30-V input (YELLOW) with the 14-V output loaded to 0 mA.

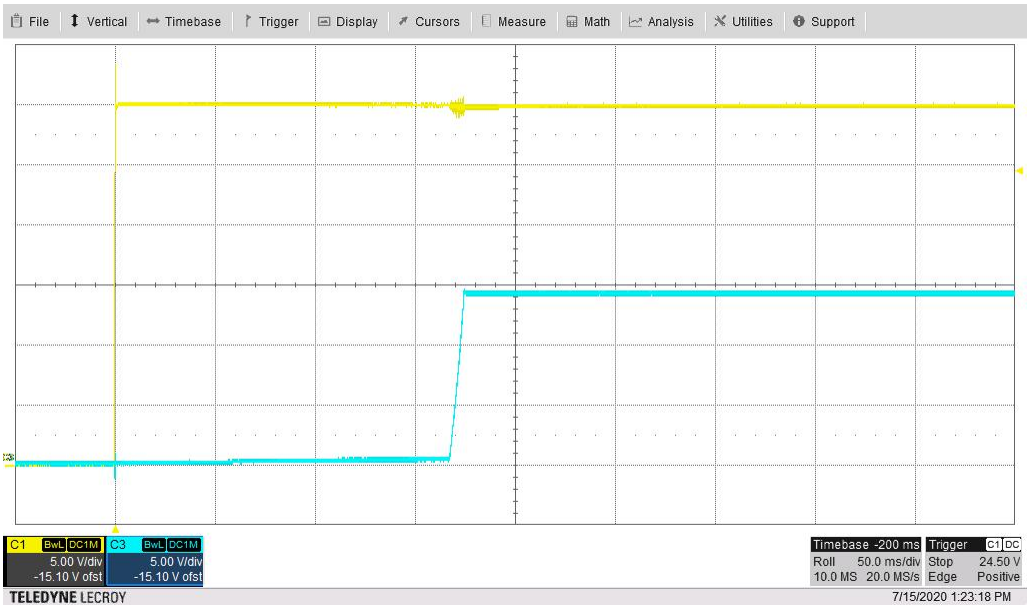

Figure 3-2. Output Voltage Start-up Waveform (V_{IN}: 5 V/div, V_{OUT}: 5 V/div, 50 ms/div)

The following figure shows the output voltage startup waveform (BLUE) after the application of 60-V input (YELLOW) with the 14-V output loaded to 130 mA.

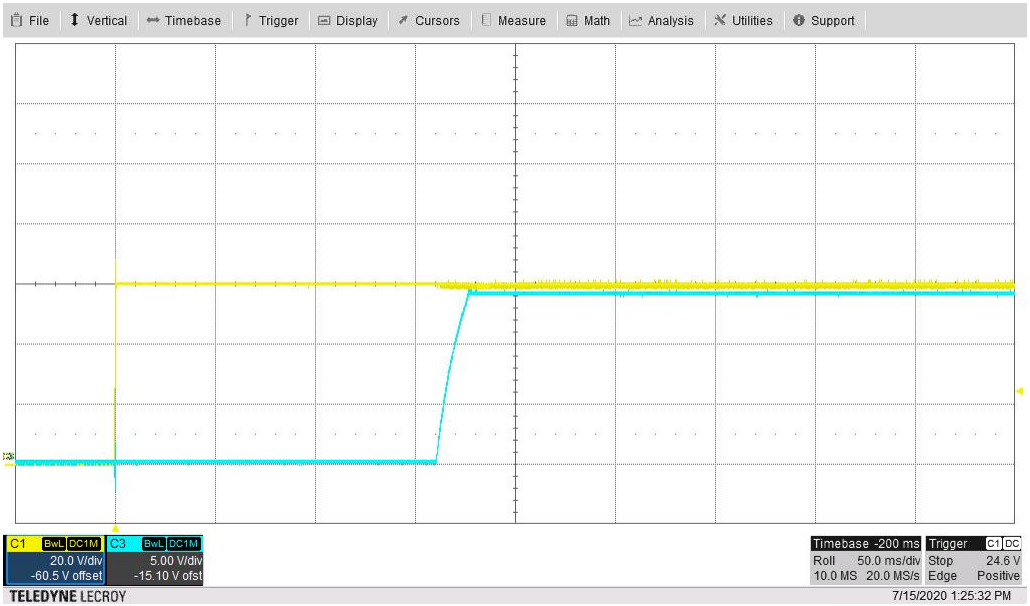

Figure 3-3. Output Voltage Start-up Waveform (V_{IN}: 20 V/div, V_{OUT}: 5 V/div, 50 ms/div)

The following figure shows the output voltage startup waveform (BLUE) after the application of 60-V input (YELLOW) with the 14-V output loaded to 0 mA.

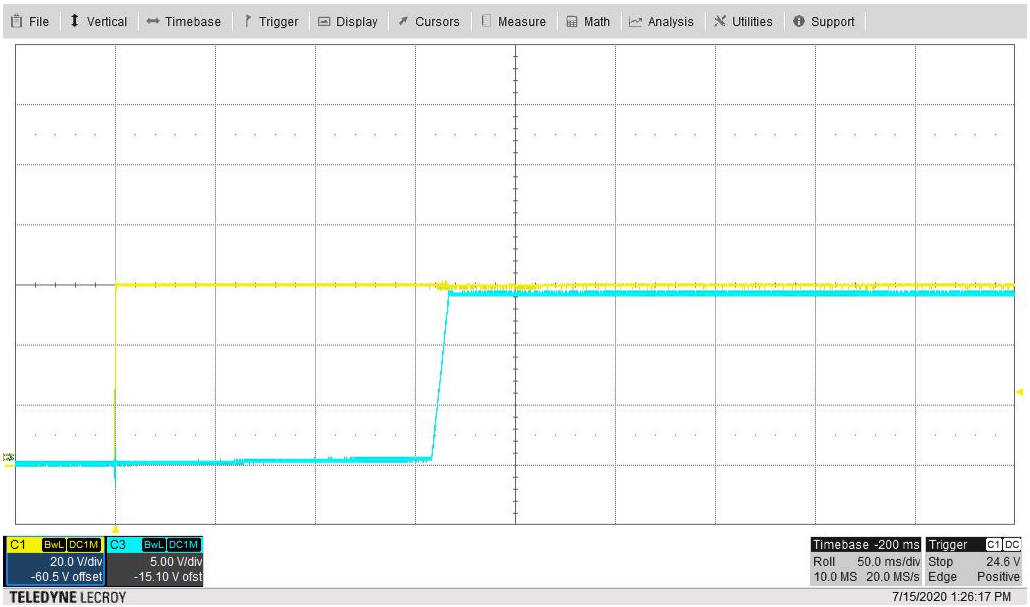

Figure 3-4. Output Voltage Start-up Waveform (V_{IN}: 20 V/div, V_{OUT}: 5 V/div, 50 ms/div)

The following figure shows the output voltage startup waveform (BLUE) after the application of 120-V input (YELLOW) with the 14-V output loaded to 130 mA.

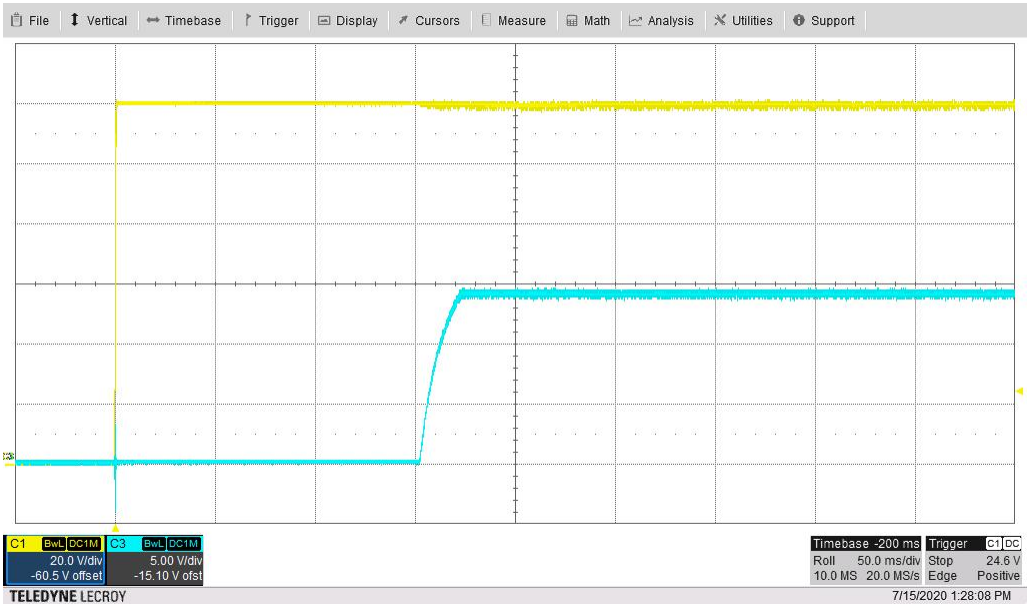

Figure 3-5. Output Voltage Start-up Waveform (V_{IN}: 20 V/div, V_{OUT}: 5 V/div, 50 ms/div)

The following figure shows the output voltage startup waveform (BLUE) after the application of 120-V input (YELLOW) with the 14-V output loaded to 0 mA.

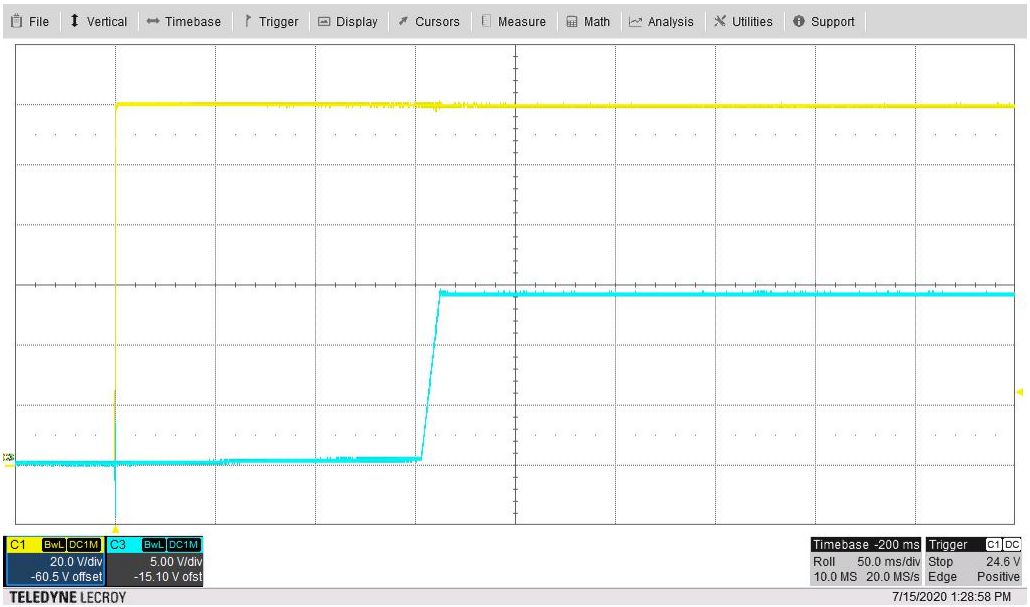

Figure 3-6. Output Voltage Start-up Waveform (V_{IN}: 20 V/div, V_{OUT}: 5 V/div, 50 ms/div)

3.2 Switch Node

The following image shows the FET switch node voltage (YELLOW) at TP3 and the input voltage (BLUE). The input voltage is 18 V and the 14-V output is loaded to 130 mA.

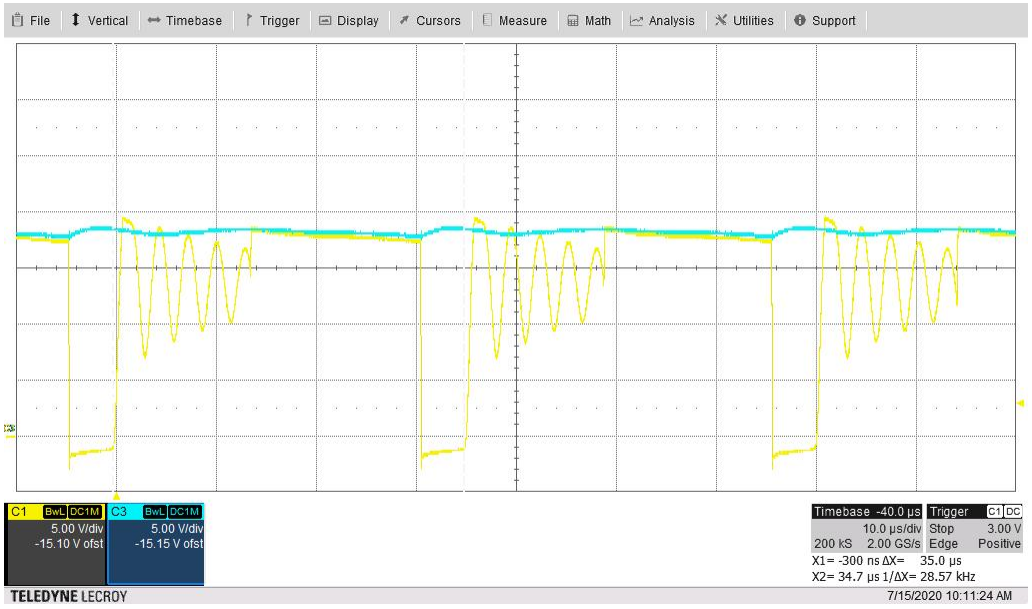

Figure 3-7. FET Switch Node Voltage (Vsnode: 5 V/div, V_{IN}: 5 V/div, 10 µs/div)

The following image (scope persistence on) shows the FET switch node voltage (YELLOW) at TP3 and the input voltage (BLUE). The input voltage is 18 V and the 14-V output is loaded to 130 mA. This shows the effects of valley switching and frequency dithering on the switch node waveform.

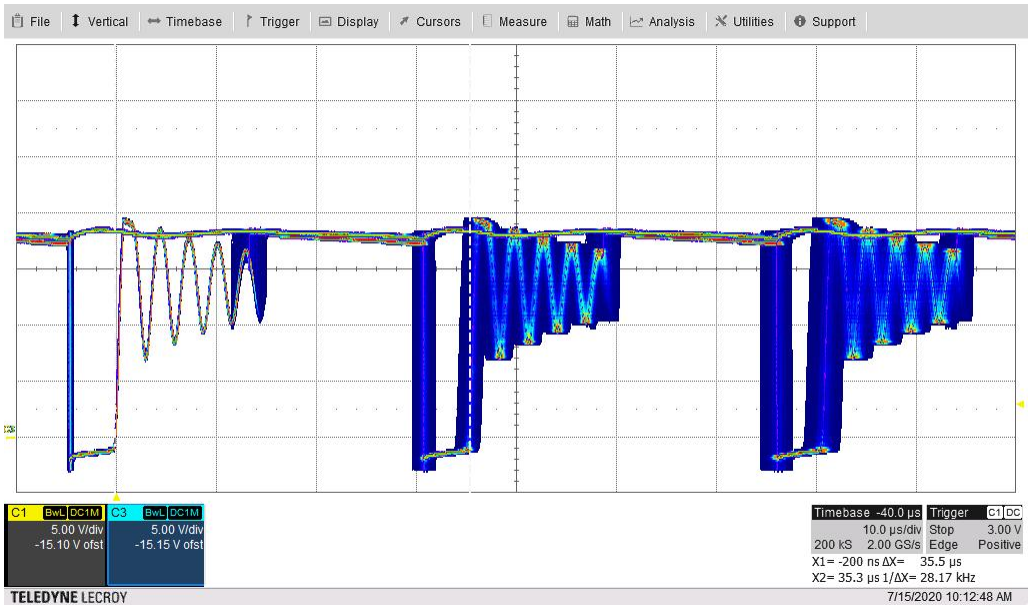

Figure 3-8. FET Switch Node Voltage (Vsnode: 5 V/div, V_{IN}: 5 V/div, 10 µs/div)

The following image shows the FET switch node voltage (YELLOW) at TP3 and the input voltage (BLUE). The input voltage is 18 V and the 14-V output is loaded to 0 mA.

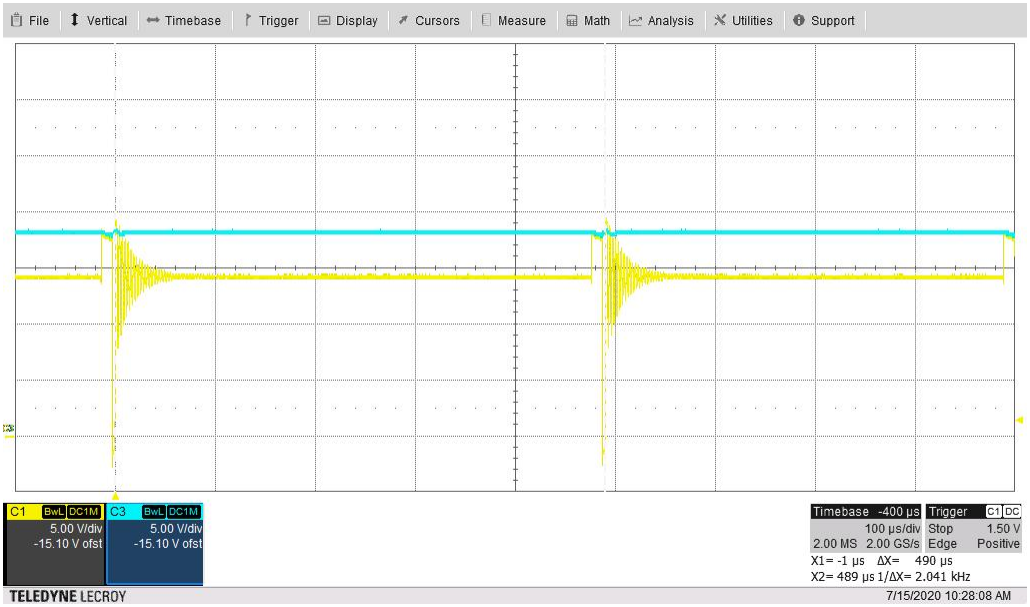

Figure 3-9. FET Switch Node Voltage (Vsnode: 5 V/div, V_{IN}: 5 V/div, 100 µs/div)

The following image shows the FET switch node voltage (YELLOW) at TP3 and the input voltage (BLUE). The input voltage is 80 V and the 14-V output is loaded to 130 mA.

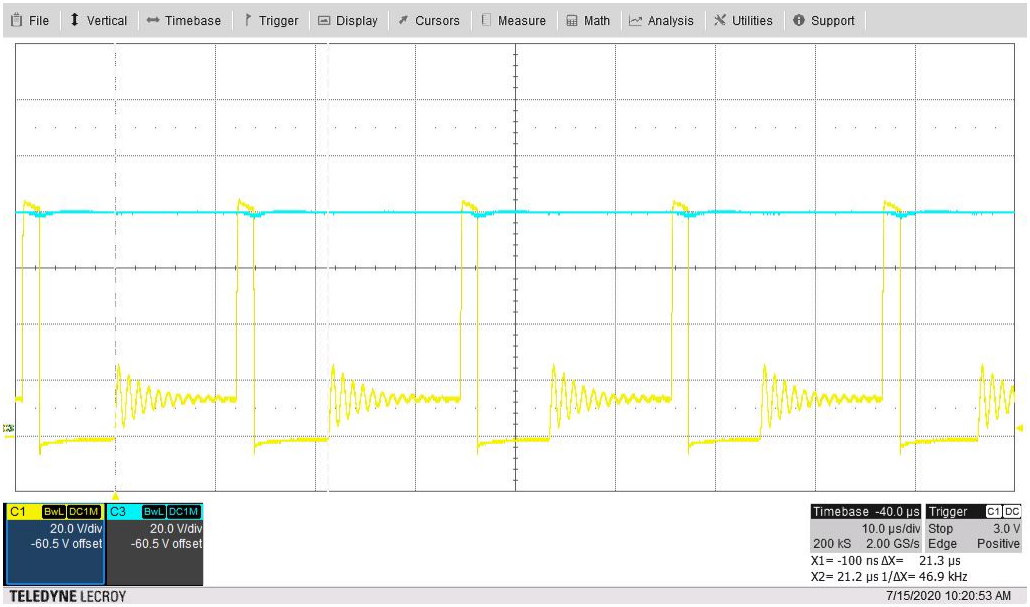

Figure 3-10. FET Switch Node Voltage (Vsnode: 20 V/div, V_{IN}: 20 V/div, 10 µs/div)

The following image shows the FET switch node voltage (YELLOW) at TP3 and the input voltage (BLUE). The input voltage is 80 V and the 14-V output is loaded to 0 mA.

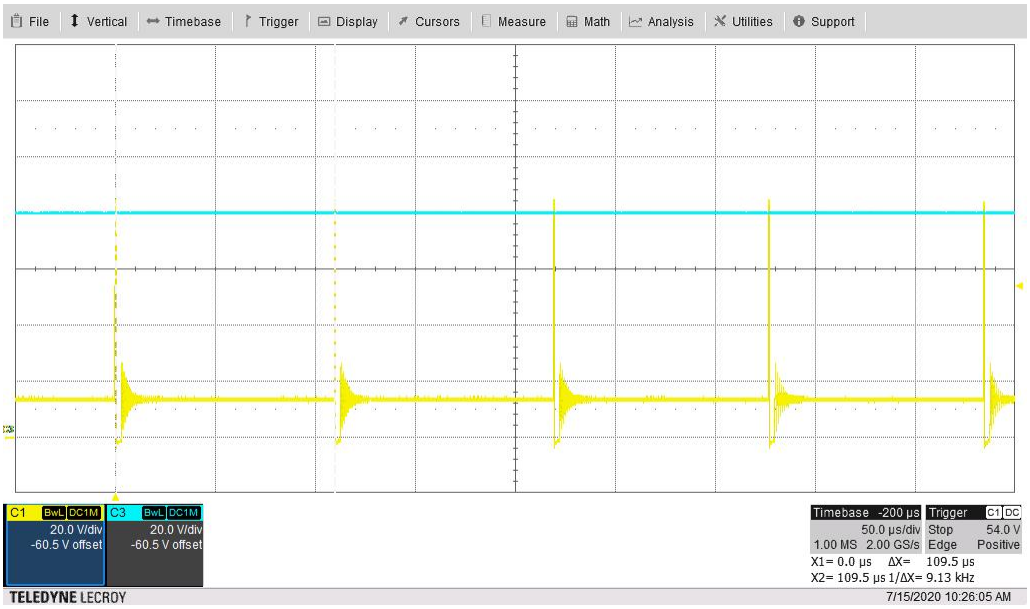

Figure 3-11. FET Switch Node Voltage (Vsnode: 20 V/div, V_{IN}: 20 V/div, 50 µs/div)

The following image shows the FET switch node voltage (YELLOW) at TP3 and the input voltage (BLUE). The input voltage is 144 V and the 14-V output is loaded to 130 mA.

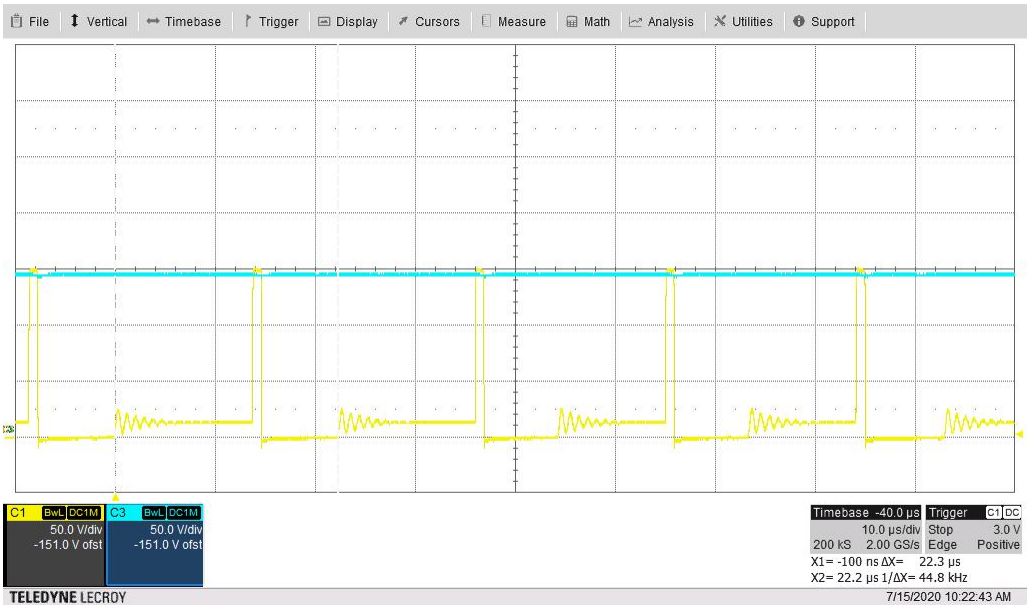

Figure 3-12. FET Switch Node Voltage (Vsnode: 50 V/div, V_{IN}: 50 V/div, 10 µs/div)

The following image shows the FET switch node voltage (YELLOW) at TP3 and the input voltage (BLUE). The input voltage is 144 V and the 14-V output is loaded to 0 mA.

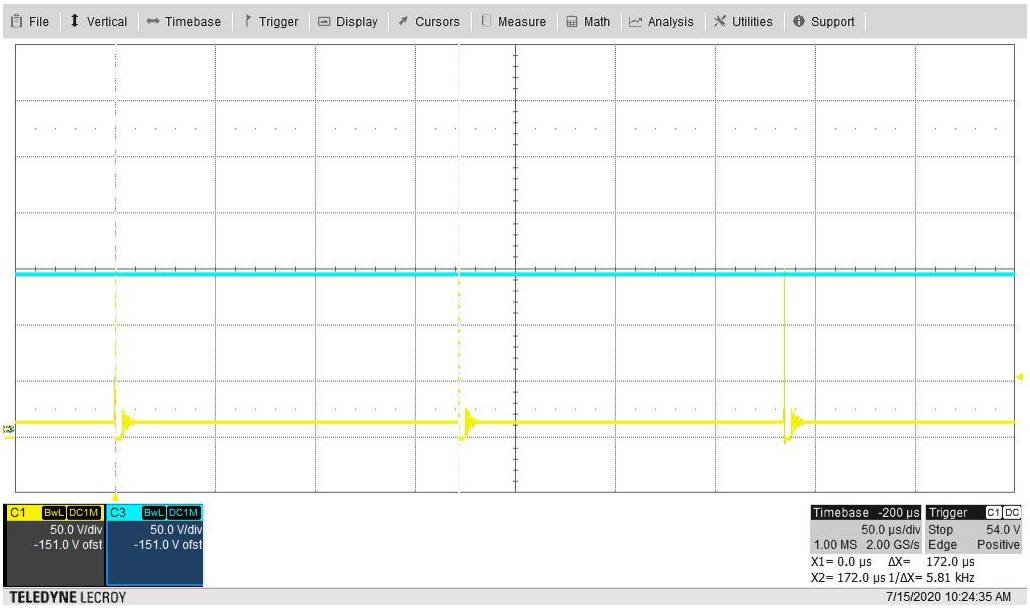

Figure 3-13. FET Switch Node Voltage (Vsnode: 50 V/div, V_{IN}: 50 V/div, 50 µs/div)

The following image shows the switching voltages on each side of C1. The waveforms show the switch node voltage at TP3 (YELLOW) and D1 cathode voltage (BLUE). The input voltage is 50 V and the 14-V output is loaded to 130 mA.

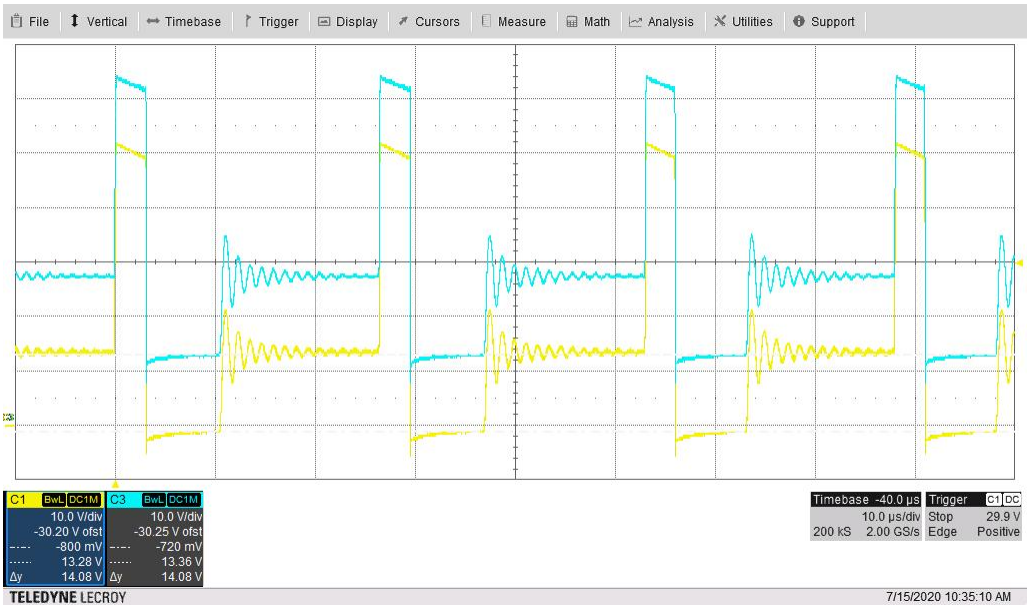

Figure 3-14. Switching Voltages (Vsnode: 10 V/div, D1-Cathode: 10 V/div, 10 µs/div)

The following image shows shows the switching voltages on each side of resistor divider R1/R2. The waveforms show the switch node voltage at TP3 (YELLOW) and the voltage at R1 (side connected to D2) (BLUE). The input voltage is 50 V and the 14-V output is loaded to 130 mA.

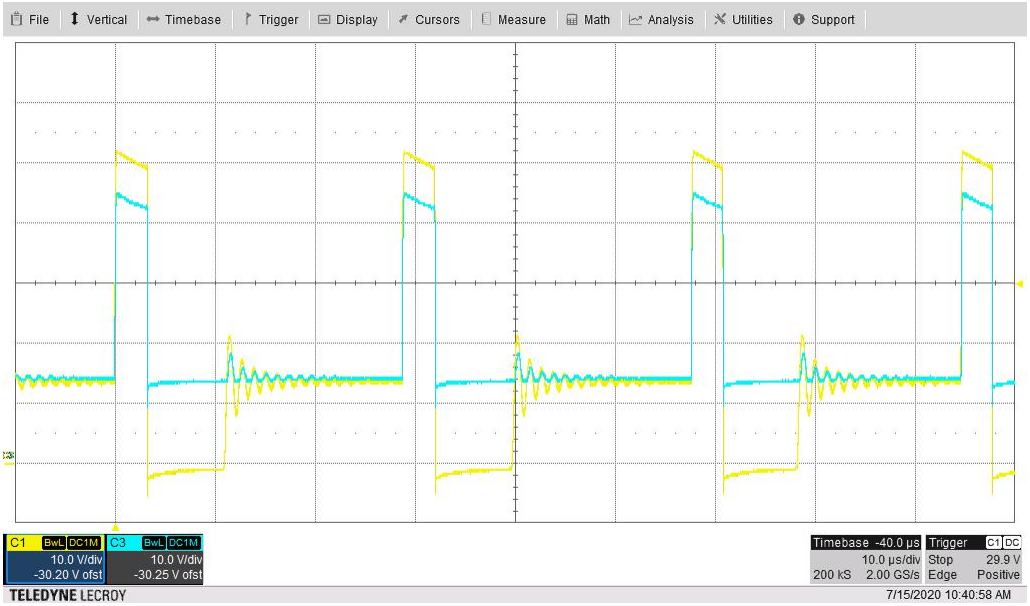

Figure 3-15. Switching Voltages (Vsnode: 10 V/div, D1-Cathode: 10 V/div, 10 µs/div)

3.3 Output Voltage Ripple

The following image illustrates the output ripple voltage (AC coupled). The input voltage is 18 V and the 14-V output is loaded to 130 mA.

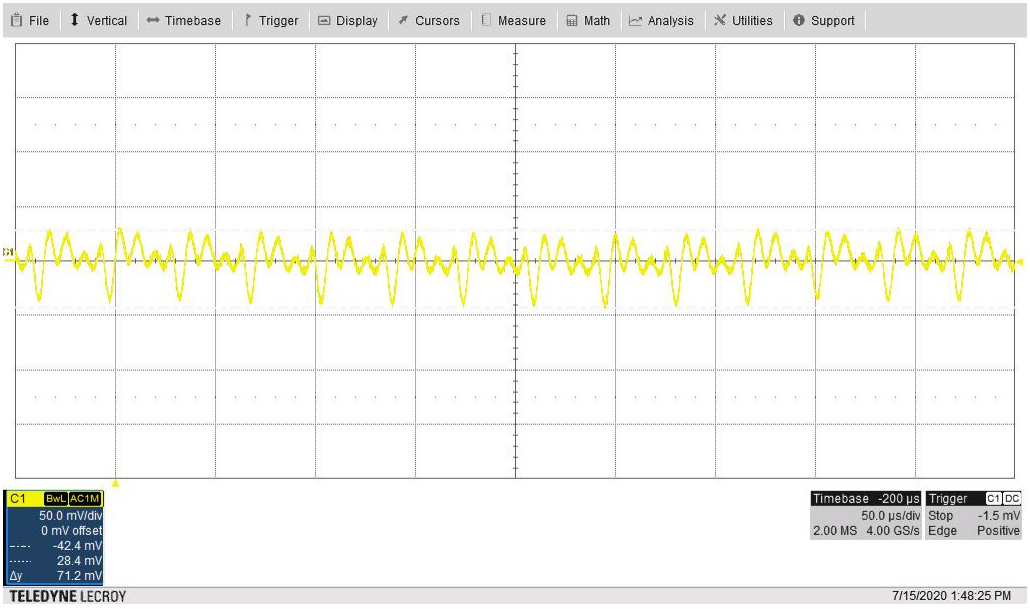

Figure 3-16. Output Voltage Ripple (AC Coupled) (V_{OUT}: 50 mV/div, 50 µs/div)

The following image illustrates the output ripple voltage (AC coupled). The input voltage is 30 V and the 14-V output is loaded to 130 mA.

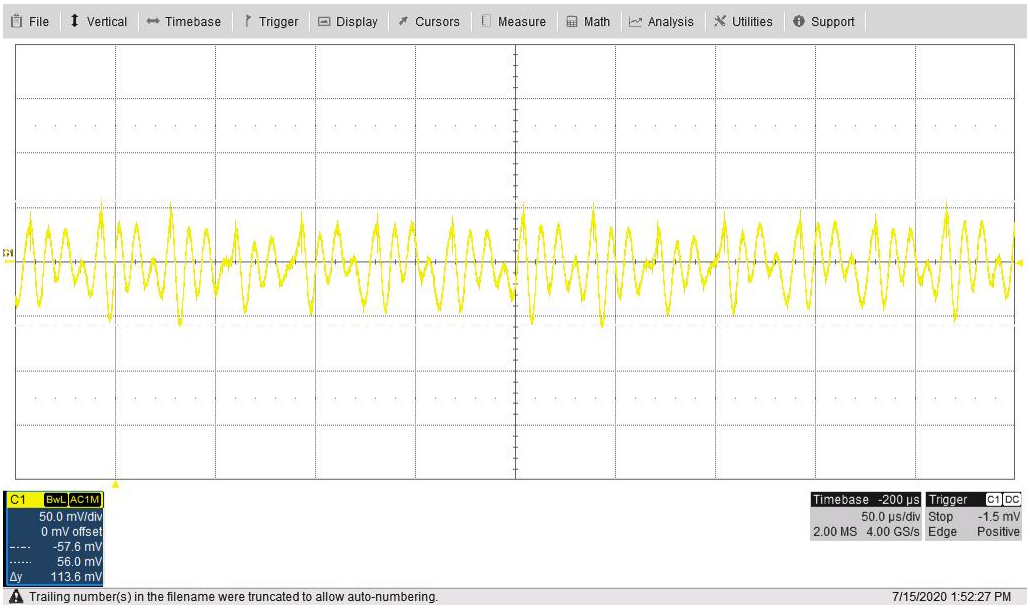

Figure 3-17. Output Voltage Ripple (AC Coupled) (V_{OUT}: 50 mV/div, 50 µs/div)

The following image illustrates the output ripple voltage (AC coupled). The input voltage is 120 V and the 14-V output is loaded to 130 mA.

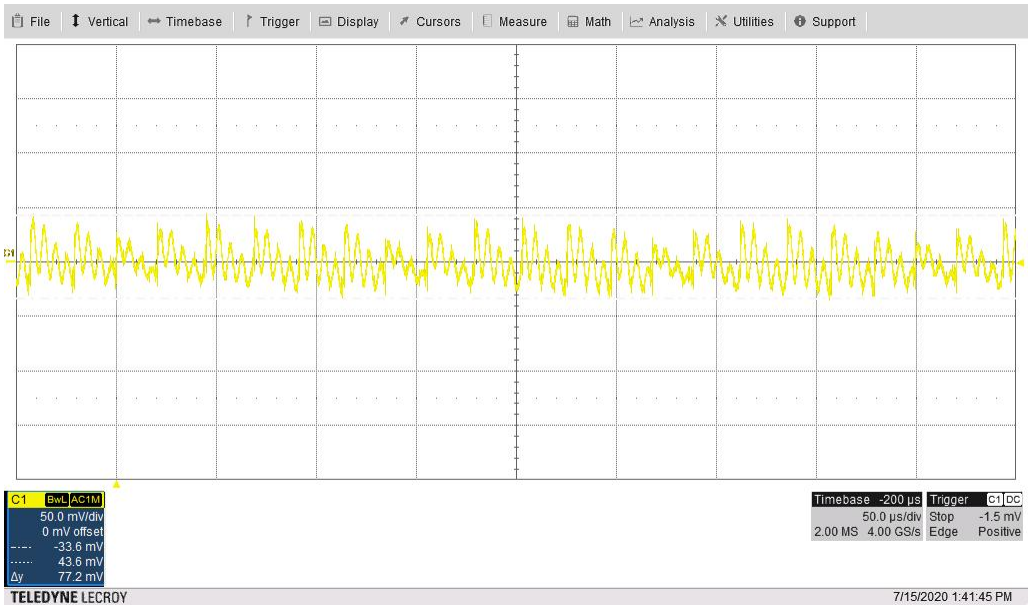

Figure 3-18. Output Voltage Ripple (AC Coupled) (V_{OUT}: 50 mV/div, 50 µs/div)

3.4 Load Transients

The following image illustrates the 14-V output voltage (AC coupled) when the load current is stepped between 80 mA and 130 mA (50-mA load step), V_{IN} = 30 V.

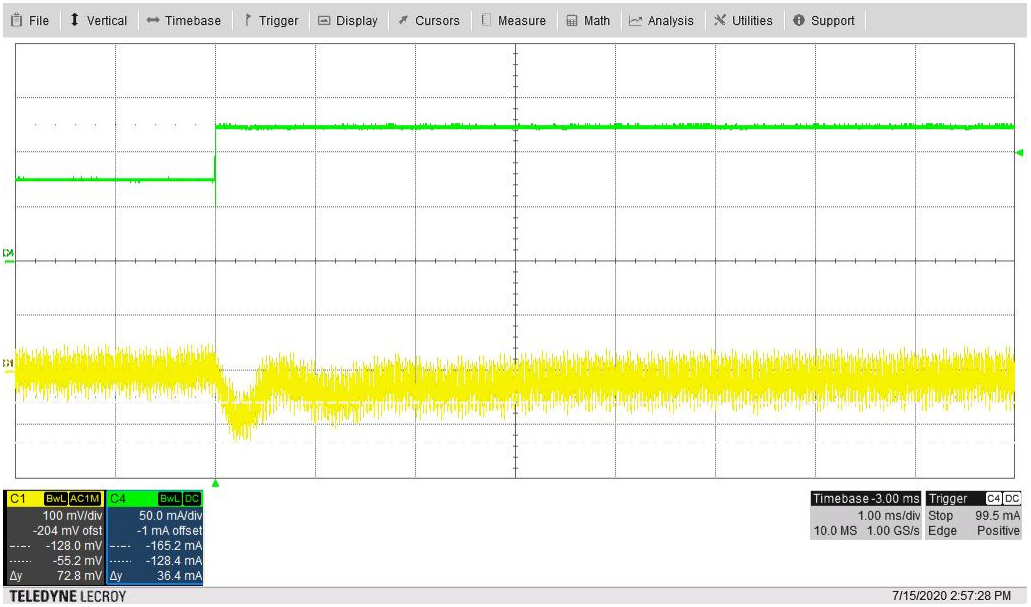

Figure 3-19. Load Transient, 14-V Output Voltage (AC Coupled) (V_{OUT}: 100 mV/div, I_{OUT}: 50 mA/div, 1 ms/div)

The following image illustrates the 14-V output voltage (AC coupled) when the load current is stepped between 130 mA and 80 mA (50-mA load step), V_{IN} = 30 V.

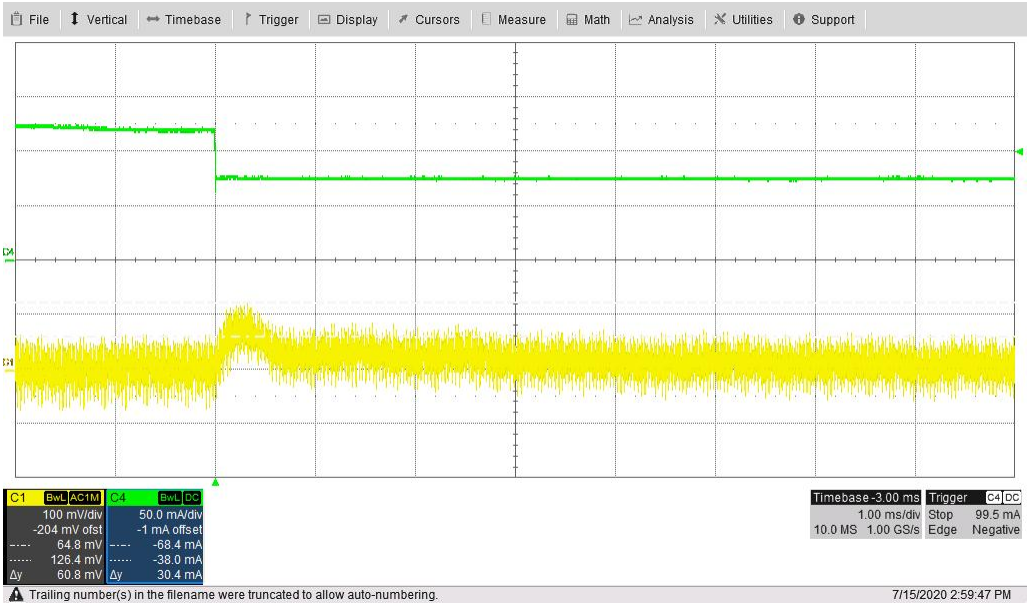

Figure 3-20. Load Transient, 14-V Output Voltage (AC Coupled) (V_{OUT}: 100 mV/div, I_{OUT}: 50 mA/div, 1 ms/div)

The following image illustrates the 14-V output voltage (AC coupled) when the load current is stepped between 80 mA and 130 mA (50-mA load step), V_{IN} = 120 V.

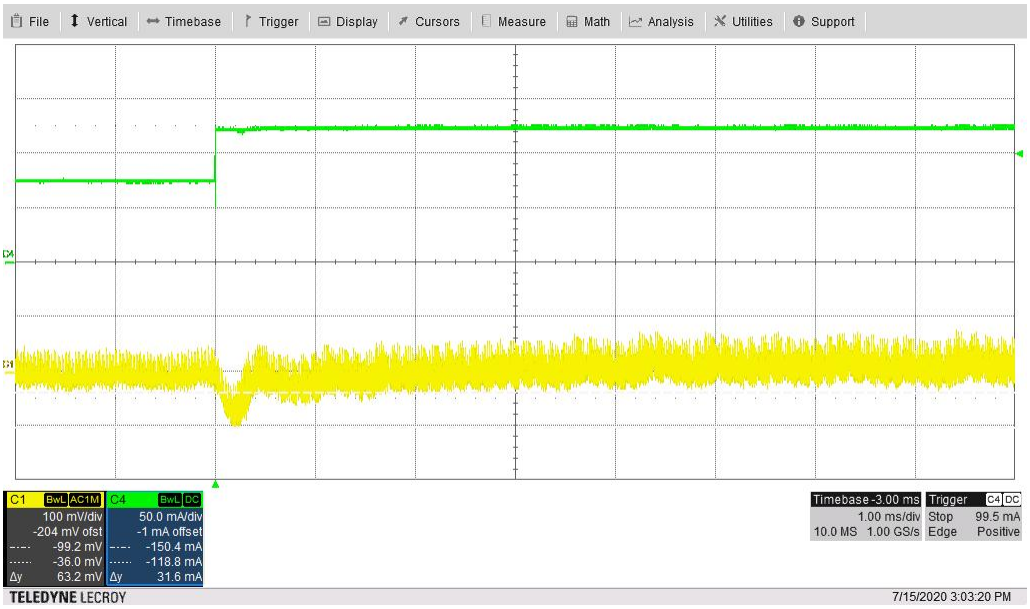

Figure 3-21. Load Transient, 14-V Output Voltage (AC Coupled) (V_{OUT}: 100 mV/div, I_{OUT}: 50 mA/div, 1 ms/div)

The following image illustrates the 14-V output voltage (AC coupled) when the load current is stepped between 130 mA and 80 mA (50-mA load step), V_{IN} = 120 V.

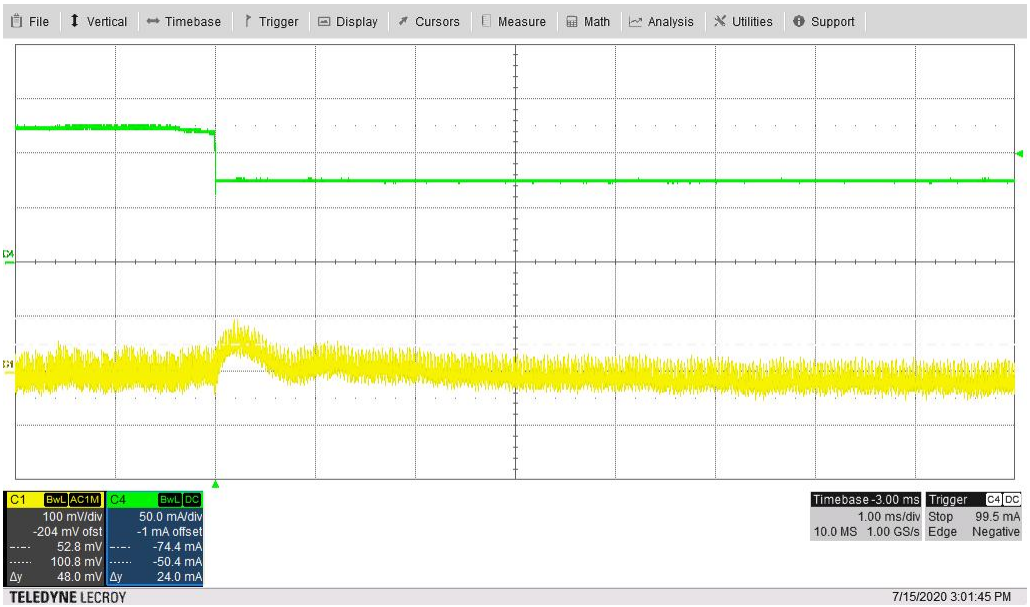

Figure 3-22. Load Transient, 14-V Output Voltage (AC Coupled) (V_{OUT}: 100 mV/div, I_{OUT}: 50 mA/div, 1 ms/div)

3.5 Short-Circuit Recovery Response

The following image illustrates the output voltage (YELLOW) recover from a hard short to ground and the output load current (GREEN), V_{IN} = 30 V and V_{OUT} is 14 V at 130 mA.

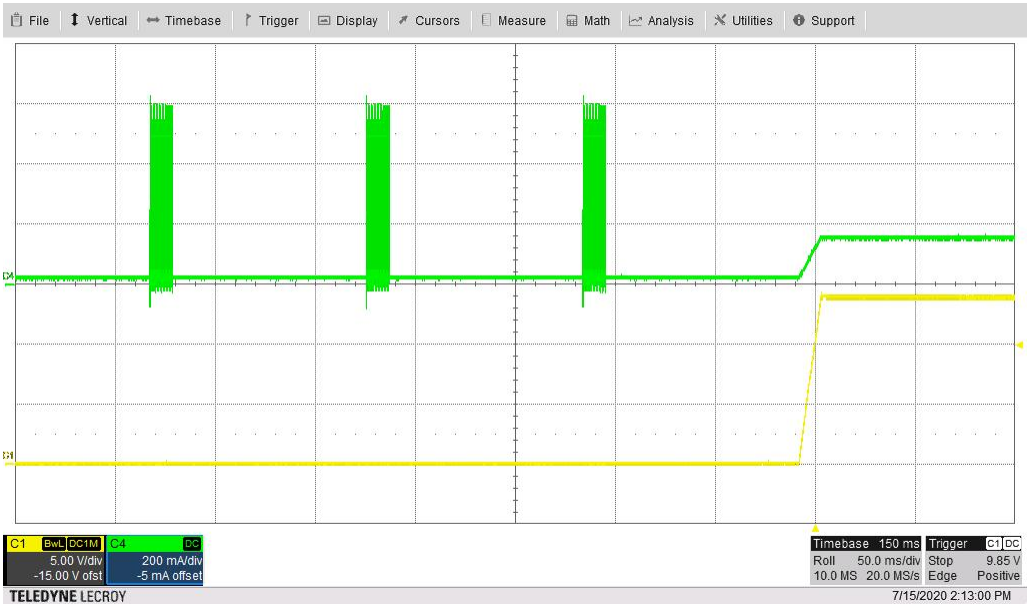

Figure 3-23. Short-Circuit Recovery (V_{OUT}: 5 V/div, I_{OUT}: 200 mA/div, 50 ms/div)

The following image illustrates the output voltage (YELLOW) recover from a hard short to ground and the output load current (GREEN), V_{IN} = 120 V and V_{OUT} is 14 V at 130 mA.

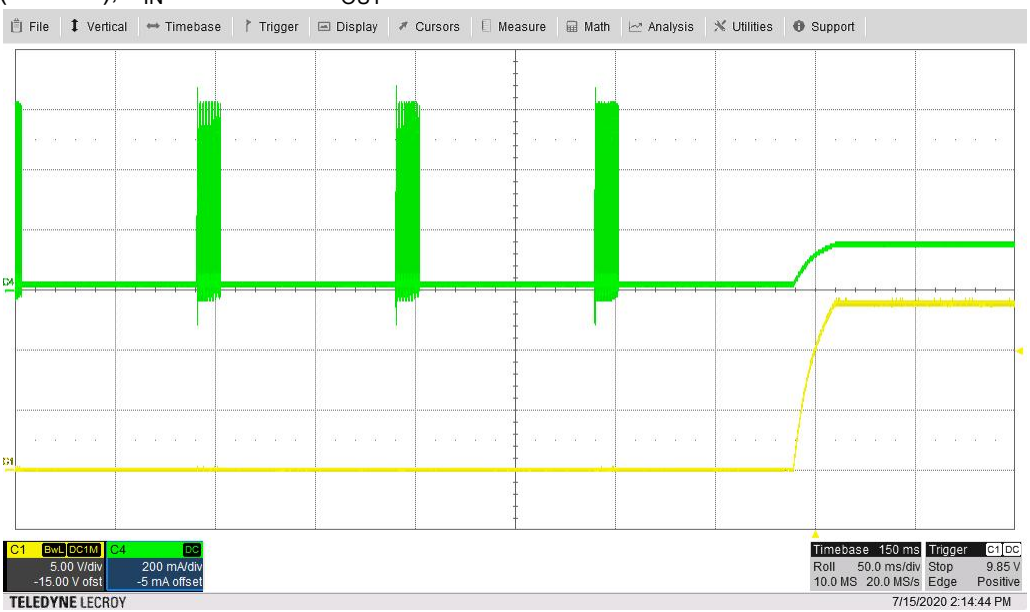

Figure 3-24. Short-Circuit Recovery (V_{OUT}: 5 V/div, I_{OUT}: 200 mA/div, 50 ms/div)

3.6 Input Voltage Transient Response

The following image shows the 14-V output voltage (AC coupled) (YELLOW) when the input voltage transitions from 120 V to 30 V (BLUE), 14 V is loaded to 130 mA.

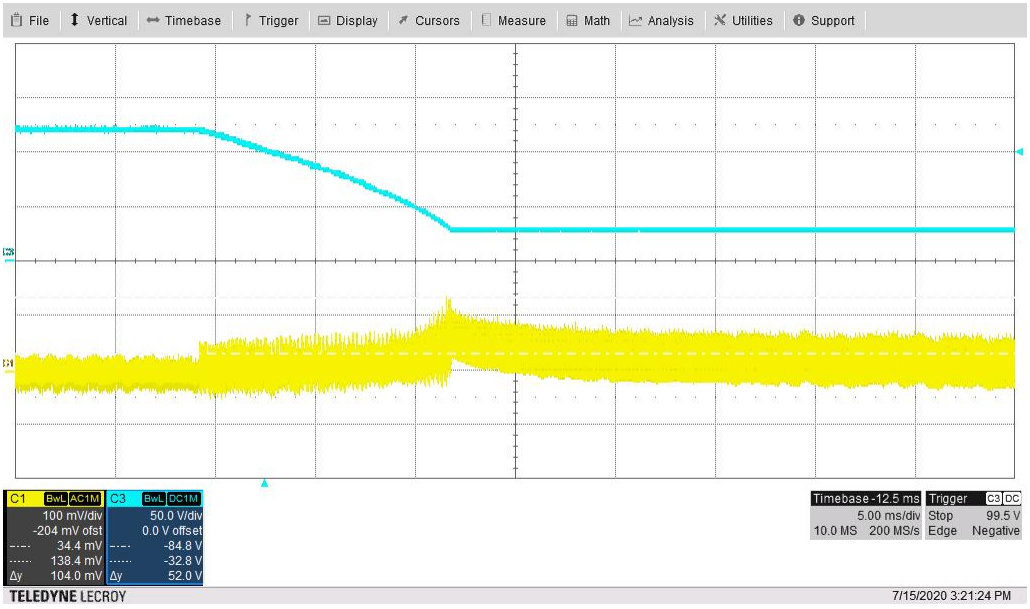

Figure 3-25. Input Voltage Transient Response (V_{OUT}: 100 mV/div, V_{IN}: 200 mA/div, 50 ms/div)

The following image shows the 14-V output voltage (AC coupled) (YELLOW) when the input voltage transitions from 30 V to 120 V (BLUE), 14 V is loaded to 130 mA.

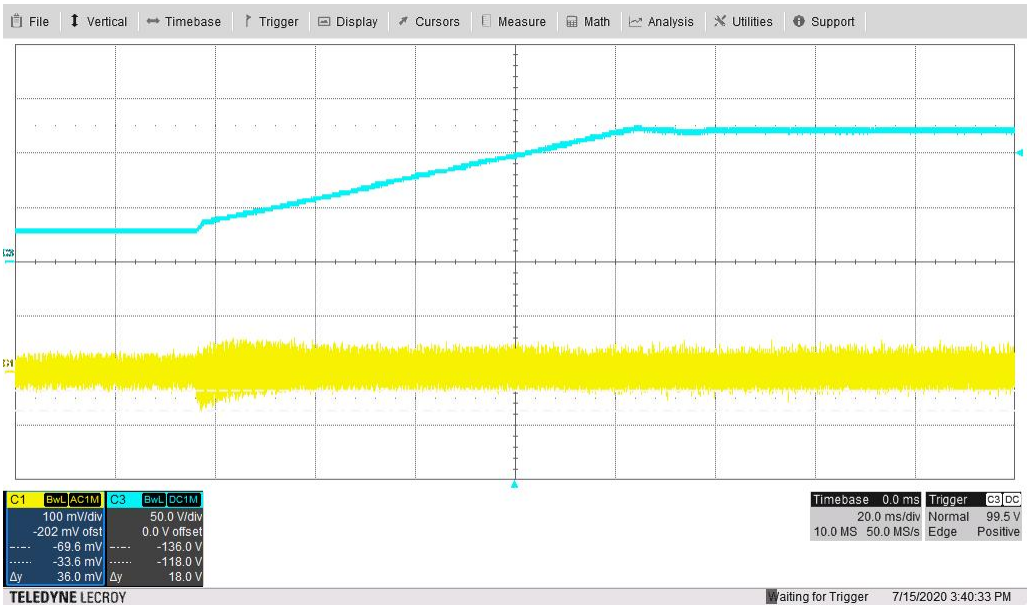

Figure 3-26. Input Voltage Transient Response (V_{OUT}: 5 V/div, I_{OUT}: 200 mA/div, 50 ms/div)

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