

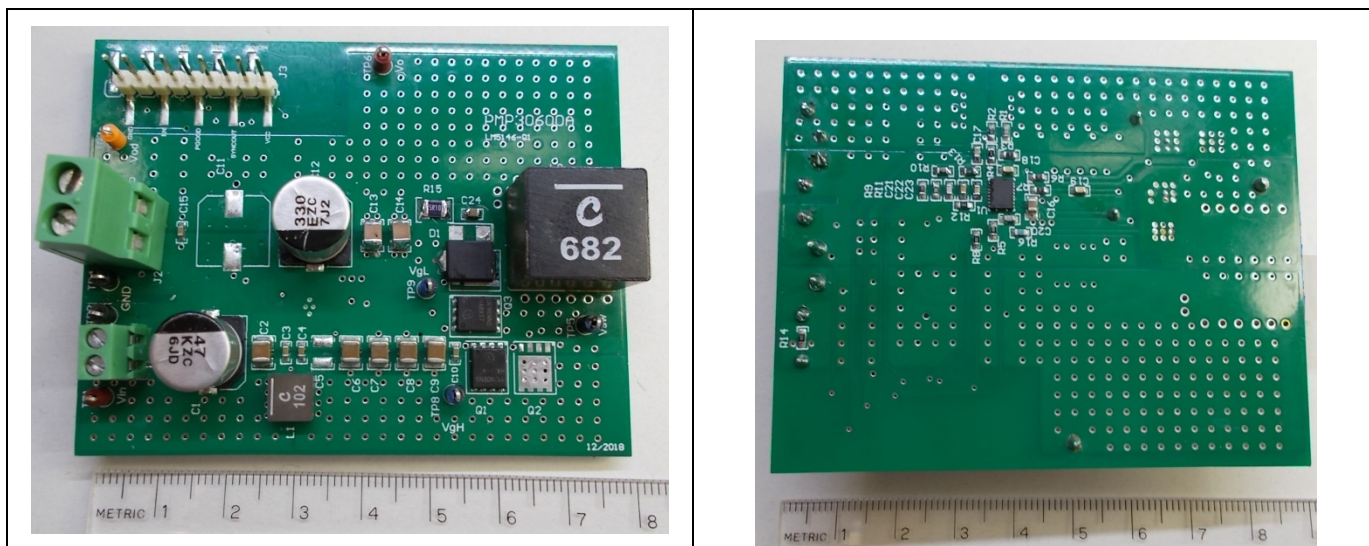
Test Report: PMP30600-TL

10-A Automotive Pre-Regulator With Extended Input Voltage Range for Trucks



Description

This reference design is a synchronous buck converter primarily to supply automotive loads. The IC is LM5146-Q1 in fixed frequency operation at 250 kHz to ensure low noise operation. To minimize conducted emissions an input filter prevents from reflected ripple. Furthermore a RC snubber attenuates noise in the RF band to reduce radiated emissions. To reduce system EMI the design is prepared either to synchronize other converters (output) or just to be externally synchronized (input). The power stage itself withstands surge voltages up to 75Vpk.



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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Range	10 V to 36 V (75 V surge)
Output Voltage	5 V
Maximum Output Current	10 A
Calculated Switching Frequency	250 kHz

1.2 Considerations

The circuit is built on PMP30600RevA

2 Testing and Results

2.1 Efficiency Graphs

The efficiency is shown in the Figure 1 below. The input voltage was set to 28V.

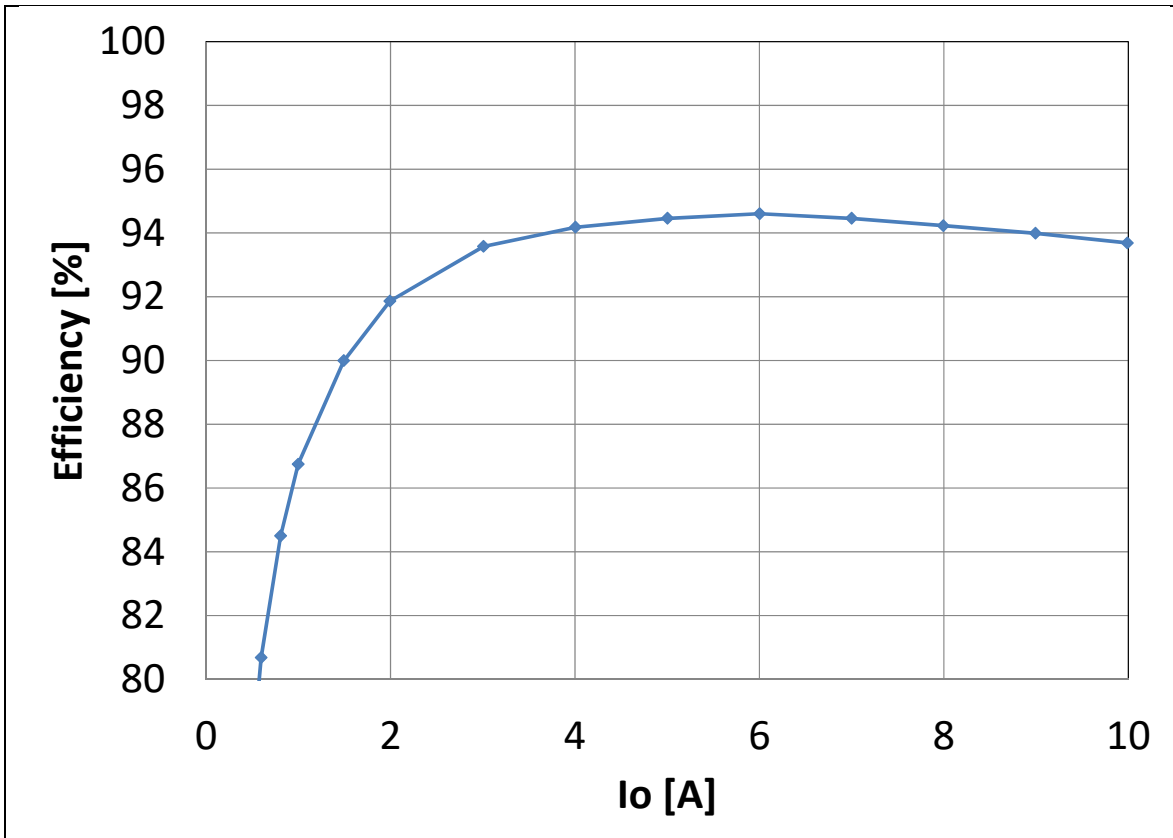


Figure 1

Full load efficiency 93.7%

Maximum efficiency 94.6% at 6A.

Effcy \geq 92.5% in a range 2.5A to 10A, It is 25% load to 100% load.

2.2 Load Regulation

The load regulation of the output is shown in the Figure 2 below. The input voltage was set to 28V.

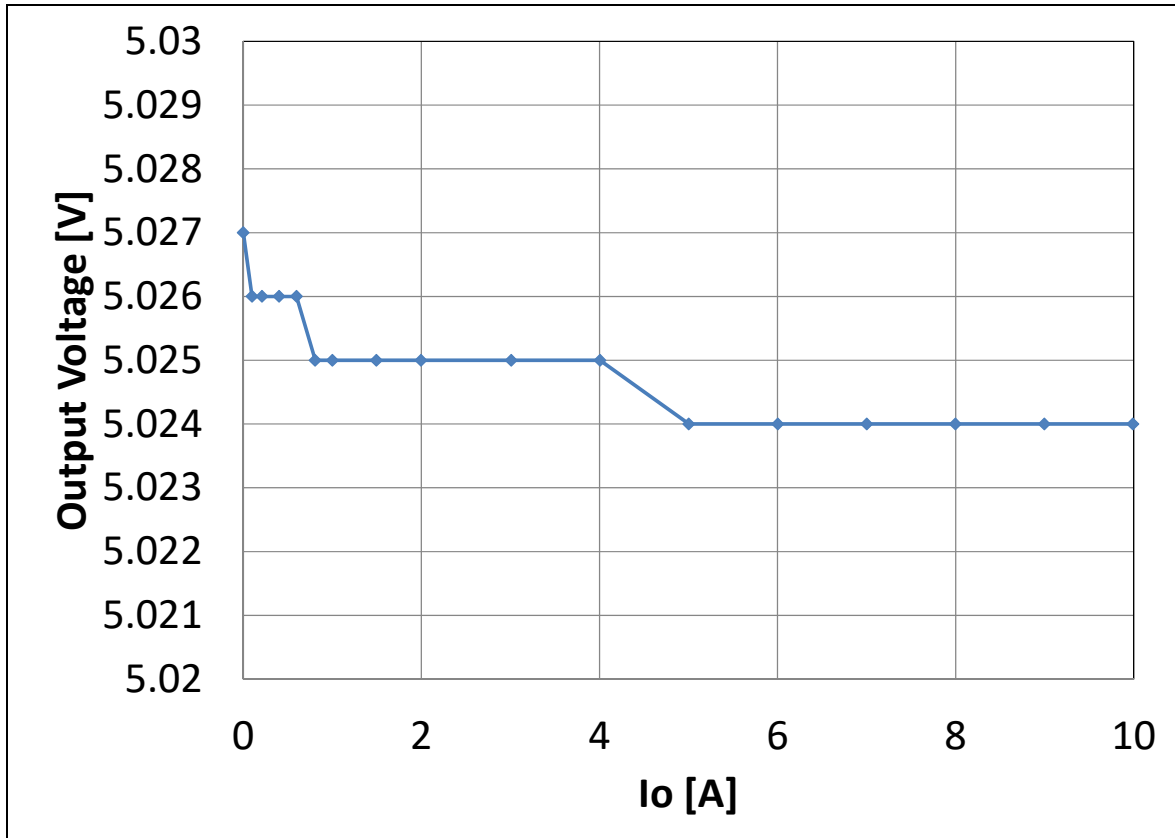


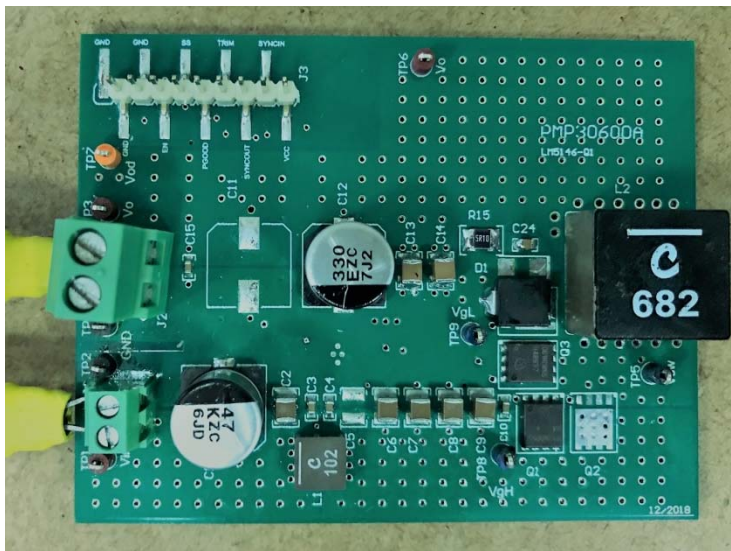
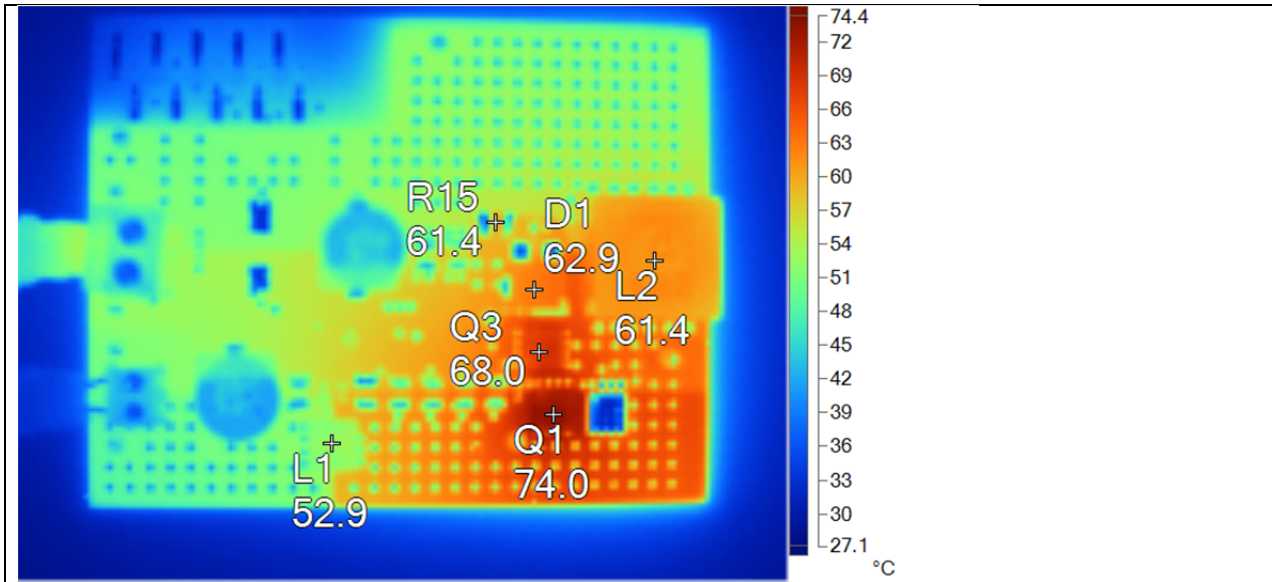
Figure 2

Min. Vout 5.024V (10A), max Vout 5.027V (No Load),

Output voltage variation 3.0mV, so 0.06%, negligible.

2.3 Thermal Images

Thermal image at 28V input and full load 10A after 20mins continuous operation [Rt = 23c]:



Name	Temperature
L1	61.4C
Q1	74.0C
Q3	68.0C
L2	52.9C
D1	62.9C
R15	61.4C

Temperature rise is below +52K, a proper design of the power stage with maximum efficiency results in relaxed thermal stress; this means higher reliability, best MTBF.

2.4 Dimensions

The extensions of the board are 79 mm x 62 mm.

3 Waveforms

3.1 Switching

3.1.1 Switch node (D1)

With input voltage set to 28V and 10A lout results in the waveform shown in Figure 3.

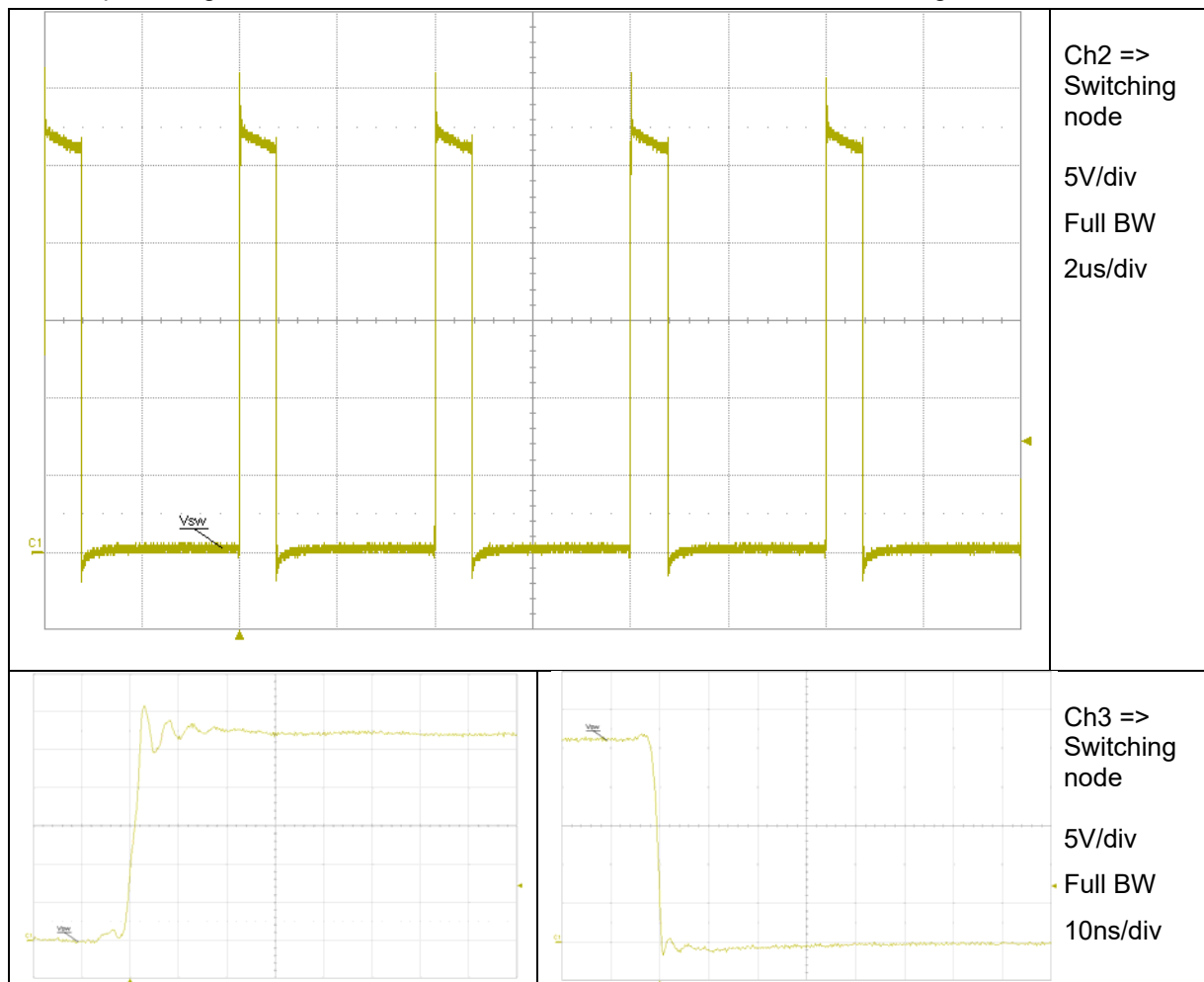
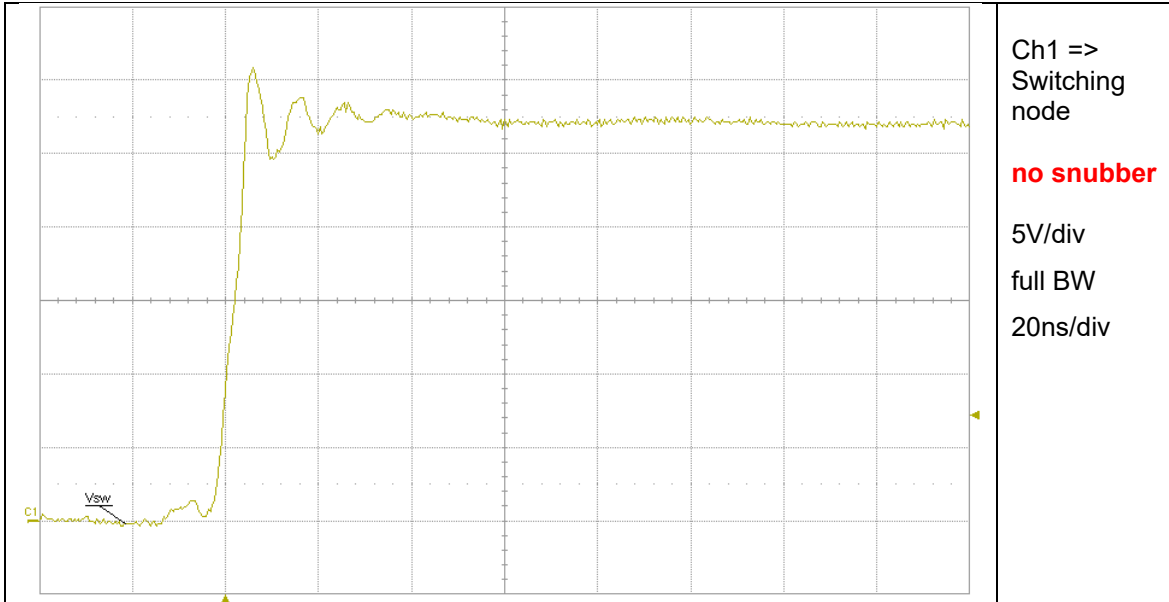


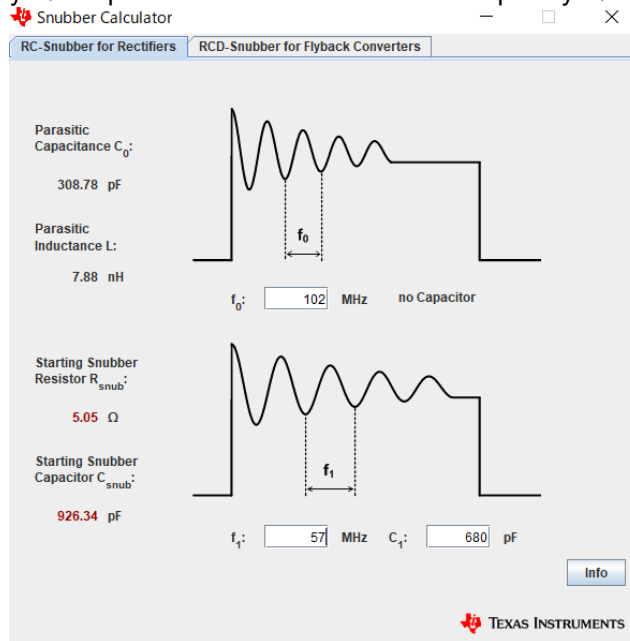
Figure 3

Nominal input voltage is 28V and the overshoot is less than 3.3V. Vds rating of BSC061N08NS5 and BSC117N08NS5 are 80V – enough margin. To fight the 102MHz ringing further a RC snubber circuit was implemented to demonstrate RF suppression:

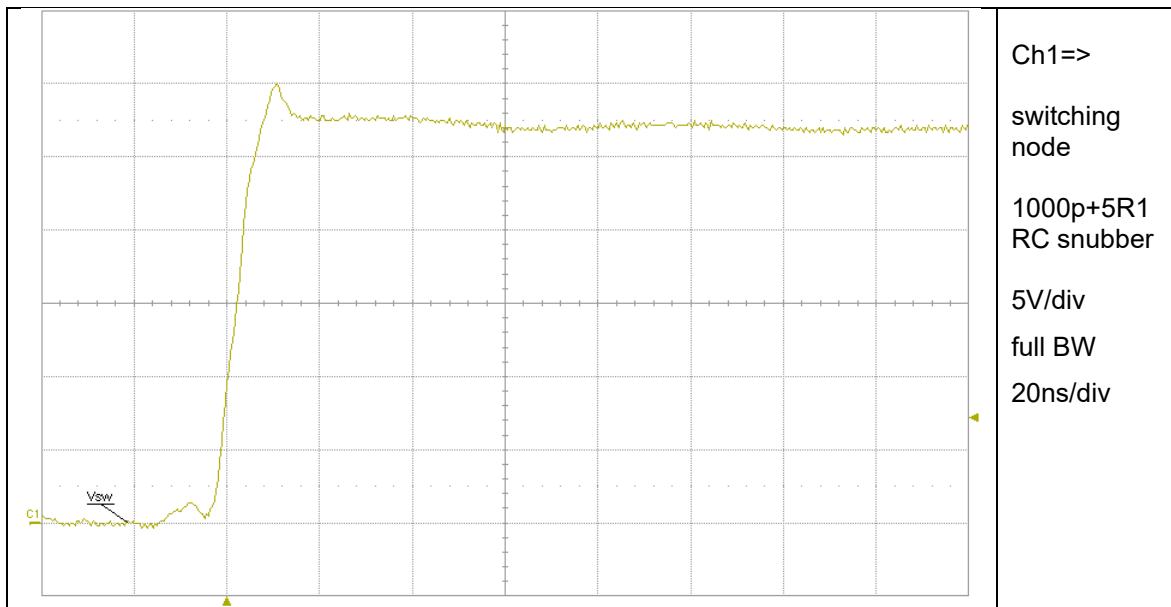
Measure ringing frequency at switch node w/ RF probe (no GND leads, use GND clip), here 102MHz – could cause trouble , radiated emissions:



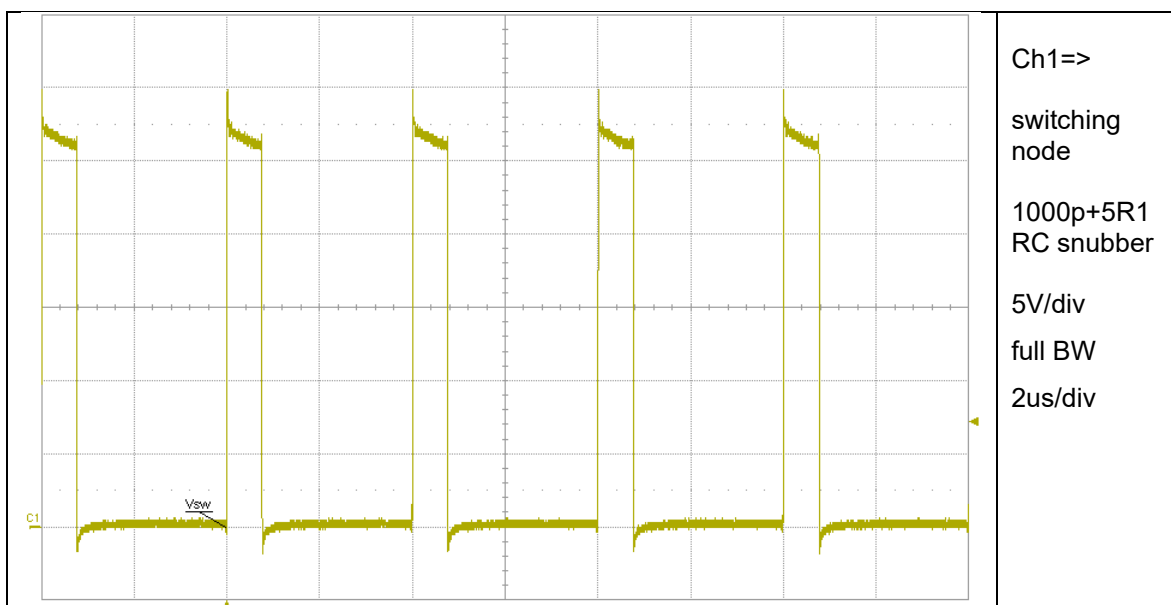
- Add capacitor from switch node to GND and the measure the shifted oscillation frequency.** here 680pF resulted in 57MHz
- Calculate the snubber register and capacitor by utilizing the Power stage designer,** Enter the ringing frequency w/o capacitor and shifted oscillation frequency w/ capacitor.



- add resistor in series and adjust capacitor value,** here RC-snubber of 1000pF / 5.1 Ohm reduced overshoot from 3.3V to 2V:



Clamping network 1000pF / 5.1 Ohm reduces RF content at the switch node, less EMI !



It has to be stated that this hard clamping of the switch node causes a drop in efficiency of 0.4%, so roughly 200mW losses at the snubber resistor.

By experience could be said that a drop in efficiency from 0.2% to 0.5% is typically caused by adding the RC snubber circuit. For a middle power design like PMP30600D geometry 1210 or 1812 might fit, but for high power designs be aware of losses up to 500mW:

- 0603 <100mW
- 0805 <150mW
- 1206 <200mW
- 1210 <250mW
- 1812 <500mW
- 2010 <750mW
- 2512 <1W

3.1.2 High-Side FET Source-Drain (referenced to VIN)

With input voltage set to 24 V and 10 A I_{out} results in the waveform shown in Figure 4.

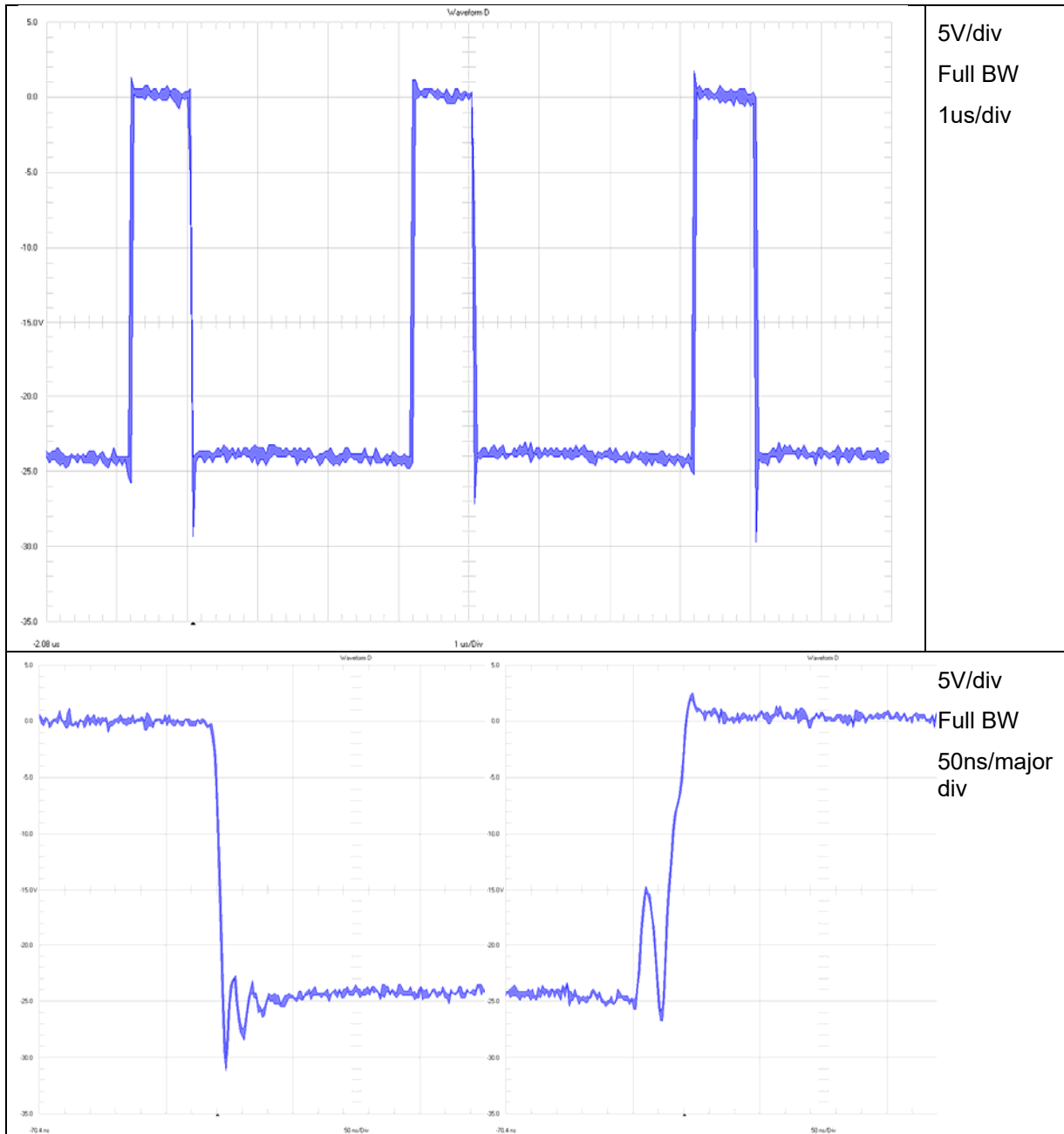


Figure 4 High-Side Source-Drain

3.1.3 Gate-Source Voltage of Low-side FET

With input voltage set to 28V and 10A Iout results in the waveform of low-side gate voltage shown in Figure 5.

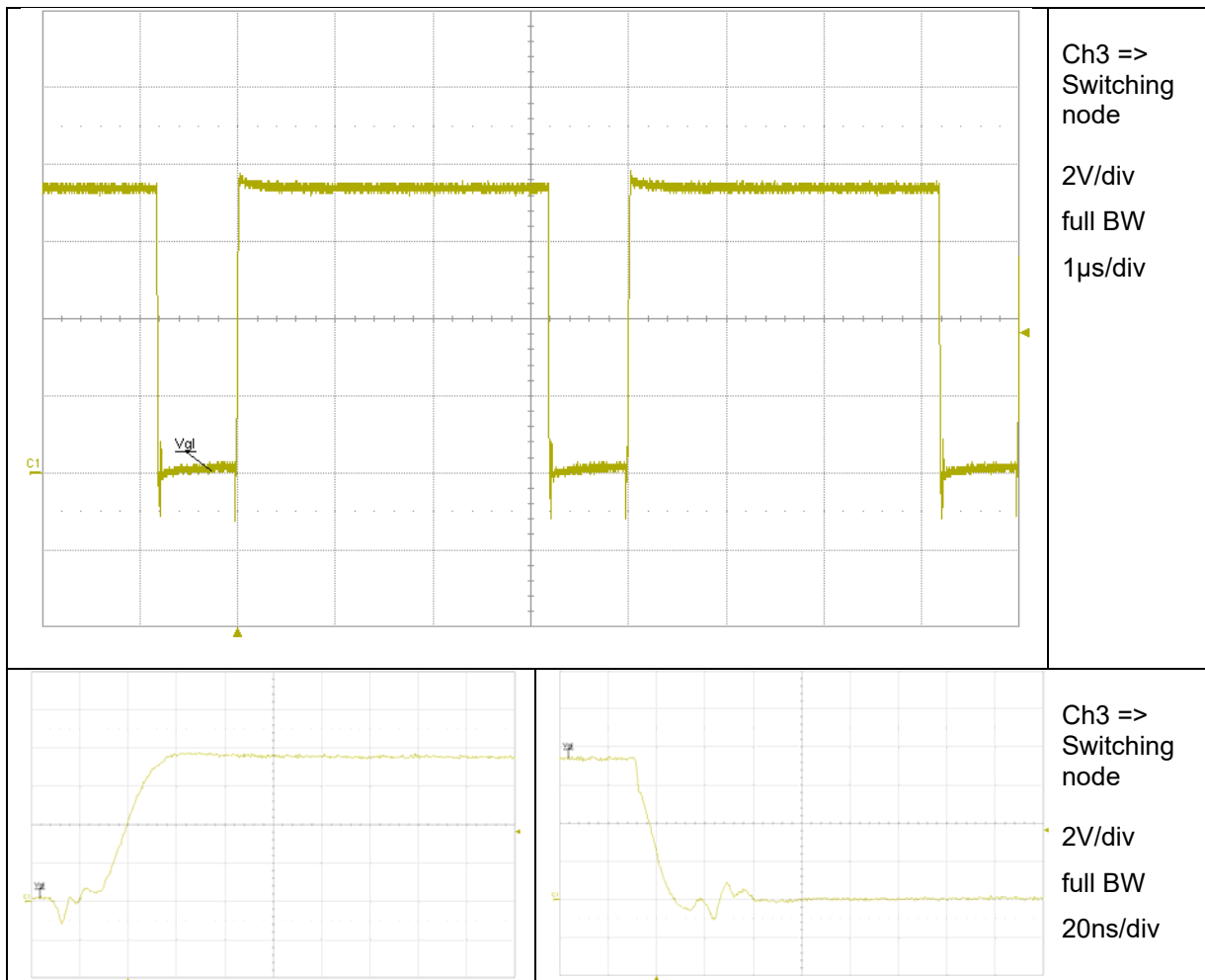


Figure 5 Low-side Gate voltage

3.1.4 Gate-Source Voltage of High-side FET

With input voltage set to 24V and 10A Iout results in the waveform of Hi-side gate to switch voltage shown in Figure 6.

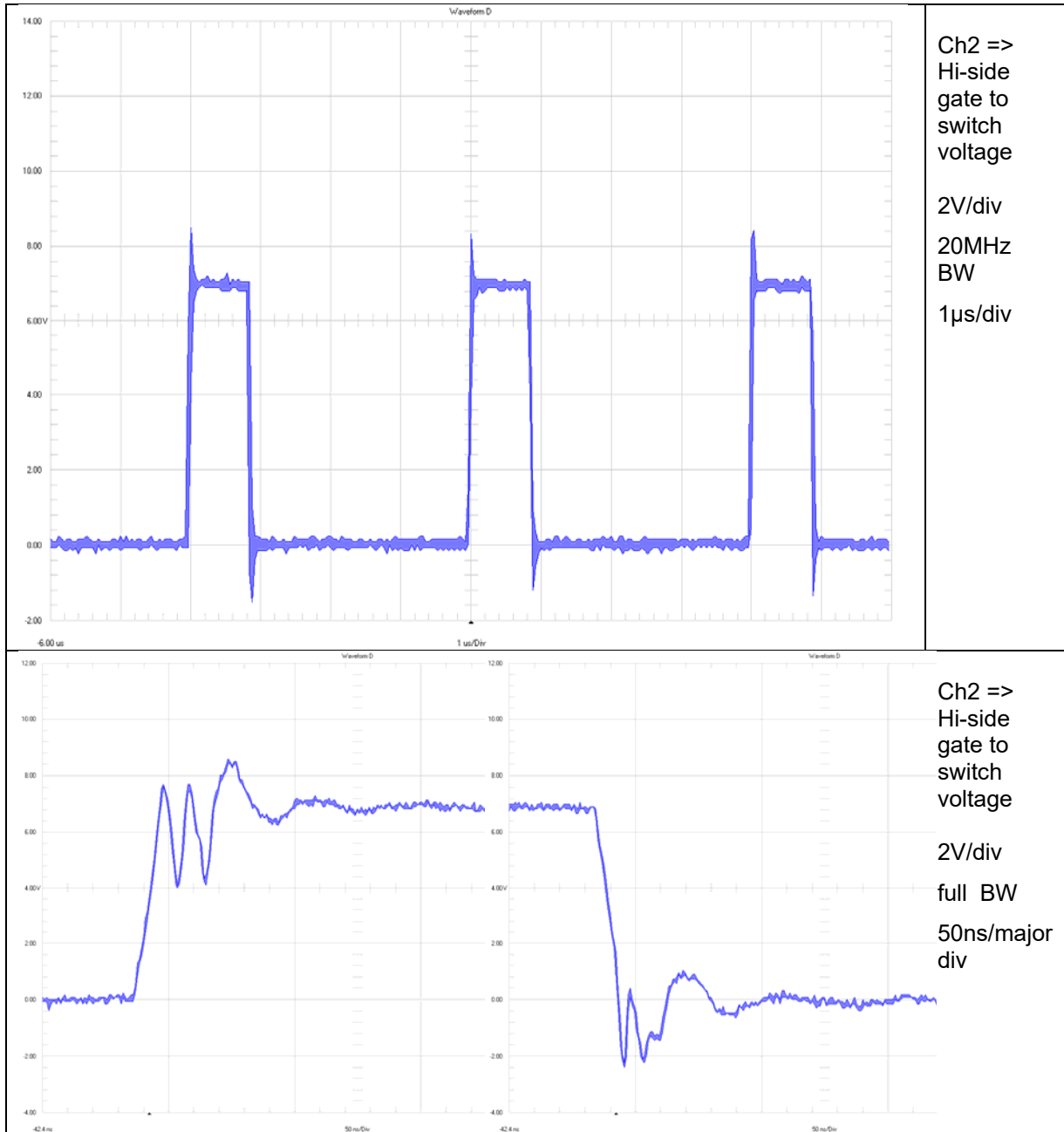


Figure 6 Hi-side Gate to switch voltage

3.2 Output Voltage Ripple

The output ripple voltage is shown in Figure 7. The image was taken with 10A load 28V input at the output. The output ripple voltage is less than 50mV except noise.

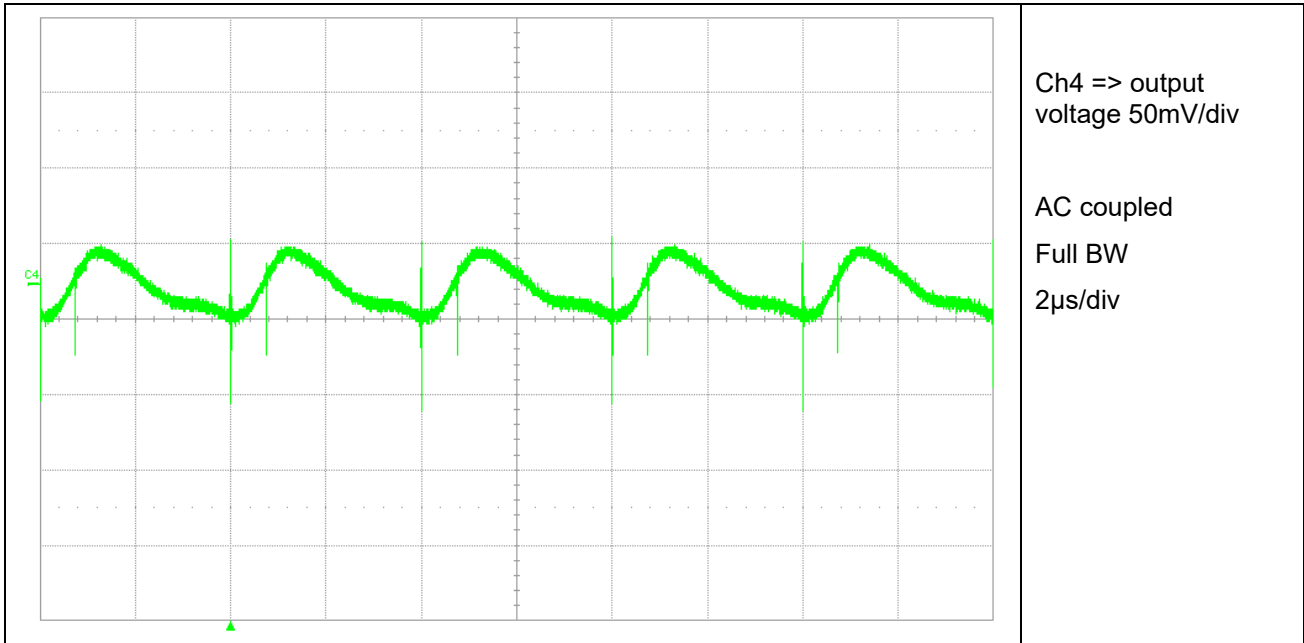


Figure 7

3.3 Input Voltage Ripple

The input ripple voltage is shown in Figure 8. The image was taken with 10A load 14V input at the input.

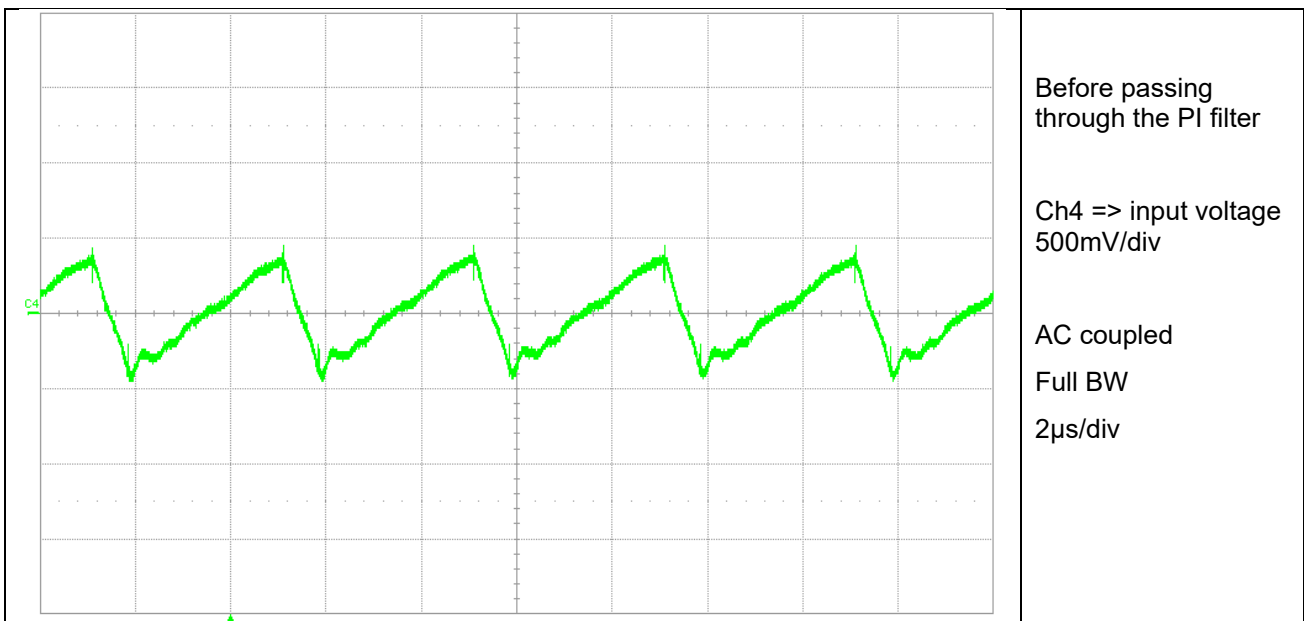
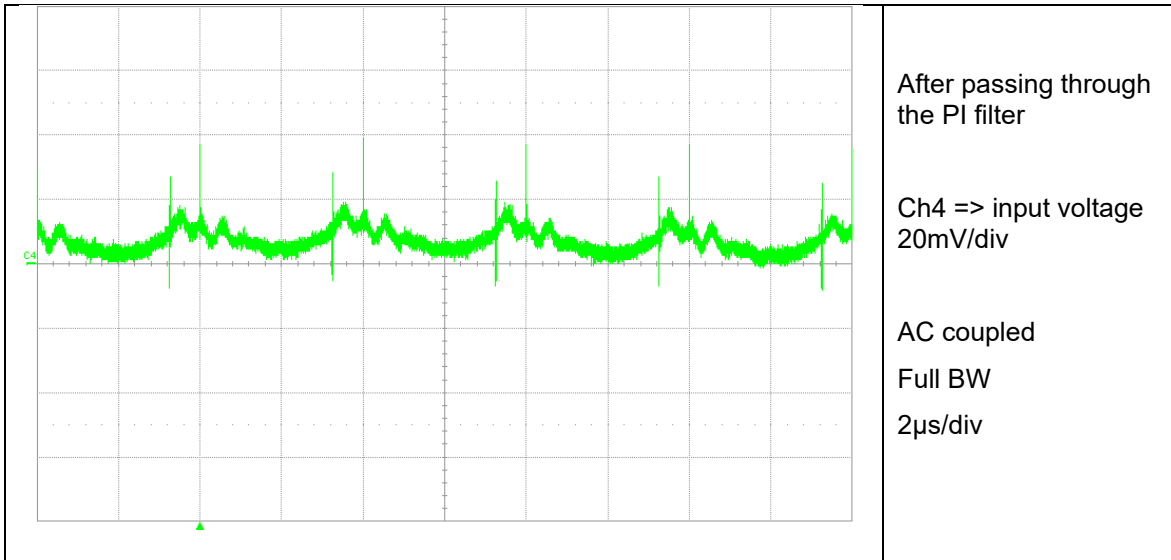
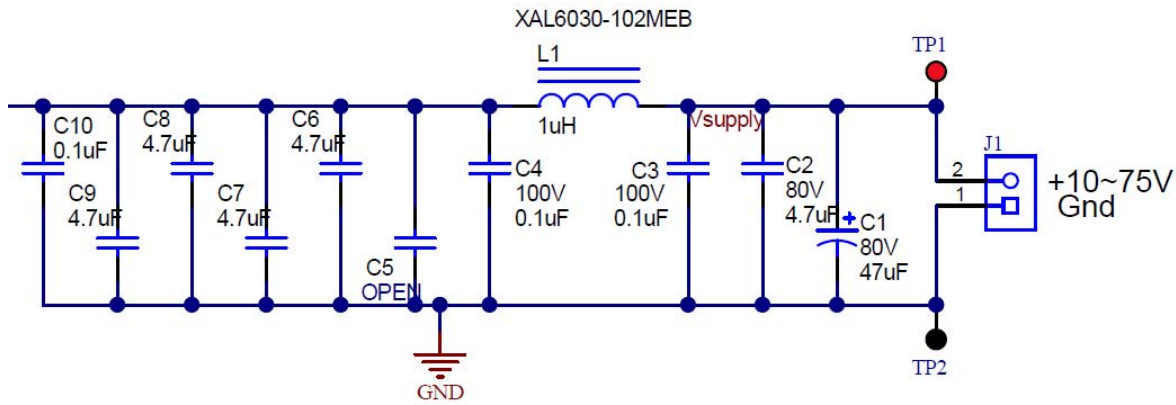


Figure 8

Input voltage ripple is around 830mV.

Finally the input voltage by using PI filter 4x4.7uF – 1.0uH – 10uF+47uF;
 A small ceramic capacitor 100nF was added to suppress glitches:

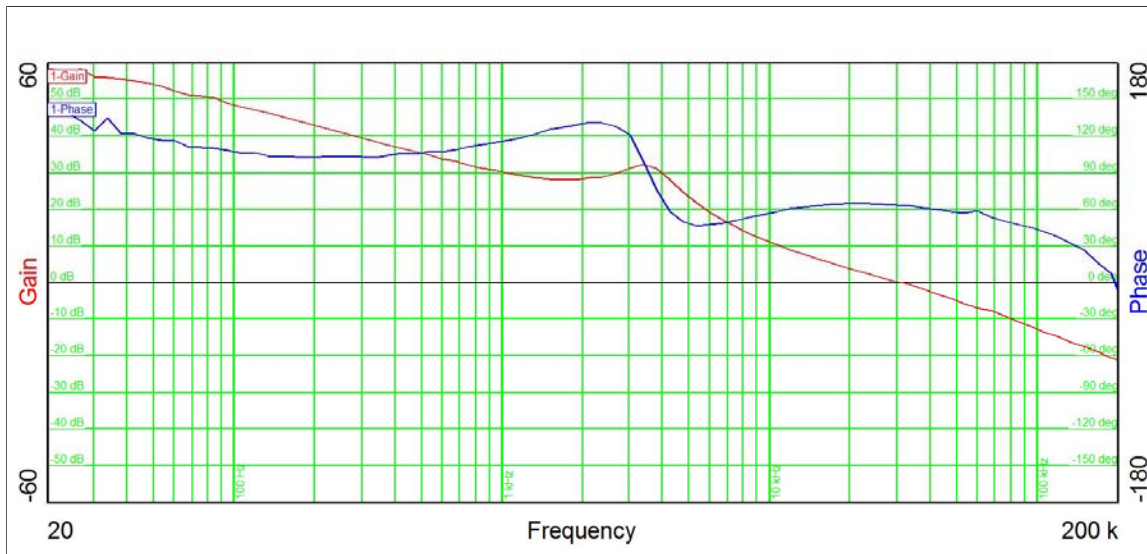


Input voltage ripple is reduced to 19mV; reduction rate is 1/43.

A tremendous reduction of reflected ripple resulted in better EMI behavior !
 The inductor prevents the source from seeing the pulse currents – less conducted emissions.

3.4 Bode Plot

Figures below shows the loop response with 10A load and 28V input.



The bandwidth is measured with NWA Venable #3120. The crossover frequency is 31kHz, the phase margin more than 60 degrees. Slope at crossover is close to -1, here -1.06.

REMEMBER:

This analysis is a small signal analysis, shows the small signal behavior of the power supply.

The only true analysis is a large signal analysis, the system response on a load transient!

3.5 Load Transients

The Figure 9 shows the response to load transients. The load is switching from 5A to 10A. The input voltage was set to 28V.

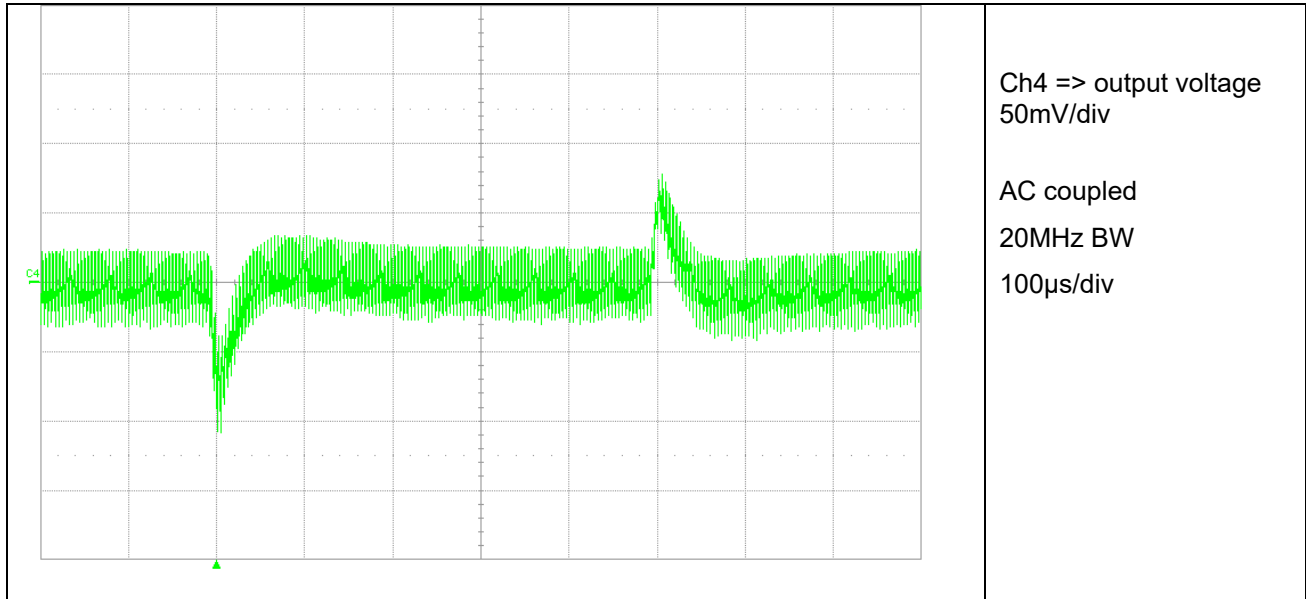


Figure 9

The voltage drop caused by 5A is around 110mV, so less than 3% of the output voltage 5V;
The combination output capacitor to loop bandwidth matches.

A proper calculation of the error amplifier compensation results in a stable design. For series production a phase margin >60 degrees and a gain margin <-15dB is recommended.

3.6 Start-up Sequence

The startup waveform is shown in the Figure 10. The input voltage was set at 28V, with 10A load at the output. Startup w/in 3.6ms, calculated 4ms:

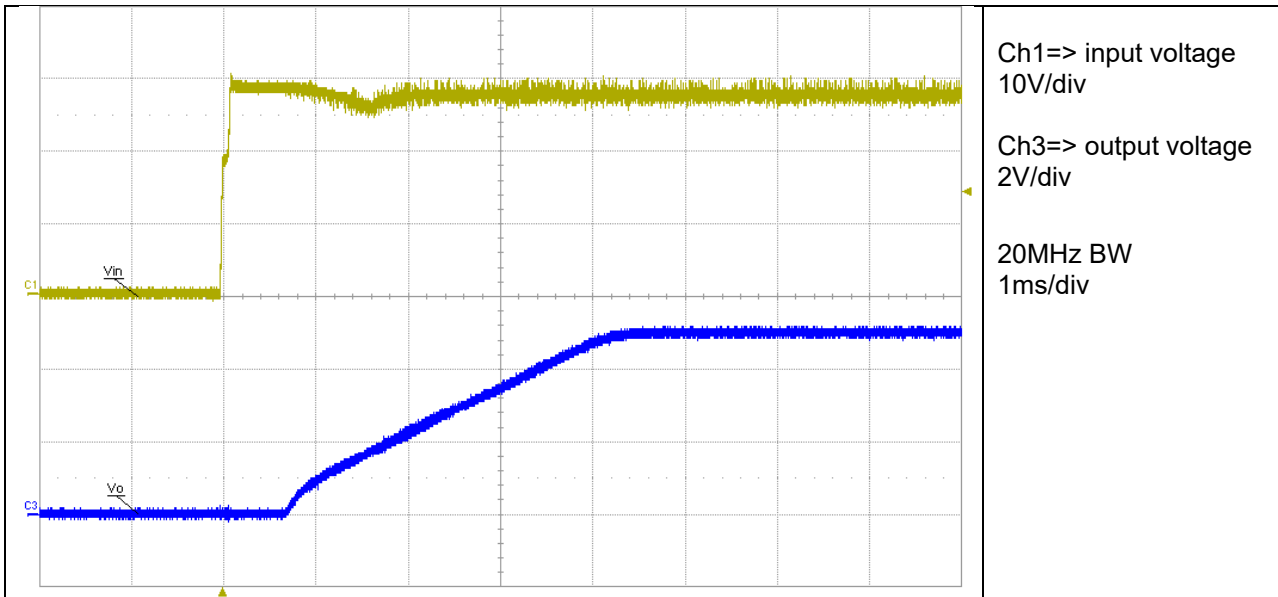


Figure 10

3.7 Shutdown

The shutdown waveform is shown in the Figure 11. The input voltage was set at 28V, with 10A load on the output.

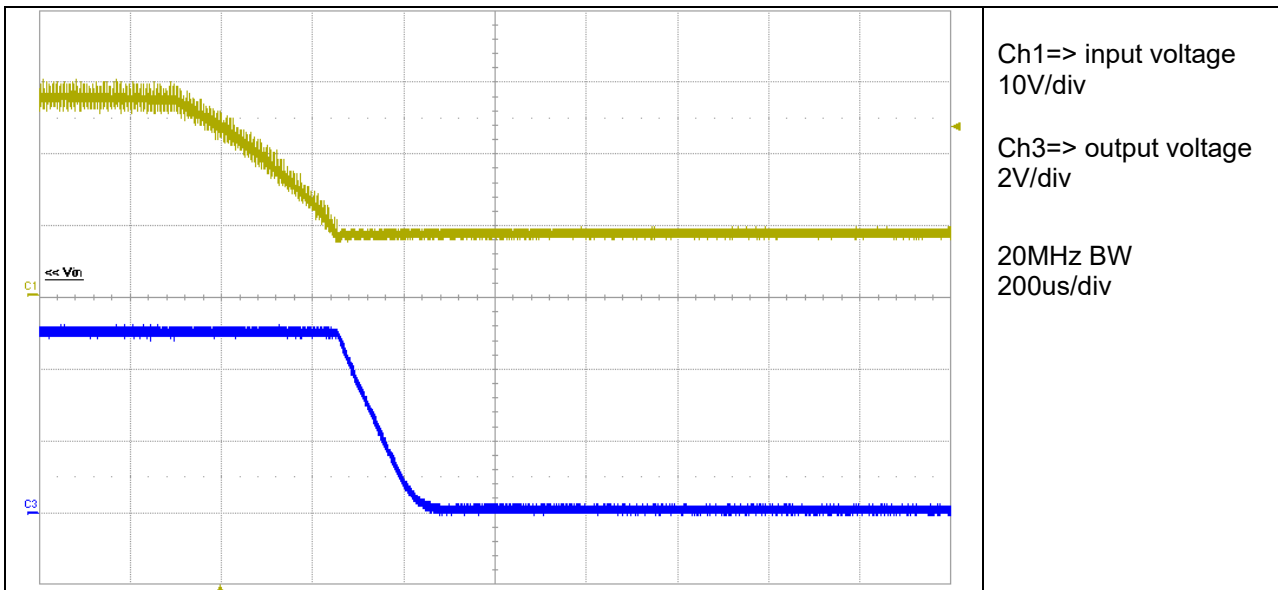


Figure 11

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