

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4	8.00mil	4.2	
5	POWER	Copper	1.40mil		
6	Dielectric 2	FR-4	40.00mil	4.2	
7	GND	Copper	1.40mil		
8	Dielectric 3	FR-4	8.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8_MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24_MIL
 MINIMUM ANNUULAR RING 0.05mm (2ML) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5_MIL, HOLES +/- 3_MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3_MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER RED
 MATTE SEM-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

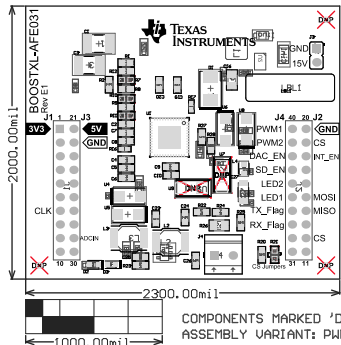
ARRAY/PANEL: CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
 Z22 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z23 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z24 ■ This Assembly Note will show in the PcbDoc and associated outputs



PCB PART NUMBER: BOOSTXL-AFE031	BOARD #26	BOOSTXL-AFE031	DATE: 3/23/2019	TIME: 12:07:52 PM	USER: J191
LAYER NAME = Bottom	TID #: N/A	AN: AN	# 011		
PLATT NAME = Top	GENERATED: 3/23/2019	TIME: 12:07:52 PM	USER: J191		

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ENGINEER: [Name]	LAYOUT BY: [Name]
SCALE: 0.71	ALTIM DESIGNER VERSION: 17.1.9.592

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4	8.00mil	4.2	
5	POWER	Copper	1.40mil		
6	Dielectric 2	FR-4	40.00mil	4.2	
7	GND	Copper	1.40mil		
8	Dielectric 3	FR-4	8.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8_MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24_MIL
 MINIMUM ANNUAL RING 0.05mm (2ML) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5_MIL, HOLES +/- 3_MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3_MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER RED
 MATTE SEM-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

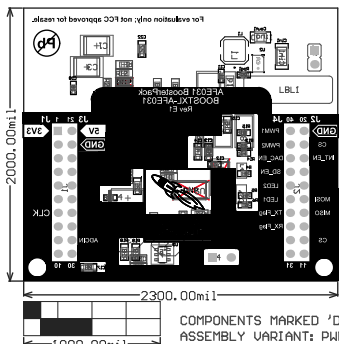
ARRAY/PANEL: CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
 Z22 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z23 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z24 ■ This Assembly Note will show in the PcbDoc and associated outputs



COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. THIS BOARD IS A VARIATION OF THE BOARD SHOWN IN THE REFERENCE DOCUMENTATION.
 ASSEMBLY VARIANT: PWM_Mode

REV: 1	DATE: 3/23/2010	BY: [Signature]	DESCRIPTION: [Signature]
LAYER NAME = Bottom		TID #: N/A	#: 011
PLOT NAME: IN: PcbDoc		GENERATED: 3/23/2010 12:38:12	FILE: [Signature]

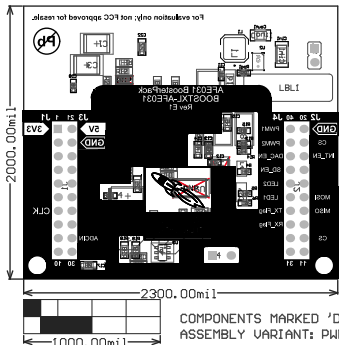
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ENGINEER: [Signature]	LAYOUT BY: [Signature]
Enter name of project	Added the Layout?
SCALE: 0.71	ALTIM DESIGNER VERSION: 17.1.9.592

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
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7	GND	Copper	1.40mil		
8	Dielectric 3	FR-4	8.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION	
MIN. TRACK WIDTH:	8_MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24_MIL
MINIMUM ANNUAL RING 0.05mm (2ML) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5_MIL, HOLES +/- 3_MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3_MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input checked="" type="checkbox"/> FR-4 High Tg <input type="checkbox"/> OTHER _____	
THICKNESS: <input checked="" type="checkbox"/> 62 ML (1.6mm) +/-10% <input type="checkbox"/> OTHER _____	
TOLERANCE: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/- _____	
BOW & TWIST: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/- _____	
DRILLING:	
REFERENCE: <input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS: <input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER _____	
BOARD FINISH:	
SILKSCREEN: <input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR: <input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER _____	
SOLDER RESIST COLOR: <input type="checkbox"/> GREEN <input checked="" type="checkbox"/> OTHER RED <input type="checkbox"/> MATTE <input type="checkbox"/> SEM-GLOSS	
SURFACE FINISH: <input checked="" type="checkbox"/> IMMERSION GOLD (ENG) <input type="checkbox"/> ENEPG <input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER _____	
ARRAY/PANEL: <input type="checkbox"/> CUT AND TRIM PER M1 BOARD OUTLINE <input type="checkbox"/> N.C. ROUTE <input checked="" type="checkbox"/> V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3 <input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS: MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
 Z22 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z23 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z24 ■ This Assembly Note will show in the PcbDoc and associated outputs



BOARD #	BOOSTXL-BOARD	DATE	03/23/2013	TIME	12:38:47 PM	USER	TI\jcm322a
LAYER NAME	Bottom	TID #	N/A	REV	01	DATE	03/23/2013
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PROJECT TITLE: BOOSTXL-PARTNUM	
DESIGNED FOR: Public Release	
FILE NAME: AFE031-BOOSTXL_PCB.PcbDoc	
ENGINEER: Enter name of project	LAYOUT BY: Who did the Layout?
SCALE: 0.71	ALTM DESIGNER VERSION: 17.1.9.592

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
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9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8_MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24_MIL
 MINIMUM ANNUAL RING 0.05mm (2ML) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5_MIL, HOLES +/- 3_MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3_MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER RED
 MATTE SEM-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

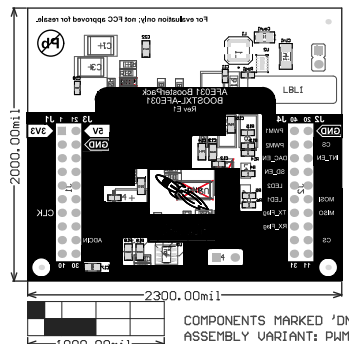
ARRAY/PANEL: CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
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 Z23 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z24 ■ This Assembly Note will show in the PcbDoc and associated outputs



PCB VARIANT: BOOSTXL_PCB LAYER NAME = BOOSTXL_PCB_Bottom PLOT NAME: BOOSTXL_PCB_Layer Assembly Drawing	BOARD #26 TID #: N/A GENERATED: 3/23/2019 12:39:00 PM	BOOSTXL_PCB E1 SUN 3:00: IN 2:10: 08:03: 08:00: 08:00:	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	ENGINEER: [Name] LAYOUT BY: [Name] SCALE: 0.71 ALTIM DESIGNER VERSION: 17.1.9.592
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