







Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4	8.00mil	4.2	
5	POWER	Copper	1.40mil		
6	Dielectric 2	FR-4	40.00mil	4.2	
7	GND	Copper	1.40mil		
8	Dielectric 3	FR-4	8.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 8\_MIL  
 MIN. CLEARANCE: 0.2 mm  
 MIN. VIA PAD SIZE: 24\_MIL  
 MINIMUM ANNUAL RING 0.05mm (2ML) EXTERNAL  
 PER IPC-D-275 CLASS 2 LEVEL C  
 REGISTRATION TOLERANCES: METAL +/- 5\_MIL, HOLES +/- 3\_MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3\_MIL

**MATERIAL:**  
 FR-408  FR-4 High Tg  OTHER \_\_\_\_\_  
 THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER \_\_\_\_\_  
 TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_  
 BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRILLING:**  
 REFERENCE:  AS SHOWN  NC\_DRILL FILES  
 PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

**BOARD FINISH:**  
 SILKSCREEN:  TOP  BOTTOM  
 SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_  
 SOLDER RESIST COLOR:  GREEN  OTHER RED  
 MATTE  SEM-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENG)  ENEPG  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

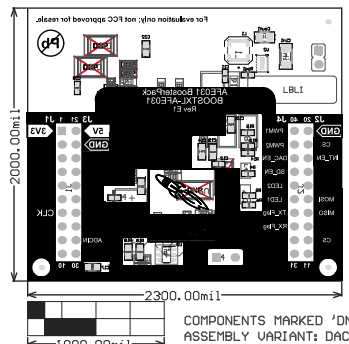
**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS ->  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  
 MICROSECTION:  YES  
 BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.  
 Z22 ■ This Assembly Note will show in the PcbDoc and associated outputs  
 Z23 ■ This Assembly Note will show in the PcbDoc and associated outputs  
 Z24 ■ This Assembly Note will show in the PcbDoc and associated outputs



<p>ACB VARGDEKE RNDLEDPFMDIDBPVSEDE</p> <p>LAYER NAME = <b>Bottom</b></p> <p>PL0T NAME: <b>Bottom</b></p>	<p>BOARD #26</p> <p>TID #: N/A</p> <p>GENERATED: 3/23/2019 12:42:28 PM</p>	<p>BOOSTXL PCB</p> <p>DATE: 3/23/2019</p> <p>DESIGNED BY: [Name]</p>	<p>TEXAS INSTRUMENTS</p>	<p>Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.</p>	<p>ENGINEER: [Name]</p> <p>SCALE: 0.71</p>	<p>LAYOUT BY: [Name]</p> <p>ALTIM DESIGNER VERSION: 17.1.9.592</p>
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