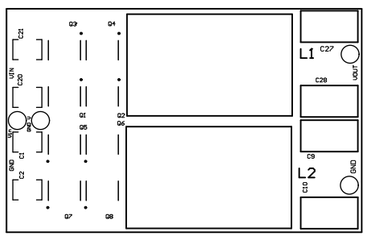
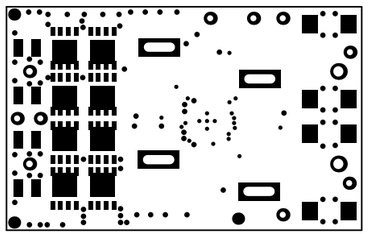
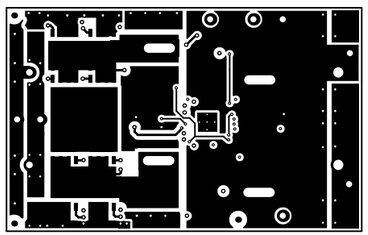


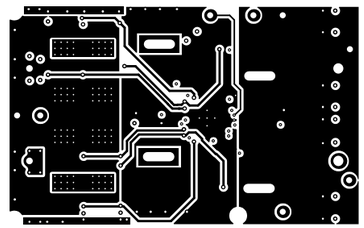
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7819	
LAYER NAME = Top Overlay	ARTWORK # = 880007819.pcb_minorRev	
PLOT NAME = Top Overlay	GENERATED : 6/14/2012 3:48:01 PM	NATIONAL SEMICONDUCTOR

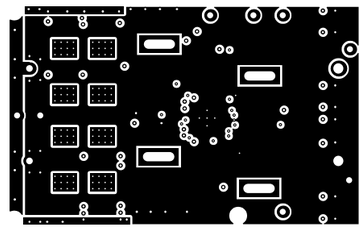


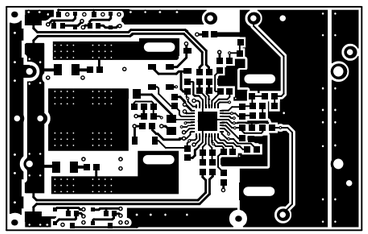
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7819	
LAYER NAME = Top Solder	ARTWORK # = 880007819.pcb_minorRev	
PLOT NAME = Top Solder Mask	GENERATED : 6/14/2012 3:48:02 PM	NATIONAL SEMICONDUCTOR



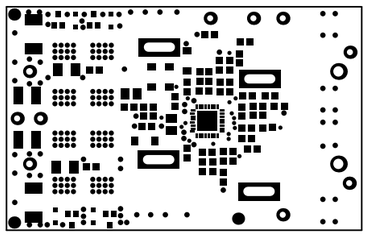
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7819	
LAYER NAME = Top Layer	ARTWORK # = 880007819.pcb_minorRev	
PLOT NAME = Top Layer	GENERATED : 6/14/2012 3:48:02 PM	NATIONAL SEMICONDUCTOR



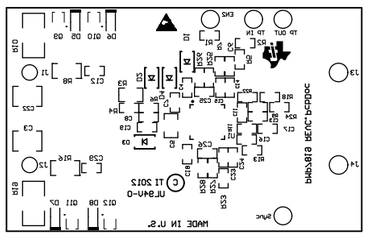




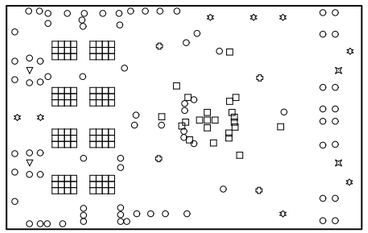
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7819	
LAYER NAME = Bottom Layer	ARTWORK # = 880007819.pcb_minorRev	
PLOT NAME = Bottom Layer	GENERATED : 6/14/2012 3:48:04 PM	NATIONAL SEMICONDUCTOR



ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7819	
LAYER NAME = Bottom Solder	ARTWORK # = 880007819.pcb_minorRev	
PLOT NAME = Bottom Solder Mask	GENERATED : 6/14/2012 3:48:04 PM	NATIONAL SEMICONDUCTOR



ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7819	
LAYER NAME = Bottom Overlay	ARTWORK # = 880007819.pcb_minorRev	
PLOT NAME = Bottom Overlay	GENERATED : 6/14/2012 3:48:05 PM	NATIONAL SEMICONDUCTOR

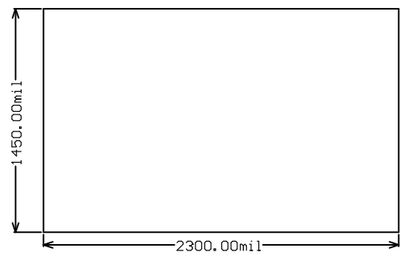


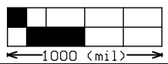
Symbol	Hit Count	Tool Size	Physical Length	Rout Path Length	Plated	Hole Type
□	119	10mil (0.254mm)			PTH	Round
○	80	15mil (0.381mm)			PTH	Round
✡	8	40mil (1.016mm)			PTH	Round
▽	2	44mil (1.118mm)			PTH	Round
⌘	2	67mil (1.702mm)			PTH	Round
⌔	4	60mil (1.524mm)	203mil (5.156mm)	143mil (3.632mm)	PTH	Slot
	215 Total					

Slot definitions : **Rout Path Length** = Calculated from tool start centre position to tool end centre position.
Physical Length = Rout Path Length + Tool Size = Slot length as defined in the PCB layout

Drill Table

ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7819	
LAYER NAME = Drill Drawing	ARTWORK # = 880007819.pcb_minorRev	
PLOT NAME = Drill Drawing	GENERATED : 6/14/2012 3:48:05 PM	NATIONAL SEMICONDUCTOR





ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7819	
LAYER NAME = M2 Board Dimensions	ARTWORK # = 880007819.pcb_minorRev	
PLOT NAME = Board Dimensions	GENERATED : 6/14/2012 3:48:06 PM	NATIONAL SEMICONDUCTOR

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