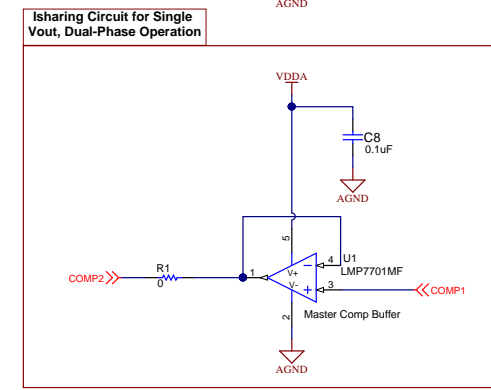


5.0Vout @ 45A MAX
(5.0V @ 22.5A / Phase)

Input Voltage = 6Vin to 18Vin
(5.5Vin Min.; 42Vin Peak)

FB1 = VDDA => Vout = 3.3V
FB1 = GND => Vout = 5.0V
OR use RDIV for 3.8Vout



Orderable: PMP15026	Designed for:	Mod. Date: 6/16/2017	
TID # PMP15032	Project Title: LMS140 Dual Interleaved Sync Buck (AEG)	Sheet: 1 of 2	
Number: PMP15032	Rev: A	Assembly Variant: 001	
SVN Rev: Unknown revision	File: PMP15032A_SchDoc	Size: C	
Drawn By:	Contact: http://www.ti.com/support	© Texas Instruments 2016	

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H1
SJ61A2

H2
SJ61A2

H3
SJ61A2

H4
SJ61A2

DNP
FID1

DNP
FID2

DNP
FID3

DNP
FID4

DNP
FID5

DNP
FID6

PCB Number: PMP15032
PCB Rev: A

LOGO2
CAUTION HOT SURFACE

LOGO3
CAUTION HOT SURFACE

Label Table	
Variant	Label Text
001	

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Orderable: PMP15026	Designed for:	Mod. Date: 6/16/2017
TID #: PMP15032	Project Title: LM5140 Dual Interleaved Sync Buck (AEQ)	
Number: PMP15032	Rev: A	Sheet Title: Hardware
SVN Rev: Unknown revision	Assembly Variant: 001	Sheet: 2 of 2
Drawn By:	File: PMP15032A-HW.SchDoc	Size: B
Engineer: T Allinder	Contact: http://www.ti.com/support	



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