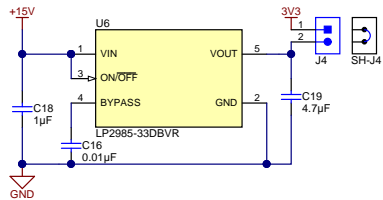
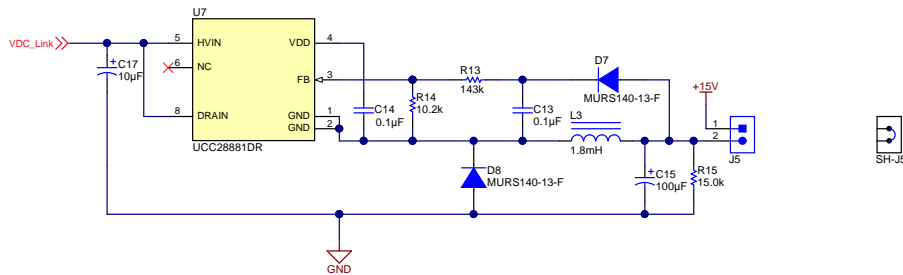
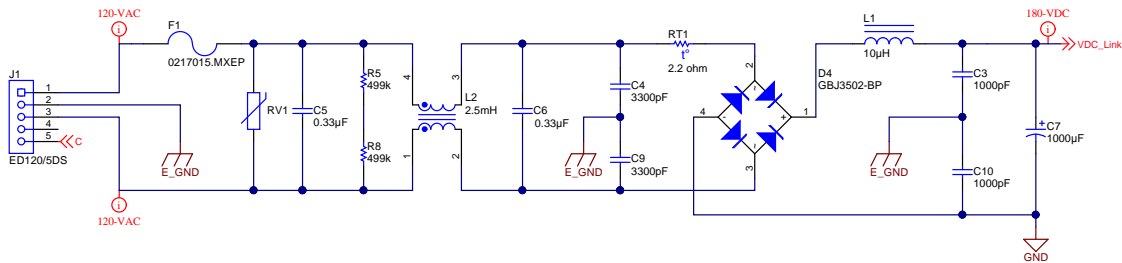


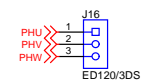
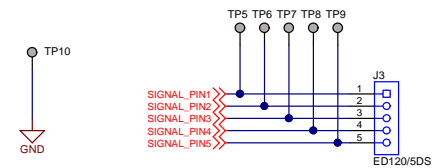
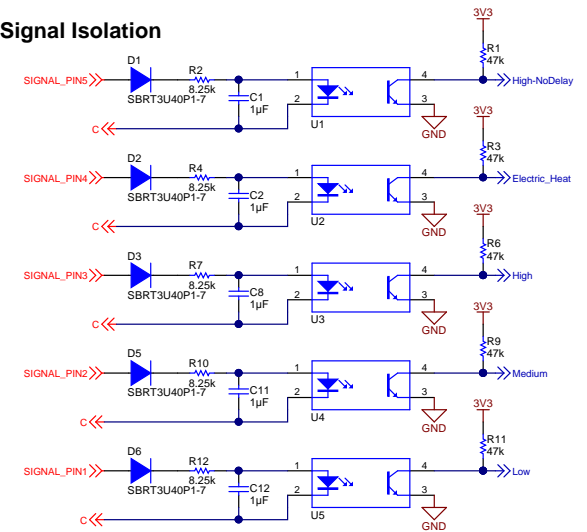
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TID #: TIDA-01353	Project Title: TIDA-01353	
Number: TIDA-01353   Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 1 of 5
Drawn By:	File: Block Diagram_SchDoc	Size: B
Engineer: Brian Dempsey	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	



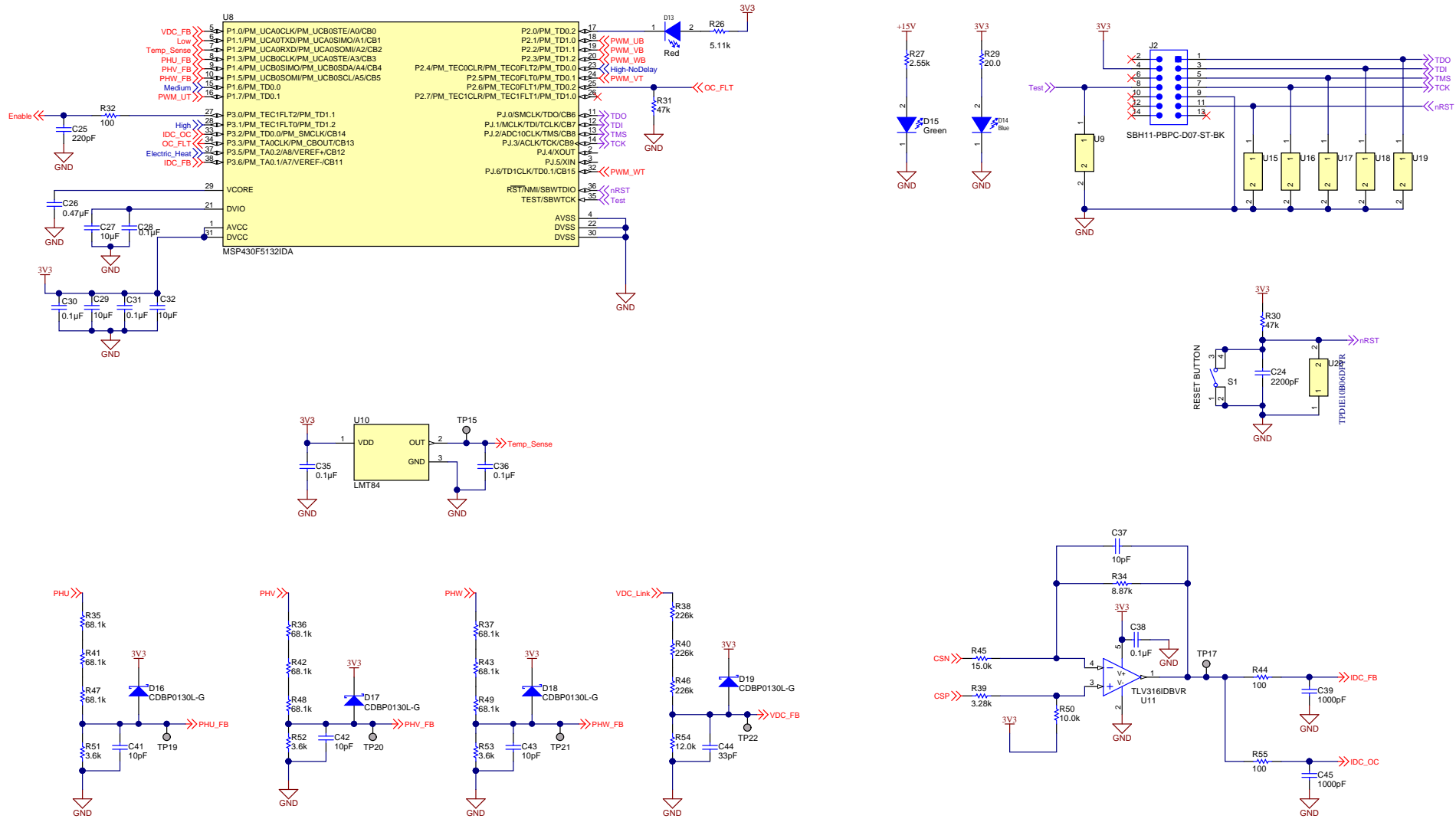


### Signal Isolation



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TID #: TIDA-01353	Project Title: TIDA-01353	
Number: TIDA-01353   Rev: E1	Sheet Title:	
SVN Rev. Version control disabled	Assembly Variant: 001	Sheet: 2 of 5
Drawn By:	File: TIDA-01353_System Power_SchDoc	Size: B
Engineer: Brian Dempsey	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

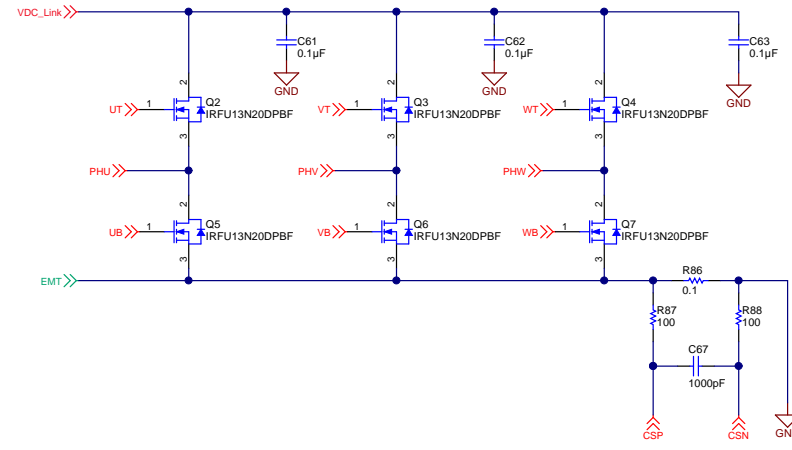
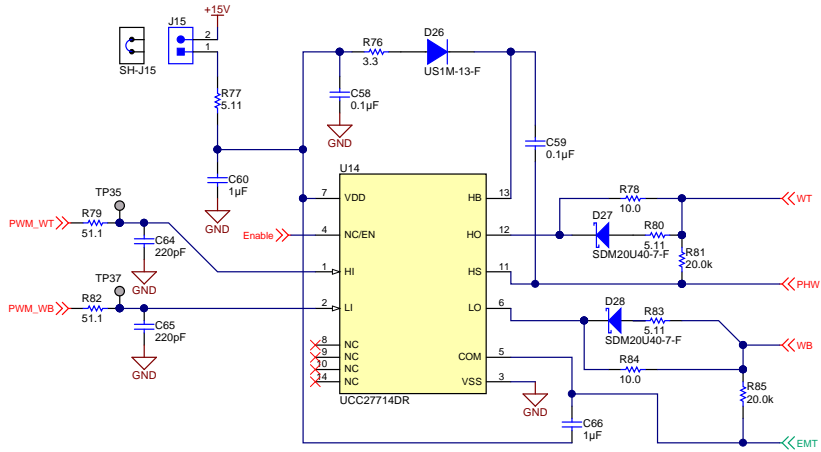
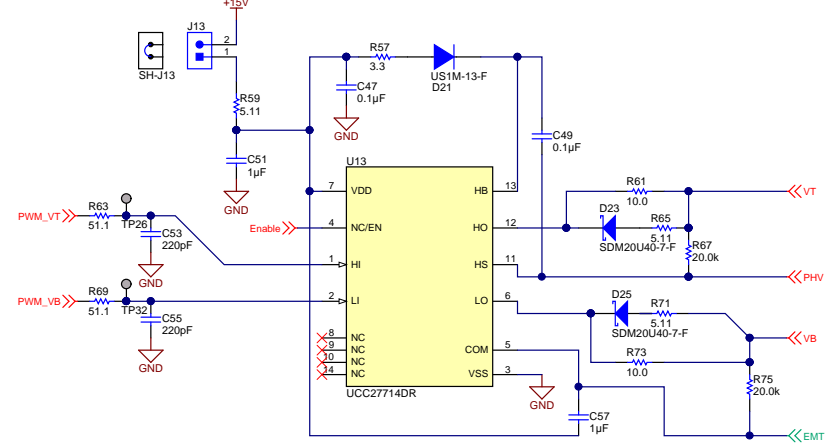
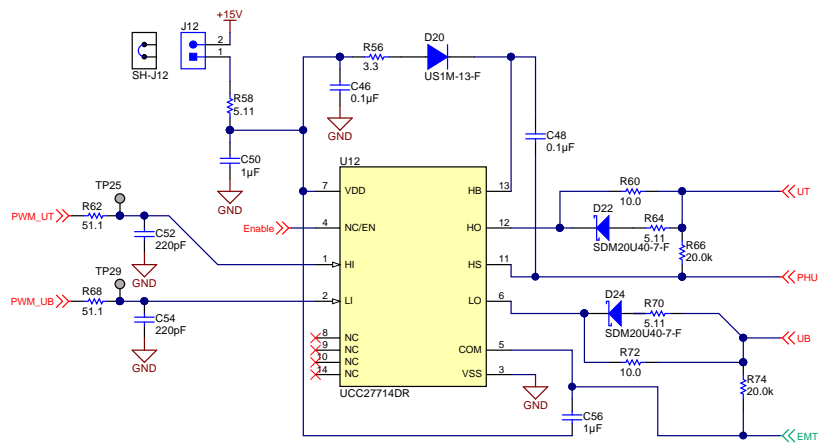


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TID #: TIDA-01353	Project Title: TIDA-01353	
Number: TIDA-01353   Rev: E1	Sheet Title:	
SVN Rev. Version control disabled	Assembly Variant: 001	Sheet: 3 of 5
Drawn By:	File: TIDA-01353_MCU and Peripherals_SchDoc	Size: B
Engineer: Brian Dempsey	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	



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TID #: TIDA-01353	Project Title: TIDA-01353	
Number: TIDA-01353   Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 4 of 5
Drawn By:	File: TIDA-01353_Motor Control SchDoc	Size: B
Engineer: Brian Dempsey	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	



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H1 1 NY PMS 440 0025 PH  
 H2 1 NY PMS 440 0025 PH  
 H3 1 NY PMS 440 0025 PH  
 H4 1 NY PMS 440 0025 PH

H5 1902C  
 H6 1902C  
 H7 1902C  
 H8 1902C

DNP FID1  
 DNP FID2  
 DNP FID3  
 DNP FID4  
 DNP FID5  
 DNP FID6

PCB Number: TIDA-01353  
 PCB Rev: E1  
 PCB LOGO Texas Instruments  
 PCB LOGO Pb-Free Symbol  
 PCB LOGO FCC disclaimer

HIGH VOLTAGE  
 PCB LOGO Logo5  
 PCB LOGO Logo6  
 Hot Surface

Variant	Label Text
001	-001

LBL1  
 PCB Label  
 Size: 0.65" x 0.20"

ZZ1  
 Label Assembly Note  
 This Assembly Note is for PCB labels only

ZZ2  
 Assembly Note  
 These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3  
 Assembly Note  
 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4  
 Assembly Note  
 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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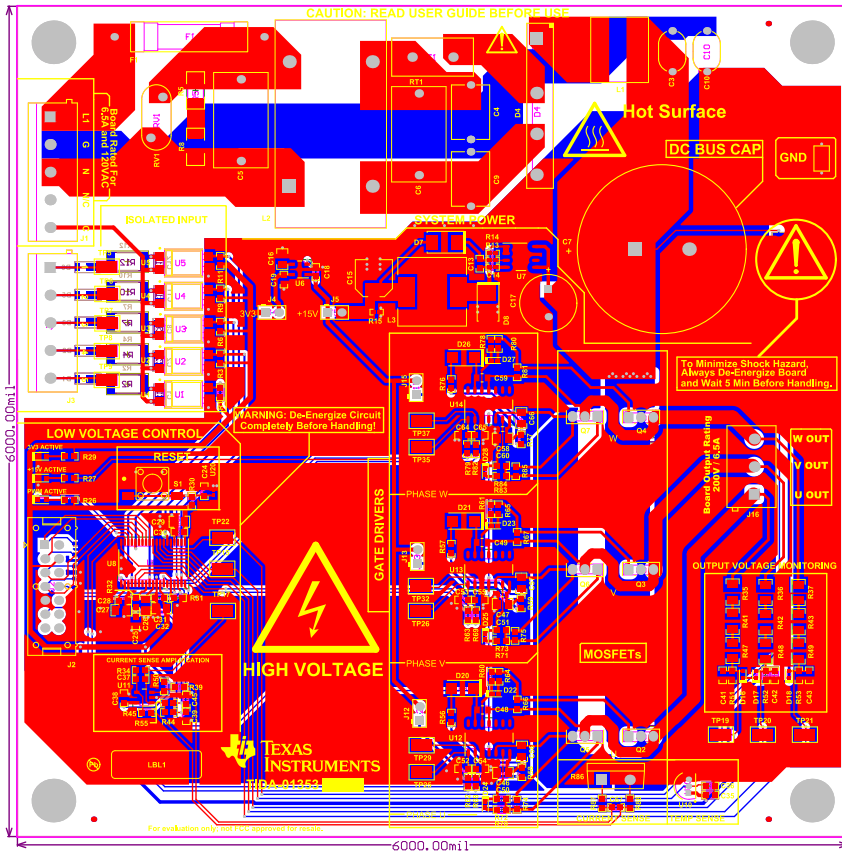
Orderable: N/A	Designed for: Public Release	Mod. Date: 11/23/2016
TID #: TIDA-01353	Project Title: TIDA-01353	
Number: TIDA-01353   Rev: E1	Sheet Title:	
SVN Rev. Version control disabled	Assembly Variant: 001	Sheet: 5 of 5
Drawn By:	File: TIDA-01353_EVM_Hardware.SchDoc	Size: B
Engineer: Brian Dempsey	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	



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Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	2.80mil		
4	Dielectric	FR-4 High TG	56.00mil	4.8	
5	Bottom Layer	Copper	2.80mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	
7	Bottom Overlay				

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.  
 Z22 ■ These assemblies are ESD sensitive. ESD precautions shall be observed.  
 Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.  
 Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 8\_MIL  
 MIN. CLEARANCE: 0.2 mm  
 MIN. VIA PAD SIZE: 22\_MIL  
 MINIMUM ANNULAR RING 0.15mm (6MIL) EXTERNAL  
 PER IPC-D-275 CLASS 2 LEVEL C  
 REGISTRATION TOLERANCES: METAL +/- 5\_MIL, HOLES +/- 3\_MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3\_MIL

**MATERIAL:**

FR-408  FR-4 High Tg  OTHER \_\_\_\_\_  
 THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER \_\_\_\_\_  
 TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_  
 BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES  
 PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM  
 SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_  
 SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENEPG  
 IM. TN/SILVER OR EQUIV  OTHER \_\_\_\_\_

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:**

ANSI IPC-A-600F CLASS ->  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**

MICROSECTION:  YES  
 BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER

COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED OR PLACED ON BOARD TO MINIMIZE SHOCK HAZARD. ALWAYS DE-ENERGIZE BOARD AND WAIT 5 MIN BEFORE HANDLING.  
 ASSEMBLY VARIANT: [No Variations]

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**TEXAS INSTRUMENTS**

PROJECT TITLE:  
TIDA-01353

DESIGNED FOR:  
Public Release

FILE NAME:  
TIDA-01353.PcbDoc

ENGINEER:  
Brian Dempsey

LAYOUT BY:  
Krypton Solutions/RS

SCALE: 1.00

ALTIUM DESIGNER VERSION:  
16.1.12.290

ADDITIONAL COMMENTS FROM TOP/SIDE	BOARD #	DATE	DESIGNED BY	DESIGNED FOR	DATE	DESIGNED BY	DESIGNED FOR
LAYER NAME = TOP	TID #:	DATE	DESIGNED BY	DESIGNED FOR	DATE	DESIGNED BY	DESIGNED FOR
PLACEMENT IN TOP Layer	DATE	DESIGNED BY	DESIGNED FOR	DATE	DESIGNED BY	DESIGNED FOR	DESIGNED FOR

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