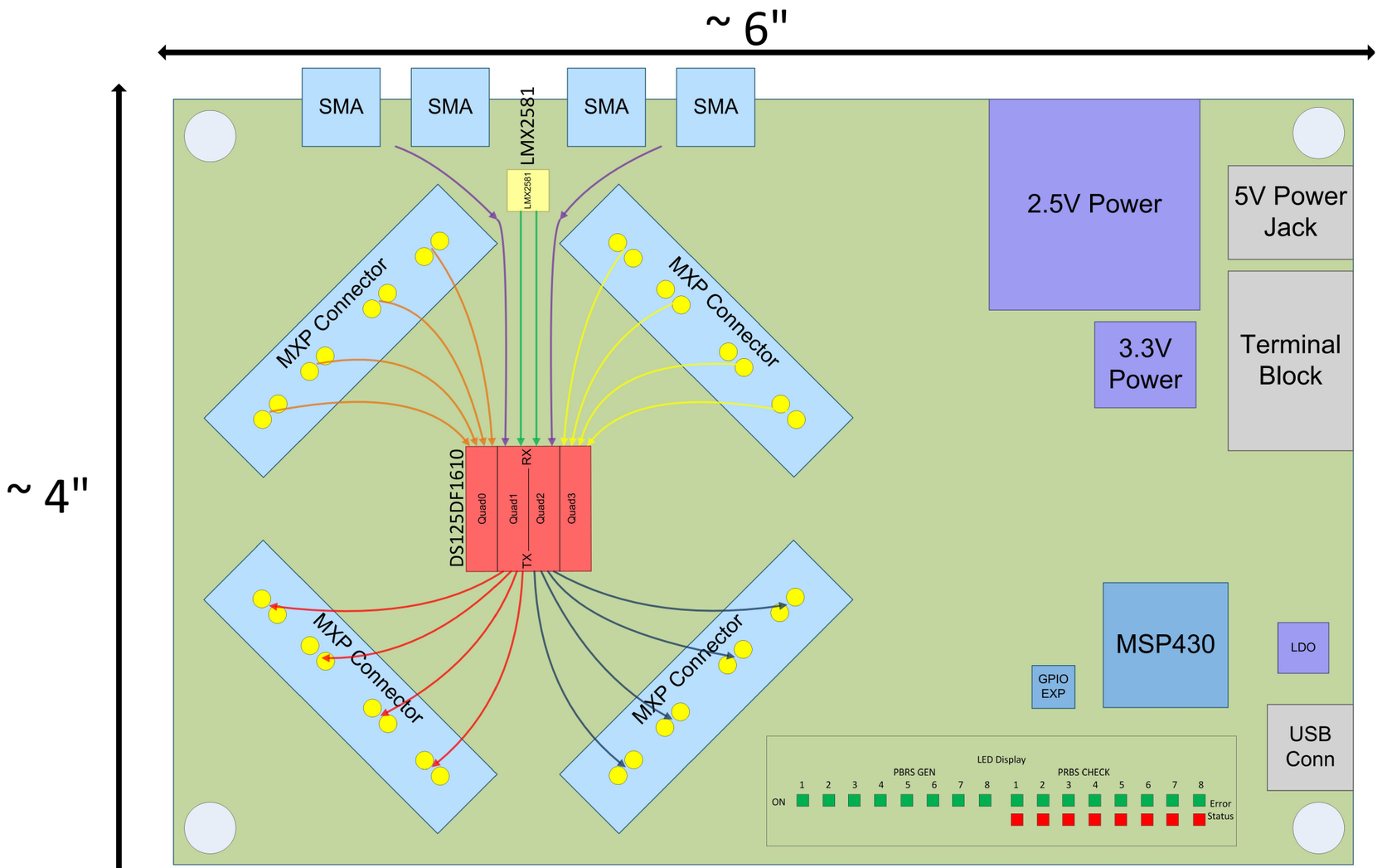
Notes:

1. High-speed traces:
   - Minimize trace length from device to MXP connectors
   - Target 100 Ohm differential impedance
   - When traces break to connectors, the impedance should be 50 ohm single-ended
   - Tightly couple within a pair; be careful not to couple between pairs
   - Implement stripline routing with 6 mil trace width and 9 mil spacing
   - Backdrill differential through holes
2. The goal is to make the board as small as possible. The placement below is a recommendation
3. There should be four thru-holes on the four corners so that the board may be mounted with mechanical standoffs
4. OK to put MSP430 and power circuitry on the bottom side (except for LEDs and test points)
5. AC coupling caps on the TX nets should have GND cut outs
6. Add ground fill to increase board stiffness
7. Any silkscreen notes you wish to add are okay - the more silkscreen comments the better

Revision History	
Revision	Notes
A0	First revision



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TID #: 00426	Project Title: 12-Gbps BERT Board Reference Design	
Number: TIDA-00426 Rev: A0	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 1 of 8
Drawn By:	File: CoverSheet.SchDoc	Size: B
Engineer: Gui Borba	Contact: http://www.ti.com/support	

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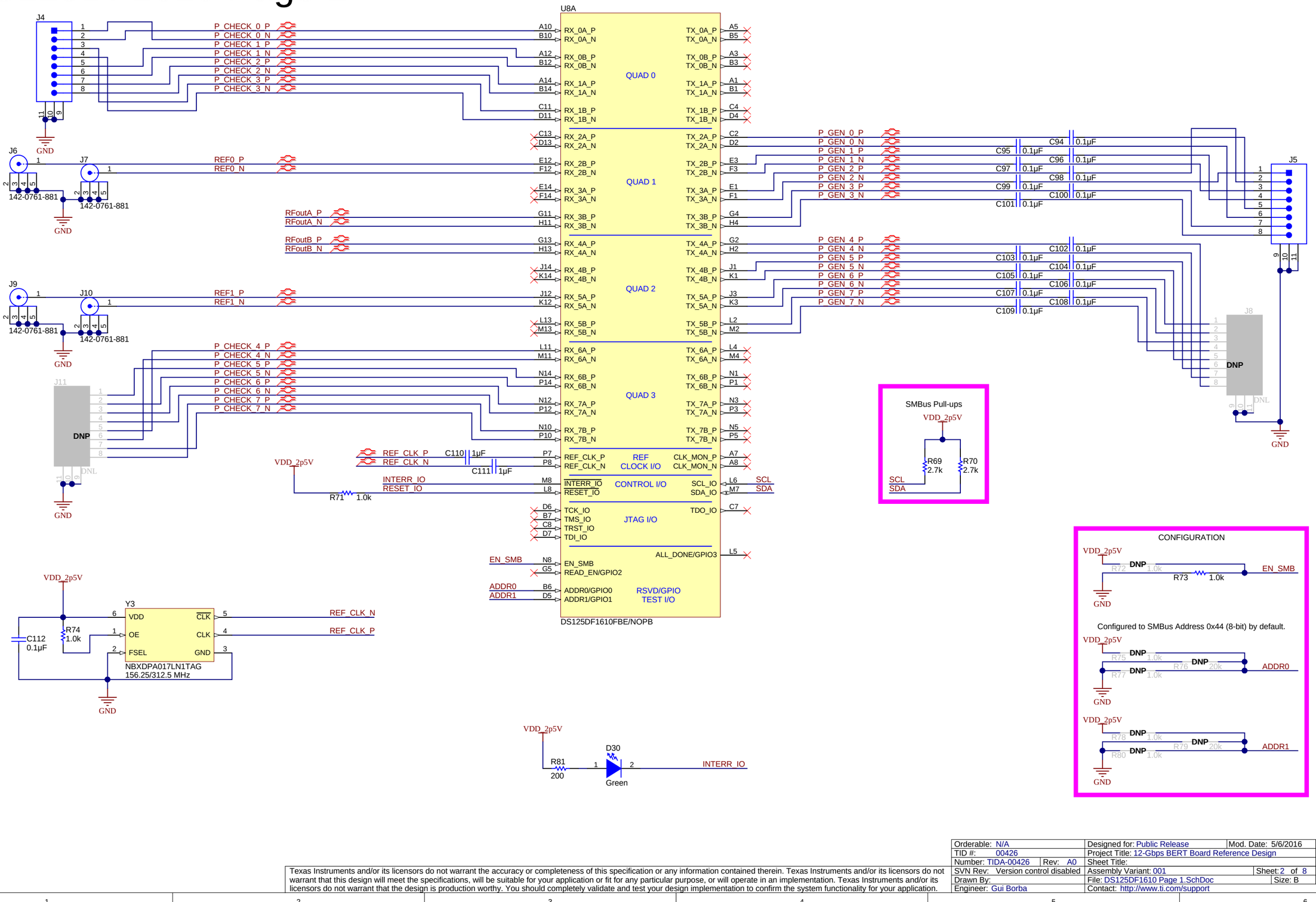

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Number: TIDA-00426	Rev: A0	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: 001	Sheet: 2 of 8
Drawn By:		File: DS125DF1610 Page 1.SchDoc	Size: B
Engineer: Gui Borba		Contact: http://www.ti.com/support	

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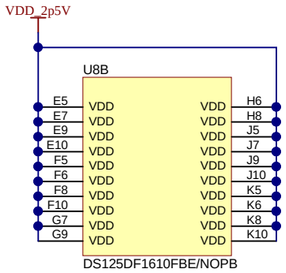

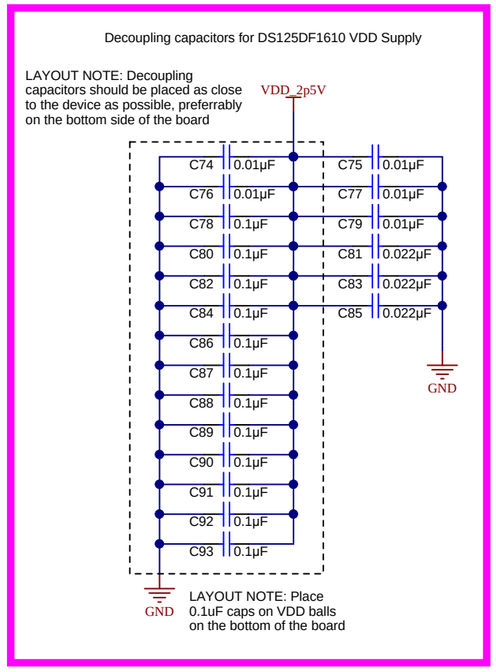

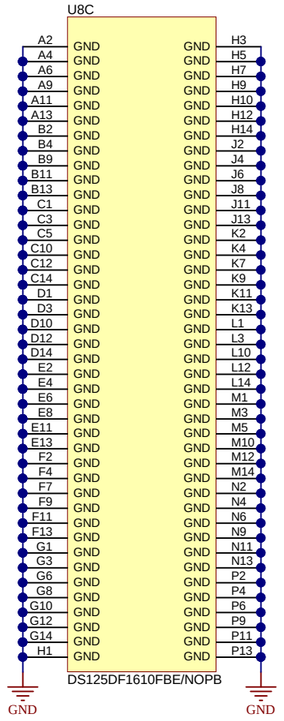

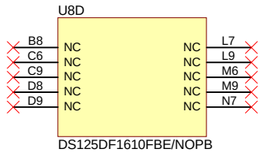

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SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 3 of 8
Drawn By:	File: DS125DF1610 Page 2.SchDoc	Size: B
Engineer: Gui Borba	Contact: http://www.ti.com/support	

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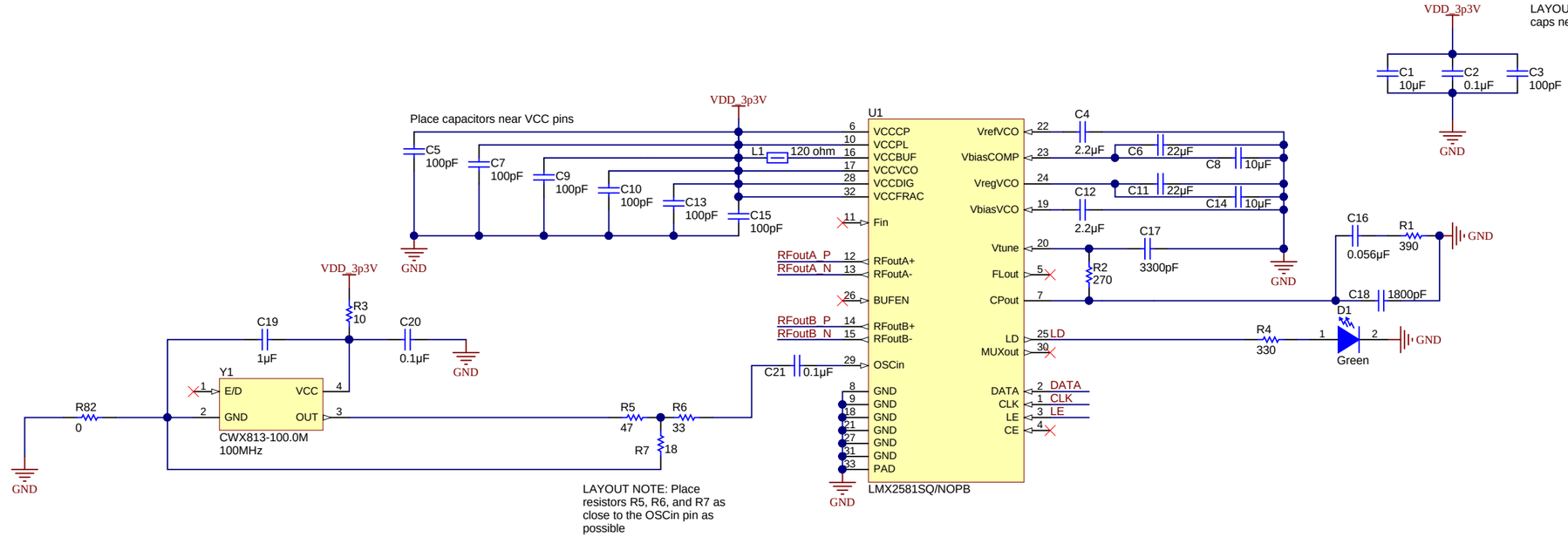
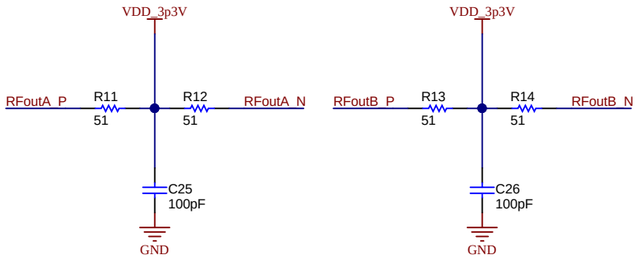
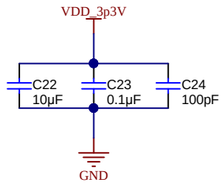
FREQUENCY SYNTHESIZER

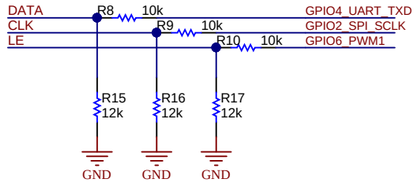


LAYOUT NOTE: Place resistor pull-ups as close to the chip as possible and keep their traces short





LAYOUT NOTE: Place caps near the part



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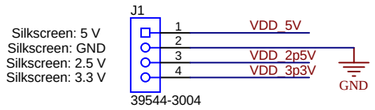
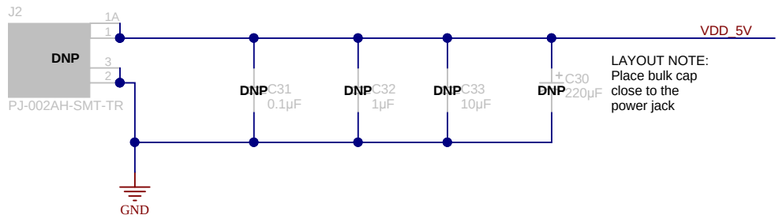
Number: TIDA-00426 Rev: A0	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 4 of 8
Drawn By:	File: LMX.SchDoc	Size: B
Engineer: Gui Borba	Contact: http://www.ti.com/support	

POWER



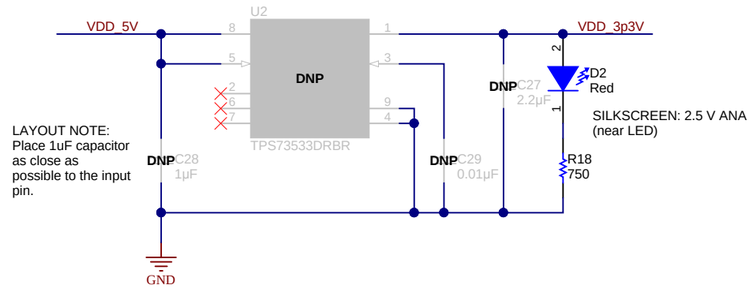
LAYOUT NOTE: Place barrell connector and terminal block close to each



LAYOUT NOTE: Place bulk cap close to the power jack

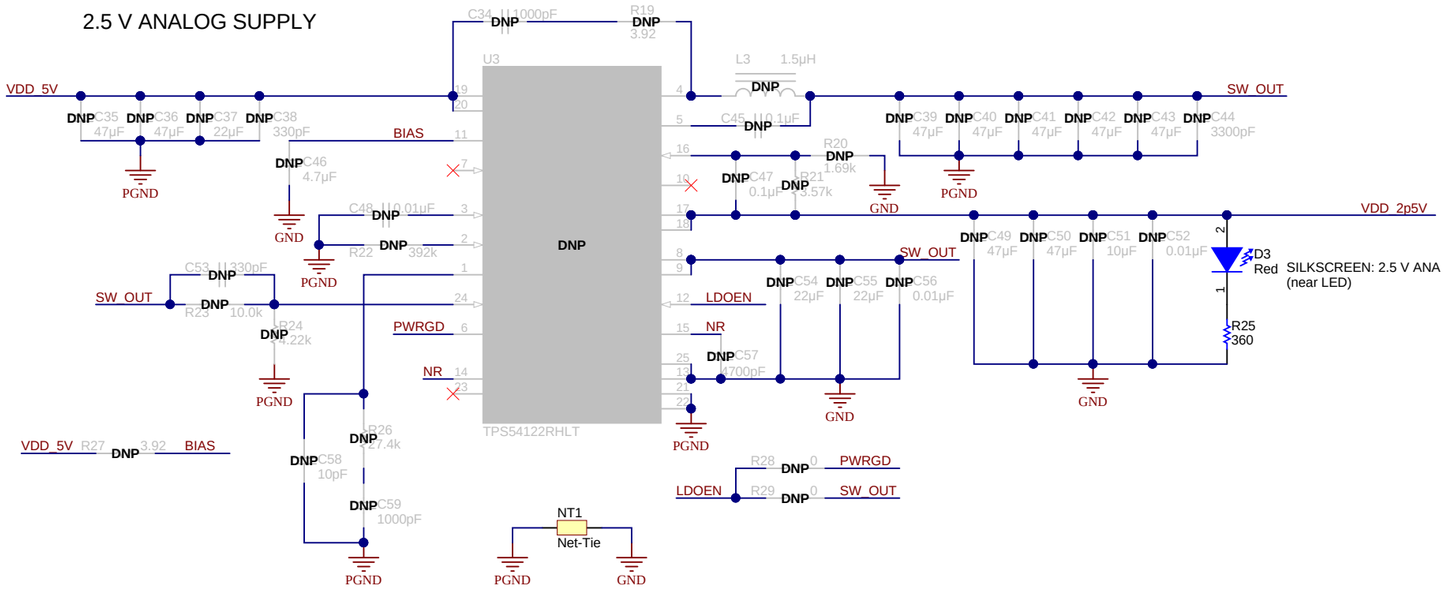
LAYOUT NOTE: power may be placed on the bottom layer, but LEDs must be placed on the top layer

3.3 V ANALOG SUPPLY



LAYOUT NOTE: Place 1uF capacitor as close as possible to the input pin.

2.5 V ANALOG SUPPLY



LAYOUT NOTES:
- Place the inductor, boot capacitor, and output capacitor of the dc-dc converter on the layers of the board (such as the bottom layer) that help minimize the spread of switching noise into the LDO area on the board.
- Connect the boot capacitor and inductor L1 as close as possible to the PH pin to reduce parasitic inductance of long traces.
- To help shield the compensation components (the soft-start capacitors, the CLK/RT resistor, and the dc-dc feedback resistors) from noise, ground these components to a power ground that is shielded from the highcurrent ground plane. To achieve this shielding, use a separate trace to the PGND pin.
- The RT/CLK pin is sensitive to noise so place the RT resistor as close as possible to the device, routed with a short connection.
- Place the noise-reduction capacitor as close as possible to the device to avoid noise pickup into the LDO reference.
- Isolate the ground planes on the input and output from each other, connected through a separate trace route that parallels the power-loop routing from the dc-dc output to the LDO input.
- Terminate the low-noise analog ground of the LDO circuits (such as the voltage set point divider, the LDO input, and output capacitors) to ground using a wide ground trace separate from the power ground plane.
- Place the LDO input and output capacitors as close to the device as possible.
- Bypass the VIN pin to ground using a low-ESR ceramic capacitor with an X5R or X7R dielectric, placed as close as possible to the VIN and PGND pins.
- For operation at the full-rated load, the top-side ground area together with the internal ground plane must provide adequate heat dissipation.
- Minimize PCB conductor planes to prevent excessive capacitive coupling.
- Use TID-0338 as an example (more info can also be found in SLVU829)

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Number: TIDA-00426 Rev: A0	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 5 of 8
Drawn By:	File: Power.SchDoc	Size: B
Engineer: Gui Borba	Contact: http://www.ti.com/support	

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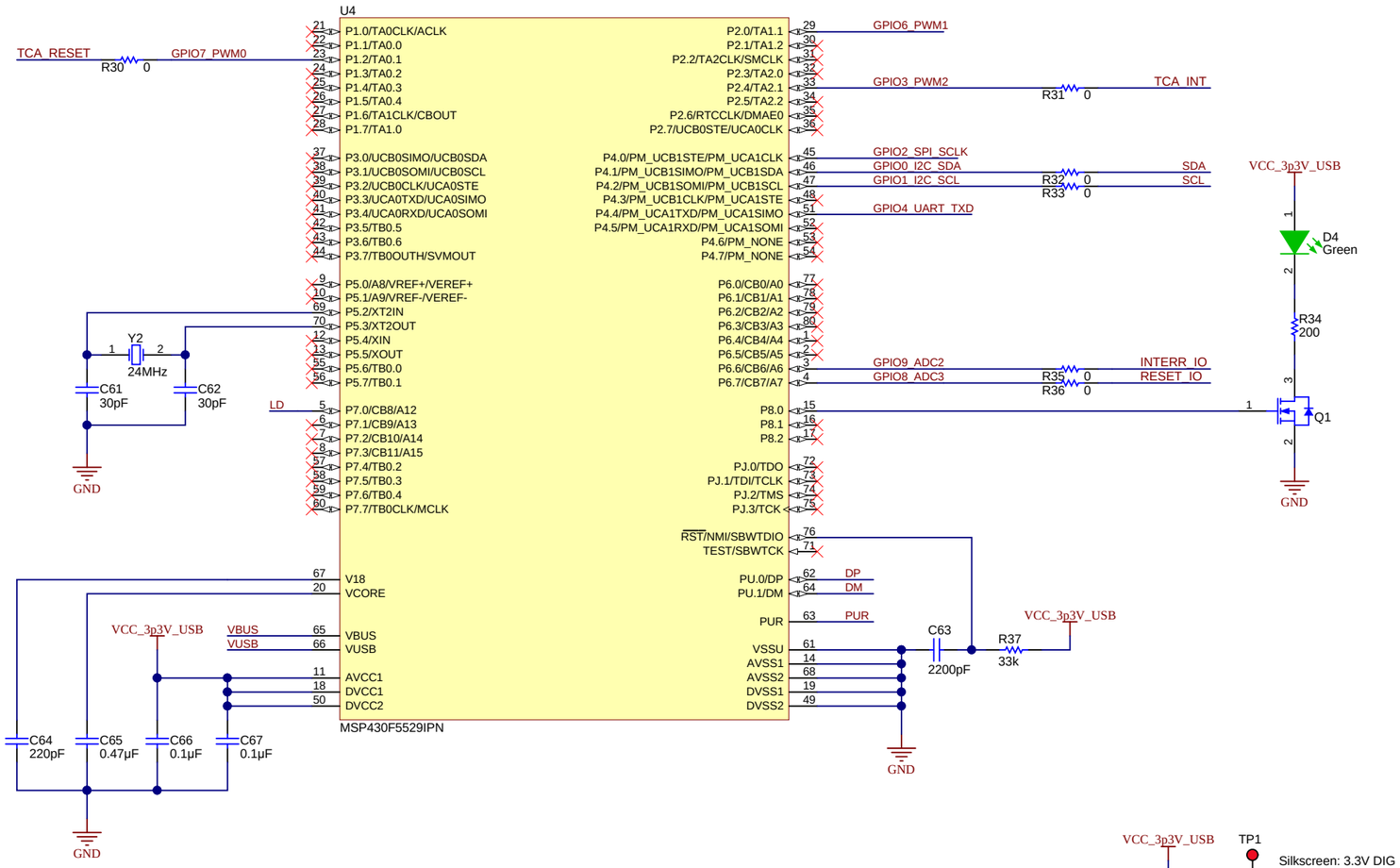
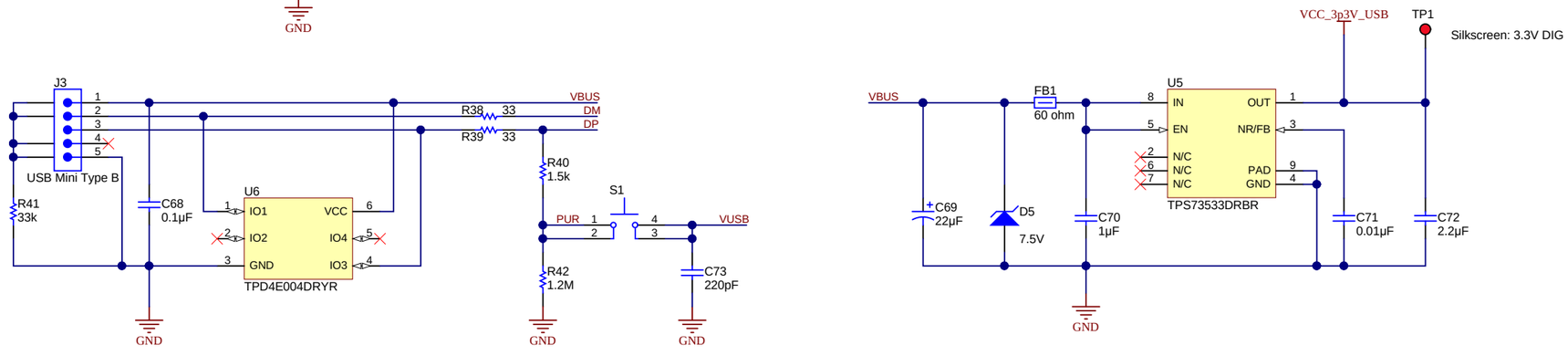
USB2ANY





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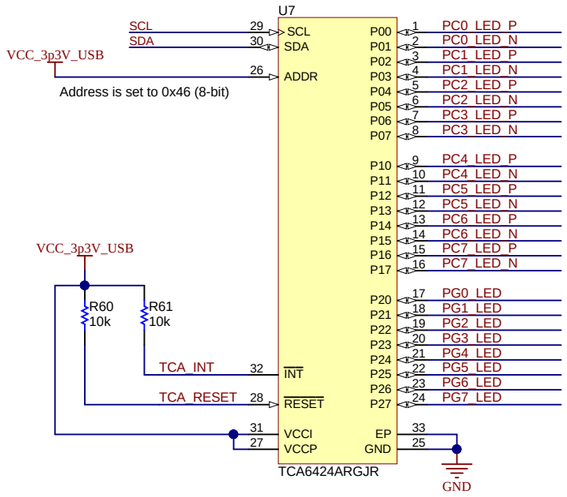
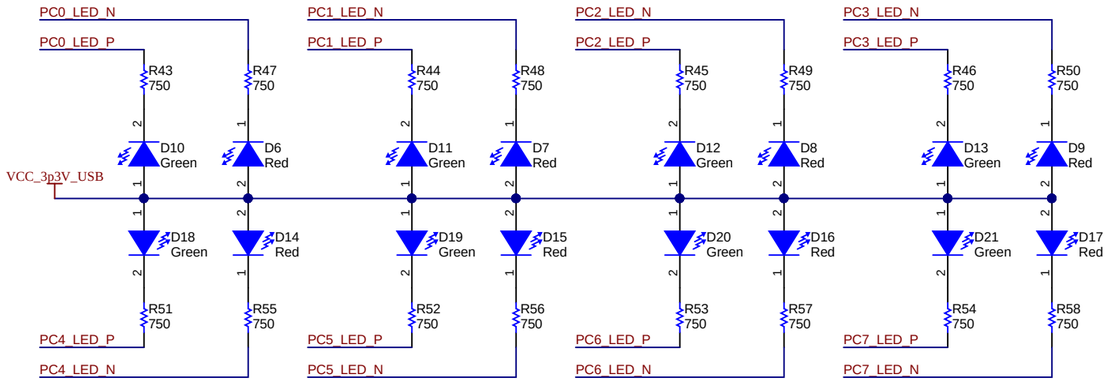
SVN Rev: Version control disabled		Assembly Variant: 001	Sheet: 6 of 8
Drawn By:		File: USB2ANY.SchDoc	Size: B
Engineer: Gui Borba		Contact: http://www.ti.com/support	

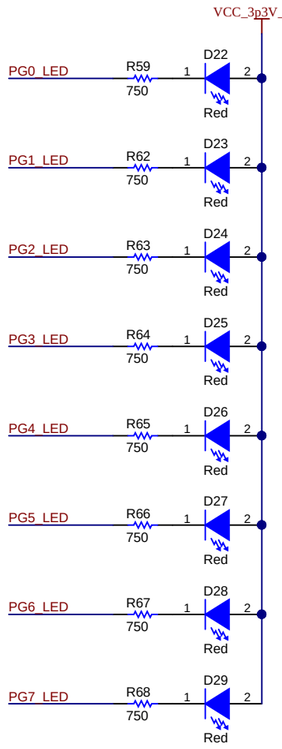


Pattern checker "ERROR STATUS" indicator LEDs



SILKSCREEN: Create a box around this section with a title "Pattern Checker Error Status Indicators" and label each diode with the channel name i.e "PC0", "PC1" etc

Pattern Generator "POWER ON" Indicator LEDs



SILKSCREEN: Create a box around this section with a title "Pattern Generator Power On Indicators" and label each diode with the channel name i.e "PG0", "PG1" etc

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Number: TIDA-00426 Rev: A0	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 7 of 8
Drawn By:	File: LED Indicator.SchDoc	Size: B
Engineer: Gui Borba	Contact: http://www.ti.com/support	

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H2
NY PMS 440 0025 PH

H3
NY PMS 440 0025 PH

H4
NY PMS 440 0025 PH

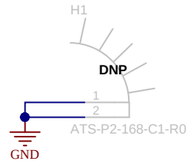
H5
NY PMS 440 0025 PH

H6
1902C

H7
1902C

H8
1902C

H9
1902C



DNP
FID1

DNP
FID2

DNP
FID3

PCB Number: TIDA-00426
PCB Rev: A0

PCB
LOGO
Texas Instruments

PCB
LOGO
Pb-Free Symbol

Label Table	
Variant	Label Text
001	8CH_EXT-PSU
002	8CH_INT-PSU
003	16CH_EXT-PSU
004	16CH_INT-PSU

ZZ1
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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Number: TIDA-00426 Rev: A0	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 8 of 8
Drawn By:	File: TID_Hardware.SchDoc	Size: B
Engineer: Gui Borba	Contact: http://www.ti.com/support	

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