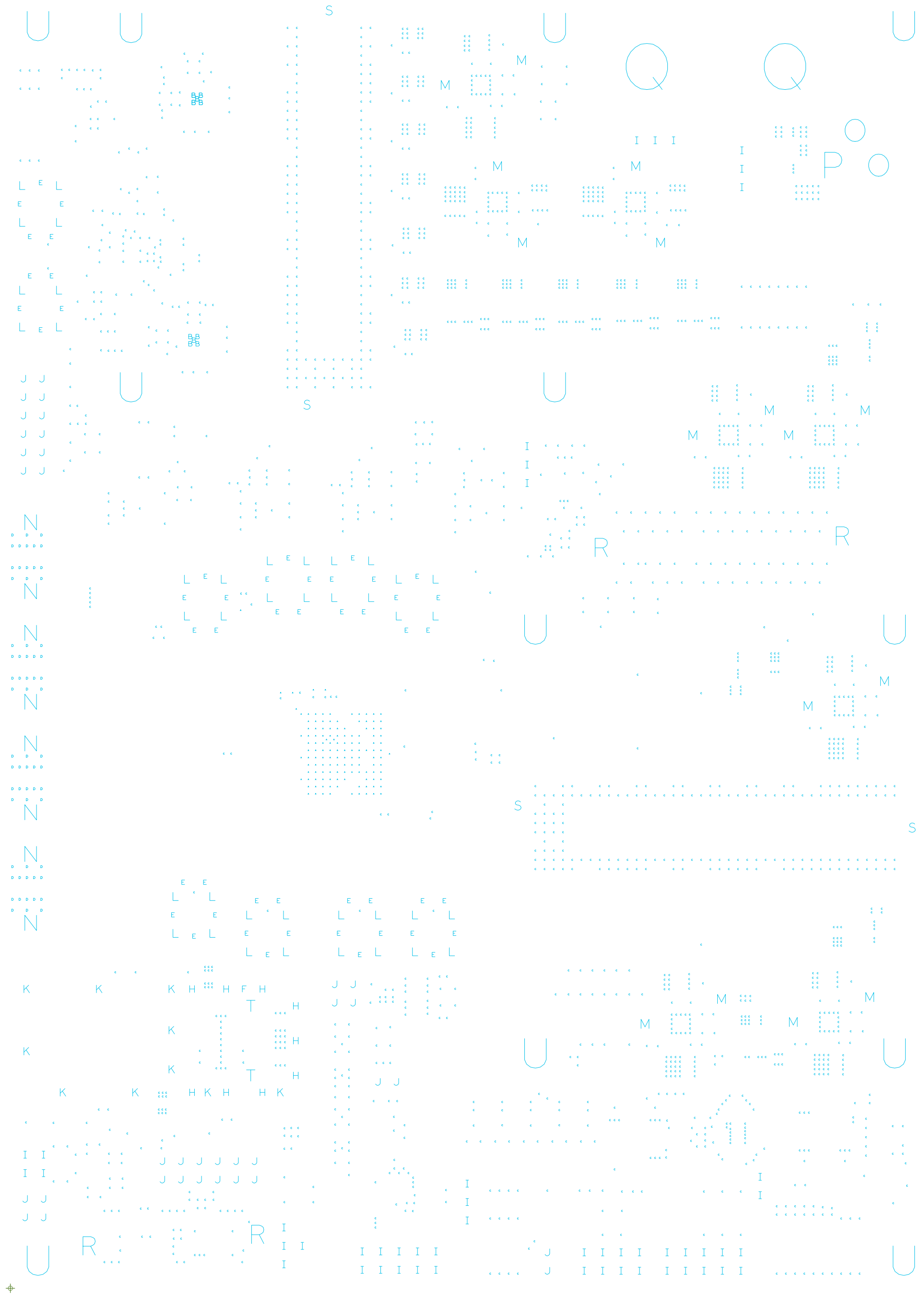
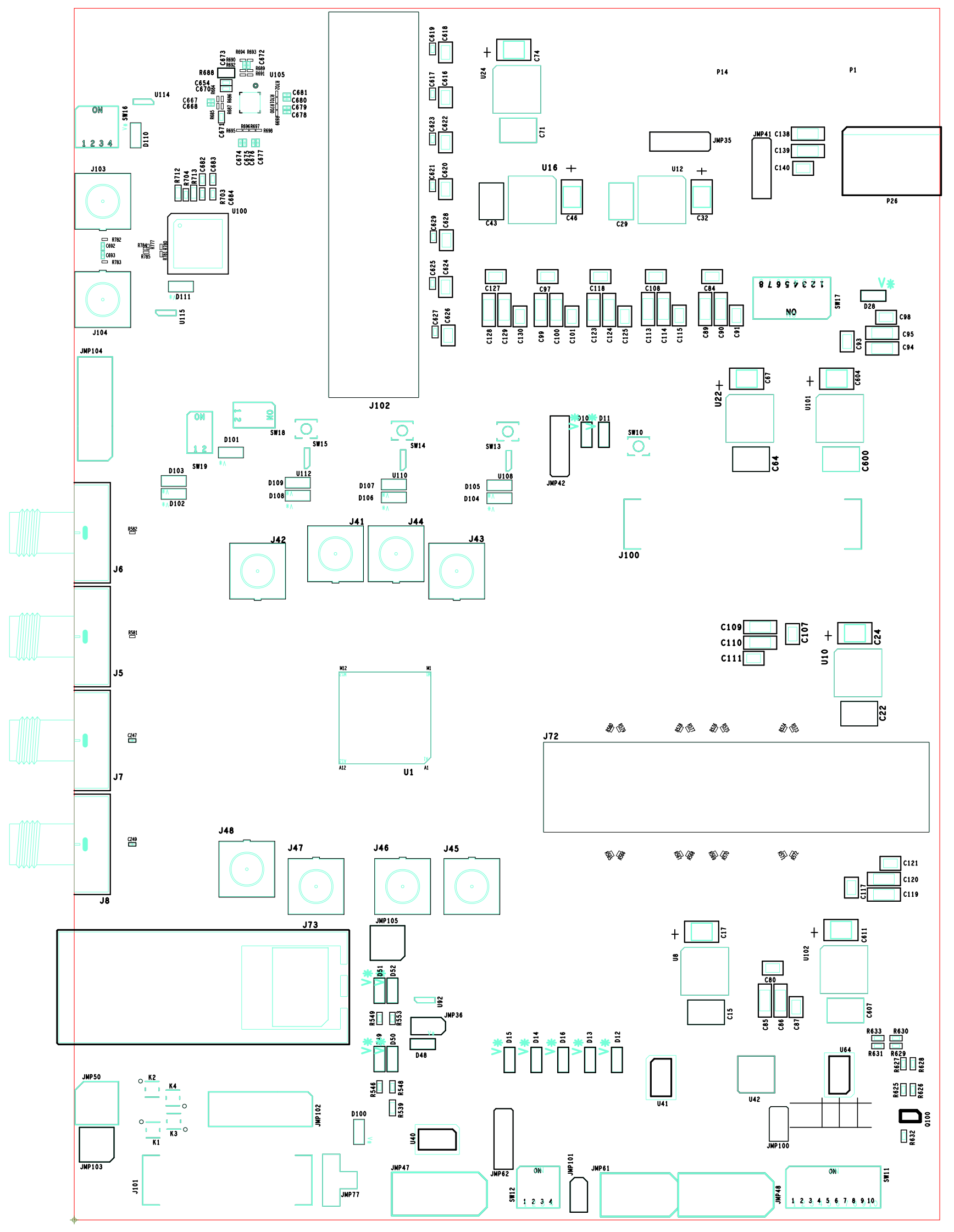


DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
A	6.0	+0.0/-0.0	PLATED	129
B	8.0	+0.0/-8.0	PLATED	15
C	8.0	+3.0/-12.0	PLATED	2085
D	12.2	+3.0/-3.0	PLATED	64
E	24.0	+0.0/-0.0	PLATED	50
F	33.46	+0.0/-0.0	PLATED	1
H	37.4	+0.0/-0.0	PLATED	9
I	38.0	+0.0/-0.0	PLATED	50
J	38.0	+0.0/-0.0	PLATED	36
K	41.34	+0.0/-0.0	PLATED	10
L	44.0	+0.0/-0.0	PLATED	40
M	50.0	+0.0/-0.0	PLATED	16
N	82.68	+3.0/-3.0	PLATED	8
O	120.0	+2.0/-2.0	PLATED	2
P	140.0	+0.0/-0.0	PLATED	1
Q	250.0	+0.0/-0.0	PLATED	2
R	47.01	+0.0/-0.0	NON-PLATED	4
S	50.0	+0.0/-0.0	NON-PLATED	4
T	61.02	+0.0/-0.0	NON-PLATED	2
U	130.0	+0.0/-0.0	NON-PLATED	12

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	TLK10xxx EVM MOTHER BOARD	04/16/13	J. NERGER



UNLESS OTHERWISE SPECIFIED	SIGNATURES		DATE
DIMENSIONS ARE IN INCHES TOLERANCES ON; 2 PL DECIMALS ± 3 PL DECIMALS ± ANGLES ± FRACTIONS ±	DRAWN	LT/DFW TEST	04/16/13
	CHECKED	J. NERGER	04/16/13
	ENGRG	J. NERGER	04/16/13
	ISSUED	J. NERGER	04/16/13

Texas Instruments Inc.
12500 TI Boulevard
Dallas, TX 75243

ASSEMBLY

TLK10xxx EVM MOTHER BOARD

SIZE

FSCM NO

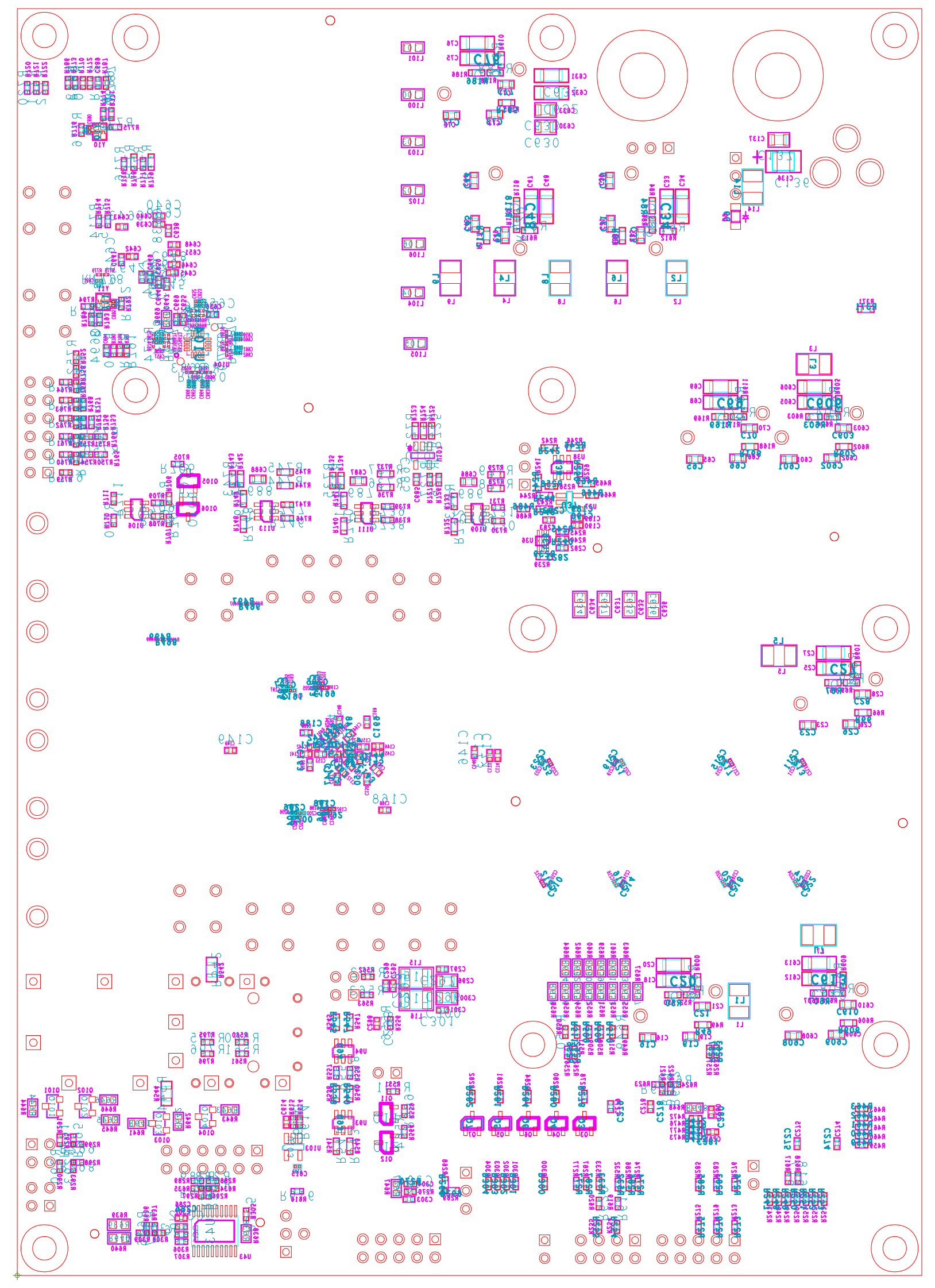
DWG NO 6566789

SCALE

SHEET **1 / 2**

WO# 73776

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	TLK10xxx EVM MOTHER BOARD	04/16/13	J. NERGER



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON;
2 PL DECIMALS ±
3 PL DECIMALS ±
ANGLES ±
FRACTIONS ±

SIGNATURES		DATE
DRAWN	LT/DFW TEST	04/16/13
CHECKED	J. NERGER	04/16/13
ENGRG	J. NERGER	04/16/13
ISSUED	J. NERGER	04/16/13

Texas Instruments Inc.
12500 TI Boulevard
Dallas, TX 75243

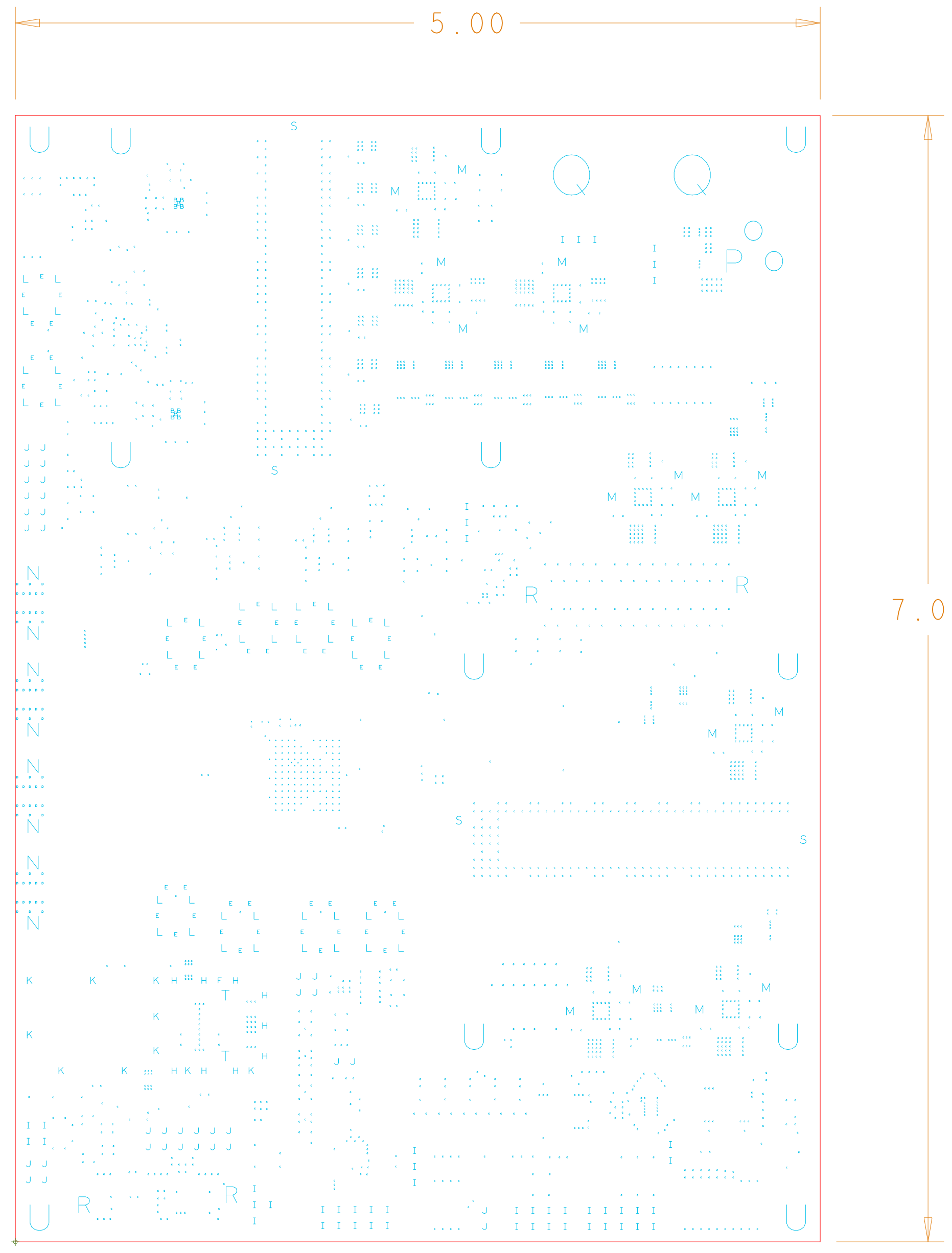
ASSEMBLY

TLK10xxx EVM MOTHER BOARD

SIZE
FSCM NO
DWG NO 6566789
SCALE
SHEET **2 / 2**

WO# 73776

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	TLK10xxx EVM MOTHER BOARD	04/16/13	J. NERGER



DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
A	6.0	+0.0/-0.0	PLATED	129
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P	140.0	+0.0/-0.0	PLATED	1
Q	250.0	+0.0/-0.0	PLATED	2
R	47.01	+0.0/-0.0	NON-PLATED	4
S	50.0	+0.0/-0.0	NON-PLATED	4
T	61.02	+0.0/-0.0	NON-PLATED	2
U	130.0	+0.0/-0.0	NON-PLATED	12

TOP
LAYER 1 — Copper Foil 0.5oz / Plate to 1.0oz min Layer 1
ROGERS 4350 — Pre-preg 0.005" (material)
LAYER 2
FR-4 — Core 0.005" 1.0oz / 1.0oz Layer 2 & 3
LAYER 3
FR-4 — Pre-preg 0.010" (material)
LAYER 4
FR-4 — Core 0.005" 1.0oz / 1.0oz Layer 4 & 5
LAYER 5
FR-4 — Pre-preg 0.005" (material)
LAYER 6
FR-4 — Core 0.005" 1.0oz / 1.0oz Layer 6 & 7
LAYER 7
FR-4 — Pre-preg 0.010" (material)
LAYER 8
FR-4 — Core 0.005" 1.0oz / 1.0oz Layer 8 & 9
LAYER 9
FR-4 — Pre-preg 0.010" (material)
LAYER 10
FR-4 — Core 0.005" 1.0oz / 1.0oz Layer 10 & 11
LAYER 11
FR-4 — Pre-preg 0.005" (material)
LAYER 12
FR-4 — Core 0.005" 1.0oz / 1.0oz Layer 12 & 13
LAYER 13
FR-4 — Pre-preg 0.010" (material)
LAYER 14
FR-4 — Core 0.005" 1.0oz / 1.0oz Layer 14 & 15
LAYER 15
ROGERS 4350 — Pre-preg 0.005" (material)
LAYER 16 — Copper Foil 0.5oz / Plate to 1.0oz min Layer 14
BOTTOM

GENERAL NOTES. UNLESS OTHERWISE SPECIFIED

1. ALL FABRICATION ITEMS MUST MEET OR EXCEED BEST INDUSTRY PRACTICE : IPC-A-600C (Commercial std.)
2. LAMINATE MATERIAL : ROGERS 4350B or EQUIVALENT BETWEEN LAYERS 1 & 2 AND LAYERS 15 &16
   FR4 POLYCLAD OR EQUIVALENT FOR ALL OTHER LAYERS
3. COPPER WEIGHT : 1oz START INTERNAL, 1/2oz START EXTERNAL
4. FINISHED BOARD THICKNESS : .111 +/-10%
5. MAXIMUM WARP AND TWIST TO BE : .005 INCH PER INCH
6. MINIMUM COPPER WALL THICKNESS OF PLATED-THRU HOLES TO BE .001 INCH. THERE MUST BE 1MIL OR GREATER PLATING ON EACH SIDE OF THE BARREL WHEN VIEWED IN THE CROSS SECTION
7. MINIMUM ANNULAR RING OF PLATED-THRU HOLES TO BE .002 INCH
8. MINIMUM ALLOWABLE LINE REDUCTION TO BE 20% OR .002 WHICHEVER IS GREATER
9. 0.010 SIGNAL LINES ON LAYERS 1 & 16 TO BE IMPEDANCE CONTROLLED 50 OHMS +/- 10%
10. 0.006 SIGNAL LINES ON LAYER 3 & 14 TO BE IMPEDANCE CONTROLLED 50 OHMS +/- 10%
11. 0.004.5 SIGNAL LINES ON LAYER 1,3, & 16 TO BE IMPEDANCE CONTROLLED 100 OHMS +/- 10%
12. DIELECTRIC CONSTANTS ARE
    ROGERS 4350: 3.6
    FR4 POLYCLAD: 4.1
13. VIA'S IN SMT DEVICE PADS TO BE FILLED WITH NON-CONDUCTIVE EPOXY. ANY VOID IN THE FILL MATERIAL MUST NOT BE GREATER THAN 25% OF THE FINISHED HOLE DIAMETER. SEE DRILL NOTE #1
14. A CROSS SECTION MOUNT AND DIGITAL PHOTO'S OF VIA'S TO BE PROVIDED
15. USE THE (DRPP) DUTCH REVERSE PLATING PROCESS

PROCESS NOTES

1. CIRCUITRY ON OUTER LAYERS TO BE PLATED WITH : NICKEL GOLD
2. SOLDERMASK BOTH SIDES PER ARTWORK : BLUE LPI
3. SILKSCREEN BOTH SIDES PER ARTWORK : COLOR = WHITE

DRILL NOTES

1. 0.0081" DRILL SHOULD NOT BE EXPOY FILLED.
2. 0.0081" DRILL IS A REFERENCE NAME, ALL 0.0081" DRILLS SHOULD BE DRILLED TO 0.008".

UNLESS OTHERWISE SPECIFIED	SIGNATURES		DATE
DIMENSIONS ARE IN INCHES TOLERANCES ON; 2 PL DECIMALS + 3 PL DECIMALS + ANGLES + FRACTIONS +	DRAWN	LT/DFW TEST	04/16/13
	CHECKED	J. NERGER	04/16/13
	ENGRG	J. NERGER	04/16/13
	ISSUED	J. NERGER	04/16/13

Texas Instruments Inc.
12500 TI Boulevard
Dallas, TX 75243

FABRICATION

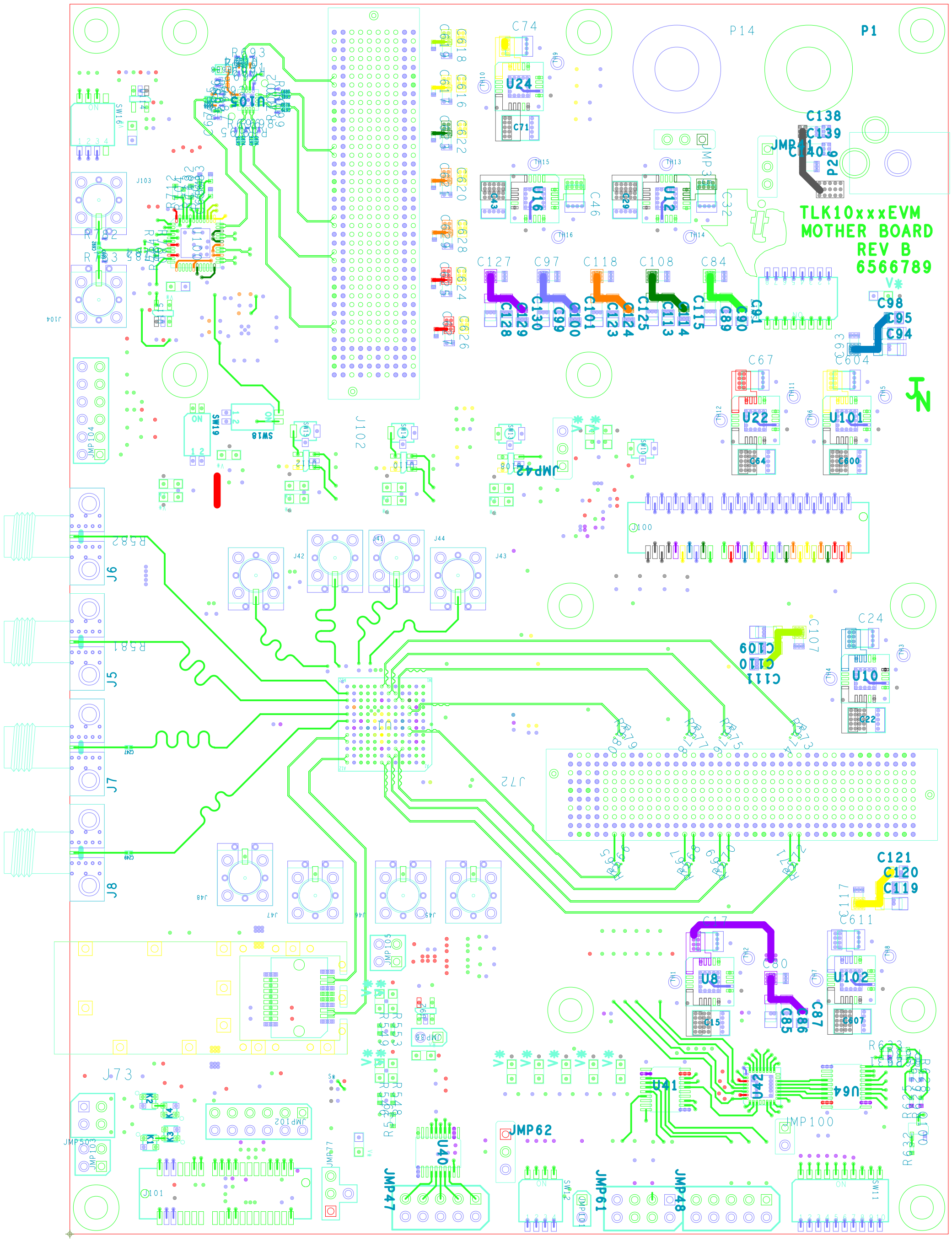
TLK10xxx EVM MOTHER BOARD

SIZE	FSCM NO	DWG NO
		6566789

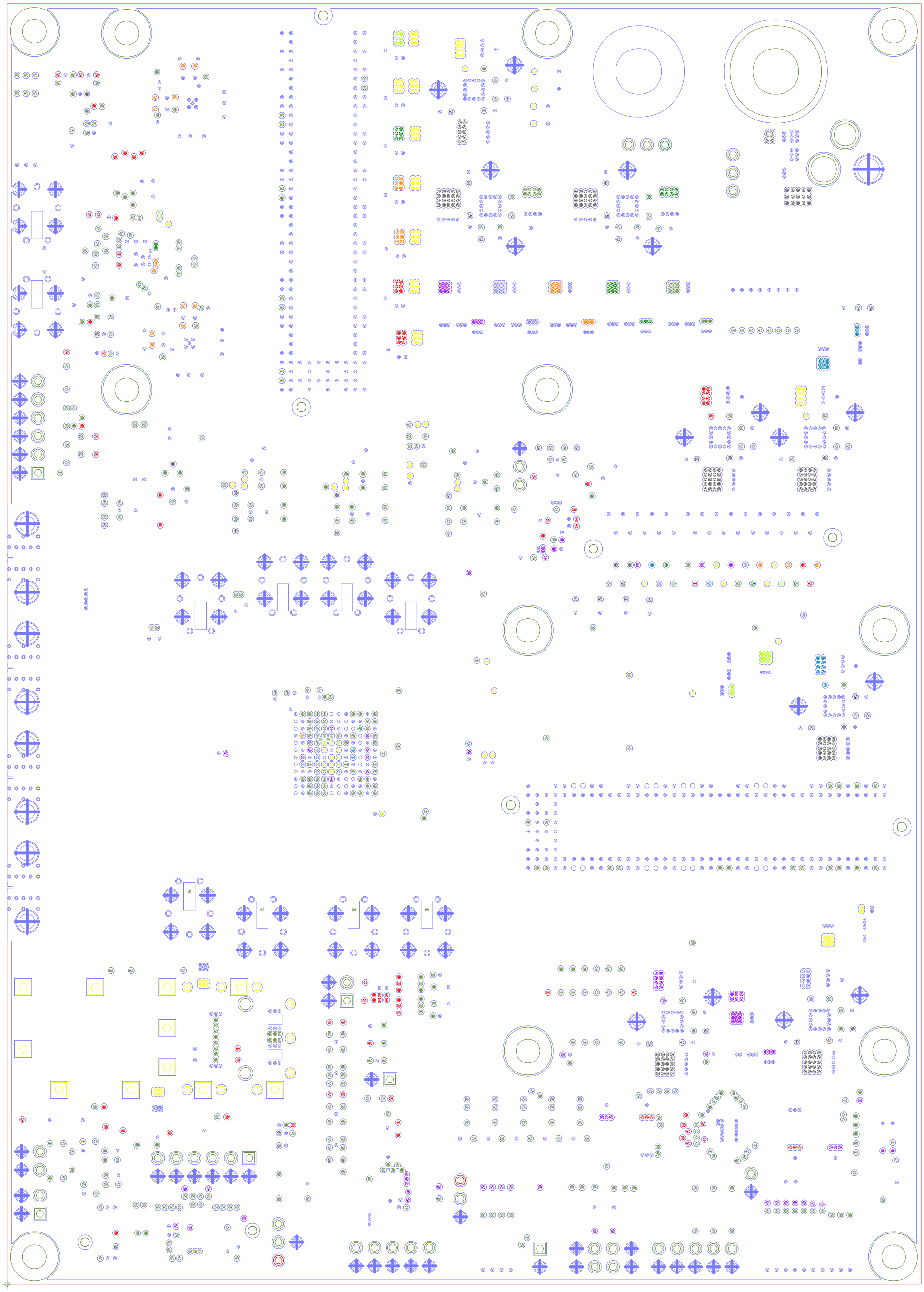
SCALE

SHEET **1 / 1**

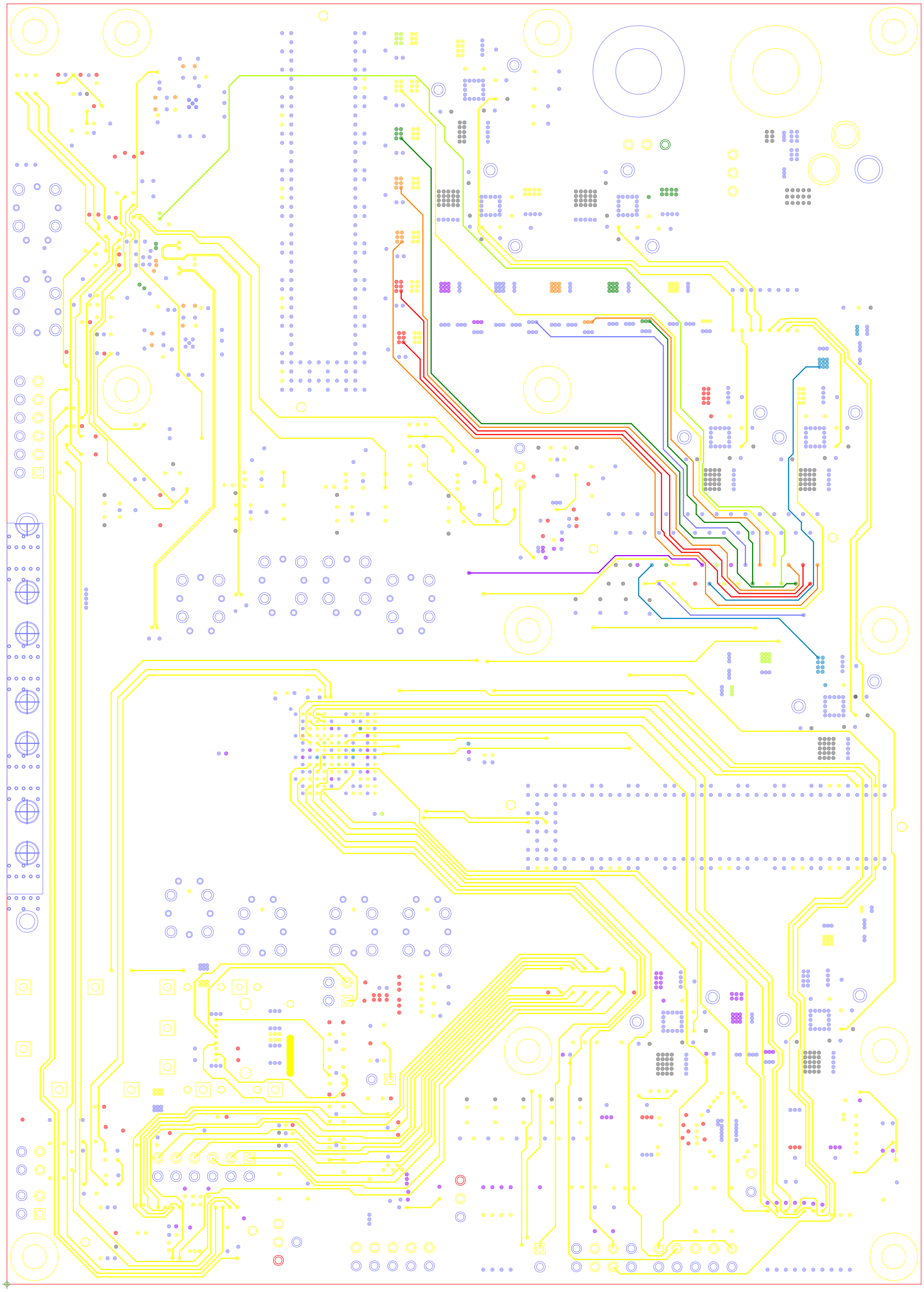
WO# 73776



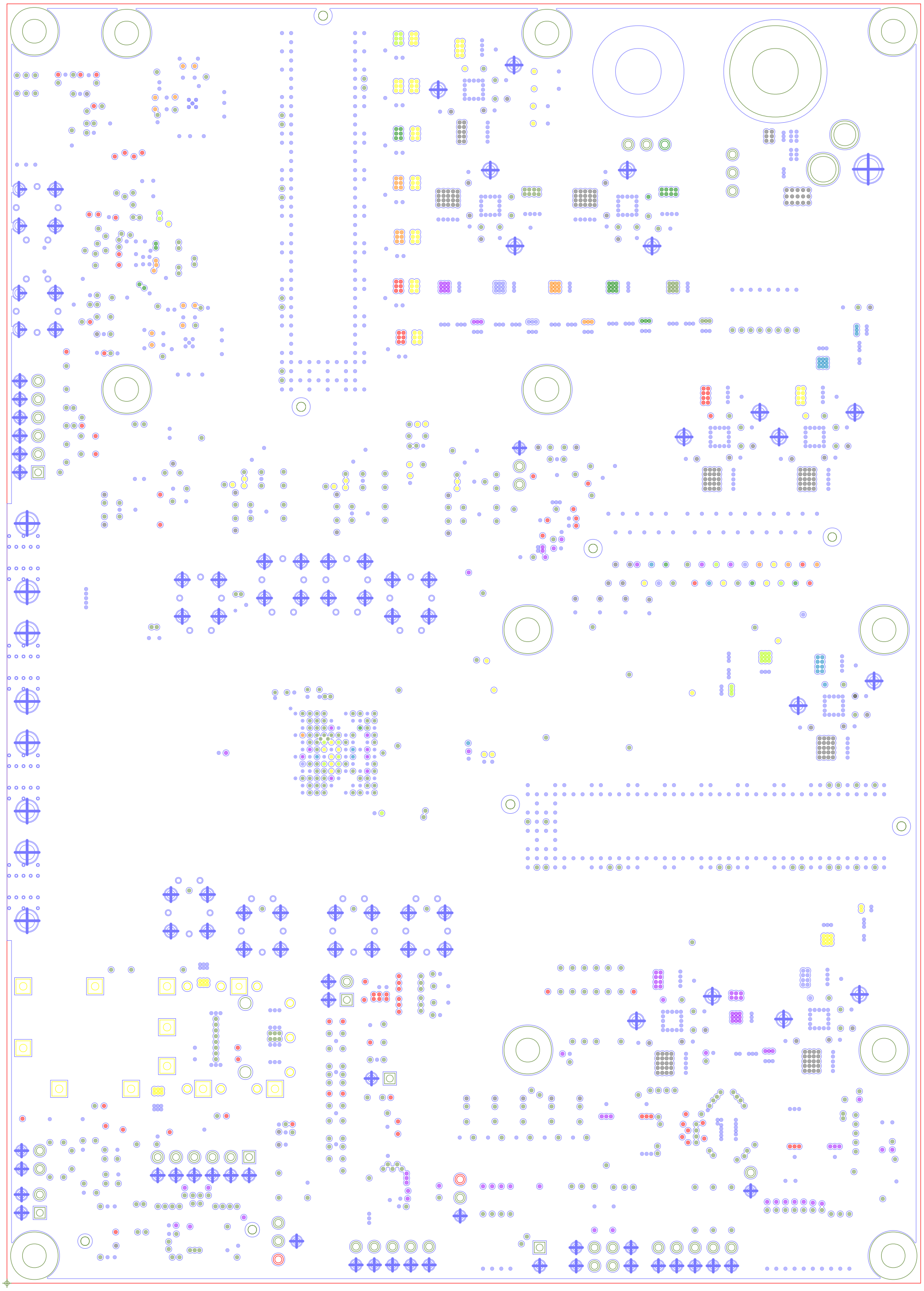
LAYER1-TOP-DUT SIDE



LAYER2-GND



LAYER3-SIGNAL



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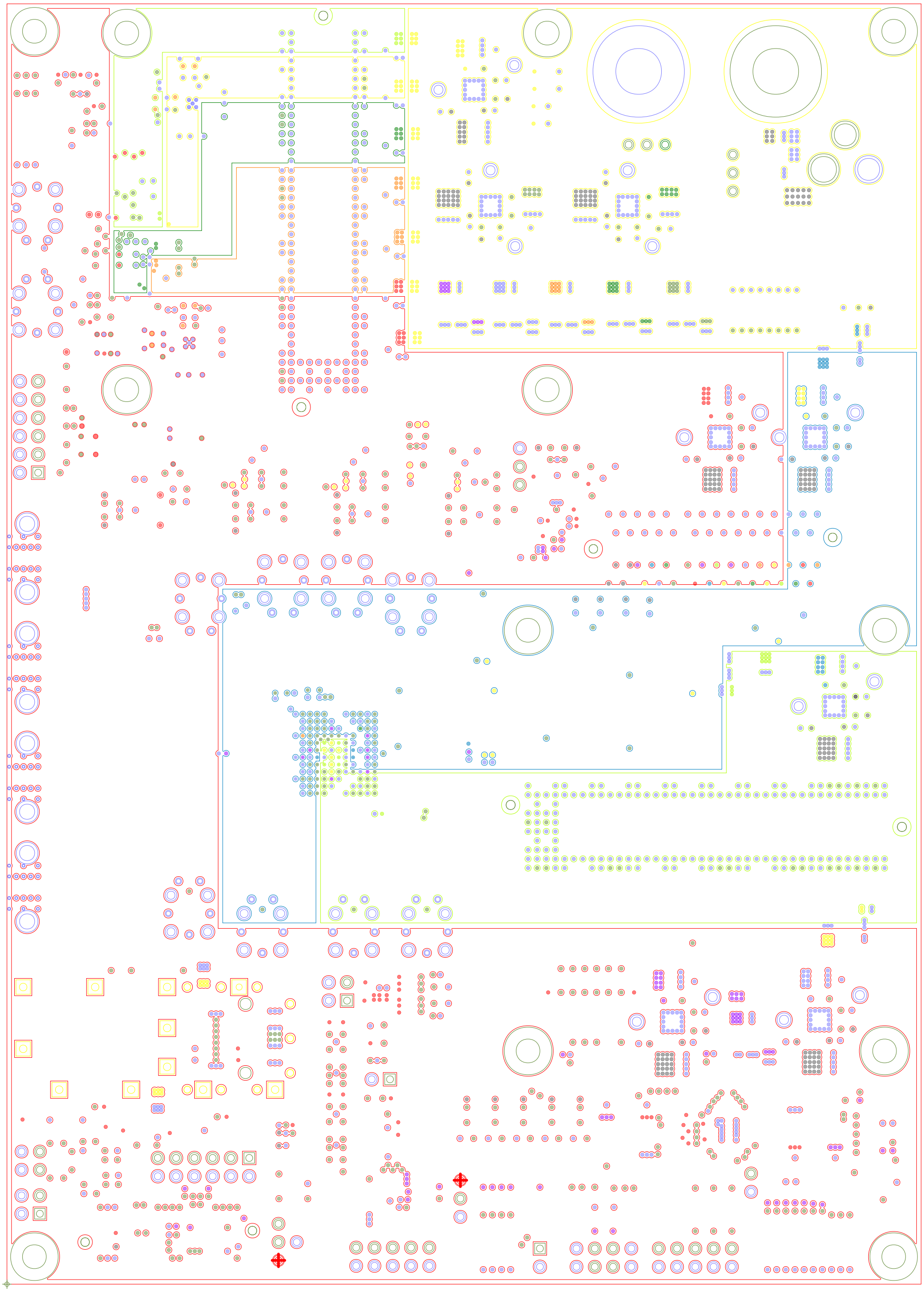
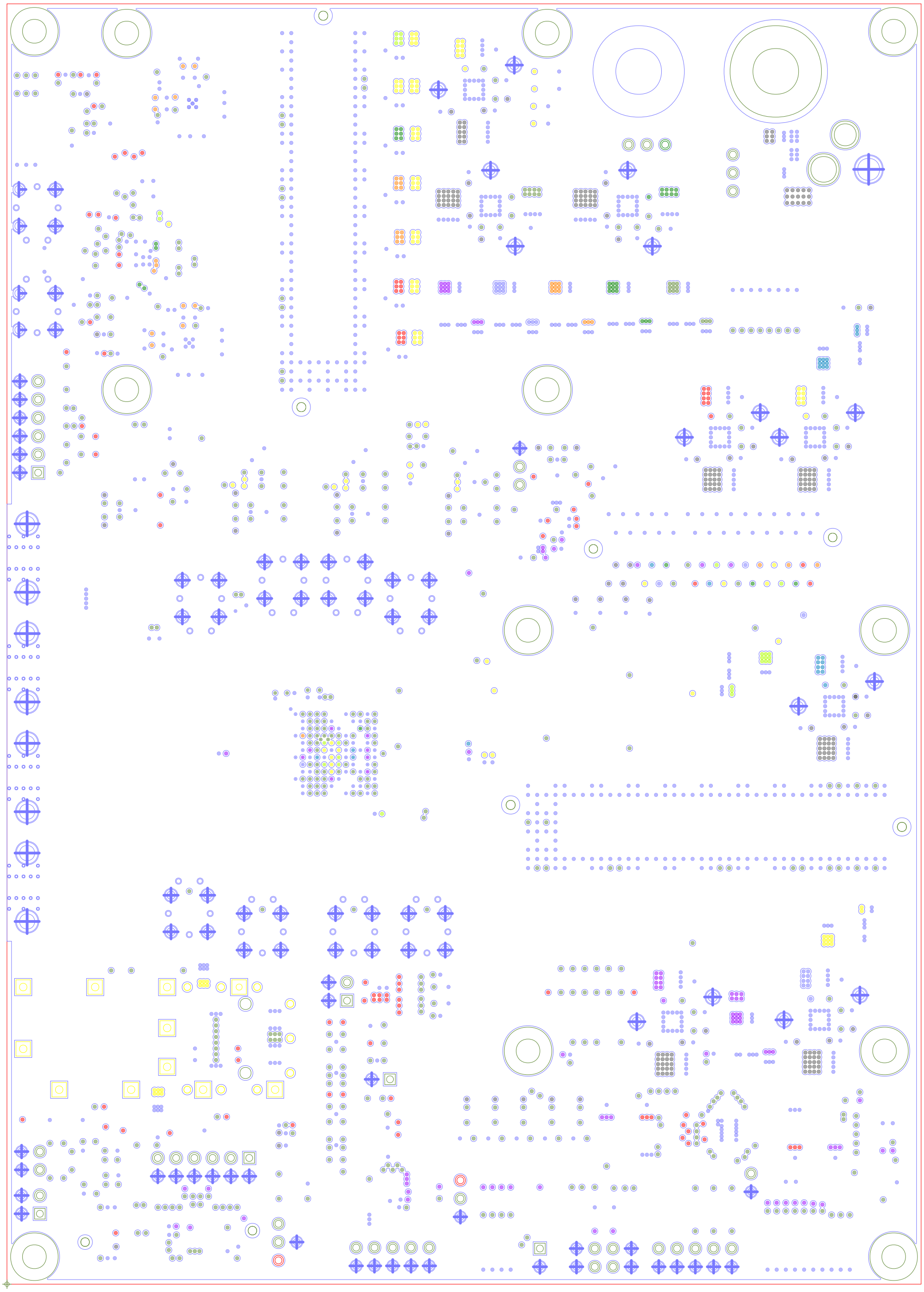
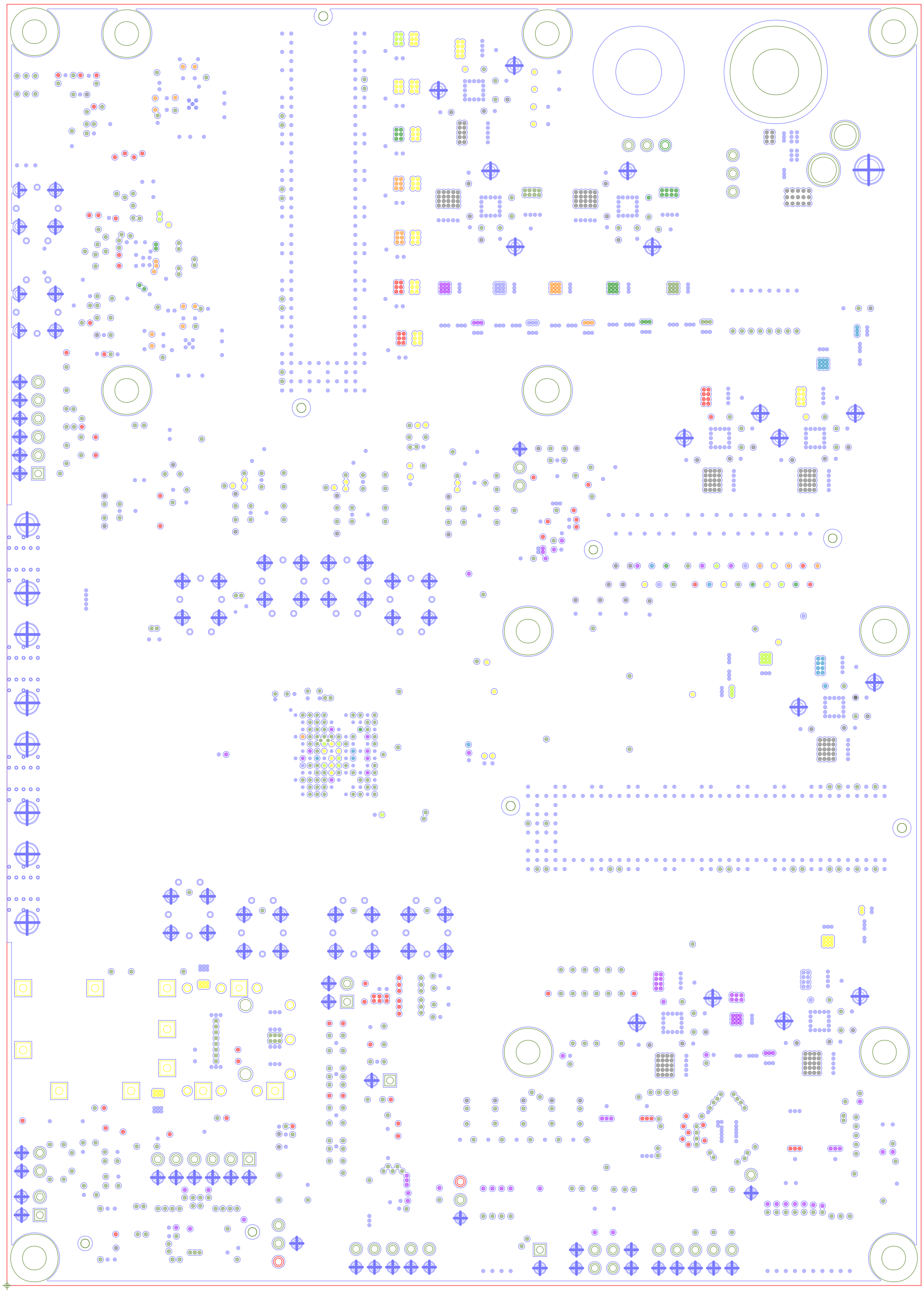


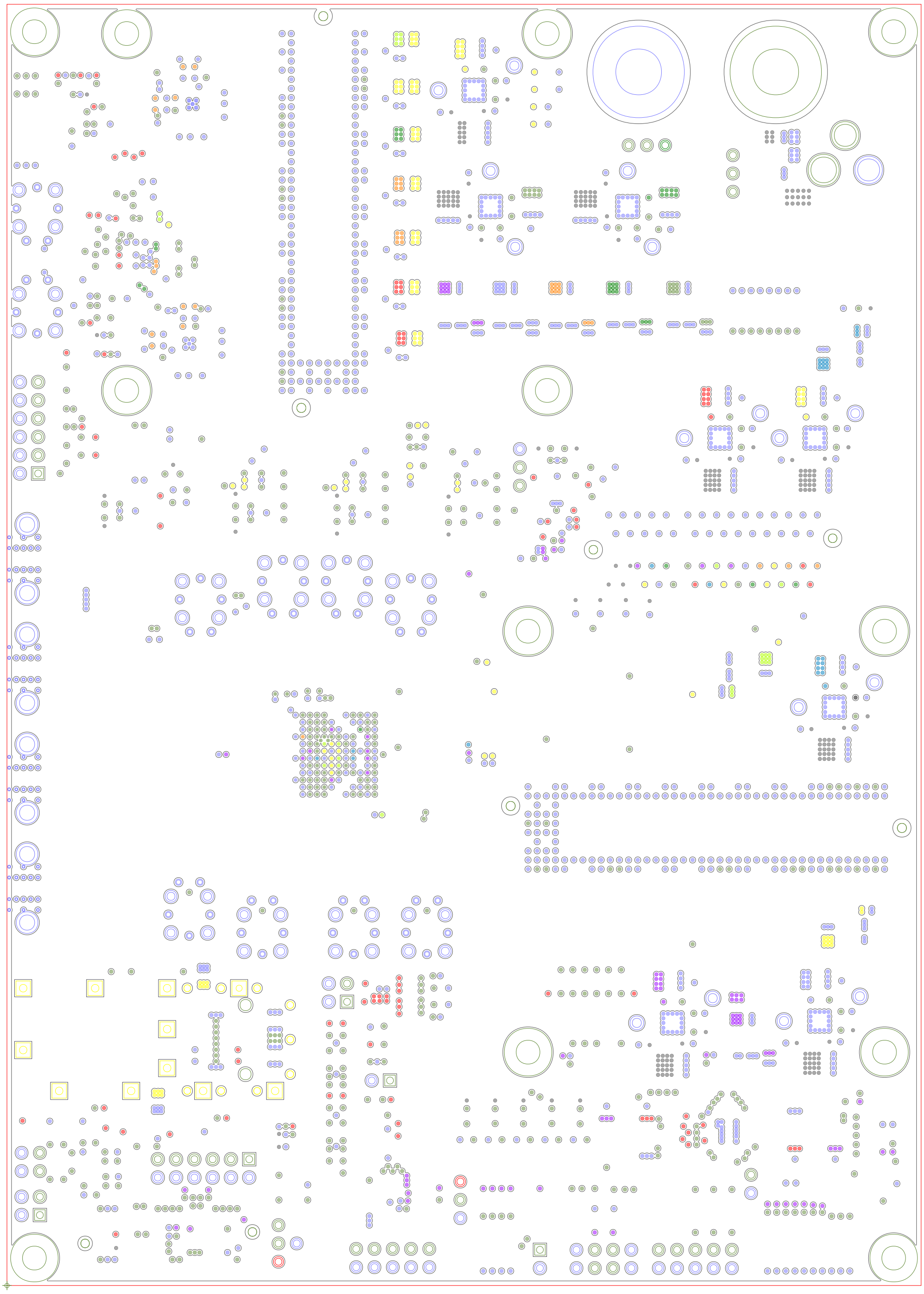
LAYER5-PWR



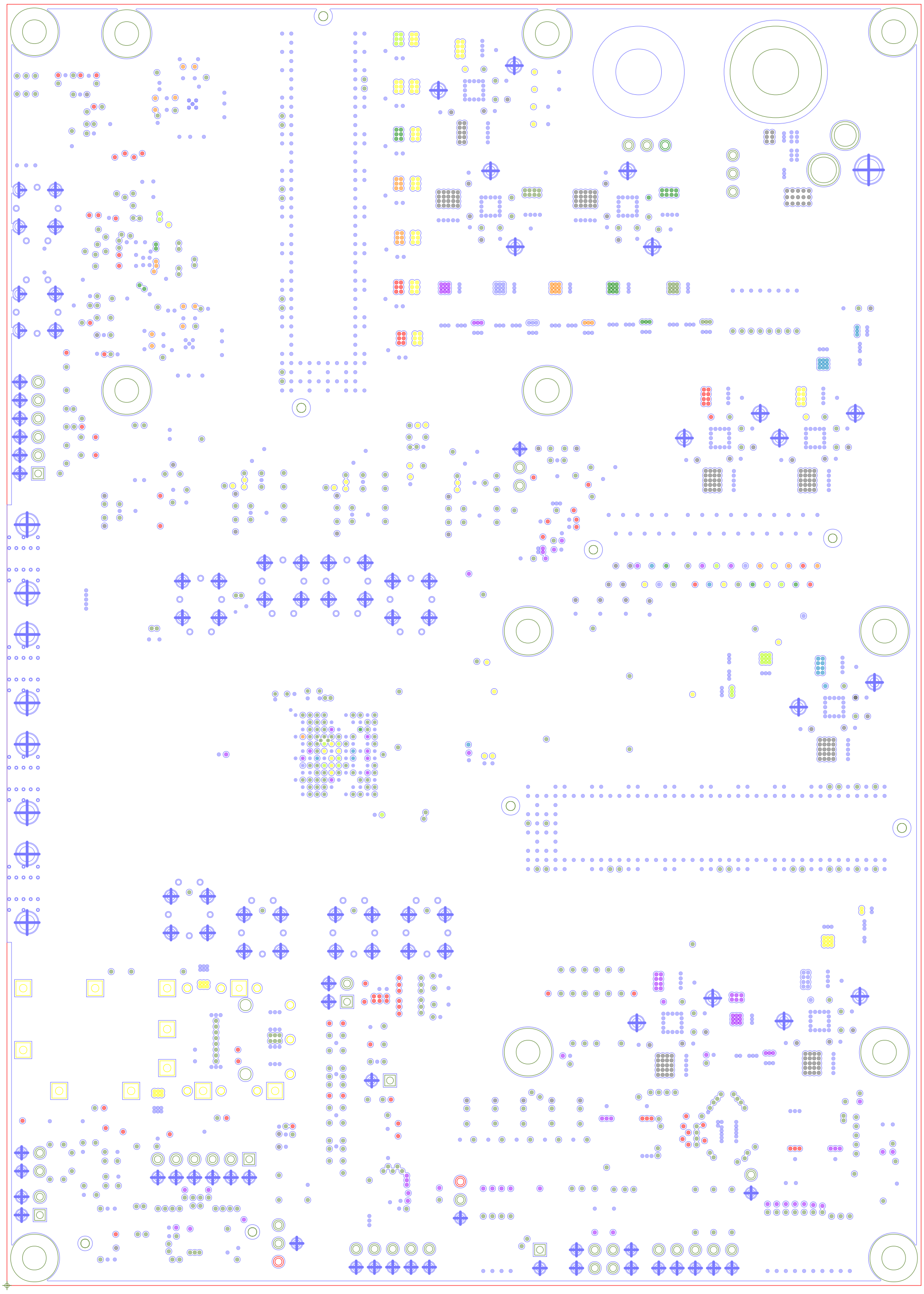
LAYER6-GND



LAYER9-GND



LAYER10-PWR



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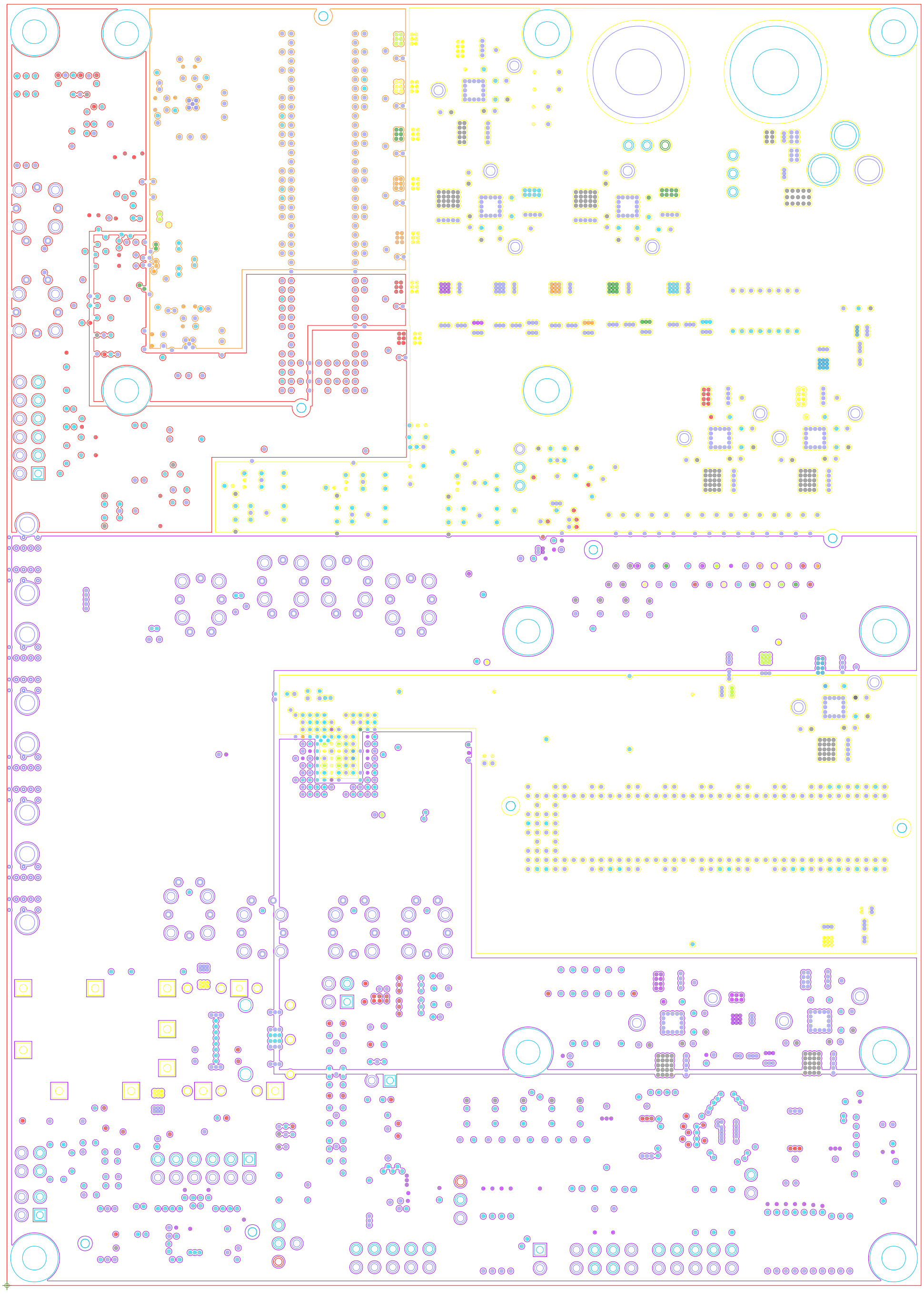
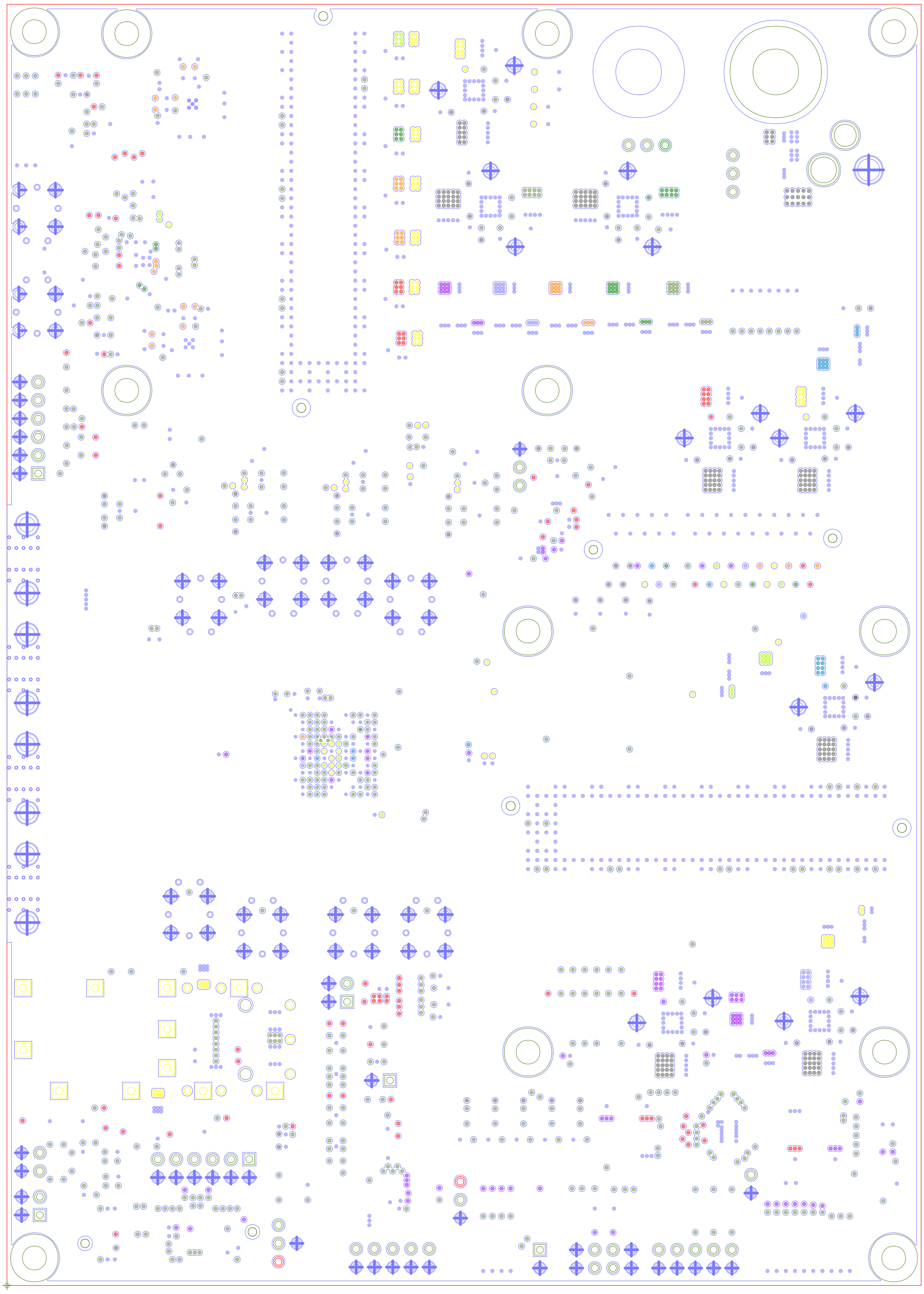
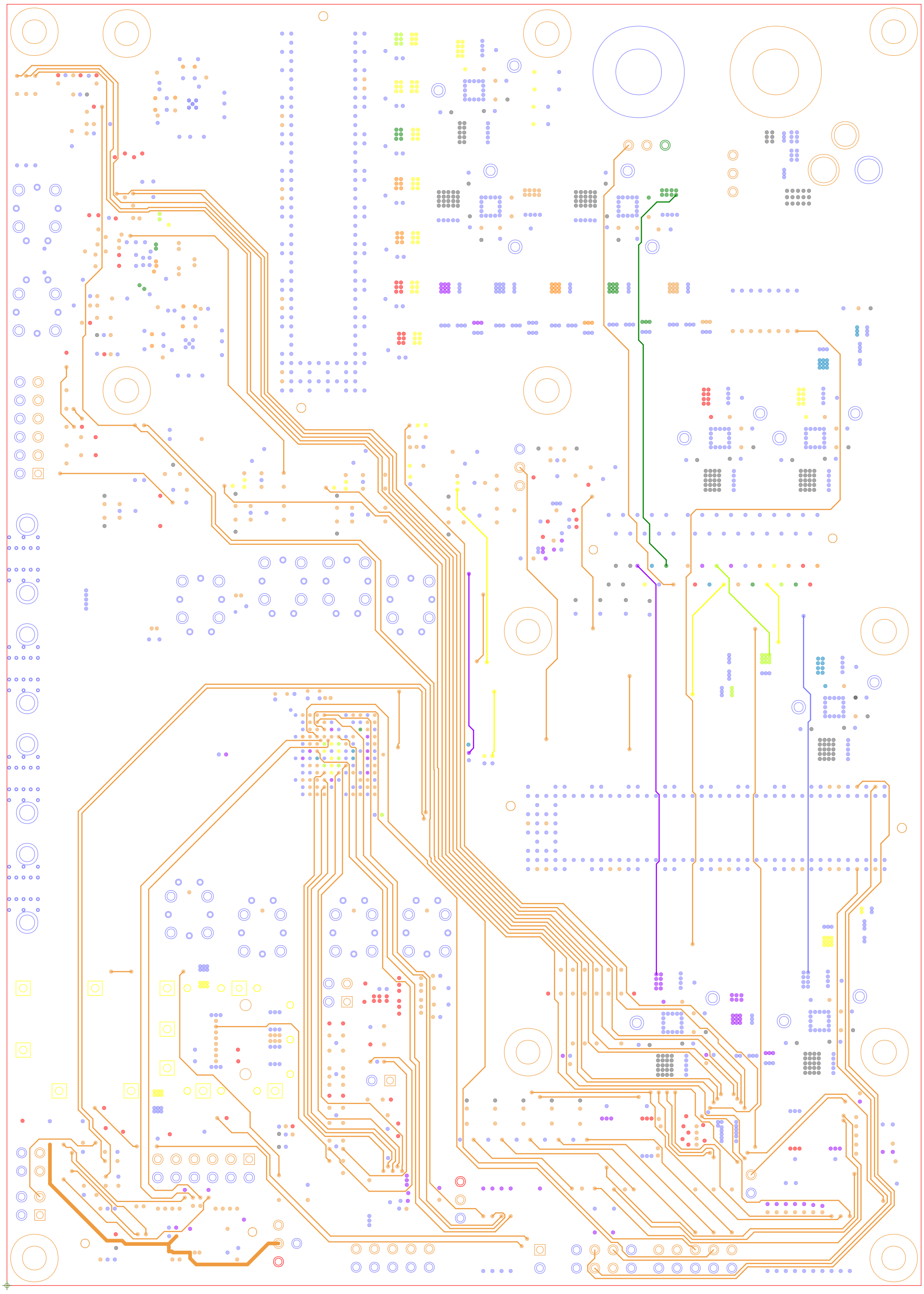


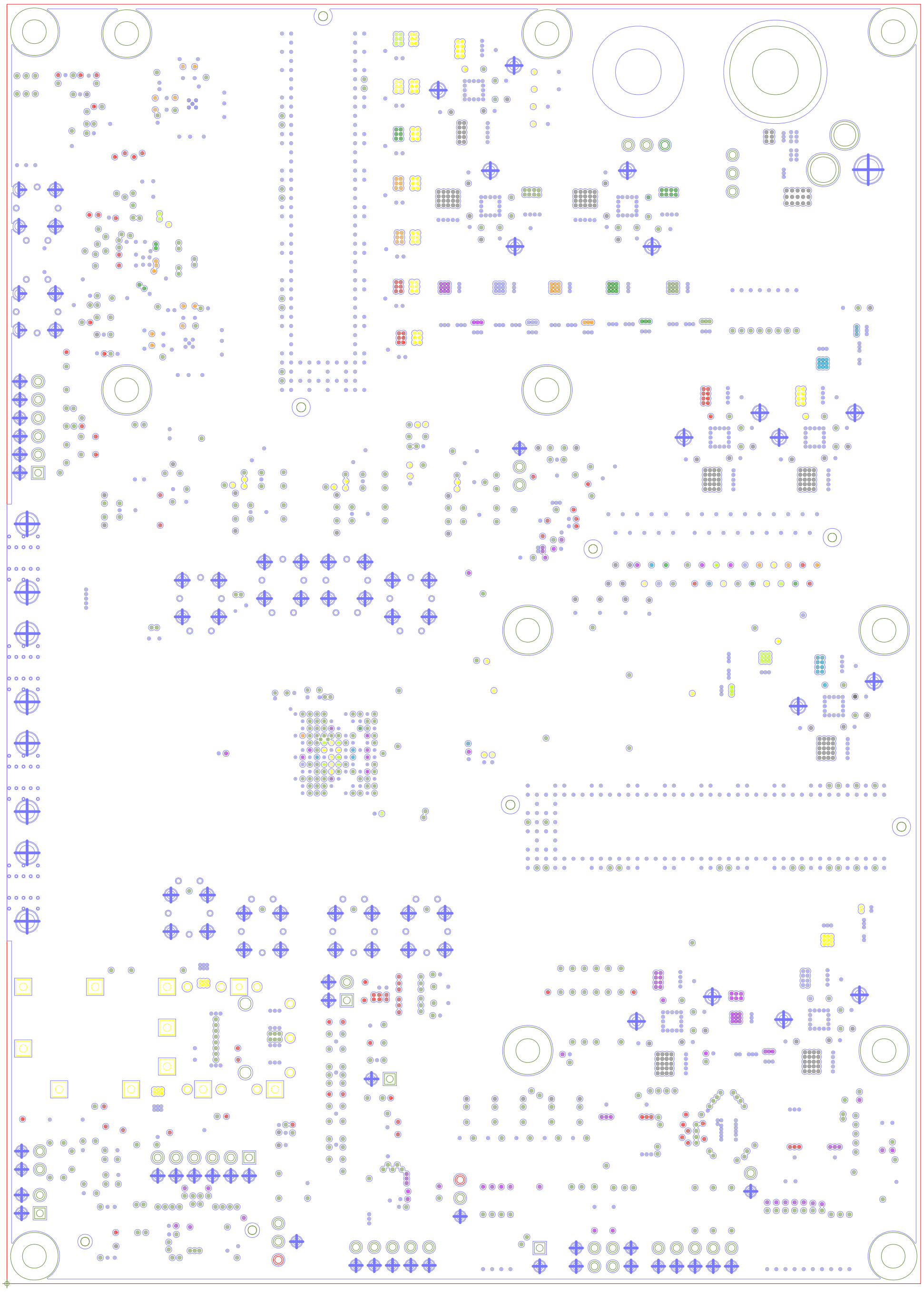
LAYER12-PWR



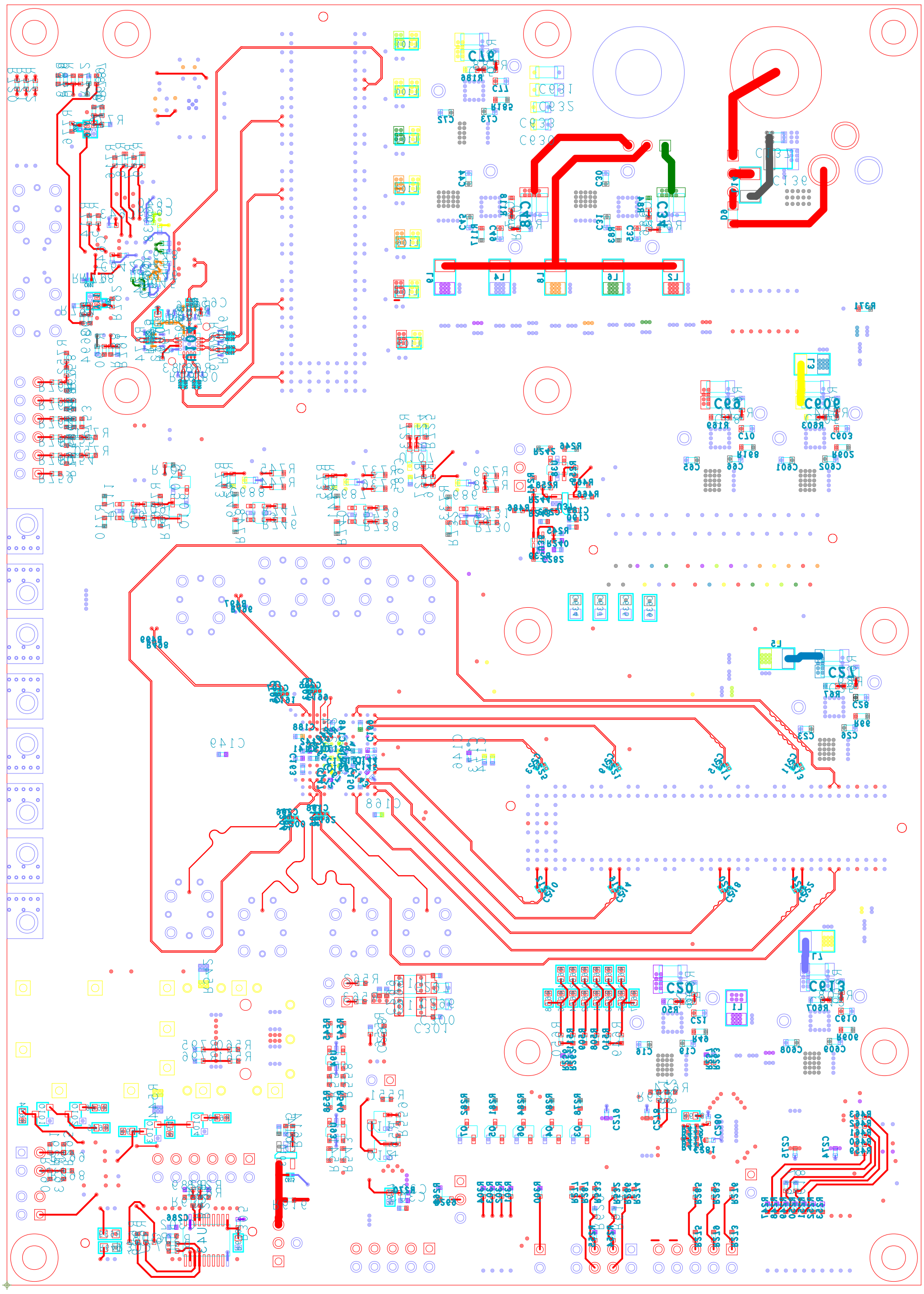
LAYER13-GND



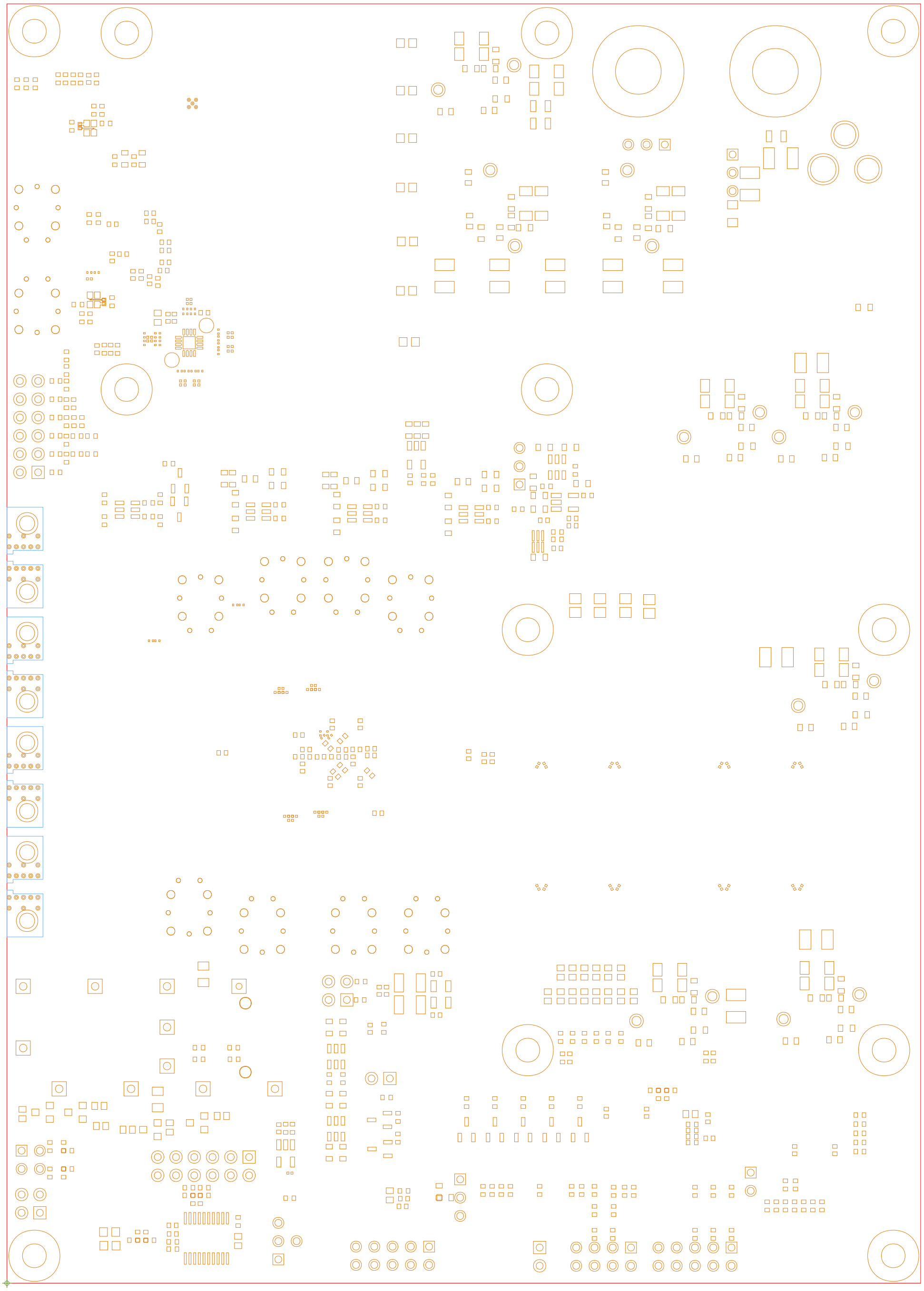
LAYER14-SIGNAL

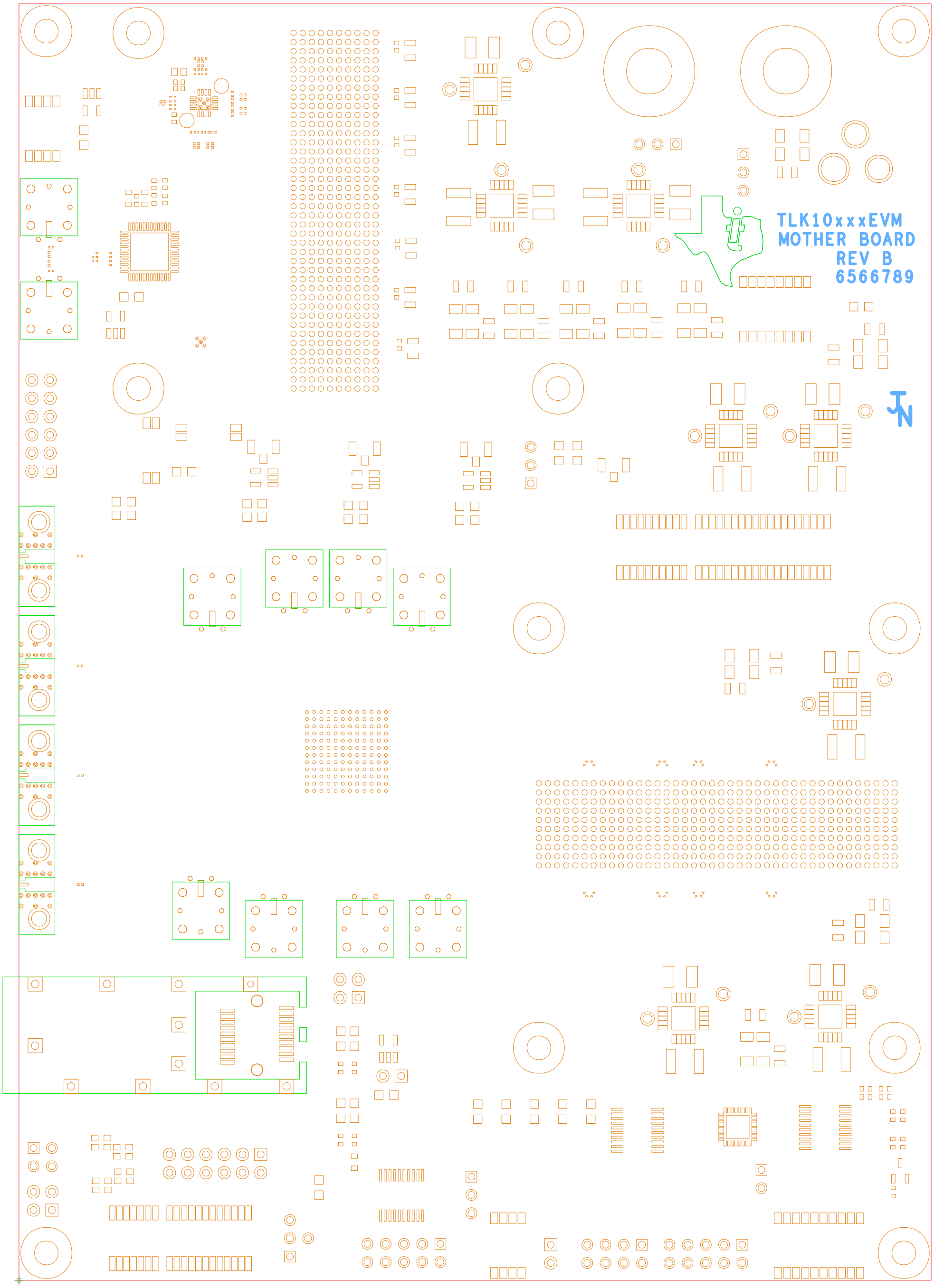


LAYER15-GND

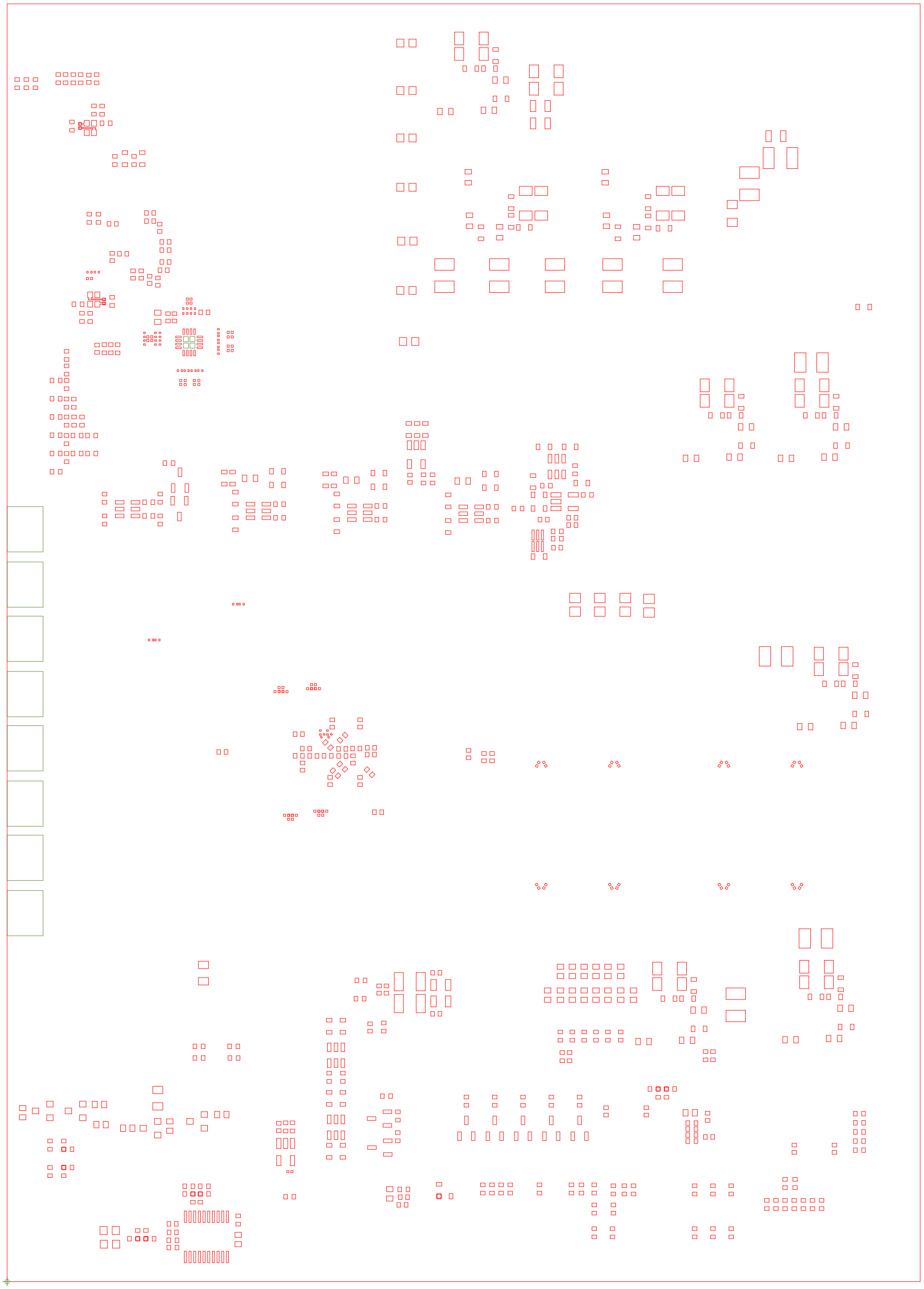


LAYER16-BOTTOM(TESTER)SIDE


MB



MT



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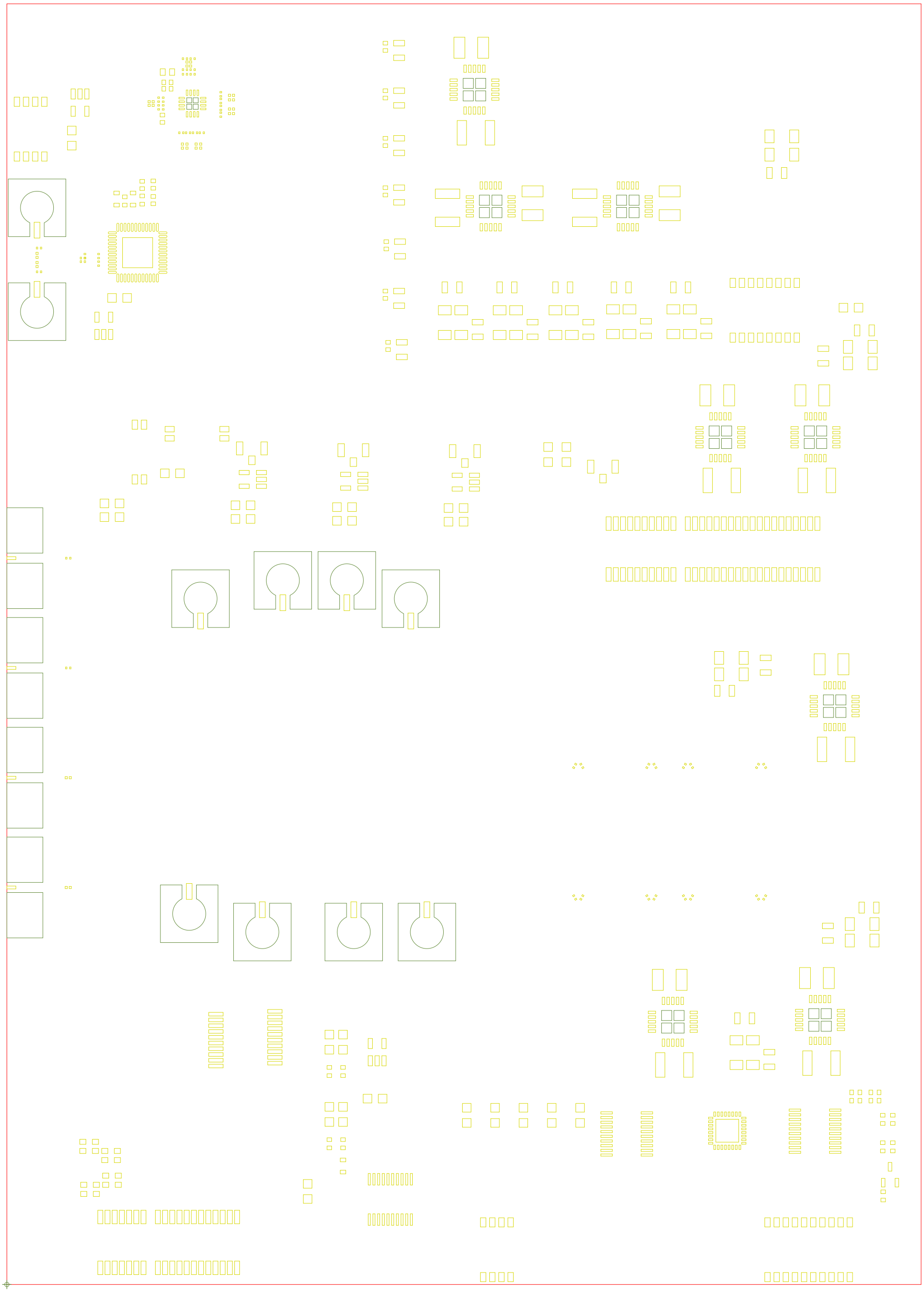
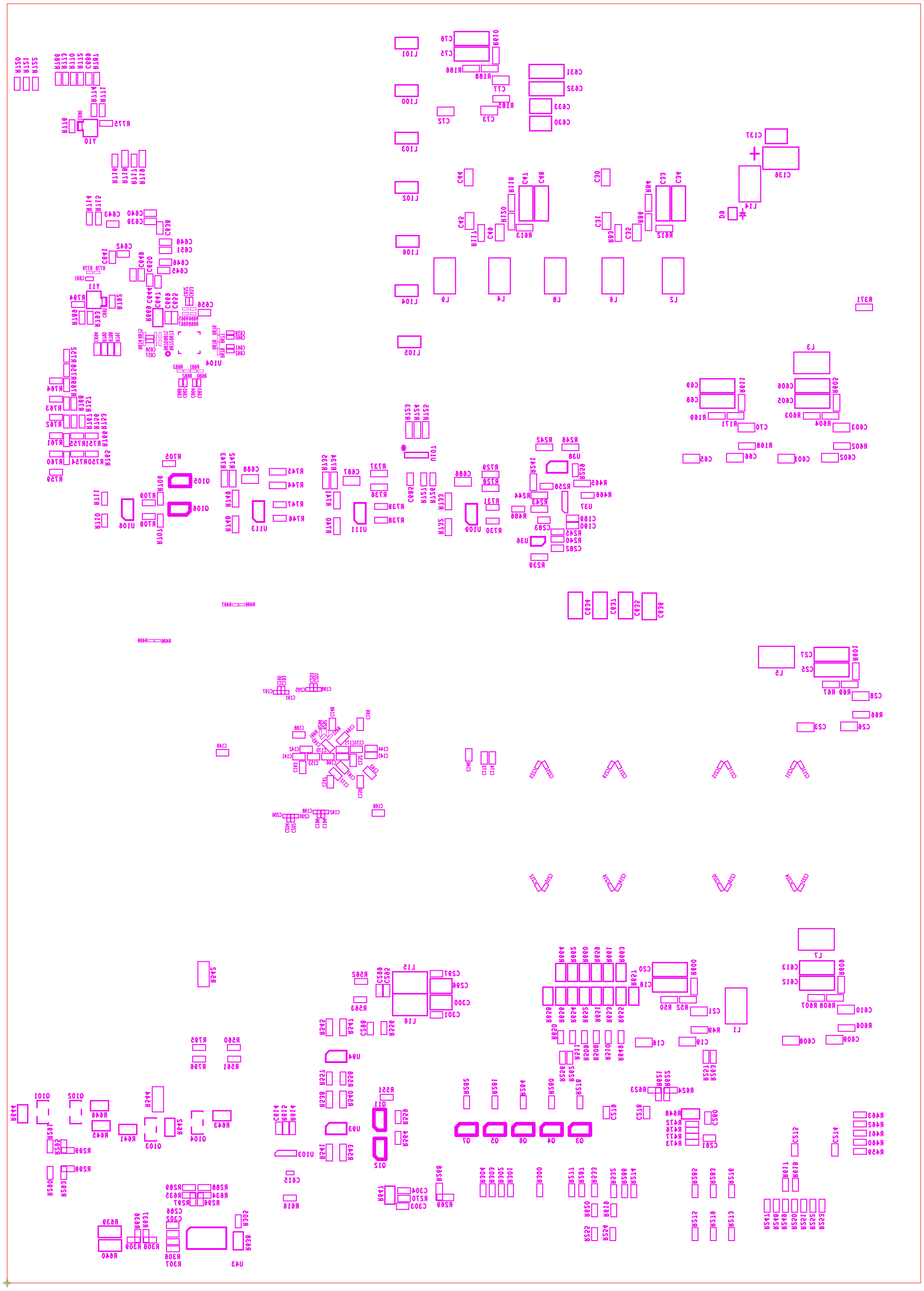
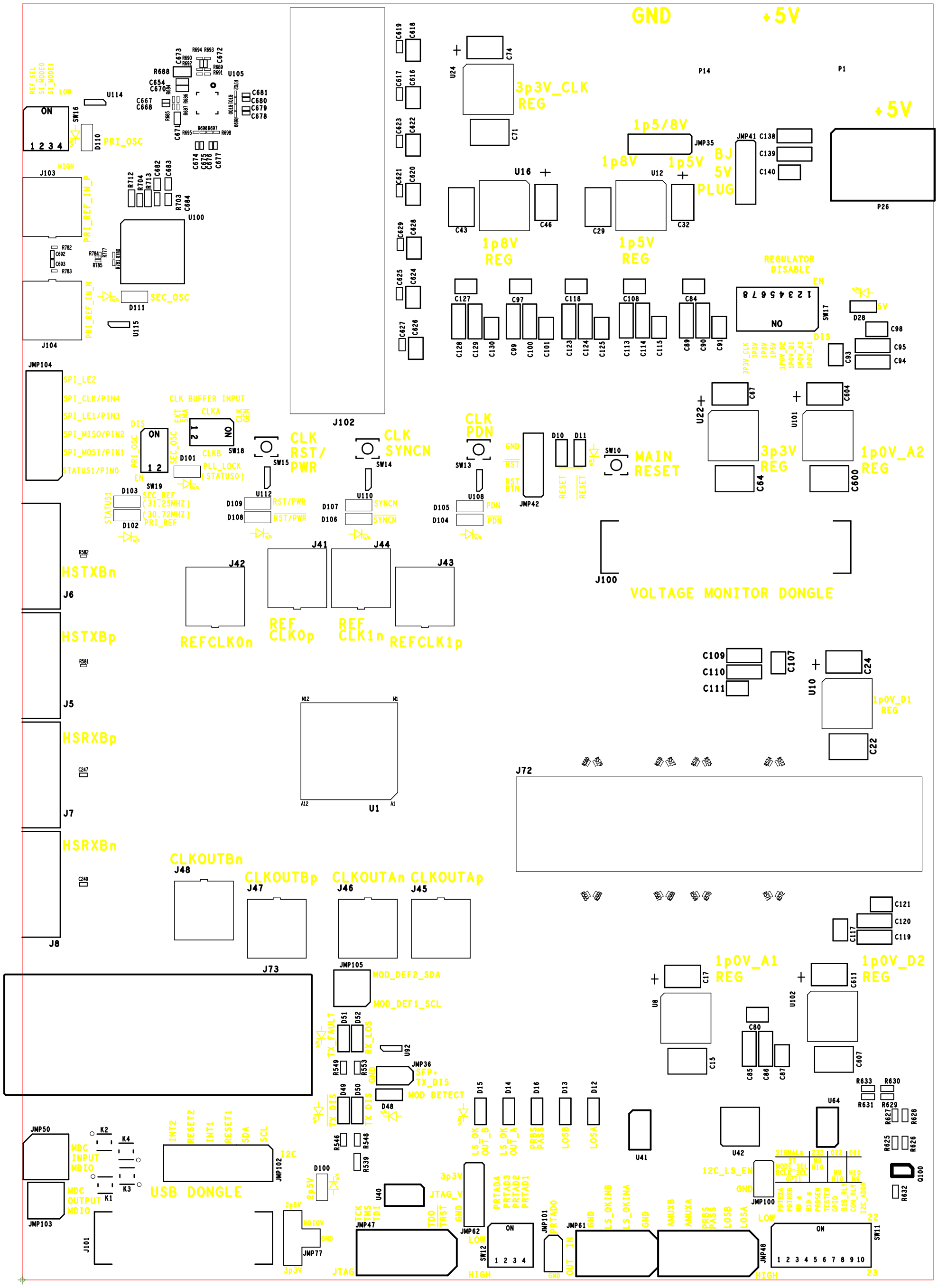


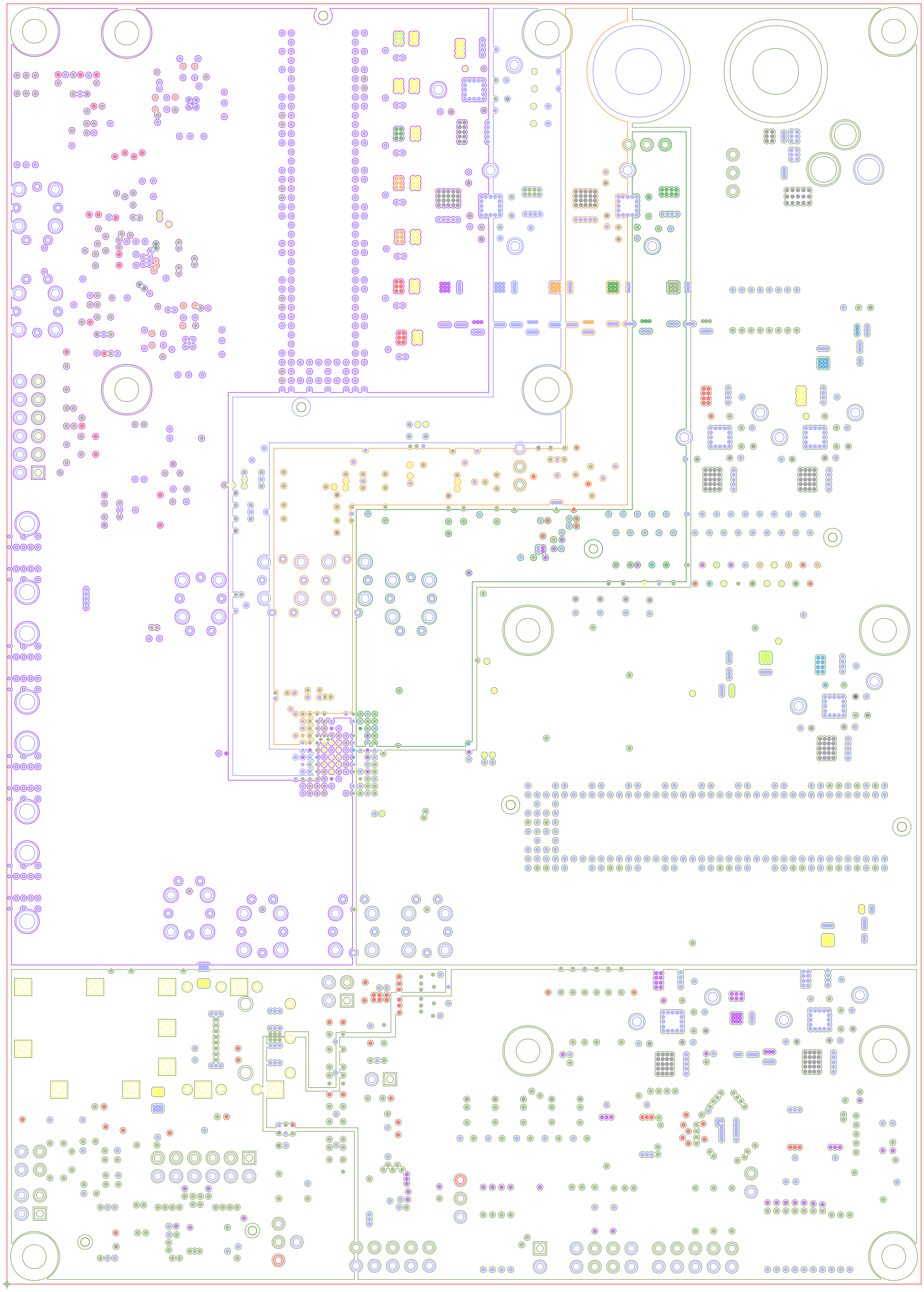
SPT



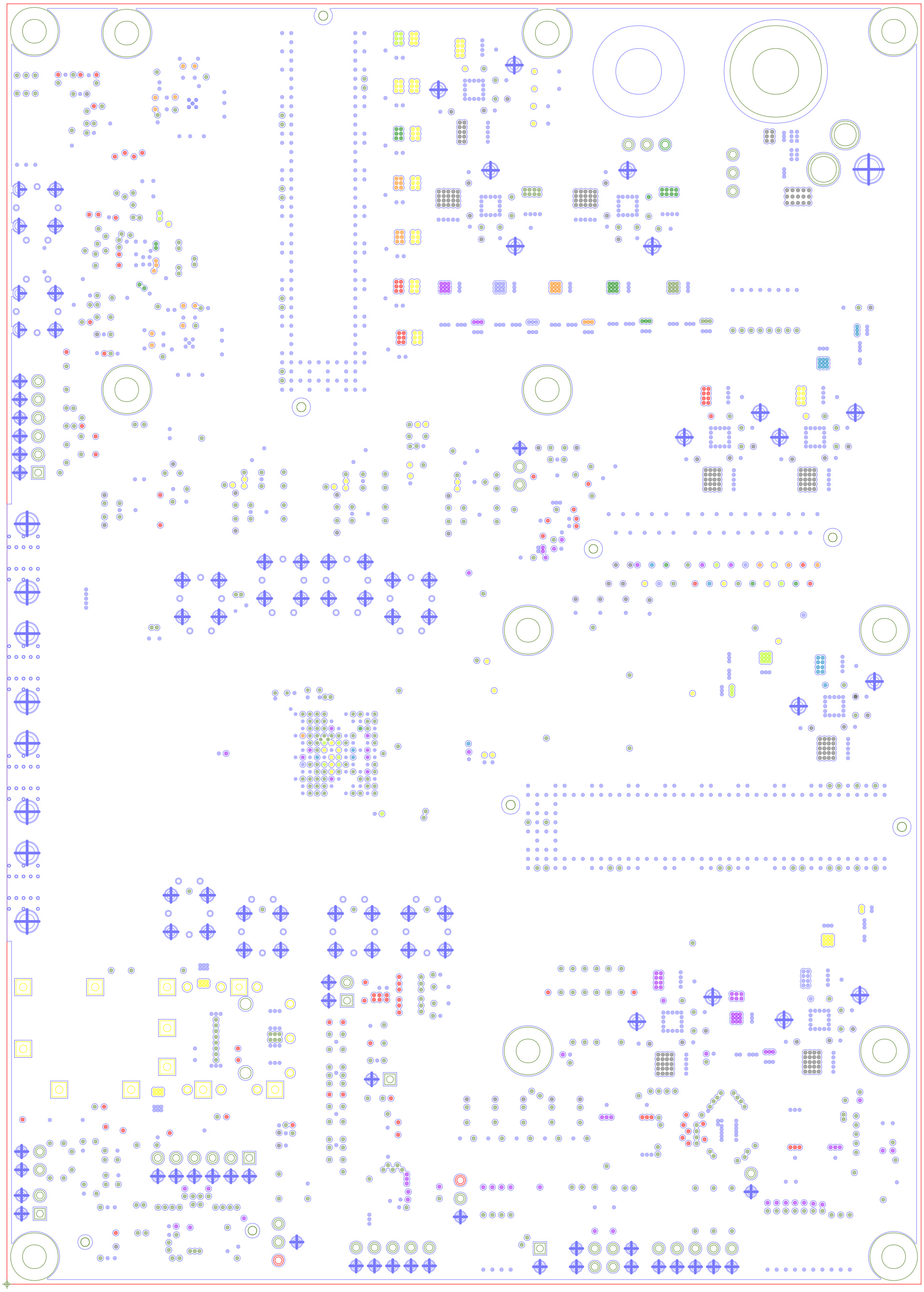
SBW


GND
+5V
+5V
P14
P1
P26
3p3V_CLK REG
U24
C74
C71
1p5/8V
JMP35
1p8V
1p5V
BJ 5V PLUG
JMP41
C138
C139
C140
U16
U12
C43
C46
C29
C32
1p8V REG
1p5V REG
REGULATOR DISABLE
EN
DIS
NO
SW17
C127
C97
C118
C108
C84
C128
C129
C130
C99
C100
C101
C123
C124
C125
C113
C114
C115
C89
C90
C91
5V
D28
C98
C95
C94
C93
C67
C604
U22
U101
3p3V REG
1p0V_A2 REG
C64
C600
MAIN RESET
SW10
D10
D11
RESET
JMP42
GND
RST
RST BTN
J100
VOLTAGE MONITOR DONGLE
C109
C110
C111
C107
C24
U10
1p0V_D1 REG
C22
J72
J102
C619
C618
C617
C616
C623
C622
C621
C620
C629
C628
C625
C624
C627
C626
REF_SEL
S1_MODE0
S1_MODE1
LOW
ON
1 2 3 4
SW16
U114
D110
PRI_OSC
HIGH
J103
PRI_REF_IN_P
U105
U100
SEC_OSC
D111
U115
PRI_REF_IN_N
J104
JMP104
SPI_LE2
SPI_CLK/PIN4
SPI_LE1/PIN3
SPI_MISO/PIN2
SPI_MOSI/PIN1
STATUS1/PIN0
CLK BUFFER INPUT
CLKA
CLKB
EXT SMA
CLK GEN
SW18
PRI_OSC
SEC_OSC
DIS
D101
PLL_LOCK (STATUS0)
EN
SW19
D103
SEC_REF (31.25MHZ)
(30.72MHZ) PRI_REF
D102
STATUS1
CLK RST/ PWR
SW15
U112
D109
D108
RST/PWR
CLK SYNCN
SW14
U110
D107
D106
SYNCN
CLK PDN
SW13
U108
D105
D104
PDN
J42
J41
J44
J43
REFCLK0n
REF CLK0p
REF CLK1n
REFCLK1p
HSTXBn
J6
HSTXBp
J5
HSRXBp
J7
HSRXBn
J8
U1
CLKOUTBn
J48
CLKOUTBp
J47
CLKOUTAn
J46
CLKOUTAp
J45
C121
C120
C119
C117
1p0V_A1 REG
1p0V_D2 REG
U8
C17
U102
C611
C80
C15
C85
C86
C87
C607
J73
JMP105
MOD_DEF2_SDA
MOD_DEF1_SCL
TX_FAULT
RX_LOS
D51
D52
U92
JMP36
SFP+ TX_DIS
MOD DETECT
GND
TX DIS
TX DIS
D49
D50
D48
D15
D14
D16
D13
D12
LS_OK OUT_B
LS_OK OUT_A
PRBS PASS
LOSB
LOSA
U41
U42
U64
Q100
JMP50
MDC INPUT MDIO
MDC OUTPUT MDIO
JMP103
K2
K4
K1
K3
INT2
RESET2
INT1
RESET1
SDA
SCL
I2C
JMP102
USB DONGLE
J101
D100
2p5V
JMP77
3p3V
MDIOV
U40
3p3V
JTAG_V
TCK TMS TDI
TDO TRST
GND
JMP47
JTAG
JMP62
SW12
LOW
HIGH
ON
1 2 3 4
JMP101
PRTAD0
PRTAD4 PRTAD3 PRTAD2 PRTAD1
IN
OUT
GND
JMP61
LS_OKINB
LS_OKINA
AMUXB
AMUXA
PRBS PASS
LOSB
LOSA
JMP48
I2C_LS_EN
JMP100
LOW
HIGH
SW11
1 2 3 4 5 6 7 8 9 10
22
23

STW



LAYER8-PWR



LAYER7-GND

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