Page 2 Block Diagram

Page 3 Analog Front End (Current)

Page 4 Analog Front End Opamp (Voltage) + LDO + ZCD

Page 5 JTAG Interface + LEDs + Decoupling Capacitors

Page 6 MSP430F6779 + Crystal

Page 7 Interfaces

Page 8 Hardware - MIiscellaneous

Revision History

Revision	Notes

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Number: TIDA-00222 Rev: E1
SVN Rev: Not in version control
Drawn By:
Engineer: Prahlad Supeda

Designed for: Public Release Mod. Date: 7/14/2014
Project Title: TIDA-0022 - ISE3004
Sheet Title: Index Page
Assembly Variant: 001 Sheet: 1 of 8
File: Pg1 Index Page.SchDoc Size: B
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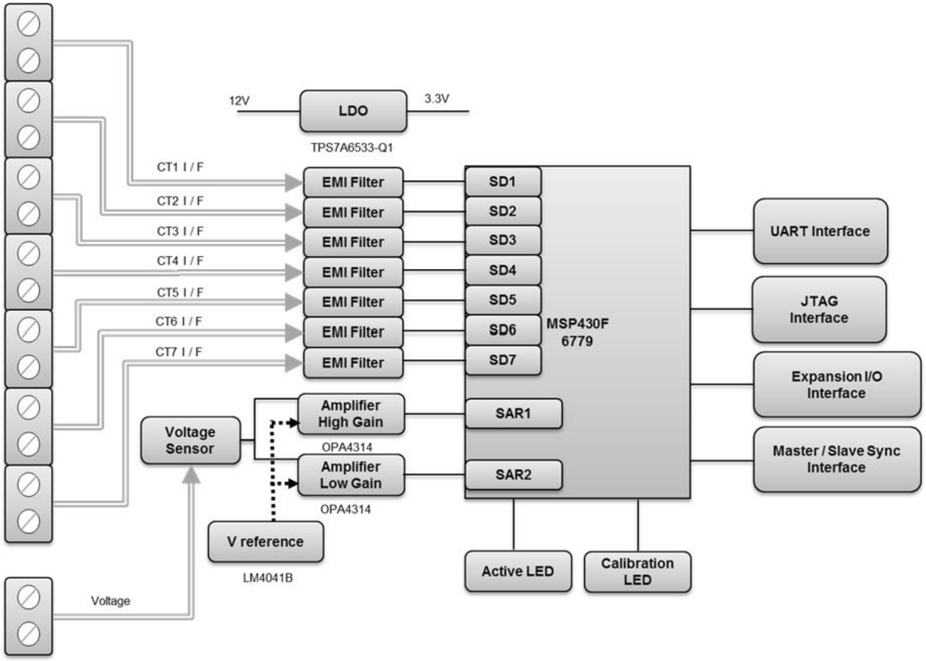

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	Project Title: TIDA-0022 - ISE3004		
Number: TIDA-00222 Rev: E1	Sheet Title: Block Diagram		
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 2 of 8	
Drawn By:	File: Pg2 Block Diagram.SchDoc	Size: B	http://www.ti.com
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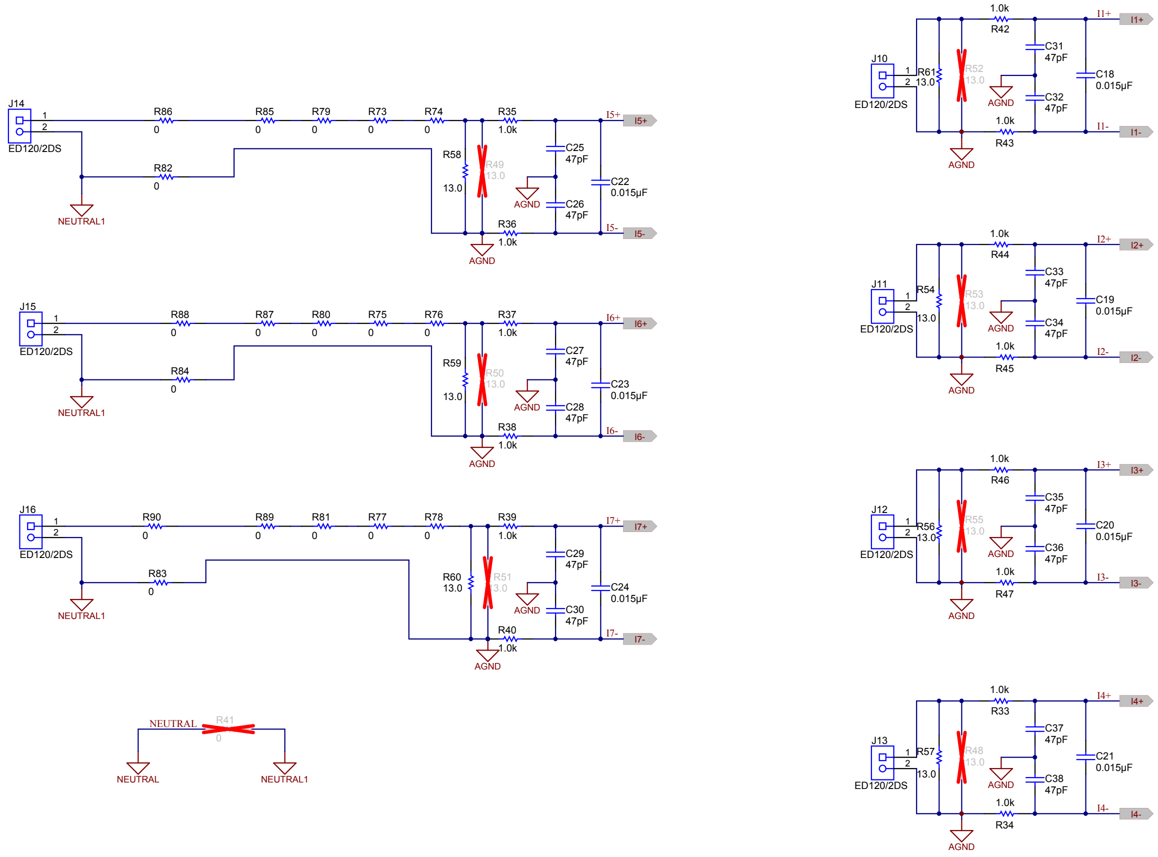

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Project Title: TIDA-0022 - ISE3004
Sheet Title: Analog Front End (Current)
Assembly Variant: 001 Sheet: 3 of 8
File: Pg3.Analog Front End (Current).SchDoc Size: B
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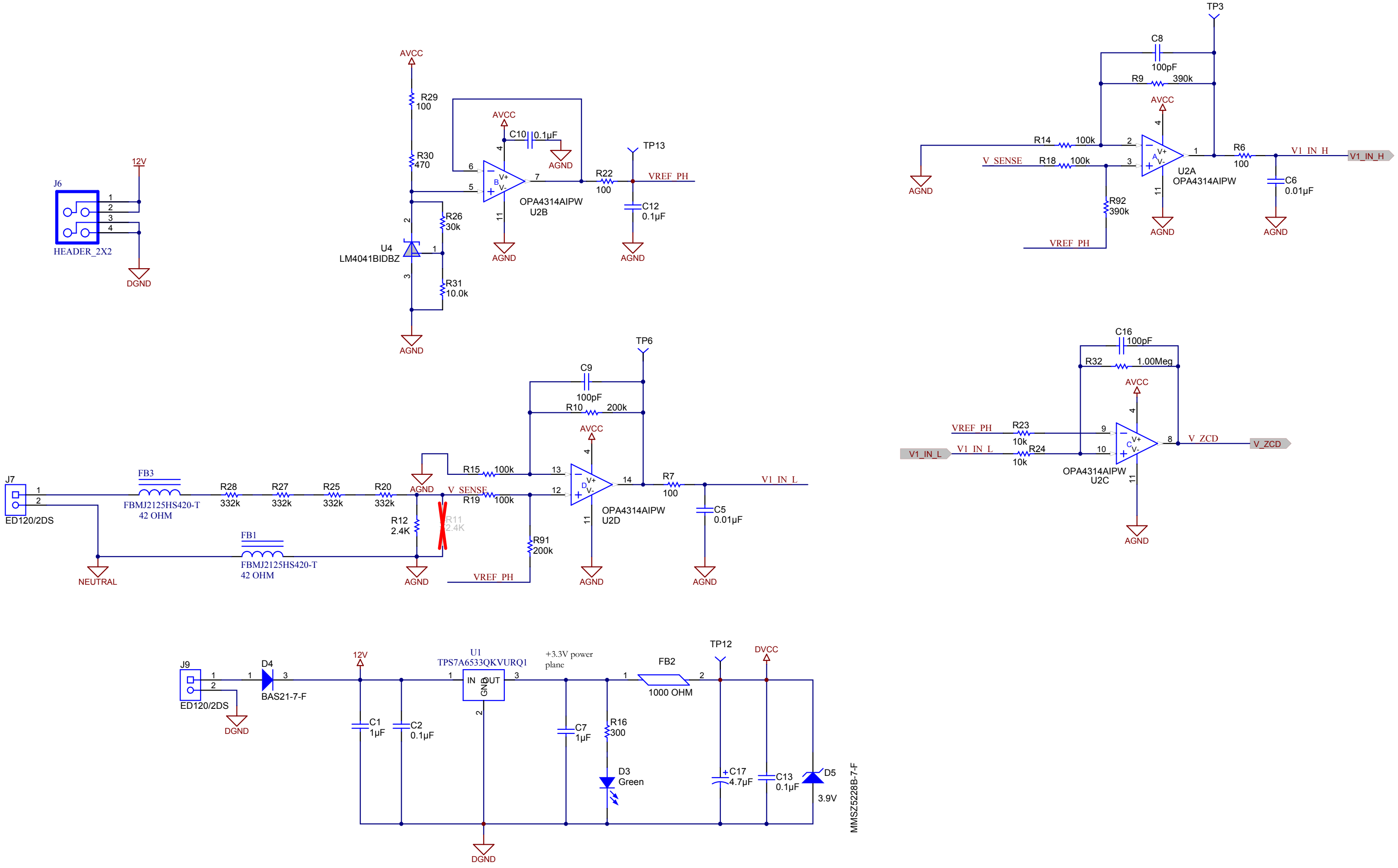

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Mod. Date: 9/23/2014
Project Title: TIDA-0022 - ISE3004
Number: TIDA-00222
Rev: E1
Sheet Title: Analog Front End Opamp (Voltage) + LDO + ZCD
SVN Rev: Not in version control
Assembly Variant: 001
Sheet: 4 of 8
Drawn By:
File: Pg4.Analog Front End Opamp (Voltage) + LDO + ZCD.SchDoc
Size: B
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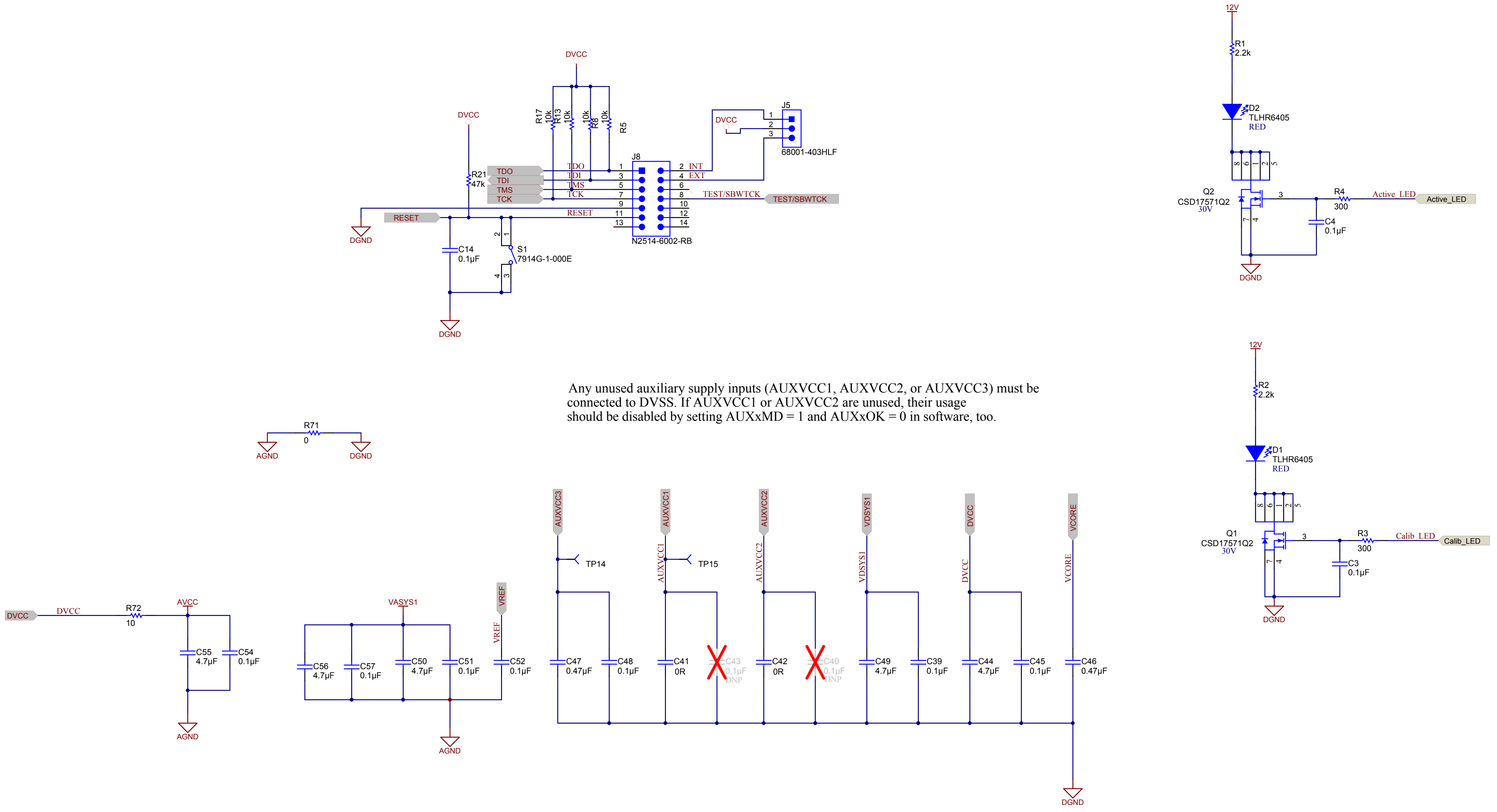

Any unused auxiliary supply inputs (AUXVCC1, AUXVCC2, or AUXVCC3) must be connected to DVSS. If AUXVCC1 or AUXVCC2 are unused, their usage should be disabled by setting AUXxMD = 1 and AUXxOK = 0 in software, too.

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Mod. Date: 7/14/2014
Project Title: TIDA-0022 - ISE3004
Number: TIDA-00222
Rev: E1
Sheet Title: JTAG Interface + LEDs + Decoupling Capacitors
SVN Rev: Not in version control
Assembly Variant: 001
Sheet: 5 of 8
Drawn By:
File: Pg5.JTAG Interface + LEDs + Decoupling Capacitors.SchDoc
Size: B
Engineer: Prahlad Supeda
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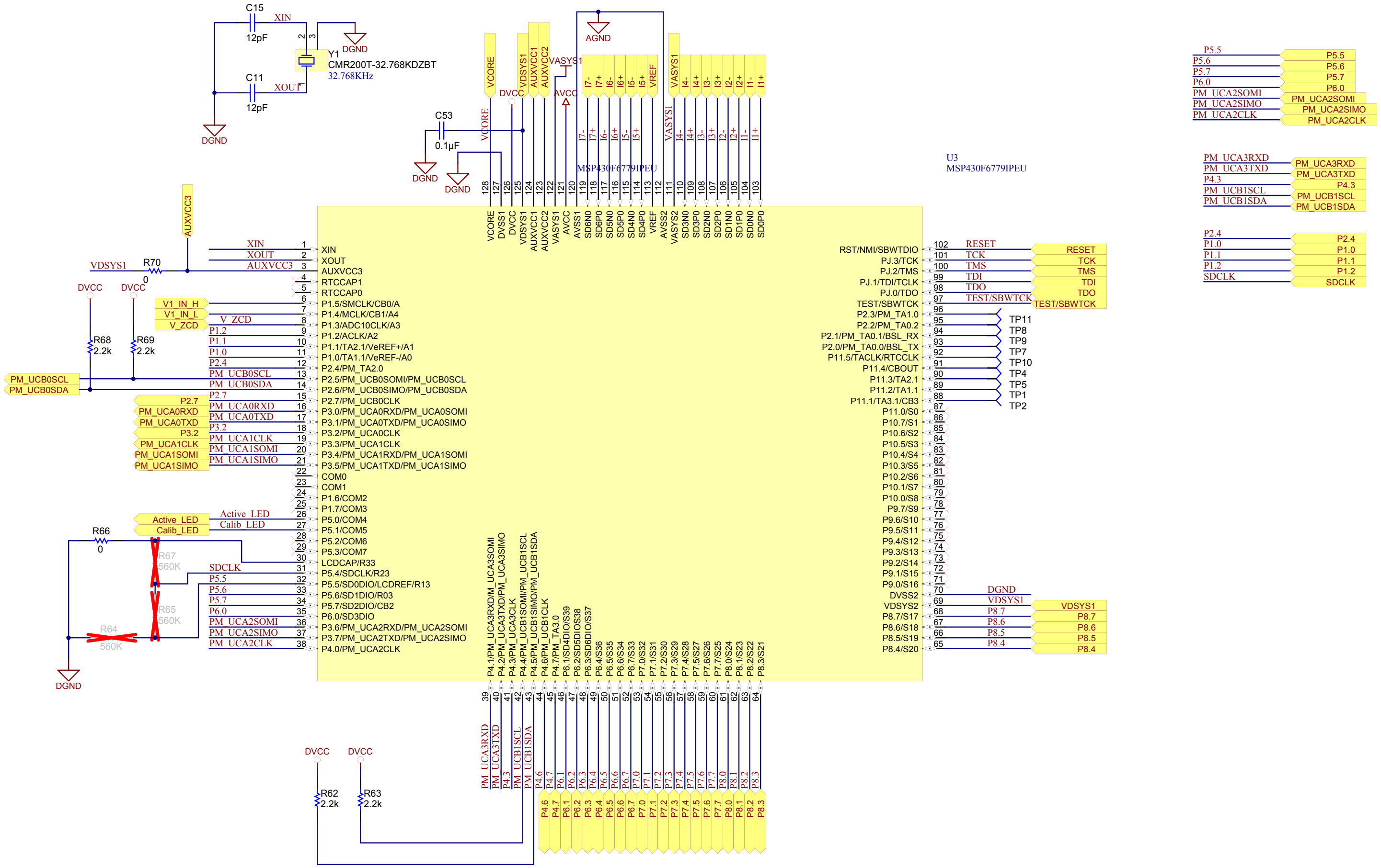

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SVN Rev: Not in version control
Drawn By:
Engineer: Prahlad Supeda

Designed for: Public Release Mod. Date: 7/14/2014
Project Title: TIDA-0022 - ISE3004
Sheet Title: MSP430F6779 + Crystal
Assembly Variant: 001 Sheet: 6 of 8
File: Pg6.MSP430F6779 + Crystal.SchDoc Size: B
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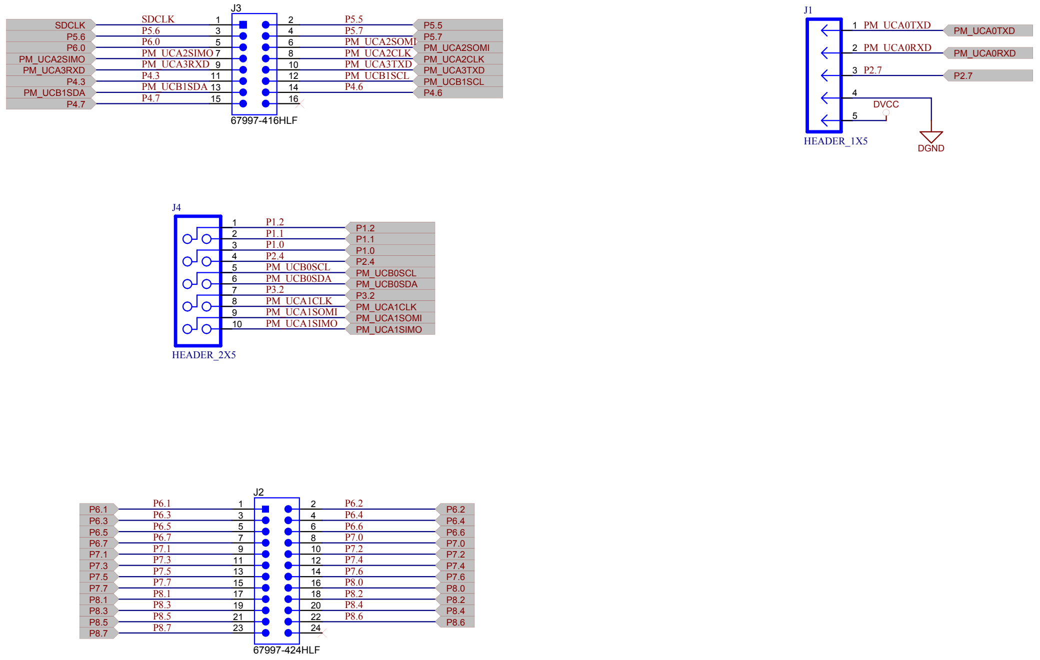

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Designed for: Public Release
Mod. Date: 7/14/2014
Project Title: TIDA-0022 - ISE3004
Number: TIDA-00222
Rev: E1
Sheet Title: Interfaces
SVN Rev: Not in version control
Assembly Variant: 001
Sheet: 7 of 8
Drawn By:
File: Pg7.Interfaces.SchDoc
Size: B
Engineer: Prahlad Supeda
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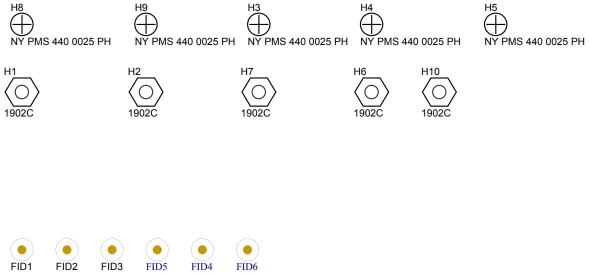

PCB Number: TIDA-00222
PCB Rev: E1

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

Label Table

Variant	Label Text
001	ChangeMe!
002	ChangeMe!

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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SVN Rev: Not in version control
Drawn By:
Engineer: Prahlad Supeda

Designed for: Public Release Mod. Date: 7/14/2014
Project Title: TIDA-0022 - ISE3004
Sheet Title: Hardware - MIiscellaneous
Assembly Variant: 001 Sheet: 8 of 8
File: Pg8.HARDWARE - MISCELLANEOUS.SchDoc Size: B
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