

Vin typ. 12V
 Vin min transient ??? -> testing
 Vin max. transient 60V

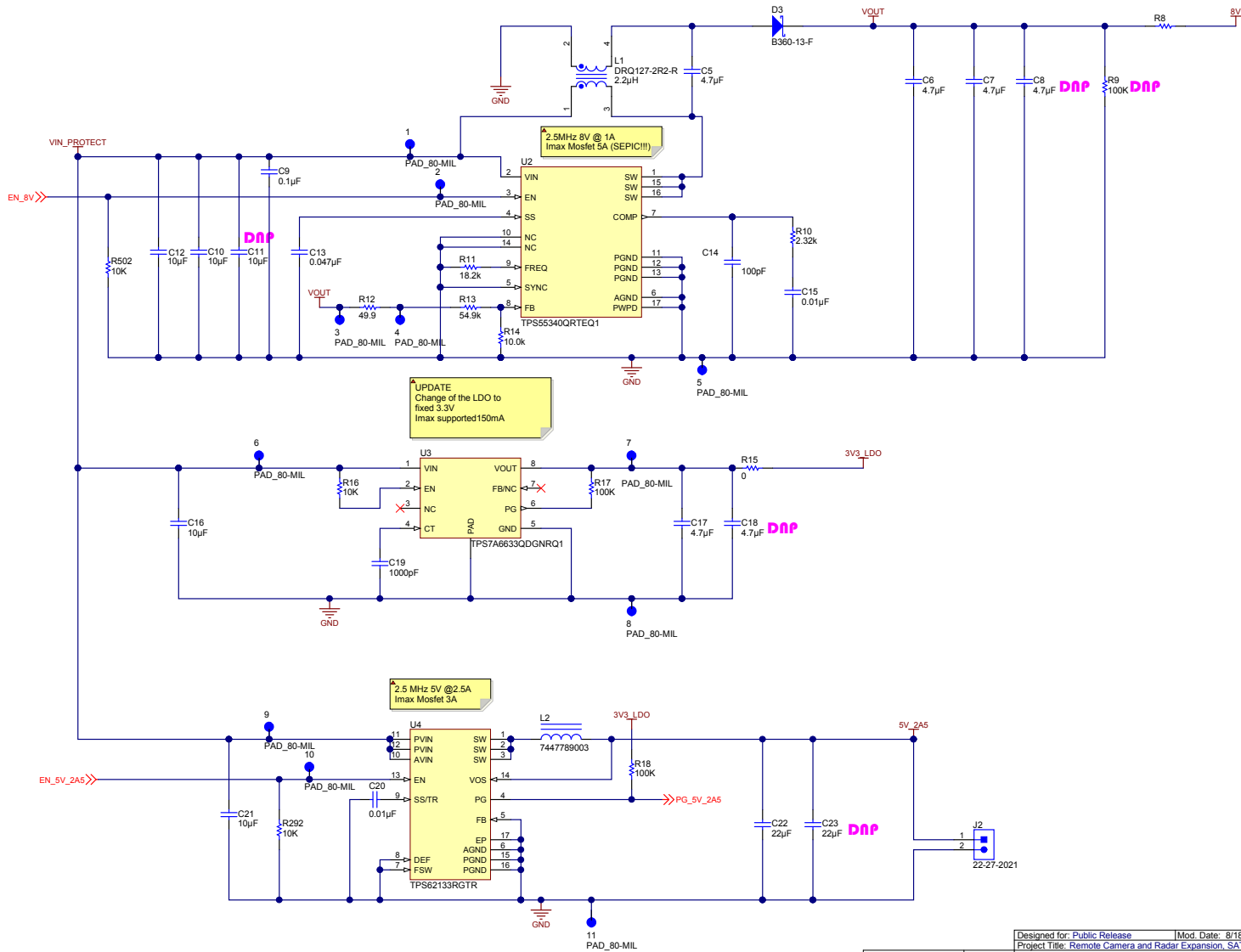
Vout limited to max 16V
 Typical: Iout 2.1A @ 12V P 25.2W
 OR
 MAX: Iout 5.5A @ 4.5V

PENDING
 System designed for 4.5V MIN to 60V MAX input transient voltages, not continuous
 define own spec, testing/measurement needed

INFORMATION
 Vref 1.24V
 Kathode 18V, max 20V
 worst case: Vin 4.5V @ 5.62A

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Number: TIDA-00271	Rev: E2	Designed for: Public Release	Mod. Date: 8/18/2014
SVN Rev: Not in version control	Assembly Variant: Variant name not interpreted	Project Title: Remote Camera and Radar Expansion_SAT0074	Sheet Title:
Drawn By:	File: protection.SchDoc	Size: B	http://www.ti.com
Engineer: Joern Oppenhaeuser	Contact: http://www.ti.com/support	© Texas Instruments 2014	

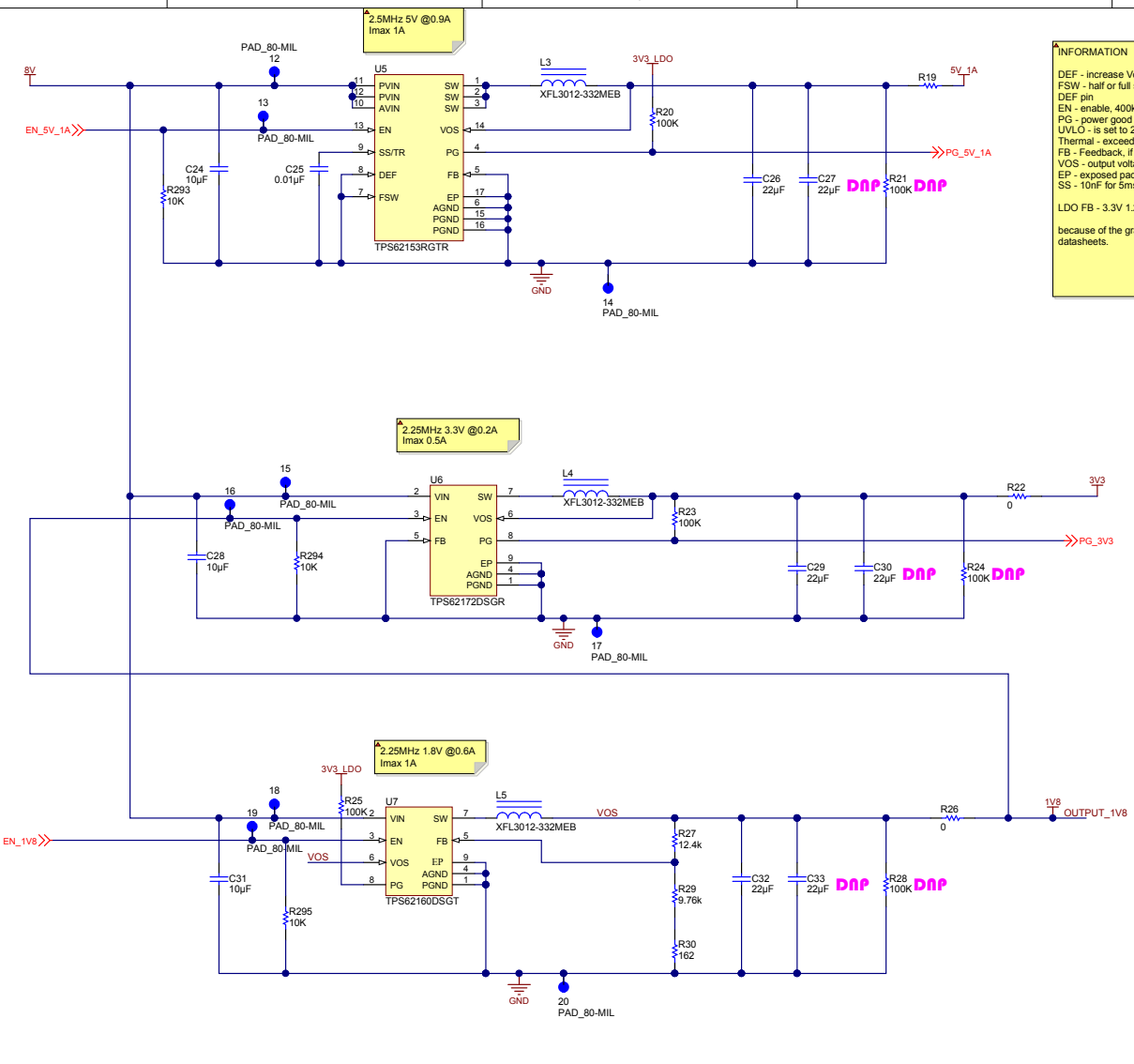


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Drawn By: _____		Sheet Title: _____	
Engineer: Joern Oppenhaeuser	File: Power_SEPIC_SchDoc	Assembly Variant: Variant name not interpreted	Sheet 3 of 13
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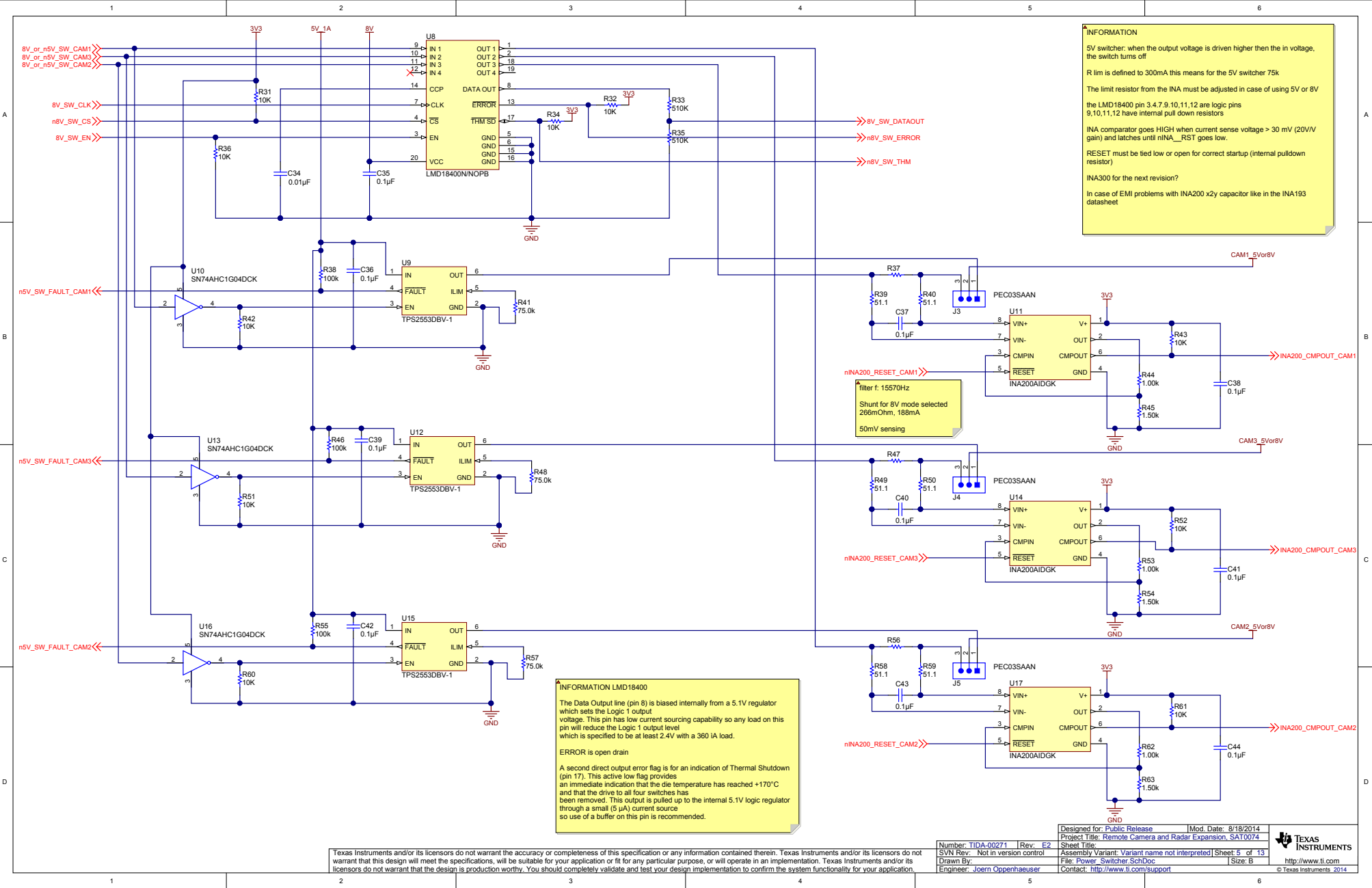


INFORMATION

DEF - increase Vout by 5%, LOW is nominal Vout, internal 400k resistor to LOW existing
 FSW - half or full switching frequency, LOW = full fsw, HIGH = half fsw, internal 400k like DEF pin
 EN - enable, 400k to low, if high the resistor is disconnected
 PG - power good pin, open drain, requires pull up, VIN must be there to stay PG pin low
 LVLG - is set to 2.7v, starts working again at 2.7V + 0.2V
 Thermal - exceeds 160°C then shutdown, -20°C starts working again
 FB - Feedback, if fixed Vout, it is recommended to pull down to GND
 VOS - output voltage sense pin
 EP - exposed pad
 SS - 10nF for 5ms
 LDO FB - 3.3V 1.25V regulation
 because of the grade of integrity, you can only choose inductor values from the datasheets.

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SVN Rev: Not in version control	File: Power_Bucks.SchDoc Size: B	
Drawn By: Engineer: Joern Oppenhaeuser	Contact: http://www.ti.com/support	



INFORMATION

5V switcher: when the output voltage is driven higher than the in voltage, the switch turns off

R lim is defined to 300mA this means for the 5V switcher 75k

The limit resistor from the INA must be adjusted in case of using 5V or 8V

the LMD18400 pin 3,4,7,9,10,11,12 are logic pins
9,10,11,12 have internal pull down resistors

INA comparator goes HIGH when current sense voltage > 30 mV (20VV gain) and latches until nINA_RST goes low.

RESET must be tied low or open for correct startup (internal pulldown resistor)

INA300 for the next revision?

In case of EMI problems with INA200 x2y capacitor like in the INA193 datasheet

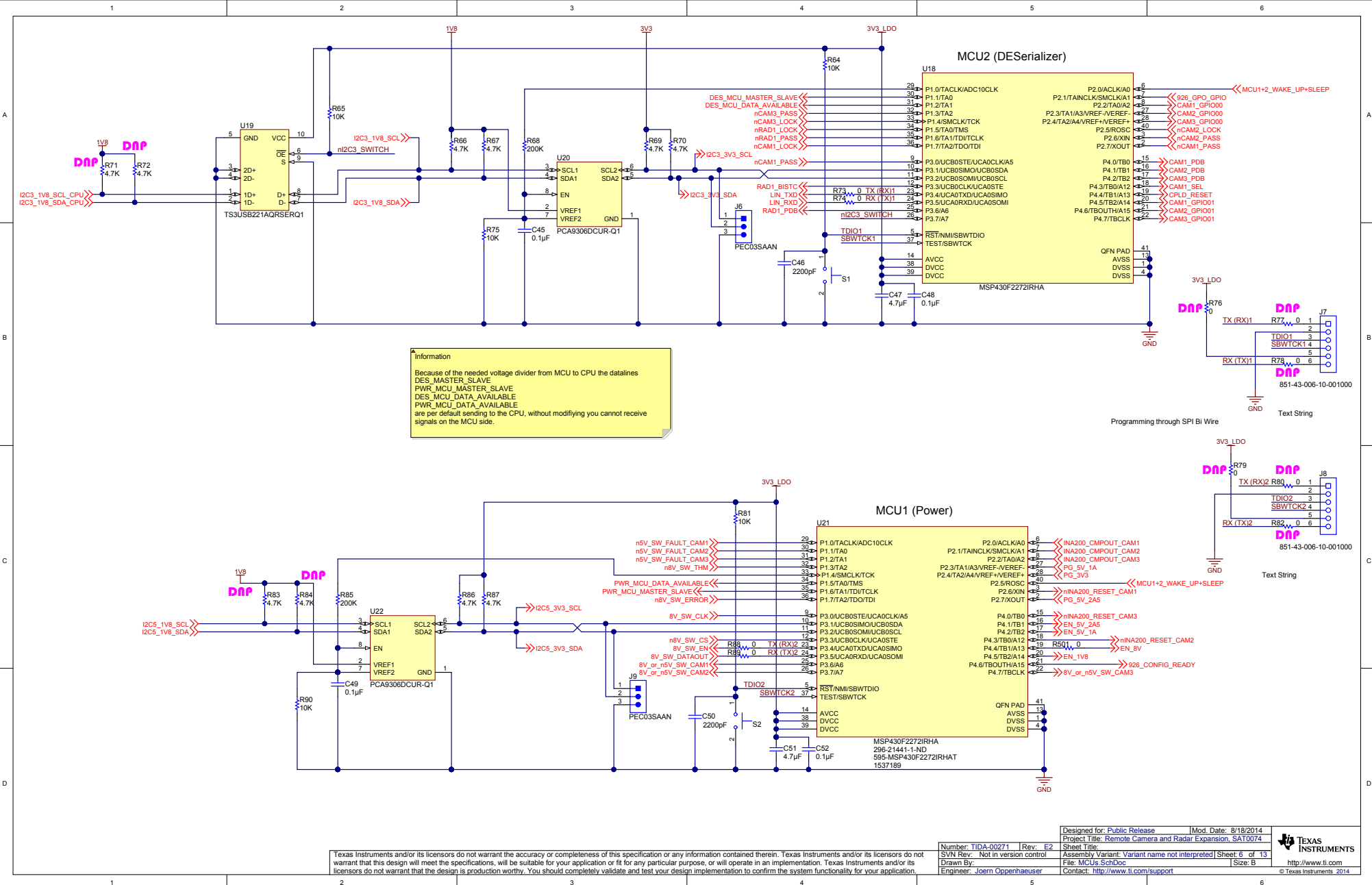
INFORMATION LMD18400

The Data Output line (pin 8) is biased internally from a 5.1V regulator which sets the Logic 1 output voltage. This pin has low current sourcing capability so any load on this pin will reduce the Logic 1 output level which is specified to be at least 2.4V with a 360 I/A load.

ERROR is open drain

A second direct output error flag is for an indication of Thermal Shutdown (pin 17). This active low flag provides an immediate indication that the die temperature has reached +170°C and that the drive to all four switches has been removed. This output is pulled up to the internal 5.1V logic regulator through a small (5 uA) current source so use of a buffer on this pin is recommended.

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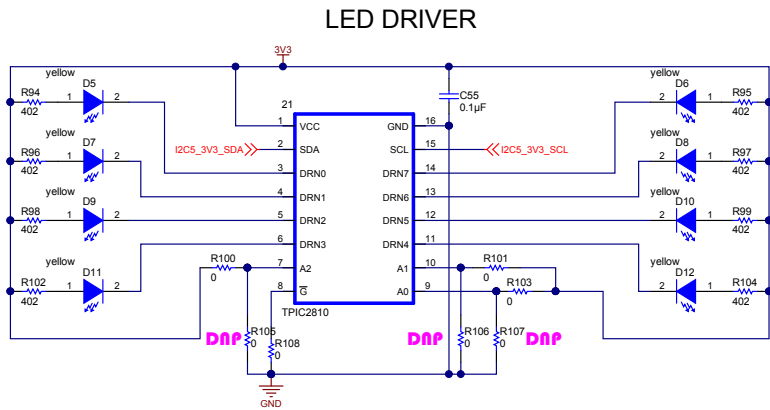
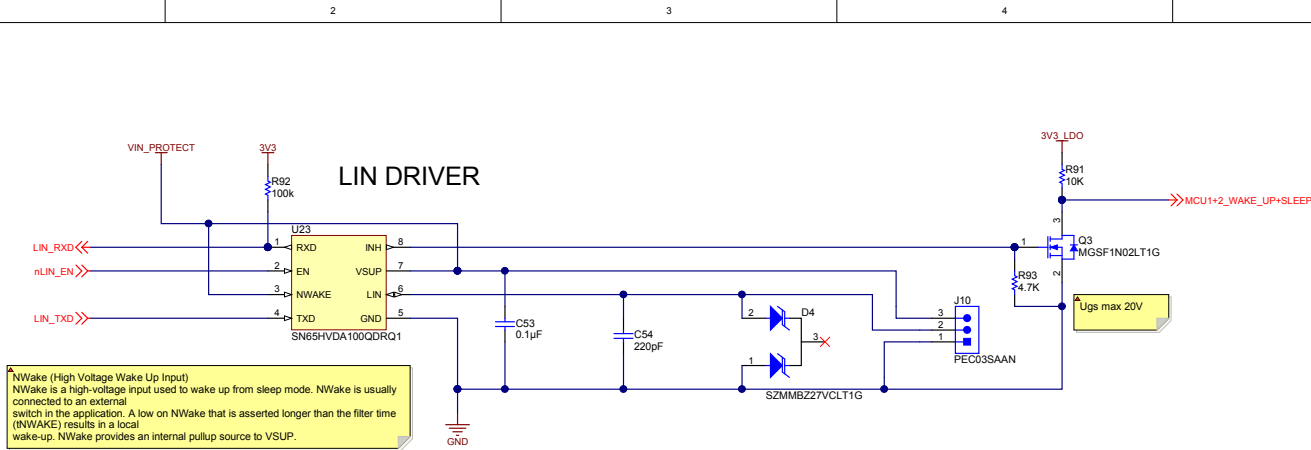
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INFORMATION

LIN
 TXD - Transmit input/output
 RXD - Receive Output
 V_{sup} - Supply Voltage
 EN - Enable input, internal pull down
 N_{WAKE} - high voltage input, to wake up from sleep
 INHIBIT - switches V_{supply} to the pin = 17V

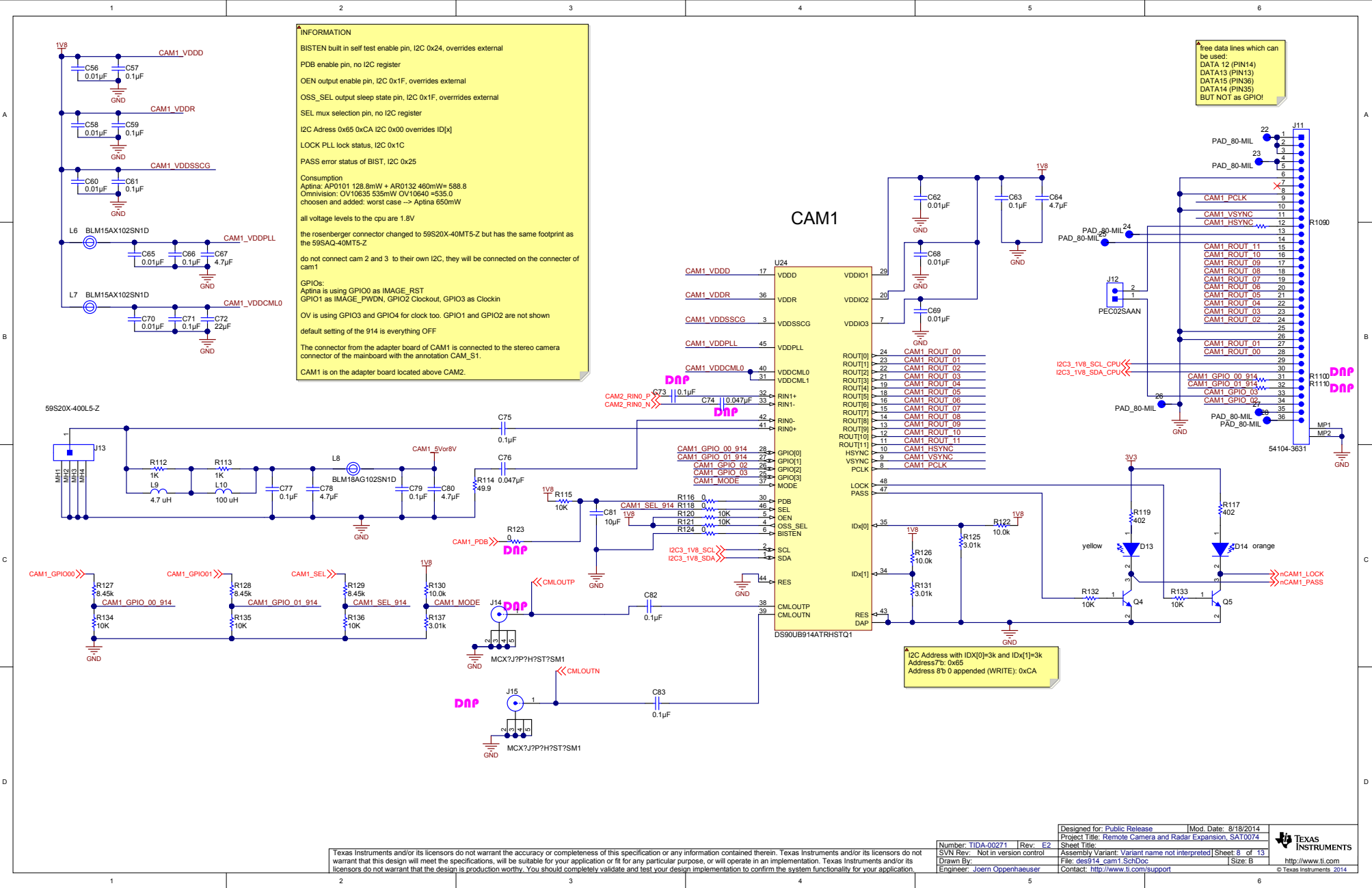
TPIC
 A0, A1, A2 are defining the I2C address via digital logic
 G enables the device outputs

For the HVDA100, the RXD pin is an output, and the TXD pin is an input.



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Number: TIDA-00271 Rev: E2	Assembly Variant: Variant name not interpreted Sheet: 7 of 13	
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Drawn By: Joern Oppenhaeuser	Contact: http://www.ti.com/support	



INFORMATION

BISTEN built in self test enable pin, I2C 0x24, overrides external

PDB enable pin, no I2C register

OEN output enable pin, I2C 0x1F, overrides external

OSS_SEL output sleep state pin, I2C 0x1F, overrides external

SEL mux selection pin, no I2C register

I2C Address 0x65 0xCA I2C 0x00 overrides ID[x]

LOCK PLL lock status, I2C 0x1C

PASS error status of BIST, I2C 0x25

Consumption
 Aptina: AP0101 128.8mW + AR0132 460mW= 588.8
 Omnivision: OV10635 535mW OV10640 =535.0
 chosen and added; worst case -> Aptina 650mW

all voltage levels to the cpu are 1.8V

the rosenberger connector changed to 59S20X-40MT5-Z but has the same footprint as the 59SAQ-40MT5-Z

do not connect cam 2 and 3 to their own I2C, they will be connected on the connector of cam1

GPIOs:
 Aptina is using GPIO0 as IMAGE_RST
 GPIO1 as IMAGE_PWDN, GPIO2 Clockout, GPIO3 as Clockin

OV is using GPIO3 and GPIO4 for clock too. GPIO1 and GPIO2 are not shown

default setting of the 914 is everything OFF

The connector from the adapter board of CAM1 is connected to the stereo camera connector of the mainboard with the annotation CAM_S1.

CAM1 is on the adapter board located above CAM2.

free data lines which can be used:
 DATA12 (PIN14)
 DATA13 (PIN13)
 DATA15 (PIN36)
 DATA14 (PIN35)
 BUT NOT as GPIO!

CAM1

CAM1_VDD	17	VDD	VDDIO1	29
CAM1_VDDR	38	VDDR	VDDIO2	20
CAM1_VDDSSCG	3	VDDSSCG	VDDIO3	7
CAM1_VDDPLL	45	VDDPLL		
CAM1_VDDCML0	40	VDDCML0		
	31	VDDCML1		
CAM1_GPIO_00_914	28	GPIO[0]		
CAM1_GPIO_01_914	27	GPIO[1]		
CAM1_GPIO_02_914	26	GPIO[2]		
CAM1_GPIO_03_914	25	GPIO[3]		
CAM1_MODE	3	MODE		
CAM1_SEL_914	30	PDB		
	48	OEN		
	49	OSS_SEL		
	5	BISTEN		
I2C3_1V8_SCL_CPU	2	SCL		
I2C3_1V8_SDA_CPU	3	SDA		
	44	RES		
	38	CMLOUTP		
	39	CMLOUTN		
	43	RES		
	43	DAP		

I2C Address with IDx[0]=3k and IDx[1]=3k
 Address'b: 0x65
 Address 8'b 0 appended (WRITE): 0xCA

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INFORMATION

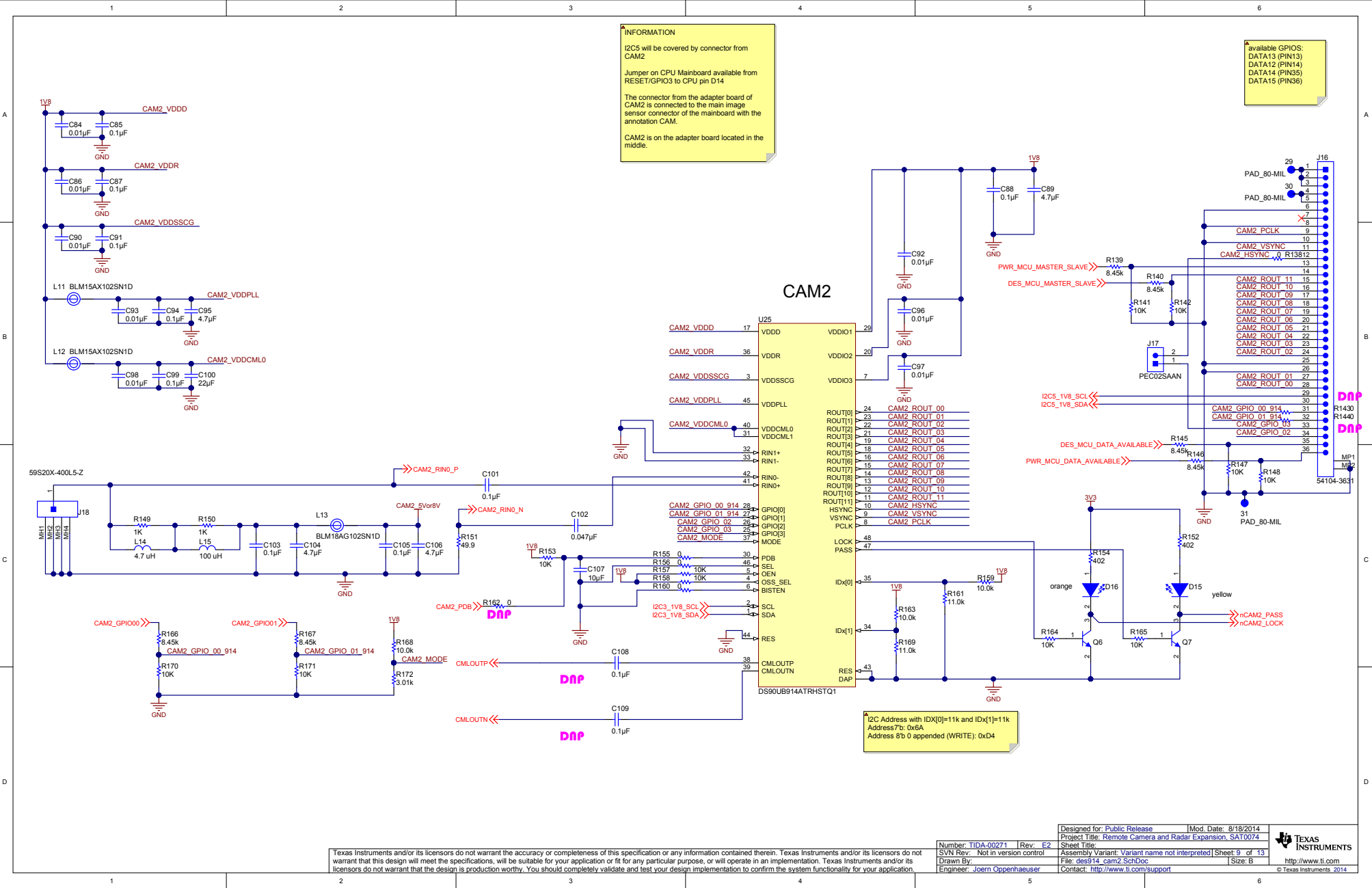
I2C5 will be covered by connector from CAM2

Jumper on CPU Mainboard available from RESET/GPIO3 to CPU pin D14

The connector from the adapter board of CAM2 is connected to the main image sensor connector of the mainboard with the annotation CAM.

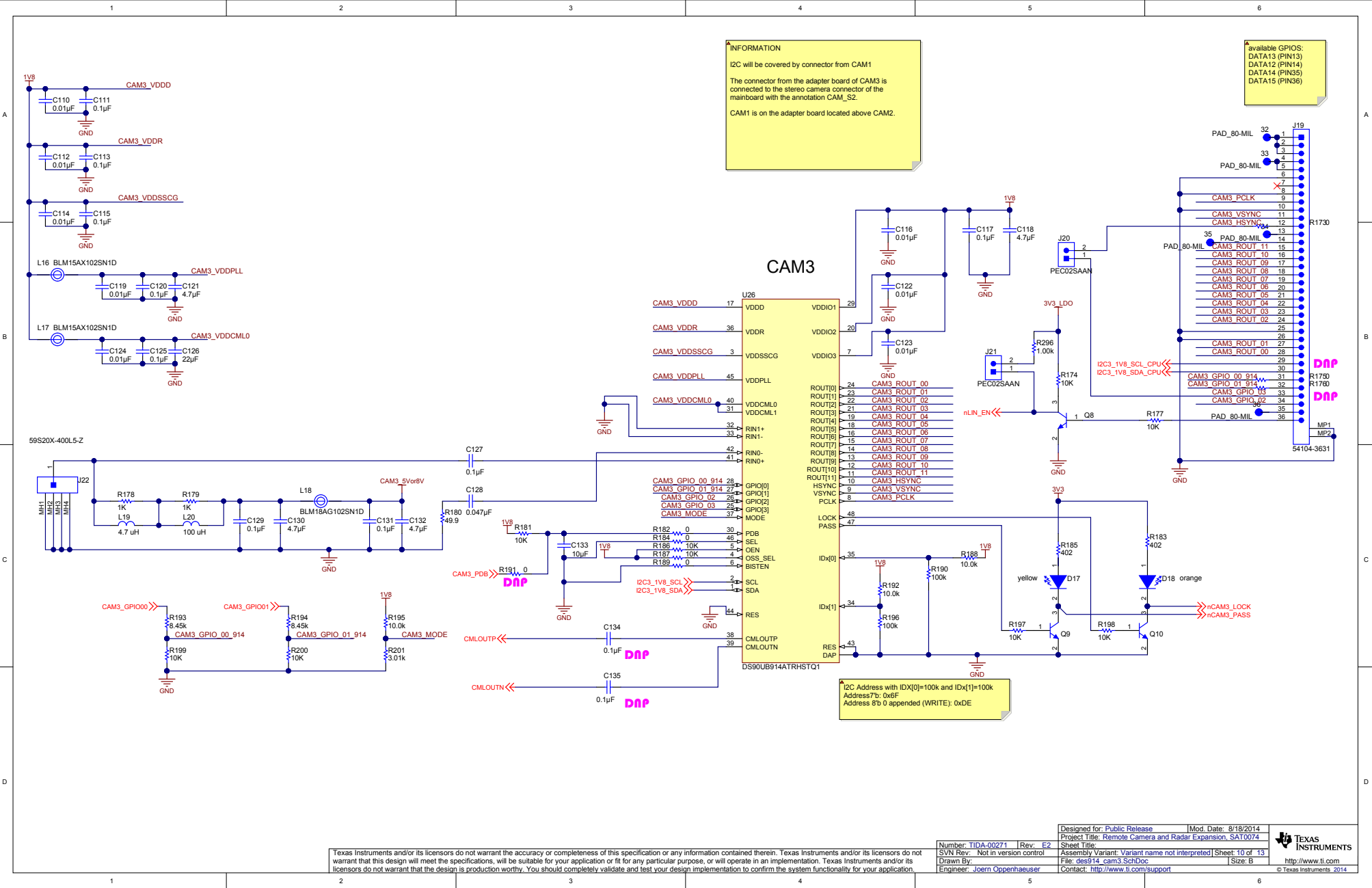
CAM2 is on the adapter board located in the middle.

Available GPIOs:
 DATA13 (PIN13)
 DATA12 (PIN14)
 DATA14 (PIN35)
 DATA15 (PIN36)



I2C Address with IDX[0]=11k and IDX[1]=11k
 Address 7b: 0x6A
 Address 8'b 0 appended (WRITE): 0xD4

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INFORMATION

I2C will be covered by connector from CAM1

The connector from the adapter board of CAM3 is connected to the stereo camera connector of the mainboard with the annotation CAM_S2.

CAM1 is on the adapter board located above CAM2.

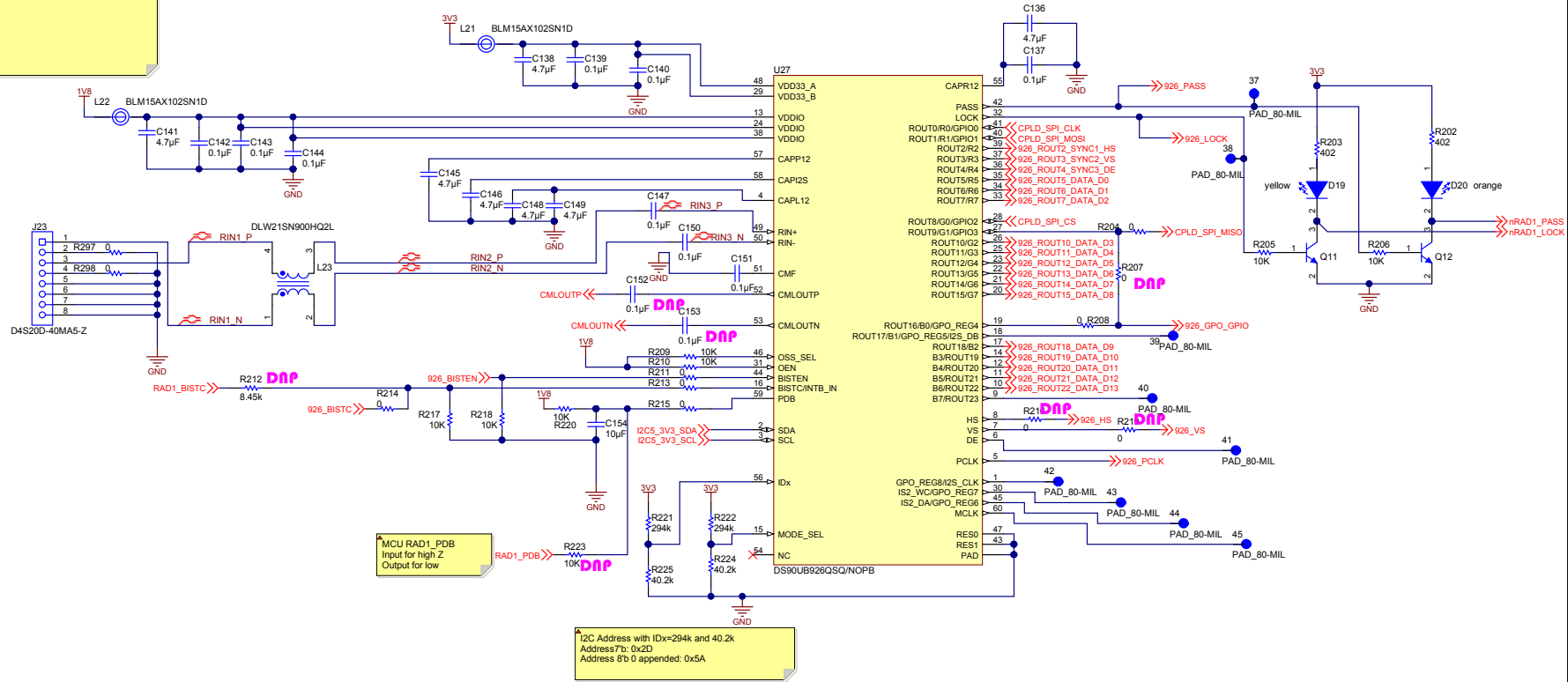
Available GPIOs:
 DATA13 (PIN13)
 DATA12 (PIN14)
 DATA14 (PIN35)
 DATA15 (PIN36)

I2C Address with IDX[0]=100k and IDX[1]=100k
 Address 7b: 0x6F
 Address 8b 0 appended (WRITE): 0xD6

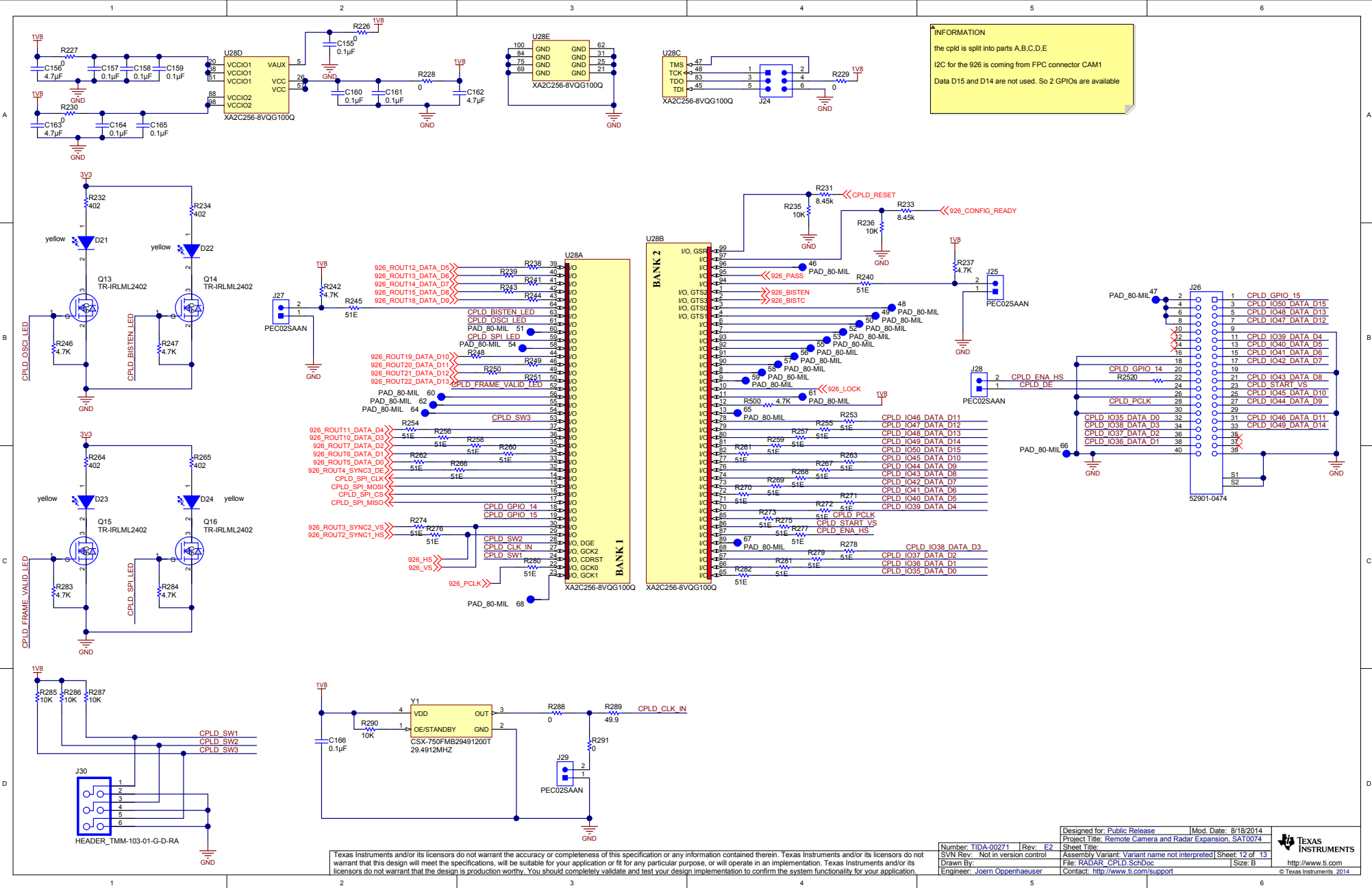
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INFORMATION

- BISTEN built in self test enable pin, no I2C
- PDB enable pin, no I2C register
- OEN output enable pin, I2C 0x02 overrides external
- OSS_SEL Output Sleep State Select pin, I2C 0x02 overrides external
- BISTC BIST Clock select, no I2C
- I2C Address 0x2D 0x5A
- LOCK status PLL lock, I2C 0x1C
- PASS error status of BIST



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INFORMATION
 the cpld is split into parts A,B,C,D,E
 I2C for the 926 is coming from FPC connector CAM1
 Data D15 and D14 are not used. So 2 GPIOs are available

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Drawn By: [Name]	File: RADAR_CPLD_SchDoc
Engineer: Joern Oppenhauser	Contact: http://www.ti.com/support
Sheet 12 of 13	Size: B

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PCB
LOGO
Texas Instruments



PCB Number: TIDA-00271
PCB Rev: E2

You should delete the nylon screws/standoffs and/or the bump-ons as needed for your design (or substitute other parts from Hardware.Int.Lib). Bump-ons are cheaper, but provide less clearance.

Deleting anything else from this page may result in your EVM submission being rejected (until you add them back).

Update the Label Text in the Label Table as needed for each Assembly Variant.

You can delete this note too.

Label Table	
Variant	Label Text
001	ChangeMe!
002	ChangeMe!

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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