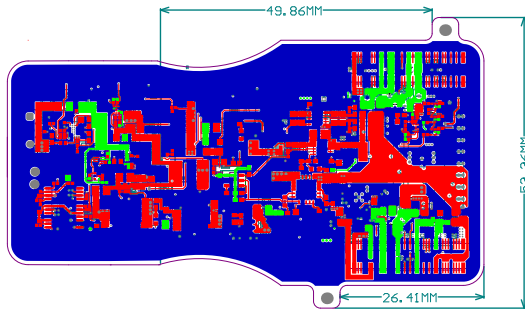


Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4	
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER <input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG) <input type="checkbox"/> ENEPG <input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE <input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3 <input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE <input checked="" type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE <input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE <input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE <input type="checkbox"/> TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	

NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



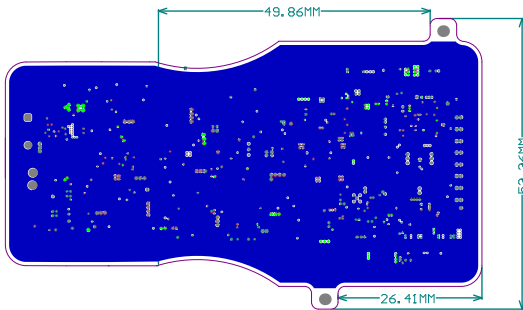
COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. BOARD ASSEMBLY VARIANT: [No Variations]

REV: 00	DATE: 09/12/2013	BY: [Name]	DESCRIPTION: [Description]
LAYER NAME = Top Layer		TID #: 00101010269	DATE: 09/12/2013 3:12:35 PM
PLOT NAME: [Name]		TEXAS INSTRUMENTS	

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ENGINEER:	LAYOUT BY:
Bill. Xu	Bill. Xu
SCALE: 1.00	ALTIUM DESIGNER VERSION:
	24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric	FR-4	7.87mil	4.2	
3	Dielectric 2	CF-004	0.69mil		
4	Signal 1	PP-006	7.87mil	4.1	
5	Dielectric 3	CF-004	0.69mil		
6	Power 1	PP-006	7.87mil	4.1	
7	Dielectric 4	CF-004	0.69mil		
8	Power 2	PP-006	7.87mil	4.1	
9	Dielectric 5	CF-004	0.69mil		
10	Signal 2	PP-006	7.87mil	4.1	
11	Dielectric 6	CF-004	0.69mil		
12	Layer 1	FR-4	7.87mil	4.1	
	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4	
THICKNESS:	62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
DRILLING:	
REFERENCE: <input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS: <input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN: <input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR: <input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER	
SOLDER RESIST COLOR: <input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER <input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS	
SURFACE FINISH: <input checked="" type="checkbox"/> IMMERSION GOLD (ENIG) <input type="checkbox"/> ENEPG <input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE <input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF: <input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3 <input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER:
Bill. Xu

LAYOUT BY:
Bill.Xu

SCALE: 1.00

ALTUM DESIGNER VERSION:
24.9.1.31



COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. COMPONENTS MARKED 'NO VARIATIONS' SHOULD NOT BE ORDERED. COMPONENTS MARKED 'NO VARIATIONS' SHOULD NOT BE ORDERED.

REV: 00	DATE: 09/12/2013	BY: [Signature]	DESCRIPTION: [Signature]
LAYER NAME =	TID #: 010269	DATE: 09/12/2013	TIME: 3:12:38 PM
PLT: [Signature]	DATE: 09/12/2013	TIME: 3:12:38 PM	TXI INSTRUMENTS

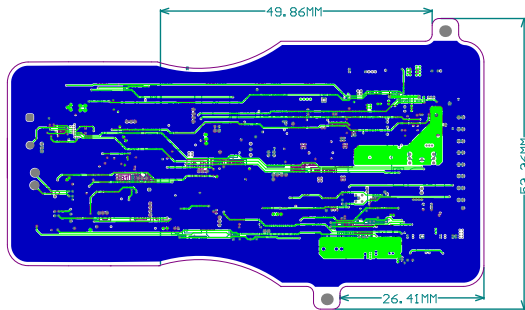
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Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4	
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER <input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG) <input type="checkbox"/> ENEPG <input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE <input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3 <input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE <input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE <input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE <input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE <input type="checkbox"/> TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	

NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD. COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD. ASSEMBLY VARIANT: [No Variations]

REV: 00	DATE: 09/12/2013	BY: [Name]	DESCRIPTION: [Description]
LAYER NAME = [Name]		TID #: 0000000000000000	DATE: 09/12/2013 3:12:40 PM
PLOT NAME: [Name]		I TEXAS INSTRUMENTS	

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ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTIE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

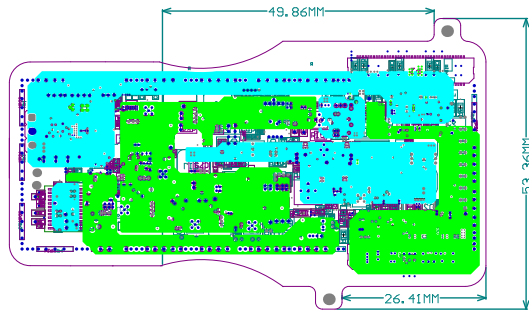
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. COMPONENTS MARKED 'NO VARIATIONS' SHOULD NOT BE ORDERED. COMPONENTS MARKED 'NO VARIATIONS' SHOULD NOT BE ORDERED.

REV: 00	DATE: 09/12/2013	TIME: 3:12:43 PM	USER: jpl
LAYER NAME = Top		TID #: 01010269	DATE: 09/12/2013
PLOT NAME: Top1		GENERATED: 09/12/2013	TIME: 3:12:43 PM

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ENGINEER: Bill. Xu	LAYOUT BY: Bill. Xu
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

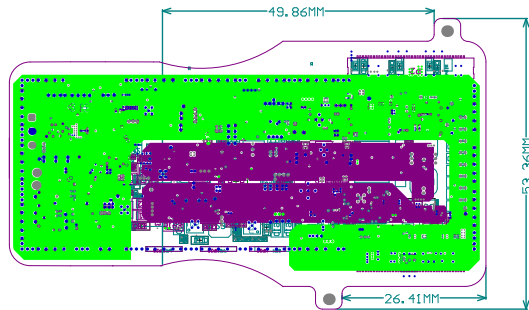
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



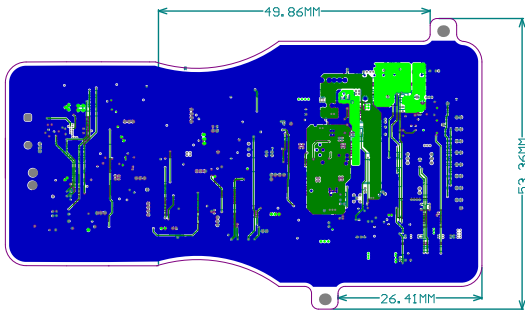
COMPONENTS MARKED 'DNP' SHOULD NOT BE ASSUMED TO BE PRESENT IN THE BOARD.
 ASSEMBLY VARIANT: [No Variations]

REV: 00	DATE: 09/12/2013	BY: [Name]	DESCRIPTION: [Description]
LAYER NAME = [Name]		TID #: 00101010269	# DIT: [Value]
PLOT DATE: 09/12/2013		GENERATED: 09/12/2013	3:12:48 PM

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ENGINEER: Bill. Xu	LAYOUT BY: Bill. Xu
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
3	Dielectric 2	CF-004	0.69mil		
4	Signal 1	PP-006	7.87mil	4.1	
5	Dielectric 3	CF-004	0.69mil		
6	Power 1	PP-006	7.87mil	4.1	
7	Dielectric 4	CF-004	0.69mil		
8	Power 2	PP-006	7.87mil	4.1	
9	Dielectric 5	CF-004	0.69mil		
10	Signal 2	PP-006	7.87mil	4.1	
11	Dielectric 6	CF-004	0.69mil		
12	Layer 1	FR-4	7.87mil	4.1	
13	Dielectric 1	FR-4	7.87mil	4.1	
14	Bottom Layer		2.76mil		
15	Bottom Solder	Solder Resist	1.00mil	3.5	
16	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW & TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL
 MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTIE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER:
Bill. Xu

LAYOUT BY:
Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION:
24.9.1.31



COMPONENTS MARKED 'DNP' SHOULD NOT BE ASSUMED TO BE PRESENT IN THE BOARD.
 ASSEMBLY VARIANT: [No Variations]

REV: 00	DATE: 09/12/2023	BY: [Signature]	DESCRIPTION: [Signature]
LAYER NAME =	TID #: 010269	DATE: 09/12/2023	TIME: 3:12:52 PM
PLT: [Signature]	DATE: 09/12/2023	TIME: 3:12:52 PM	BY: TEXAS INSTRUMENTS

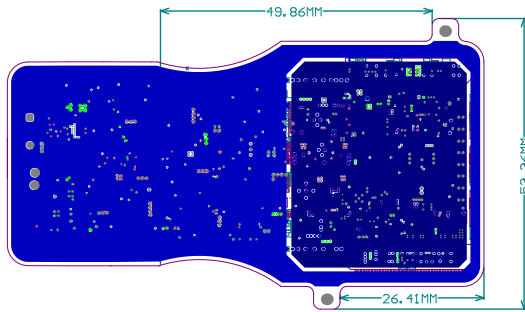
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Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4	
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/- 10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER <input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG) <input type="checkbox"/> ENEPG <input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE <input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3 <input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	

NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



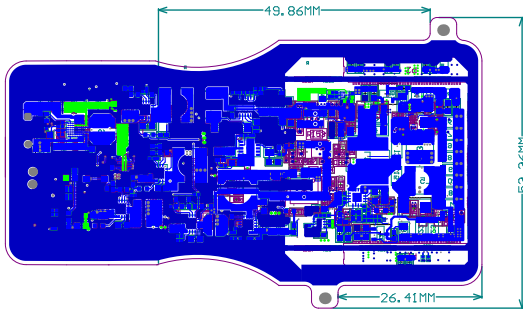
COMPONENTS MARKED 'DNP' SHOULD NOT BE ASSUMED TO BE PRESENT IN THE BOARD. COMPONENTS MARKED 'NO VARIATIONS' ARE NOT REQUIRED FOR THIS BOARD. (NO VARIATIONS)

REV: 00	DATE: 09/12/2013	BY: JTB	DESCRIPTION: Smart Probe Power Supply
LAYER NAME = Top		TID #: 010269	DATE: 09/12/2013
PLOT DATE: 09/12/2013		TIME: 3:12:56 PM	BY: JTB

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ENGINEER:	LAYOUT BY:
Bill. Xu	Bill. Xu
SCALE: 1.00	ALTIUM DESIGNER VERSION:
	24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
3	Dielectric 2	CF-004	0.69mil		
4	Signal 1	PP-006	7.87mil	4.1	
5	Dielectric 3	CF-004	0.69mil		
6	Power 1	PP-006	7.87mil	4.1	
7	Dielectric 4	CF-004	0.69mil		
8	Power 2	PP-006	7.87mil	4.1	
9	Dielectric 5	CF-004	0.69mil		
10	Signal 2	PP-006	7.87mil	4.1	
11	Dielectric 6	CF-004	0.69mil		
12	Layer 1	FR-4	7.87mil	4.1	
13	Dielectric 1	FR-4	7.87mil	4.1	
14	Bottom Layer		2.76mil		
15	Bottom Solder	Solder Resist	1.00mil	3.5	
16	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW & TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4	
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/- 10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER <input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENIG) <input type="checkbox"/> ENEPG <input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE <input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3 <input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE <input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE <input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE <input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE <input type="checkbox"/> TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER:
Bill. Xu

LAYOUT BY:
Bill. Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION:
24.9.1.31



COMPONENTS MARKED 'DNP' SHOULD NOT BE ASSUMED TO BE PRESENT IN THE BOARD.
ASSEMBLY VARIANT: [No Variations]

REV: 00	DATE: 09/12/2013	BY: JTB	DESCRIPTION: INITIAL RELEASE
LAYER NAME =	TID #: 010269	DATE: 09/12/2013	TIME: 3:12:08 PM
PLT: TIDA-010269	DATE: 09/12/2013	TIME: 3:12:08 PM	BY: JTB

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

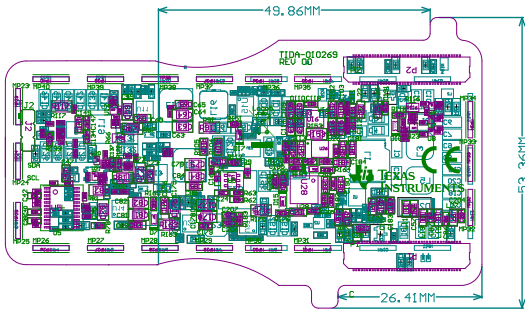
ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

- NOTES: (UNLESS OTHERWISE SPECIFIED)
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED.
 ASSEMBLY VARIANT: (No Variations) ASSEMBLY VARIANT: (No Variations)

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PROJECT TITLE: Smart Probe Power Supply
 DESIGNED FOR: Public Release
 FILE NAME: TIDA-010269.PcbDoc
 ENGINEER: Bill. Xu
 LAYOUT BY: Bill. Xu
 SCALE: 1.00
 ALTUM DESIGNER VERSION: 24.9.1.31

REV: 00	DATE: 09/13/2024	BY: [Signature]	DESCRIPTION: [Signature]
LAYER NAME = Top Silkscreen Overlay		TID #: TIDA-010269	REV: 00
PLOT NAME = Top Silkscreen Overlay		GENERATED: 9/13/2024 3:13:06 PM	BY: [Signature]

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

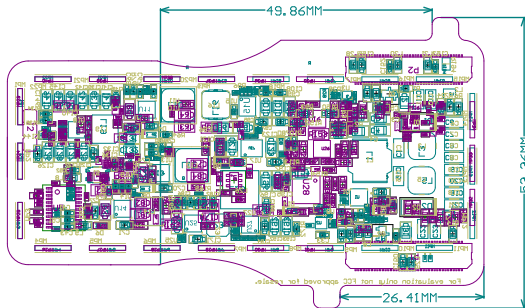
ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. THIS DOCUMENT IS UNCLASSIFIED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. THIS DOCUMENT IS UNCLASSIFIED.

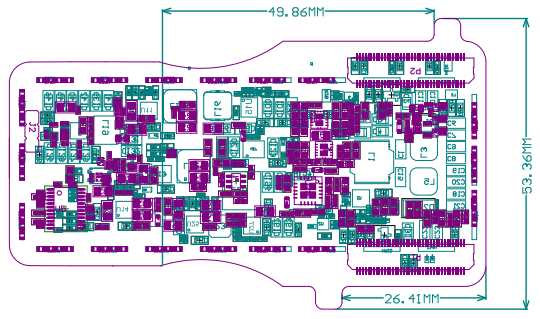
REV: 00	DATE: 09/12/2013	DESIGNED BY: SUN JIE	DESIGNED FOR: SUN JIE
LAYER NAME = Bottom	TID #: 80010A-010269	DATE: 09/12/2013	DESIGNED BY: SUN JIE
PLOT NAME: Bottom Silkscreen	GENERATED: 09/12/2013 09:10:00	DESIGNED BY: SUN JIE	DESIGNED FOR: SUN JIE

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ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
3	GND1	CF-004	0.69mil		
4	Dielectric 2	PP-006	7.87mil	4.1	
5	Signal 1	CF-004	0.69mil		
6	Dielectric 3	PP-006	7.87mil	4.1	
7	Power 1	CF-004	0.69mil		
8	Dielectric 4	PP-006	7.87mil	4.1	
9	Power 2	CF-004	0.69mil		
10	Dielectric 5	PP-006	7.87mil	4.1	
11	Signal 2	CF-004	0.69mil		
12	Dielectric 6	PP-006	7.87mil	4.1	
13	Layer 1	CF-004	0.69mil		
14	Dielectric 1	FR-4	7.87mil	4.1	
15	Bottom Layer		2.76mil		
16	Bottom Solder	Solder Resist	1.00mil	3.5	
17	Bottom Overlay				

Z23 ■ These assemblies must be checked for compliance with the following requirements:
 Z24 ■ These assemblies must comply with the following requirements:
 Z22 ■ These assemblies are ESD sensitive and must be observed.
 Z21 ■ Install label in silkscreen.



- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW & TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE ASSUMED TO BE PRESENT IN THE BOARD ASSEMBLY VARIANT: [No Variations]

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DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER
 SOLDER RESIST COLOR: GREEN OTHER
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:
 Smart Probe Power Supply

DESIGNED FOR:
 Public Release

FILE NAME:
 TIDA-010269.PcbDoc

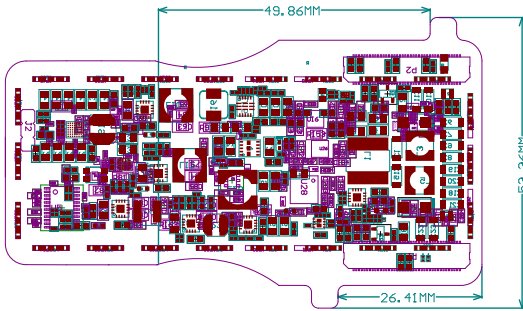
ENGINEER:
 Bill. Xu

LAYOUT BY:
 Bill.Xu

SCALE: 1.00

ALTUM DESIGNER VERSION:
 24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
	GND1	CF-004	0.69mil		
3	Dielectric 2	PP-006	7.87mil	4.1	
	Signal 1	CF-004	0.69mil		
4	Dielectric 3	PP-006	7.87mil	4.1	
	Power 1	CF-004	0.69mil		
5	Dielectric 4	PP-006	7.87mil	4.1	
	Power 2	CF-004	0.69mil		
6	Dielectric 5	PP-006	7.87mil	4.1	
	Signal 2	CF-004	0.69mil		
7	Dielectric 6	PP-006	7.87mil	4.1	
	Layer 1	CF-004	0.69mil		
8	Dielectric 1	FR-4	7.87mil	4.1	
	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD. ASSEMBLY VARIANT: [No Variations]

REV: 00	DATE: 09/13/2013	BY: [Name]	DESCRIPTION: [Description]
LAYER NAME = [Name]		TID #: 00101010269	# DIT: [Value]
PLOT NAME: [Name]		GENERATED: 9/13/2013 3:13:13 PM	TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4	
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/- 10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER <input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENIG) <input type="checkbox"/> ENEPG <input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE <input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3 <input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE <input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE <input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE <input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE <input type="checkbox"/> TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	ALTUM DESIGNER VERSION: 24.9.1.31

Z23 ■ These assemblies must be checked for compliance with the following requirements:
 Z24 ■ These assemblies must comply with the following requirements:
 Z22 ■ These assemblies are ESD sensitive and must be observed.
 Z21 ■ Install label in silkscreen.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
	GND1	CF-004	0.69mil		
3	Dielectric 2	PP-006	7.87mil	4.1	
	Signal 1	CF-004	0.69mil		
4	Dielectric 3	PP-006	7.87mil	4.1	
	Power 1	CF-004	0.69mil		
5	Dielectric 4	PP-006	7.87mil	4.1	
	Power 2	CF-004	0.69mil		
6	Dielectric 5	PP-006	7.87mil	4.1	
	Signal 2	CF-004	0.69mil		
7	Dielectric 6	PP-006	7.87mil	4.1	
	Layer 1	CF-004	0.69mil		
8	Dielectric 1	FR-4	7.87mil	4.1	
	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW & TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTIE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

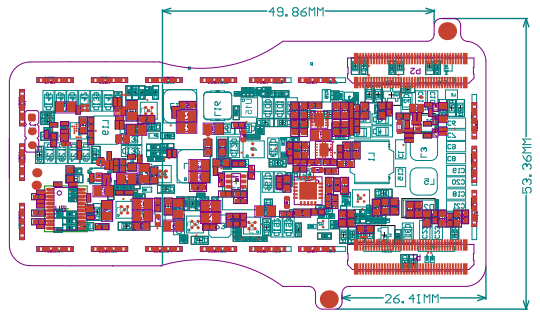
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD. COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD. COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD.

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TEXAS INSTRUMENTS

PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER:
Bill. Xu

LAYOUT BY:
Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION:
24.9.1.31

REV: 00	DATE: 09/13/2023	BY: jk	DESCRIPTION: INITIAL RELEASE
LAYER NAME = Top Solder Mask	TID #: 010269	QTY: 1	QTY: 1
PLotted: 9/13/2023 3:13:20 PM	Generated: 9/13/2023 3:13:20 PM	Author: jk	Company: TEXAS INSTRUMENTS

A

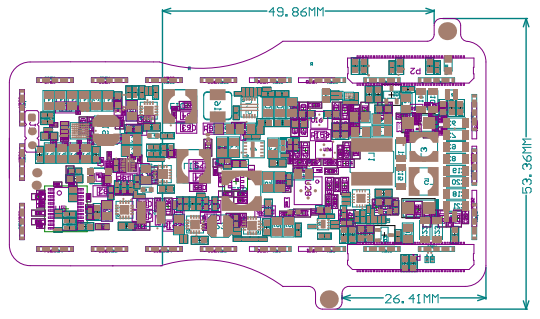
Z23 ■ These assemblies must be checked for compliance with the following requirements:
 Z24 ■ These assemblies must comply with the following requirements:
 Z22 ■ These assemblies are ESD sensitive and should be observed.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

B

C

D



NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD.
 COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD.
 ASSEMBLY VARIANT: [No Variations]

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DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL
 MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER
 SOLDER RESIST COLOR: GREEN OTHER
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:
 Smart Probe Power Supply

DESIGNED FOR:
 Public Release

FILE NAME:
 TIDA-010269.PcbDoc

ENGINEER:
 Bill. Xu

LAYOUT BY:
 Bill.Xu

SCALE: 1.00

ALTUM DESIGNER VERSION:
 24.9.1.31

REV: 00	DATE: 09/13/2013	TIME: 13:25	BY: [Signature]	DESCRIPTION: [Signature]
LAYER NAME = Top		TID #: 010269	SUN 09/13/2013 13:25	
PLOT NAME = Top		GENERATED: 9/13/2013 13:25	TEXAS INSTRUMENTS	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

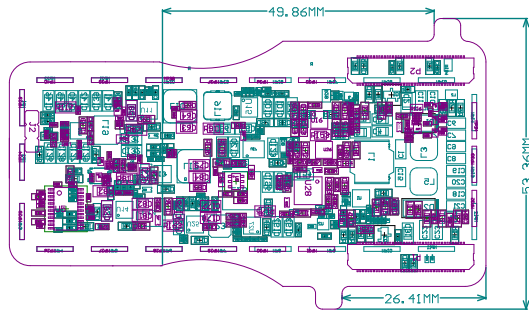
ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. BOARD ASSEMBLY VARIANT: [No Variations]

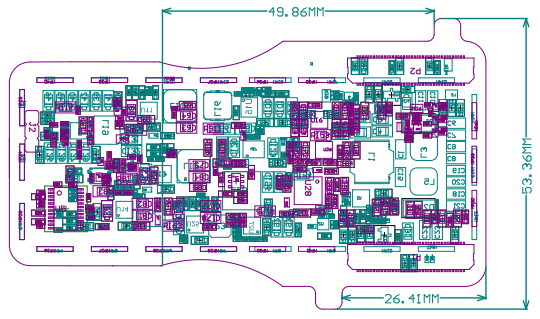
REV: 00	DATE: 08/01/2019	BY: SUN	DESCRIPTION: INCR TO 8 WIRE 5.0V REGULATOR
LAYER NAME = Top	TID #: 00101010269	# DIT	08
PLTNAME: TI Board Outline	GENERATED: 08/01/2019	3:13:28 PM	enituo b Texas Instruments

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ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	ALTUM DESIGNER VERSION: 24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

Z23 ■ These assemblies must be checked for compliance with the following requirements:
 Z24 ■ These assemblies must comply with the following requirements:
 Z22 ■ These assemblies are ESD sensitive and must be observed.
 Z21 ■ Install label in silkscreen.



- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
 ASSEMBLY VARIANT: [No Variations]

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TEXAS INSTRUMENTS

PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER:
Bill. Xu

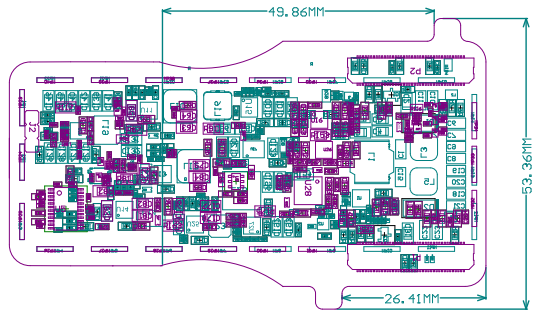
LAYOUT BY:
Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION:
24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

Z23 ■ These assemblies must be checked for compliance with the following requirements:
 Z24 ■ These assemblies must comply with the following requirements:
 Z22 ■ These assemblies are ESD sensitive and must be observed.
 Z21 ■ Install label in silkscreen.



- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER
 SOLDER RESIST COLOR: GREEN OTHER
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD.
 COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD.
 ASSEMBLY VARIANT: [No Variations]

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TEXAS INSTRUMENTS

PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER:
Bill. Xu

LAYOUT BY:
Bill.Xu

SCALE: 1.00

ALTUM DESIGNER VERSION:
24.9.1.31

REV: 00	DATE: 09/13/2023	BY: qot	DESCRIPTION: INITIAL RELEASE
LAYER NAME = Top	TID #: 010269	DATE: 09/13/2023	TIME: 3:13:35 PM
PLOT DATE: 09/13/2023 3:13:35 PM			

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

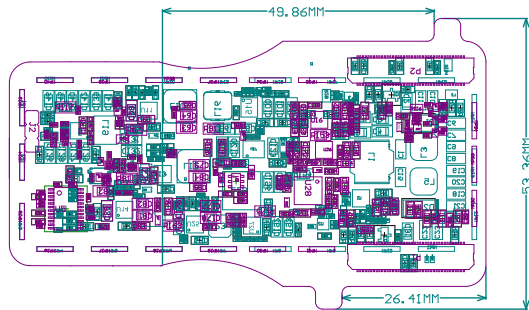
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
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 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
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COMPONENTS MARKED 'DNP' Should NOT BE POPULATED. COMPONENTS MARKED 'DNP' Should NOT BE POPULATED. COMPONENTS MARKED 'DNP' Should NOT BE POPULATED.
 ASSEMBLY VARIANT: [No Variations]

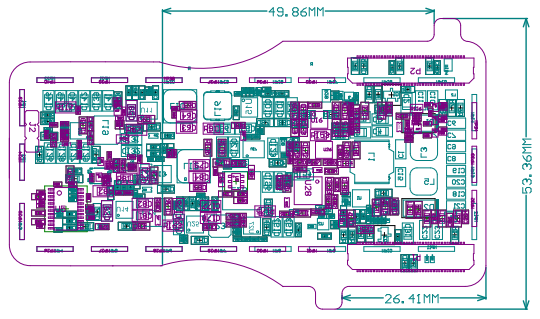
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ENGINEER: Bill. Xu
 LAYOUT BY: Bill. Xu
 SCALE: 1.00
 ALTUM DESIGNER VERSION: 24.9.1.31

REV: 00	DATE: 09/13/2013	BY: [Signature]	DESCRIPTION: [Signature]
LAYER NAME =	TID #: 00101010269	DATE: 09/13/2013	TIME: 3:13:39 PM
PLT: [Signature]	DATE: 09/13/2013	TIME: 3:13:39 PM	BY: [Signature]

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
3	Dielectric 2	PP-006	7.87mil	4.1	
4	Signal 1	CF-004	0.69mil		
5	Dielectric 3	PP-006	7.87mil	4.1	
6	Power 1	CF-004	0.69mil		
7	Dielectric 4	PP-006	7.87mil	4.1	
8	Power 2	CF-004	0.69mil		
9	Dielectric 5	PP-006	7.87mil	4.1	
10	Signal 2	CF-004	0.69mil		
11	Dielectric 6	PP-006	7.87mil	4.1	
12	Layer 1	CF-004	0.69mil		
13	Dielectric 1	FR-4	7.87mil	4.1	
14	Bottom Layer		2.76mil		
15	Bottom Solder	Solder Resist	1.00mil	3.5	
16	Bottom Overlay				

Z23 ■ These assemblies must be checked for compliance with the following requirements:
 Z24 ■ These assemblies must comply with the following requirements:
 Z22 ■ These assemblies are ESD sensitive and must be observed.
 Z21 ■ Install label in silkscreen.



- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
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 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
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 - BOARD DIMENSION: 90 MM X 53.36 MM.
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DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

TEXAS INSTRUMENTS

PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER:
Bill. Xu

LAYOUT BY:
Bill.Xu

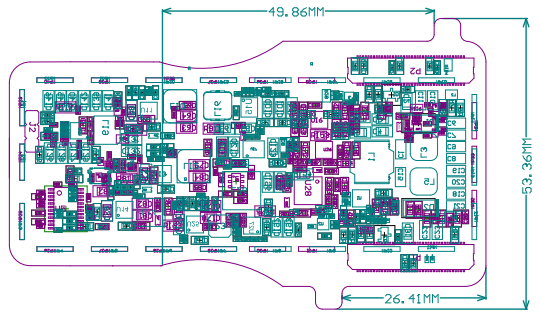
SCALE: 1.00

ALTUM DESIGNER VERSION:
24.9.1.31

REV: 00	DATE: 09/13/2023	BY: [Signature]	DESCRIPTION: [Signature]
LAYER NAME =	TID #: 010269	DATE: 09/13/2023	BY: [Signature]
PLT: [Signature]	DATE: 09/13/2023	BY: [Signature]	DESCRIPTION: [Signature]

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

Z23 ■ These assemblies must be checked for compliance with the following requirements:
 Z24 ■ These assemblies must comply with the following requirements:
 Z22 ■ These assemblies are ESD sensitive and must be observed.
 Z21 ■ Install label in silkscreen.



- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



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REV: 00	DATE: 08/01/2019	BY: SUN	DESCRIPTION: INTRN
LAYER NAME = Top		TID #: 00101010269	QTY: 1
PLOT NAME = Assembly Bottom		GENERATED: 9/18/2019 3:13:47 PM	BY: TEXAS INSTRUMENTS

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TEXAS INSTRUMENTS

PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

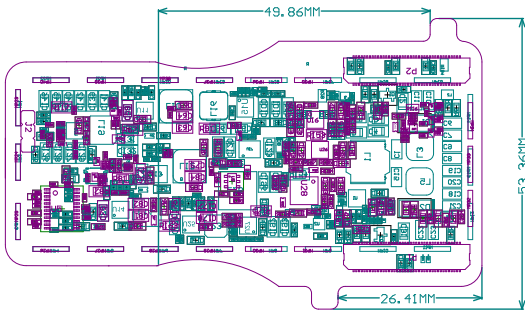
ENGINEER:
Bill. Xu

LAYOUT BY:
Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION:
24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD. COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD. ASSEMBLY VARIANT: [No Variations]

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DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408	<input type="checkbox"/> FR-4 High Tg
<input checked="" type="checkbox"/> OTHER	FR-4
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/- 10%
<input type="checkbox"/> OTHER	
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN
<input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um
<input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP
<input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE
<input type="checkbox"/> OTHER	
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN
<input type="checkbox"/> OTHER	
<input checked="" type="checkbox"/> MATTE	<input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENIG)	<input type="checkbox"/> ENEPIG
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE	<input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1
<input checked="" type="checkbox"/> 2	<input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION:	<input type="checkbox"/> YES
BARE BOARD ELEC. TEST:	<input type="checkbox"/> NONE
<input checked="" type="checkbox"/> REQUIRED	<input type="checkbox"/> PER ORDER
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER:
Bill. Xu

LAYOUT BY:
Bill. Xu

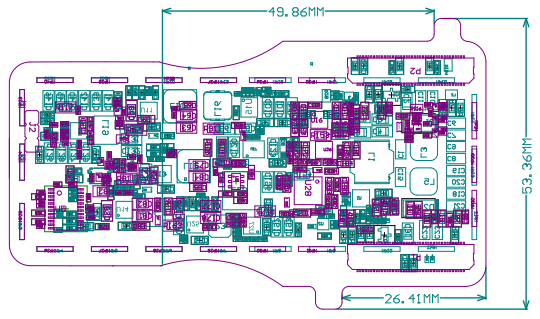
SCALE: 1.00

ALTIUM DESIGNER VERSION:
24.9.1.31

REV: 00	DATE: 09/13/2024	BY: [Name]	DESCRIPTION: [Description]
LAYER NAME = [Layer Name]			
PLOT NAME = [Plot Name]			

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

Z23 ■ These assemblies must be checked for compliance with the following requirements:
 Z24 ■ These assemblies must comply with the following requirements:
 Z22 ■ These assemblies are ESD sensitive and must be observed.
 Z21 ■ Install label in silkscreen.



- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
 ASSEMBLY VARIANT: [No Variations]

REV: 00	DATE: 09/18/2013	BY: [Name]	DESCRIPTION: [Description]
LAYER NAME = [Name]		TID #: 00101010269	DATE: 09/18/2013
PLOT DATE: 09/18/2013		TIME: 3:13:53 PM	BY: [Name]

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ENGINEER: Bill. Xu	LAYOUT BY: Bill. Xu
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
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	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

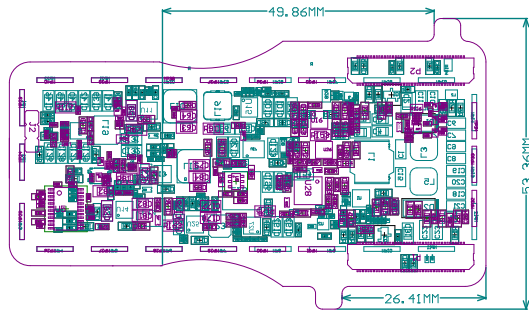
ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. THIS DOCUMENT IS UNCLASSIFIED AND NOT FOR DISTRIBUTION OUTSIDE THE COMPANY.
 ASSEMBLY VARIANT: [No Variations]

REV: 00	DATE: 09/13/2024	BY: [Name]	DESCRIPTION: [Description]
LAYER NAME = [Name]		TID #: 00010A-010269	# DIT: [Value]
PLOT NAME: [Name]		GENERATED: 9/13/2024 3:13:52 PM	BY: [Name]

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ENGINEER: Bill. Xu	LAYOUT BY: Bill. Xu
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
	GND1	CF-004	0.69mil		
3	Dielectric 2	PP-006	7.87mil	4.1	
	Signal 1	CF-004	0.69mil		
4	Dielectric 3	PP-006	7.87mil	4.1	
	Power 1	CF-004	0.69mil		
5	Dielectric 4	PP-006	7.87mil	4.1	
	Power 2	CF-004	0.69mil		
6	Dielectric 5	PP-006	7.87mil	4.1	
	Signal 2	CF-004	0.69mil		
7	Dielectric 6	PP-006	7.87mil	4.1	
	Layer 1	CF-004	0.69mil		
8	Dielectric 1	FR-4	7.87mil	4.1	
	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

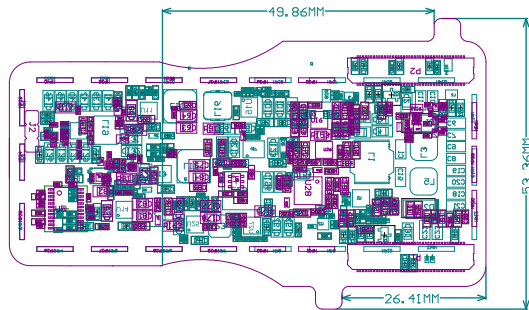
ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



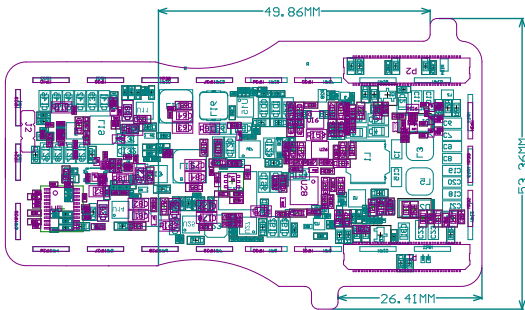
COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
 ASSEMBLY VARIANT: [No Variations]

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ENGINEER: Bill. Xu
 LAYOUT BY: Bill. Xu
 SCALE: 1.00
 ALTUM DESIGNER VERSION: 24.9.1.31

REV: 00	DATE: 09/13/2023	BY: [Signature]	DESCRIPTION: [Signature]
LAYER NAME = Top		TID #: 00101010269	DATE: 09/13/2023
PLOT NAME = [Signature]		GENERATED: 09/13/2023 3:13:59 PM	BY: [Signature]

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
3	Dielectric 2	PP-006	7.87mil	4.1	
4	Signal 1	CF-004	0.69mil		
5	Dielectric 3	PP-006	7.87mil	4.1	
6	Power 1	CF-004	0.69mil		
7	Dielectric 4	PP-006	7.87mil	4.1	
8	Power 2	CF-004	0.69mil		
9	Dielectric 5	PP-006	7.87mil	4.1	
10	Signal 2	CF-004	0.69mil		
11	Dielectric 6	PP-006	7.87mil	4.1	
12	Layer 1	CF-004	0.69mil		
13	Dielectric 1	FR-4	7.87mil	4.1	
14	Bottom Layer		2.76mil		
15	Bottom Solder	Solder Resist	1.00mil	3.5	
16	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
- SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
- FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
- FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
- FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
- BOARD DIMENSION: 90 MM X 53.36 MM.
- TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
- ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

REV: 00	DATE: 08/14/2013	BY: SUN	DESCRIPTION: INVERTER BOARD
LAYER NAME =	TID #: 00101010269	DATE: 08/14/2013	BY: SUN
PLotted in: C:\Program Files\Texas Instruments\PCB Tools\PCBPlot\PCBPlot.exe			

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DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4	
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/- 10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
DRILLING:	
REFERENCE: <input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS: <input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN: <input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR: <input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER	
SOLDER RESIST COLOR: <input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER <input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS	
SURFACE FINISH: <input checked="" type="checkbox"/> IMMERSION GOLD (ENIG) <input type="checkbox"/> ENEPG <input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE <input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF: <input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3 <input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE:
Smart Probe Power Supply

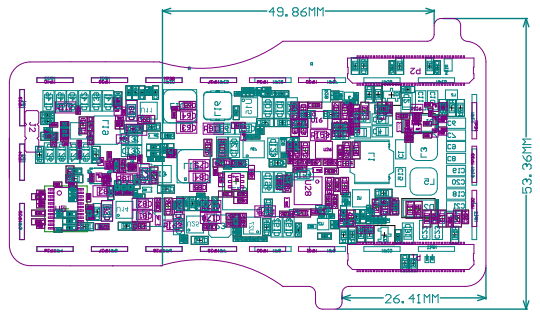
DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	
ALTIUM DESIGNER VERSION: 24.9.1.31	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
3	Dielectric 2	PP-006	7.87mil	4.1	
4	Signal 1	CF-004	0.69mil		
5	Dielectric 3	PP-006	7.87mil	4.1	
6	Power 1	CF-004	0.69mil		
7	Dielectric 4	PP-006	7.87mil	4.1	
8	Power 2	CF-004	0.69mil		
9	Dielectric 5	PP-006	7.87mil	4.1	
10	Signal 2	CF-004	0.69mil		
11	Dielectric 6	PP-006	7.87mil	4.1	
12	Layer 1	CF-004	0.69mil		
13	Dielectric 1	FR-4	7.87mil	4.1	
14	Bottom Layer		2.76mil		
15	Bottom Solder	Solder Resist	1.00mil	3.5	
16	Bottom Overlay				

Z23 ■ These assemblies must be checked for compliance with the following requirements:
 Z24 ■ These assemblies must comply with the following requirements:
 Z22 ■ These assemblies are ESD sensitive and should be observed.
 Z21 ■ Install label in silkscreen.



- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

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TEXAS INSTRUMENTS

PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER:
Bill. Xu

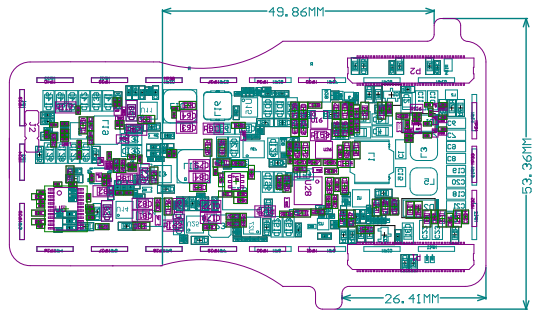
LAYOUT BY:
Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION:
24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
3	GND1	CF-004	0.69mil		
4	Dielectric 2	PP-006	7.87mil	4.1	
5	Signal 1	CF-004	0.69mil		
6	Dielectric 3	PP-006	7.87mil	4.1	
7	Power 1	CF-004	0.69mil		
8	Dielectric 4	PP-006	7.87mil	4.1	
9	Power 2	CF-004	0.69mil		
10	Dielectric 5	PP-006	7.87mil	4.1	
11	Signal 2	CF-004	0.69mil		
12	Dielectric 6	PP-006	7.87mil	4.1	
13	Layer 1	CF-004	0.69mil		
14	Dielectric 1	FR-4	7.87mil	4.1	
15	Bottom Layer		2.76mil		
16	Bottom Solder	Solder Resist	1.00mil	3.5	
17	Bottom Overlay				

Z23 ■ These assemblies must be checked for compliance with the following requirements:
 Z24 ■ These assemblies must comply with the following requirements:
 Z22 ■ These assemblies are ESD sensitive and should be observed.
 Z21 ■ Install label in silkscreen.



- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. THIS DOCUMENT IS UNCLASSIFIED AND NOT FOR DISTRIBUTION OUTSIDE THE COMPANY. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. THIS DOCUMENT IS UNCLASSIFIED AND NOT FOR DISTRIBUTION OUTSIDE THE COMPANY.

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TEXAS INSTRUMENTS

PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER:
Bill. Xu

LAYOUT BY:
Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION:
24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

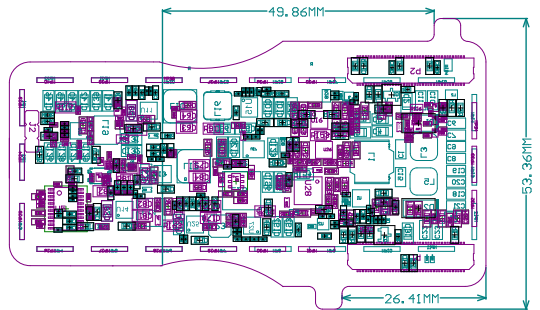
ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
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 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. BOARD ASSEMBLY VARIANT: [No Variations]

REV: 00	DATE: 08/14/2013	BY: [Signature]	DESCRIPTION: [Signature]
LAYER NAME = Top		TID #: 00101010269	QTY: 1
PLOT NAME = [Signature]		GENERATED: 08/14/2013 03:14:11 PM	BY: [Signature]

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ENGINEER: Bill. Xu	LAYOUT BY: Bill. Xu
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
	GND1	CF-004	0.69mil		
3	Dielectric 2	PP-006	7.87mil	4.1	
	Signal 1	CF-004	0.69mil		
4	Dielectric 3	PP-006	7.87mil	4.1	
	Power 1	CF-004	0.69mil		
5	Dielectric 4	PP-006	7.87mil	4.1	
	Power 2	CF-004	0.69mil		
6	Dielectric 5	PP-006	7.87mil	4.1	
	Signal 2	CF-004	0.69mil		
7	Dielectric 6	PP-006	7.87mil	4.1	
	Layer 1	CF-004	0.69mil		
8	Dielectric 1	FR-4	7.87mil	4.1	
	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

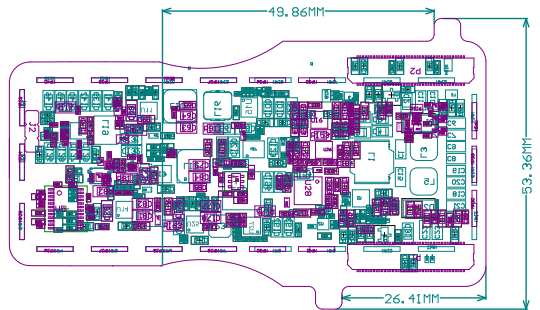
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
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 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. ASSEMBLY VARIANT: [No Variations]

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ENGINEER: Bill. Xu
 LAYOUT BY: Bill. Xu
 SCALE: 1.00
 ALTUM DESIGNER VERSION: 24.9.1.31

REV: 00	DATE: 08/14/2013	BY: [Name]	DESCRIPTION: [Description]
LAYER NAME = [Name]		TID #: [Number]	DATE: [Date]
PLOT NAME = [Name]		GENERATED: [Date]	3:14:14 PM

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

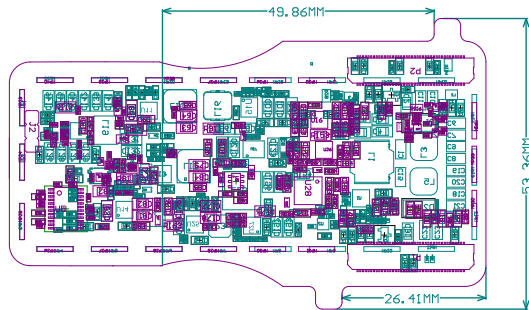
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
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COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

REV: 00	DATE: 09/17/2023	DESIGNED BY: Bill Xu	CHECKED BY: Bill Xu
LAYER NAME = Top	TID #: 010269	DATE: 09/17/2023	TIME: 14:17
PLOT NAME: Embedded Assembly			

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ENGINEER: Bill Xu	LAYOUT BY: Bill Xu
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
3	Dielectric 2	PP-006	7.87mil	4.1	
4	Signal 1	CF-004	0.69mil		
5	Dielectric 3	PP-006	7.87mil	4.1	
6	Power 1	CF-004	0.69mil		
7	Dielectric 4	PP-006	7.87mil	4.1	
8	Power 2	CF-004	0.69mil		
9	Dielectric 5	PP-006	7.87mil	4.1	
10	Signal 2	CF-004	0.69mil		
11	Dielectric 6	PP-006	7.87mil	4.1	
12	Layer 1	CF-004	0.69mil		
13	Dielectric 1	FR-4	7.87mil	4.1	
14	Bottom Layer		2.76mil		
15	Bottom Solder	Solder Resist	1.00mil	3.5	
16	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

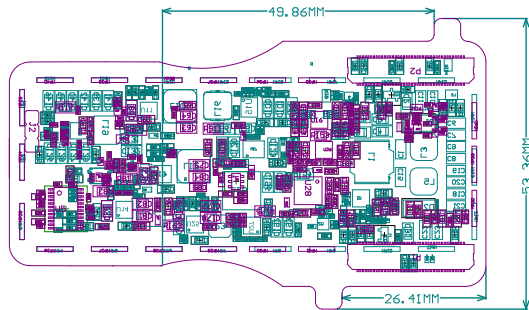
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
 ASSEMBLY VARIANT: [No Variations]

REV: 00	DATE: 09/12/2013	BY: SUN	DESCRIPTION: INVERTER BOARD
LAYER NAME = Top	TID #: 00101010269	QTY: 1	QTY: 1
PLT: 00101010269	DATE: 09/12/2013	TIME: 3:14:20 PM	BY: K

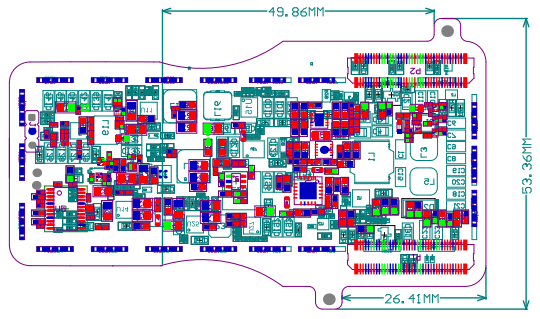
Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER: Bill. Xu	LAYOUT BY: Bill. Xu
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
3	Dielectric 2	PP-006	7.87mil	4.1	
4	Signal 1	CF-004	0.69mil		
5	Dielectric 3	PP-006	7.87mil	4.1	
6	Power 1	CF-004	0.69mil		
7	Dielectric 4	PP-006	7.87mil	4.1	
8	Power 2	CF-004	0.69mil		
9	Dielectric 5	PP-006	7.87mil	4.1	
10	Signal 2	CF-004	0.69mil		
11	Dielectric 6	PP-006	7.87mil	4.1	
12	Layer 1	CF-004	0.69mil		
13	Dielectric 1	FR-4	7.87mil	4.1	
14	Bottom Layer		2.76mil		
15	Bottom Solder	Solder Resist	1.00mil	3.5	
16	Bottom Overlay				

Z23 ■ These assemblies must be checked for compliance with the following requirements:
 Z24 ■ These assemblies must comply with the following requirements:
 Z22 ■ These assemblies are ESD sensitive because they contain the following components:
 Z21 ■ Install label in silkscreen location.

- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW & TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE ASSUMED TO BE PRESENT IN THE BOARD.
 COMPONENTS MARKED 'DNP' SHOULD NOT BE ASSUMED TO BE PRESENT IN THE BOARD.
 ASSEMBLY VARIANT: [No Variations]

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DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER
 SOLDER RESIST COLOR: GREEN OTHER
 MATTIE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:
 Smart Probe Power Supply

DESIGNED FOR:
 Public Release

FILE NAME:
 TIDA-010269.PcbDoc

ENGINEER:
 Bill. Xu

LAYOUT BY:
 Bill.Xu

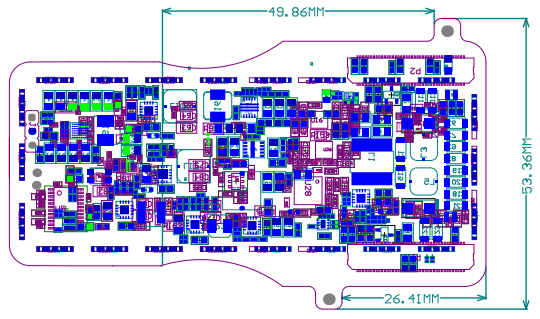
SCALE: 1.00

ALTUM DESIGNER VERSION:
 24.9.1.31

REV: 00	DATE: 09/12/2013	TIME: 3:14:29 PM	USER: jay
LAYER NAME = Top Pad Master	TID #: 010269	DATE: 09/12/2013	TIME: 3:14:29 PM
PLTNAME: Top Pad Master	GENERATED: 09/12/2013	TIME: 3:14:29 PM	USER: jay

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

Z23 ■ These assemblies must be checked for compliance with the following requirements:
 Z24 ■ These assemblies must comply with the following requirements:
 Z22 ■ These assemblies are ESD sensitive. Observe the following requirements:
 Z21 ■ Install label in silkscreen.



- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW & TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
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 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNUAL RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

DRILLING:

REFERENCE: AS SHOWN NC_DRILL FILES

PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:

SILKSCREEN: TOP BOTTOM

SILKSCREEN COLOR: WHITE OTHER

SOLDER RESIST COLOR: GREEN OTHER
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD.
 ASSEMBLY VARIANT: [No Variations]

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TEXAS INSTRUMENTS

PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER:
Bill. Xu

LAYOUT BY:
Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION:
24.9.1.31

REV: 00	DATE: 09/11/2024	BY: [Name]	DESCRIPTION: [Description]
LAYER NAME = [Name]		TID #: 010269	DATE: 09/11/2024
PLOT NAME: [Name]		GENERATED: 09/11/2024 3:14:27 PM	TEXAS INSTRUMENTS

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
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4	Power 1	CF-004	0.69mil		
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	Dielectric 5	PP-006	7.87mil	4.1	
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8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

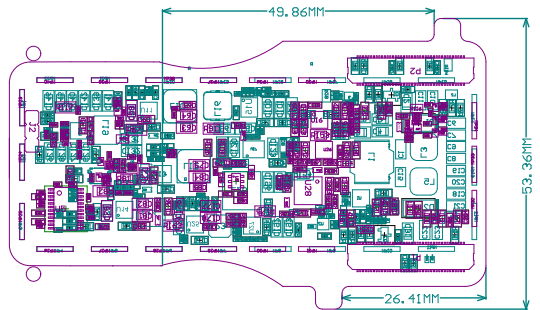
Z23 ■ These assemblies must be checked for correct assembly. If any discrepancies are observed, please contact the supplier for clarification.

Z24 ■ These assemblies must be checked for correct assembly. If any discrepancies are observed, please contact the supplier for clarification.

Z22 ■ These assemblies are ESD sensitive. Please handle with care.

Z21 ■ Install label in silkscreen location.

- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
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 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
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 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
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 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE PLACED ON THE BOARD. THIS IS AN ASSEMBLY VARIANT: (No Variations)

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DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

DRILLING:
 AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER
 SOLDER RESIST COLOR: GREEN OTHER
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc

ENGINEER:
Bill. Xu

LAYOUT BY:
Bill. Xu

SCALE: 1.00

ALTUM DESIGNER VERSION:
24.9.1.31

REV: 00	DATE: 09/18/2023	BY: JTB	DESCRIPTION: BOARD RELEASE
LAYER NAME = Top		TID #: 010269	DATE: 09/18/2023
PLOT DATE: 09/18/2023		TIME: 3:14:30 PM	FILE: TIDA-010269.PcbDoc

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair
⊙	8	5.91mil (0.150mm)	PTH	Round	Top Layer - Bottom Layer
⊙	298	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer
◇	1	8.27mil (0.210mm)	PTH	Round	Top Layer - Bottom Layer
⊗	37	8.65mil (0.220mm)	PTH	Round	Top Layer - Bottom Layer
⊙	336	9.84mil (0.250mm)	PTH	Round	Top Layer - Bottom Layer
▽	288	11.81mil (0.300mm)	PTH	Round	Top Layer - Bottom Layer
□	1	19.69mil (0.500mm)	PTH	Round	Top Layer - Bottom Layer
▽	2	31.50mil (0.800mm)	PTH	Round	Top Layer - Bottom Layer
⊙	3	35.43mil (0.900mm)	PTH	Round	Top Layer - Bottom Layer
⊙	3	120.00mil (3.048mm)	NPTH	Round	Top Layer - Bottom Layer
	976 Total				

Z23 ■ These assemblies must be checked for correct assembly. If any discrepancies are noted, please contact the assembly area.

Z24 ■ These assemblies must be checked for correct assembly. If any discrepancies are noted, please contact the assembly area.

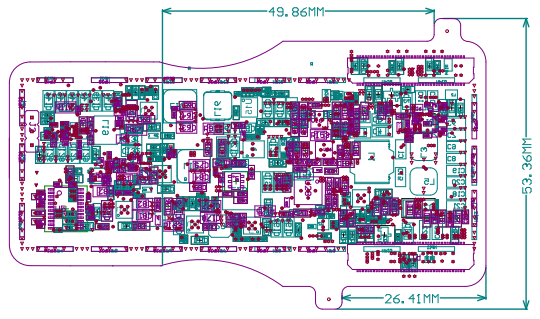
Z22 ■ These assemblies are ESD sensitive. Please observe the ESD precautions.

Z21 ■ Install label in silkscreen location.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer	FR-4	2.76mil		
	Dielectric	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer	FR-4	2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

Tolerance:
For 6 Mil +/- 6 Mil

- NOTES: <UNLESS OTHERWISE SPECIFIED>
- FABRICATE PER IPC-6012A CLASS 2
 - LAMINATE MATERIAL: FR4
 - COPPER WEIGHT: SEE STACKUP
 - BOARD THICKNESS: 1.6MM +/- 10%
 - NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
 - SURFACE FINISH: ENIG
 - SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
 - DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
 - SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
 - SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 - BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
 - SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
 - 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
 - ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
 - LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
 - FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.
 - FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
 - FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
 - BOARD DIMENSION: 90 MM X 53.36 MM.
 - TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE
 - ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
 MIN. CLEARANCE: 4.25 MIL
 MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNUAL RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/- 10% OTHER

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER
 SOLDER RESIST COLOR: GREEN OTHER
 MATTIE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:
Smart Probe Power Supply

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010269.PcbDoc



COMPONENTS MARKED 'DNP' SHOULD NOT BE ASSUMED TO BE PRESENT ON THIS BOARD.
 ASSEMBLY VARIANT: [No Variations]

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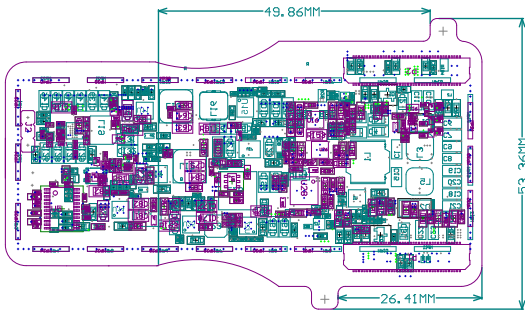
ENGINEER:
Bill. Xu

LAYOUT BY:
Bill. Xu

SCALE: 1.00

ALTIM DESIGNER VERSION:
24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
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7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- FABRICATE PER IPC-6012A CLASS 2
- LAMINATE MATERIAL: FR4
- COPPER WEIGHT: SEE STACKUP
- BOARD THICKNESS: 1.6MM +/- 10%
- NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- SURFACE FINISH: ENIG
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 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

DRILLING:

REFERENCE: AS SHOWN NC_DRILL FILES

PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:

SILKSCREEN: TOP BOTTOM

SILKSCREEN COLOR: WHITE OTHER

SOLDER RESIST COLOR: GREEN OTHER
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

REV: 00	DATE: 08/01/2019	BY: SUN	DESCRIPTION: INTRTB
LAYER NAME = 00	TID #: 00	DATE: 08/01/2019	BY: SUN
PLOT NAME: TID010269.PcbDoc			

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ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.9.1.31

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