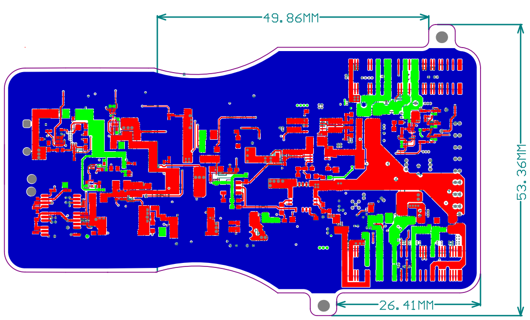
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control	
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269		M6 Assembly Bottom	
PLOT NAME = Top Layer	3:12:35 PM	GENERATED : 9/19/2024	3:12:35 PM	TEXAS INSTRUMENTS	

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

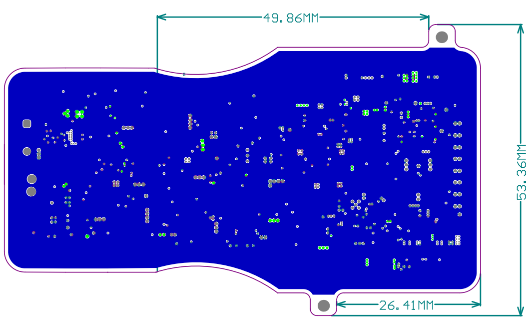
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5,8 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control	
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269			
PLOT NAME =		GENERATED : 9/19/2024 3:12:38 PM		TEXAS INSTRUMENTS	

ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

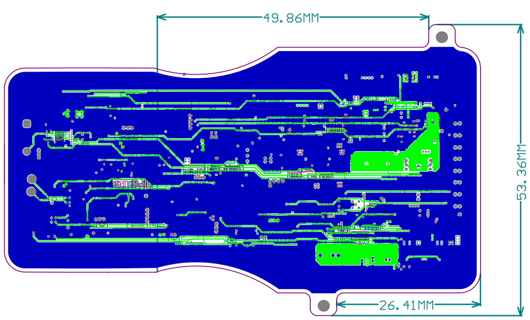
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5,8 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB REV: 00 | BOARD #: TIDA-010269 | REV: 00 | SVN REV: Not in version control
LAYER NAME = M6 Assembly Bottom | TID #: TIDA-010269 | M6 Assembly Bottom
PLOT NAME = Signal 1 | GENERATED : 9/19/2024 3:12:40 PM | TEXAS INSTRUMENTS

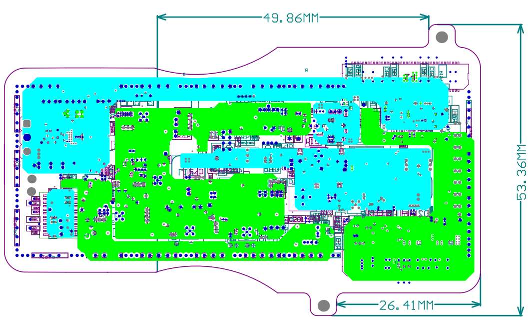
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	REV: Not in version control	
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269	M6 Assembly Bottom		
PLOT NAME = Power1	3:12:44 PM	GENERATED : 9/19/2024	3:12:43 PM	TEXAS INSTRUMENTS	

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

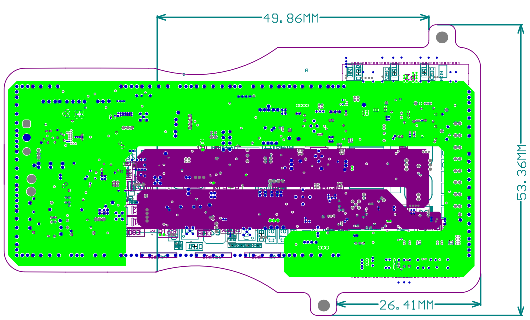
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PROJECT TITLE:	Smart Probe Power Supply
DESIGNED FOR:	Public Release
FILE NAME:	TIDA-010269.PcbDoc
ENGINEER:	Bill. Xu
LAYOUT BY:	Bill.Xu
SCALE:	1.00
ALTIUM DESIGNER VERSION:	24.9.1.31

BOARD #: TIDA-010269 REV: 00

LAYER NAME = M6 Assembly Bottom

TID #: TIDA-010269

GENERATED : 9/19/2024 3:12:48 PM

TEXAS INSTRUMENTS

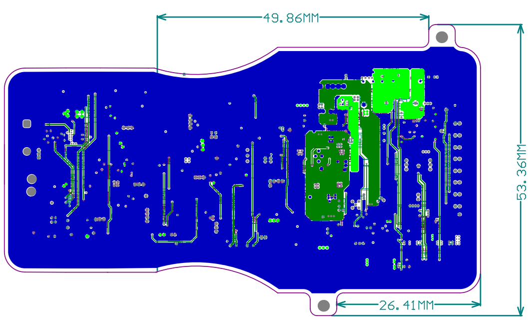
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control	
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269	M6 Assembly Bottom		
PLOT NAME = Signal 2	3:12:52 PM	GENERATED : 9/19/2024	3:12:52 PM	TEXAS INSTRUMENTS	

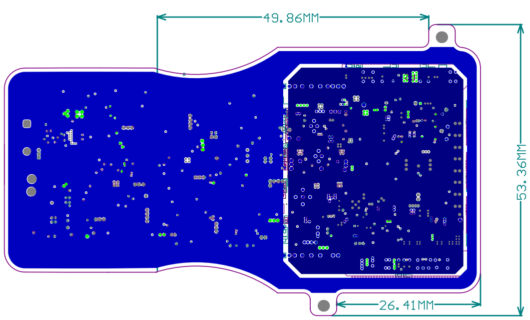
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

	00	BOARD #: TIDA-010269	REV: 00	
LAYER NAME =		TID #: TIDA-010269	M6 Assembly Bottom	
PLOT NAME =		GENERATED : 9/19/2024 3:12:56 PM		TEXAS INSTRUMENTS

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

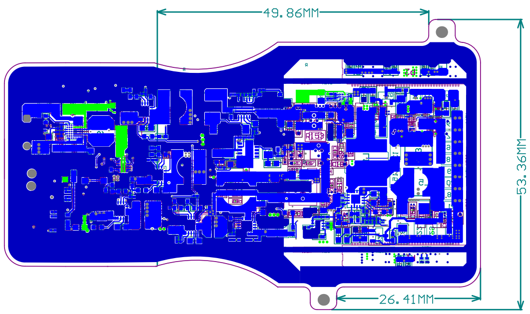
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5,8 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 / [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 / [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER / [X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG / [ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE / [ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269		M6 Assembly Bottom
PLOT NAME = Bottom Layer	3:13:00 PM	GENERATED : 9/19/2024	3:13:00 PM	TEXAS INSTRUMENTS

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

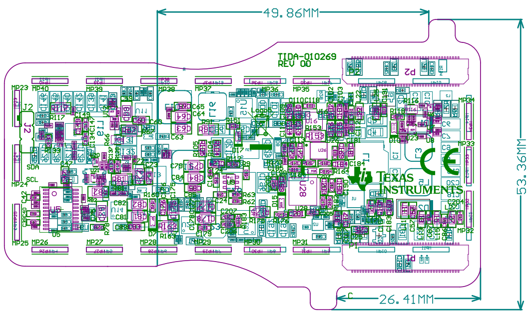
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5,8 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

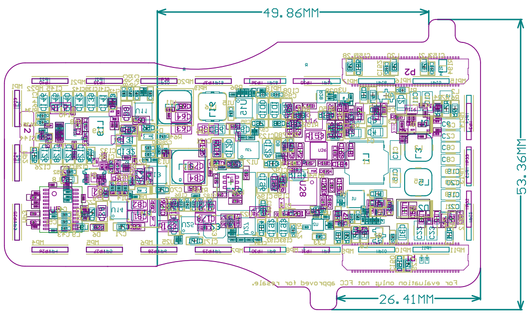
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5,8 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control	
LAYER NAME = M6 Assembly Bottom	TID #: TIDA-010269			
PLOT NAME = Bottom Silkscreen Overlay	GENERATED : 9/19/2024 3:13:09 PM		TEXAS INSTRUMENTS	

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

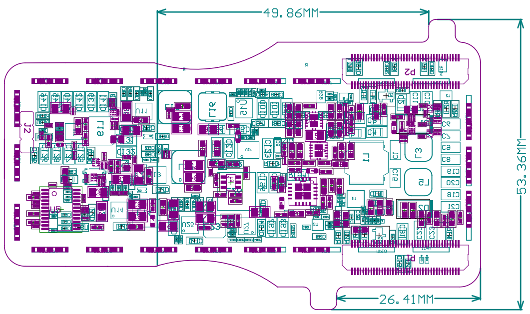
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE | 00 | BOARD #: TIDA-010269 | REV: 00 | SVN REV: Not in version control

LAYER NAME = M6 Assembly Bottom | TID #: TIDA-010269

PLOT NAME = Top Paste Mask Print | GENERATED : 9/19/2024 3:13:12 PM | TEXAS INSTRUMENTS

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

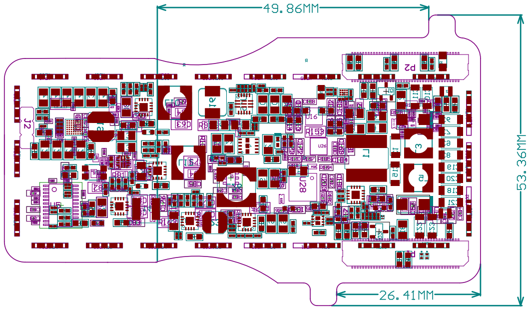
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE | BOARD #: TIDA-010269 | REV: 00 | SVN REV: Not in version control
LAYER NAME = Bottom Paste Mask | TID #: TIDA-010269 | M6 Assembly Bottom
PLOT NAME = Bottom Paste Mask Print | GENERATED : 9/19/2024 3:13:17 PM | TEXAS INSTRUMENTS

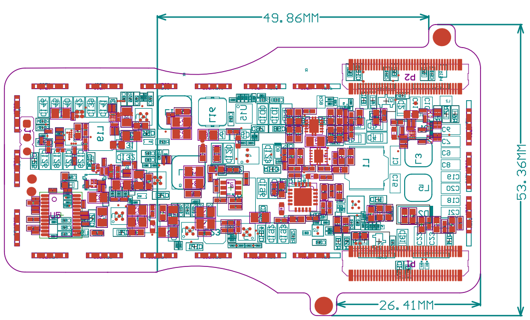
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5,8 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control
LAYER NAME = Top Solder		TID #: TIDA-010269		M6 Assembly Bottom
PLOT NAME = Top Solder Mask Print		GENERATED : 9/19/2024 3:13:20 PM		TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

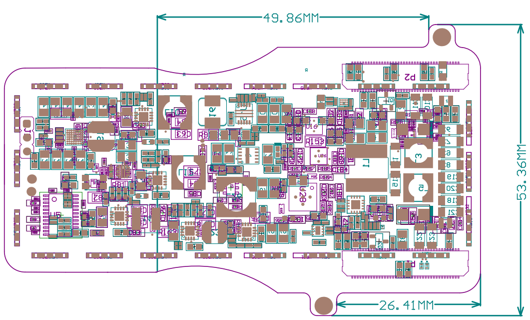
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5,8 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control		
LAYER NAME = Bottom		TID #: TIDA-010269	M6 Assembly Bottom			
PLOT NAME = Bottom Solder Mask Print		GENERATED : 9/19/2024 3:13:25 PM		TEXAS INSTRUMENTS		

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

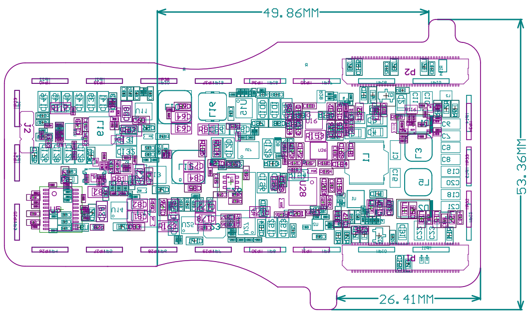
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control	
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269	M6 Assembly Bottom		
PLOT NAME = M2 Board Outline	3:13:28 PM	GENERATED : 9/19/2024	3:13:28 PM	Board Outline	TEXAS INSTRUMENTS

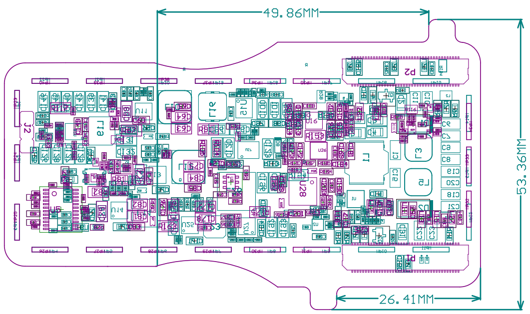
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control	
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269		M6 Assembly Bottom	
PLOT NAME = M2 Board Dimensions		GENERATED : 9/19/2024	3:13:32 PM	TEXAS INSTRUMENTS	

1 2 3 4 5 6

A

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

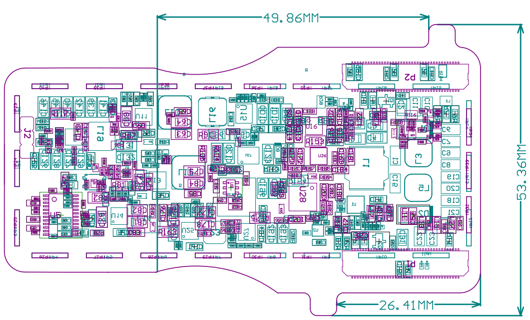
ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

B



C

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

D

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control	
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269	M6 Assembly Bottom		
PLOT NAME = MB STEP Top		GENERATED : 9/19/2024 3:13:35 PM		TEXAS INSTRUMENTS	

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

1 2 3 4 5 6

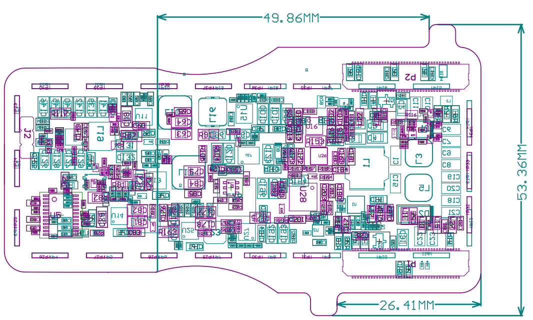
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control
LAYER NAME = M6 Assembly Bottom	TID #: TIDA-010269		
PLOT NAME = 3D STEP Bottom	GENERATED : 9/19/2024 3:13:39 PM		TEXAS INSTRUMENTS

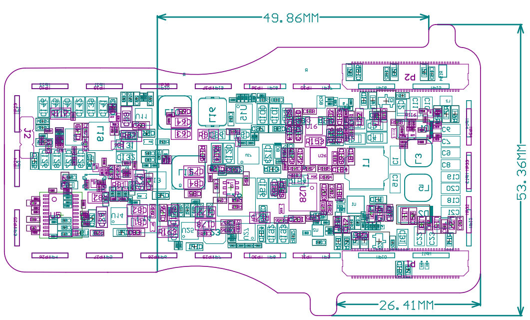
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control
LAYER NAME = M5 Assembly Top		TID #: TIDA-010269		
PLOT NAME = M5 Assembly Top		GENERATED : 9/19/2024 3:13:43 PM		TEXAS INSTRUMENTS

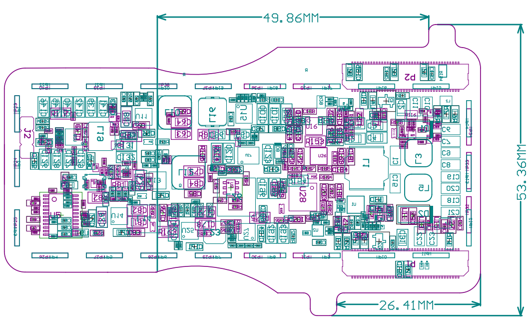
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269		M6 Assembly Bottom
PLOT NAME = M6 Assembly Bottom		GENERATED : 9/19/2024 3:13:47 PM		TEXAS INSTRUMENTS

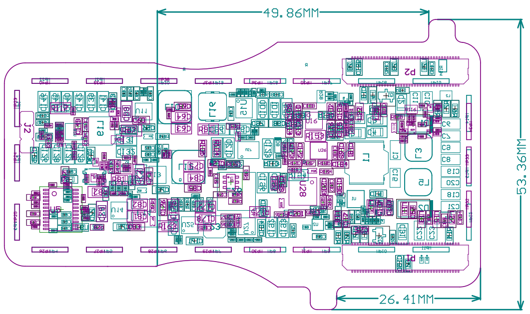
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE | 00 | BOARD #: TIDA-010269 | REV: 00 | SVN REV: Not in version control
LAYER NAME = M6 Assembly Bottom | TID #: TIDA-010269
PLOT NAME = M9 Title Sheet | GENERATED : 9/19/2024 3:13:50 PM | TEXAS INSTRUMENTS

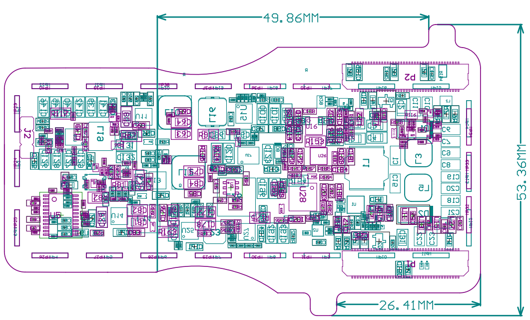
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5,8 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE 00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control
LAYER NAME = M5 Assembly Top	TID #: TIDA-010269	M6 Assembly Bottom	
PLOT NAME = M20 Fab Notes 3:13:53 PM	GENERATED : 9/19/2024 3:13:53 PM	Notes	TEXAS INSTRUMENTS

ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

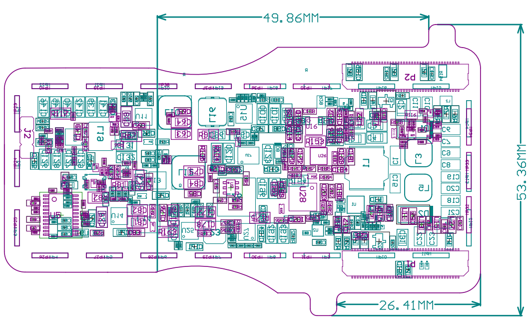
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5,8 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB NETWORK FOR FAB	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control	
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269		M6 Assembly Bottom	
PLOT NAME = Gerber Information		GENERATED : 9/19/2024 3:13:56 PM		TEXAS INSTRUMENTS	

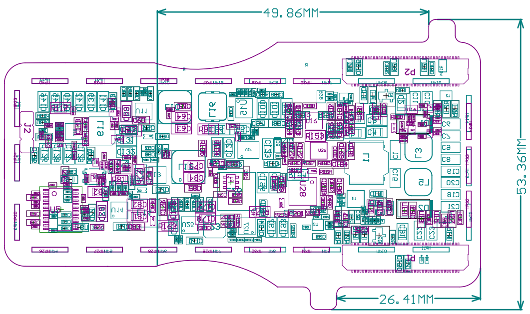
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER ____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- ____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- ____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER ____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER ____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER ____
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER ____

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc

1000.00mil

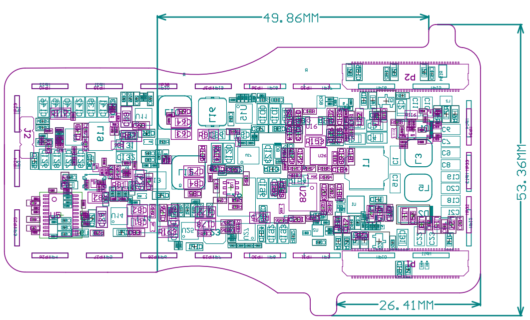
COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]
COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269	M6 Assembly Bottom	
PLOT NAME = M22 Stackup		GENERATED : 9/19/2024 3:13:59 PM		TEXAS INSTRUMENTS

ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.9.1.31

- ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.
- ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
- ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB NUMBER: TIDA-010269	00	BOARD #: TIDA-010269 REV: 00	SVN REV: Not in version control
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269	M6 Assembly Bottom
PLOT NAME = M23 Component Bodies Top		GENERATED : 9/19/2024 3:14:02 PM	TEXAS INSTRUMENTS

ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

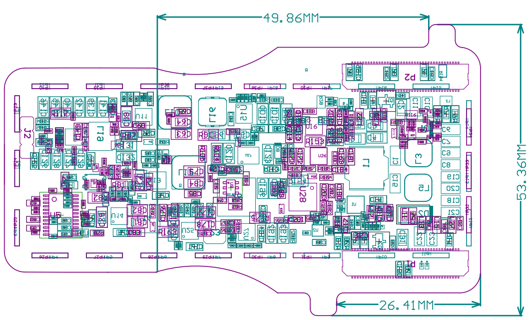
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB NUMBER: TIDA-010269 | REV: 00
LAYER NAME = M6 Assembly Bottom
PLOT NAME = Component Bodies Bottom | GENERATED : 9/19/2024 3:14:05 PM | TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

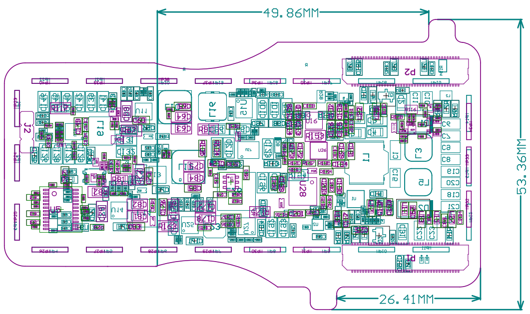
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB NUMBER: 00 | BOARD #: TIDA-010269 | REV: 00 | SVN Rev: Not in version control
LAYER NAME = M6 Assembly Bottom | TID #: TIDA-010269
PLOT NAME = M25 Courtyards Top | GENERATED : 9/19/2024 3:14:08 PM | TEXAS INSTRUMENTS

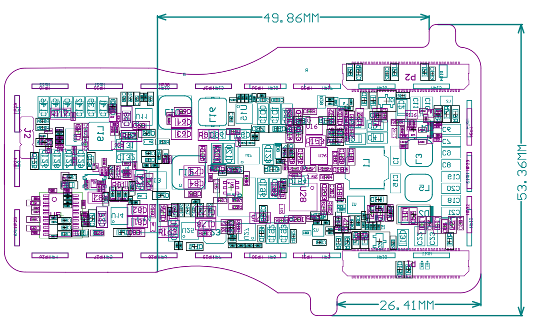
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5,8 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE | 00 | BOARD #: TIDA-010269 | REV: 00 | SVN REV: Not in version control

LAYER NAME = M6 Assembly Bottom | TID #: TIDA-010269

PLOT NAME = M26 Courtyards Bottom | GENERATED : 9/19/2024 3:14:11 PM | TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

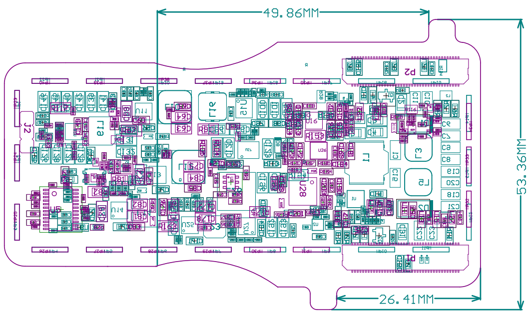
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control	
LAYER NAME = M5 Assembly Top		TID #: TIDA-010269	M6 Assembly Bottom		
PLOT NAME = Embedded Cavity		GENERATED : 9/19/2024 3:14:14 PM		TEXAS INSTRUMENTS	

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

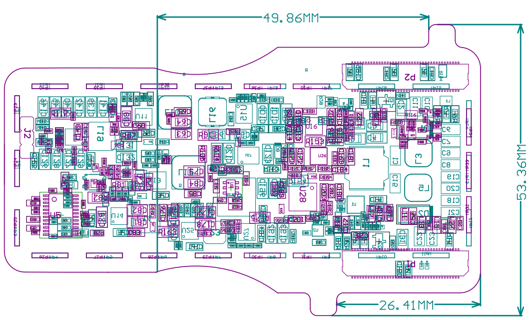
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control	
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269			
PLOT NAME = Embedded Assembly		GENERATED : 9/19/2024 3:14:17 PM		TEXAS INSTRUMENTS	

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

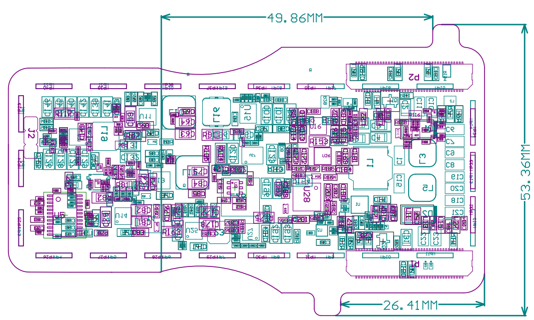
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB REV:	00	BOARD #: TIDA-010269	REV: 00	SVN REV: Not in version control	
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269		M6 Assembly Bottom	
PLOT NAME = Embedded Keepout		GENERATED : 9/19/2024 3:14:20 PM		TEXAS INSTRUMENTS	

ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

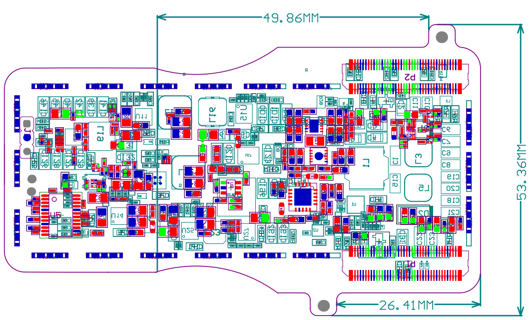
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00
SVN REV: Not in version control			
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269	
PLOT NAME = Top Pad Master		GENERATED : 9/19/2024 3:14:23 PM	TEXAS INSTRUMENTS

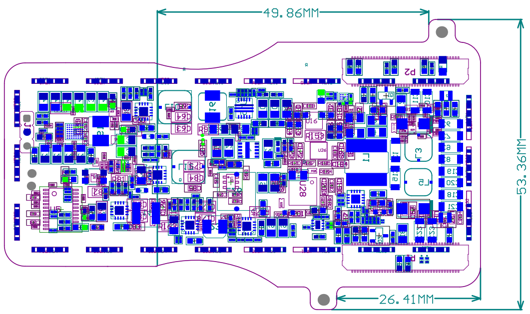
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE | 00 | BOARD #: TIDA-010269 | REV: 00 | SVN REV: Not in version control

LAYER NAME = M6 Assembly Bottom | TID #: TIDA-010269 | M6 Assembly Bottom

PLOT NAME = Bottom Pad Master | GENERATED : 9/19/2024 3:14:27 PM | TEXAS INSTRUMENTS

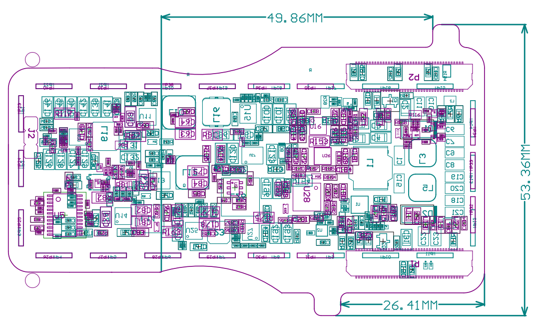
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5,8 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

ENGINEER: Bill. Xu

LAYOUT BY: Bill.Xu

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.9.1.31

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	00	BOARD #: TIDA-010269	REV: 00	REV: Not in version control
LAYER NAME = M6 Assembly Bottom		TID #: TIDA-010269		
PLOT NAME = Keep Out Layer		GENERATED : 9/19/2024 3:14:30 PM		TEXAS INSTRUMENTS

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair
⊕	8	5.91mil (0.150mm)	PTH	Round	Top Layer - Bottom Layer
◎	298	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer
◇	1	8.27mil (0.210mm)	PTH	Round	Top Layer - Bottom Layer
⌘	37	8.66mil (0.220mm)	PTH	Round	Top Layer - Bottom Layer
✡	336	9.84mil (0.250mm)	PTH	Round	Top Layer - Bottom Layer
▽	288	11.81mil (0.300mm)	PTH	Round	Top Layer - Bottom Layer
□	1	19.69mil (0.500mm)	PTH	Round	Top Layer - Bottom Layer
▼	2	31.50mil (0.800mm)	PTH	Round	Top Layer - Bottom Layer
▣	3	35.43mil (0.900mm)	PTH	Round	Top Layer - Bottom Layer
○	2	120.00mil (3.048mm)	NPTH	Round	Top Layer - Bottom Layer
	976 Total				

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

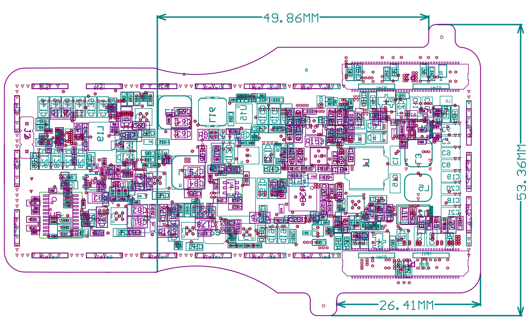
ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

Tolerance:
For 6 Mil +0/-6 Mil



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TRACES TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

FAB REV: 00
TID #: TIDA-010269
M6 Assembly Bottom
Fab Drawing For Top Layer
TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

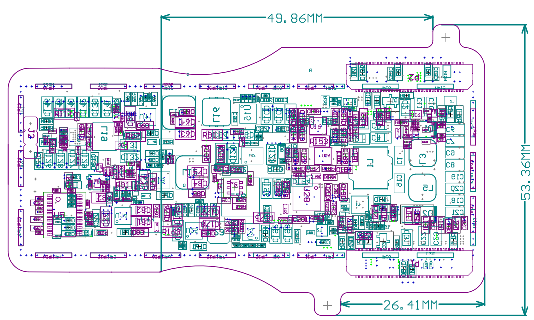
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5,8 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007) PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMASINLIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.75 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER FR-4
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

BOARD #: TIDA-010269 REV: 00
Not in version control
LAYER NAME = M6 Assembly Bottom
TID #: TIDA-010269
PLOT NAME = TIDA-010269 Guide For (Top Layer)
GENERATED: 9/19/2024 3:14:38 PM
TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply
DESIGNED FOR: Public Release
FILE NAME: TIDA-010269.PcbDoc
ENGINEER: Bill. Xu
LAYOUT BY: Bill.Xu
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.9.1.31

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