DLPC1438/DLPA2005 REFERENCE DESIGN

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ENGR	K. Lowderman		2021-06-28
SYS	Eric Pruett		2021-06-28
APVD	----		----
QA	----		----

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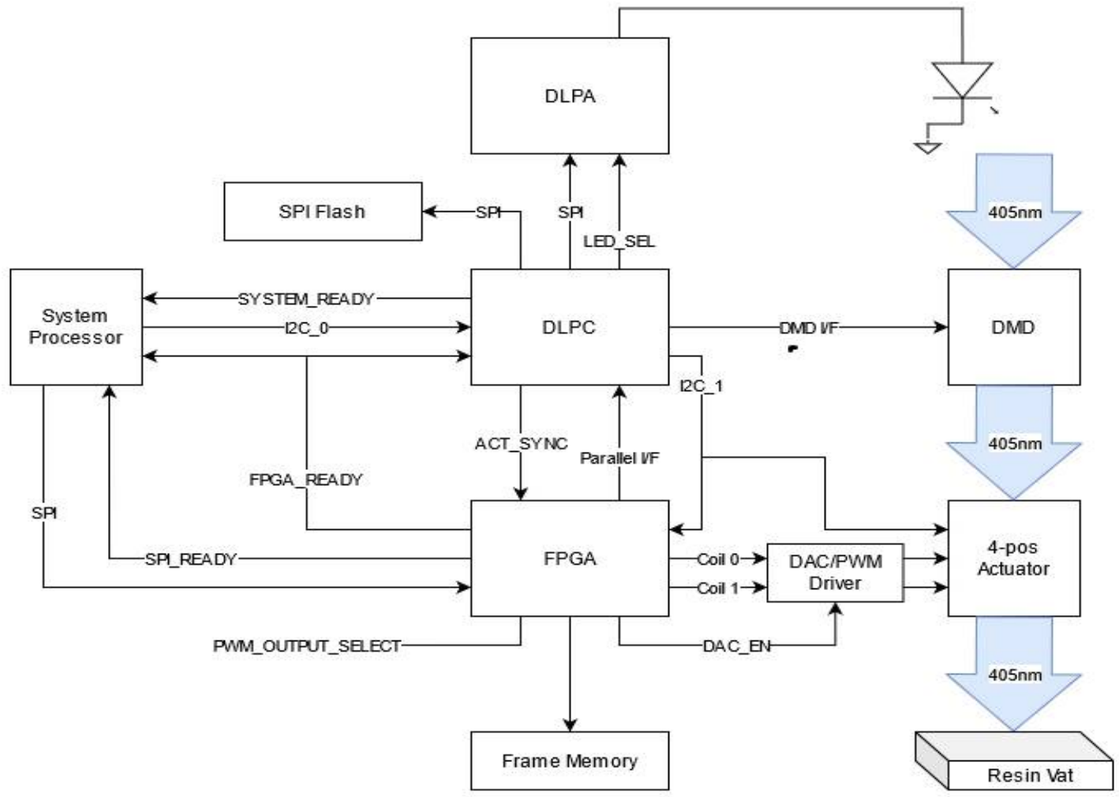

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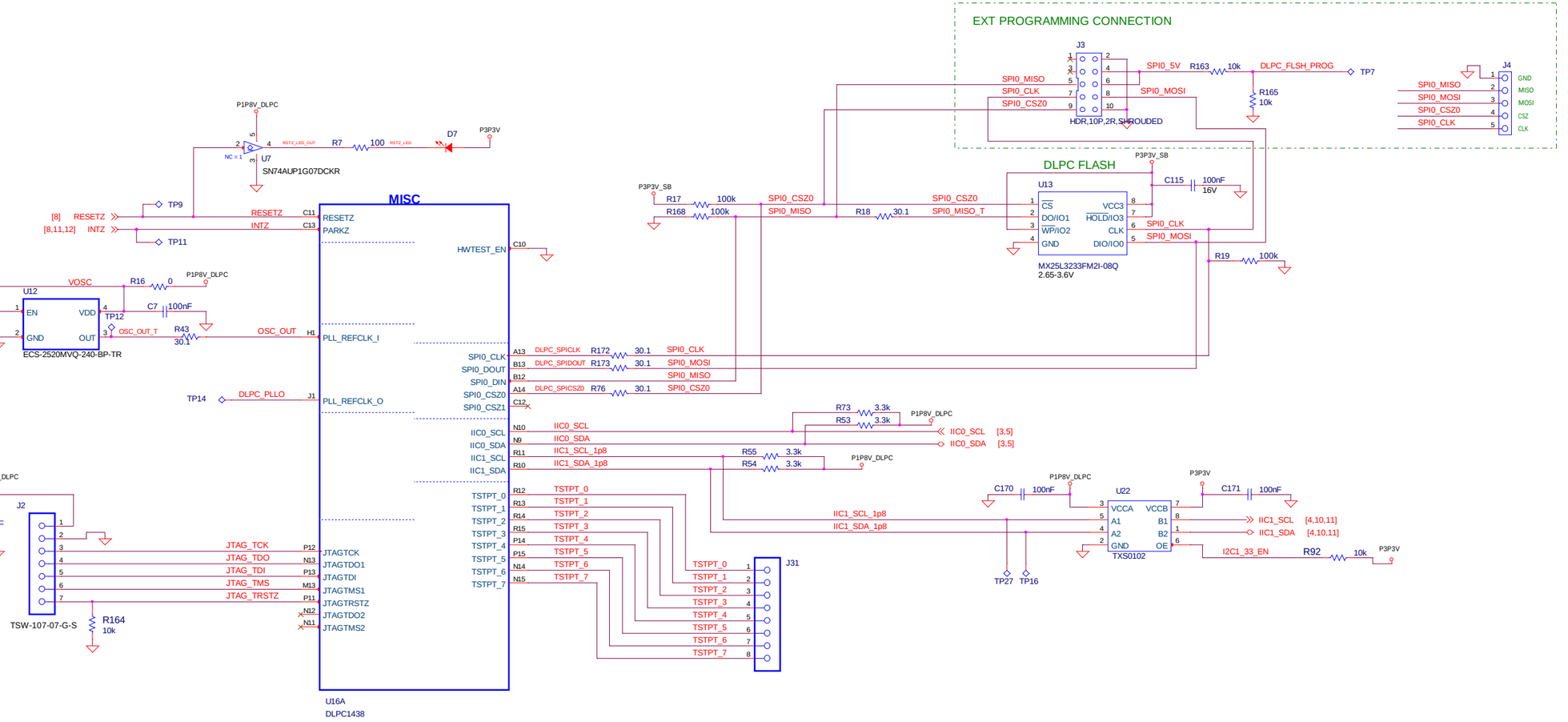

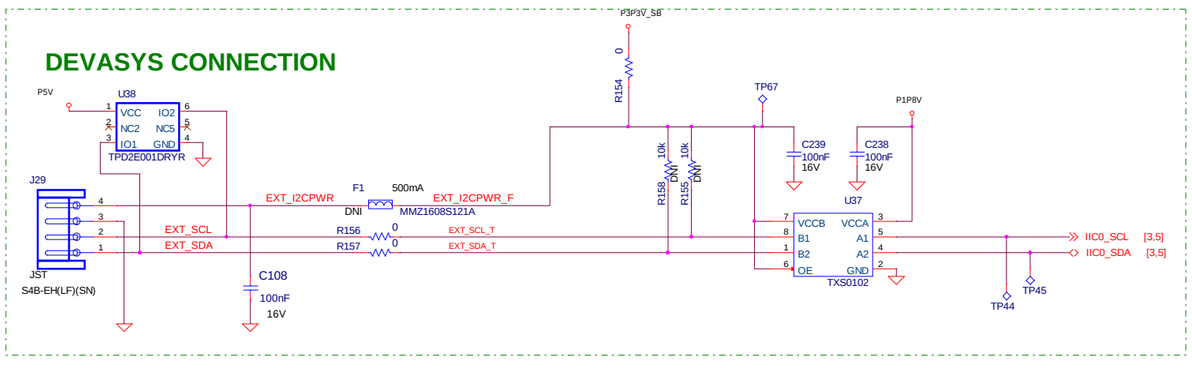

DLPC1438 Clock, Reset, SPI and Flash Memory

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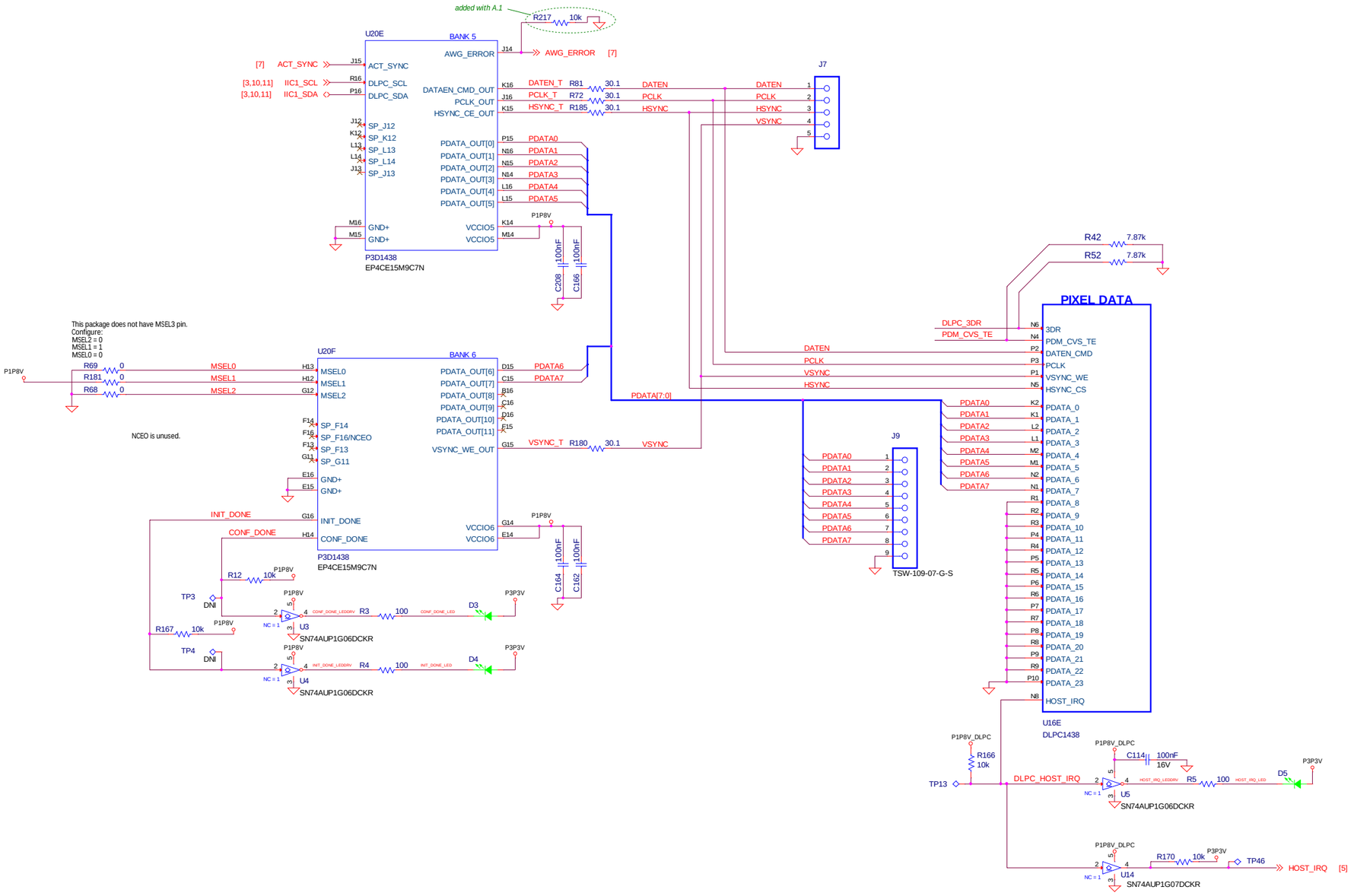

Parallel Port In

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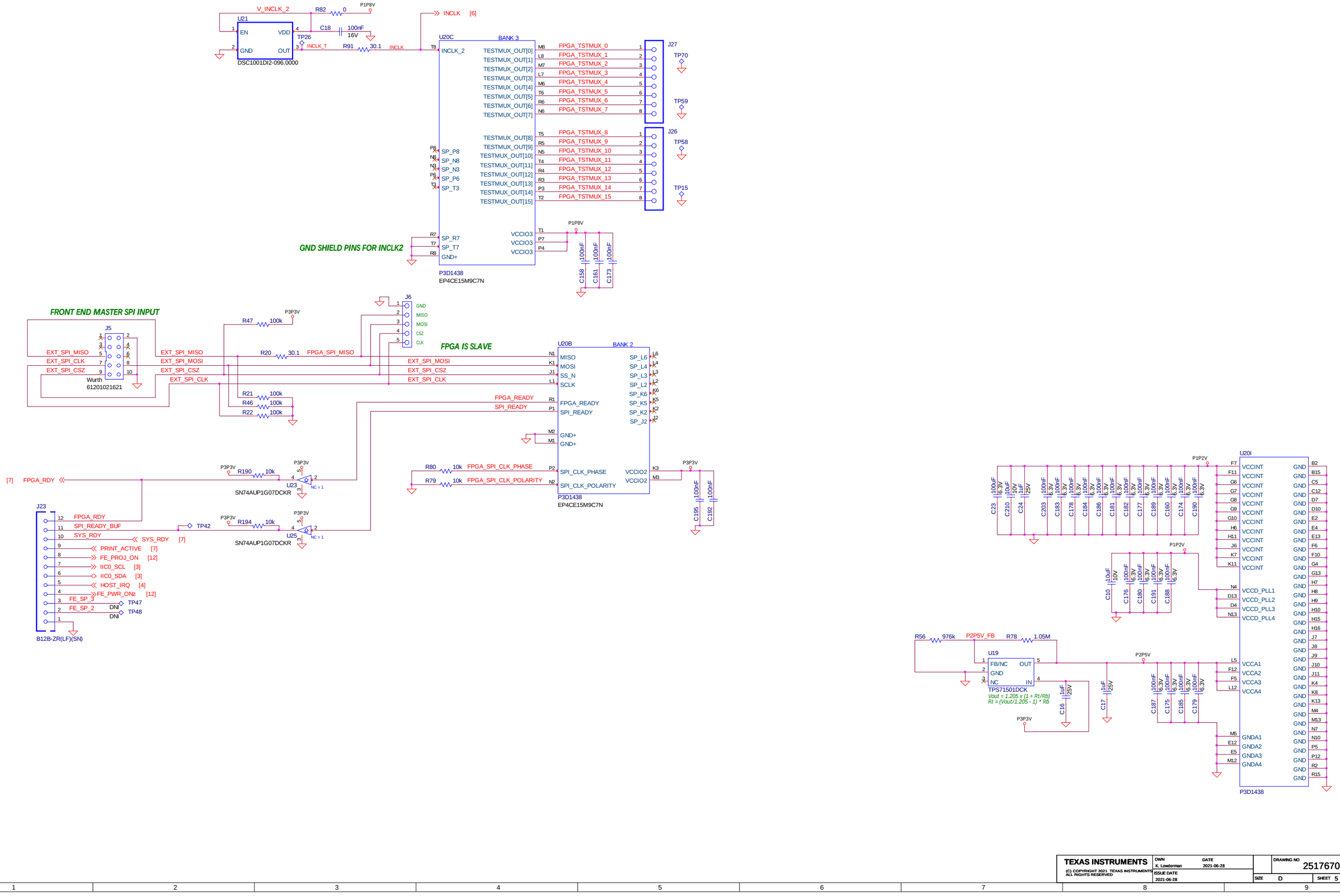

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U20H BANK 8

P3D1438
EP4CE15M9C7N

U15

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
MEM_DQ0 MEM_DQ1 MEM_DQ2 MEM_DQ3 MEM_DQ4 MEM_DQ5 MEM_DQ6 MEM_DQ7

AS4C64M8D2-25BIN
512M,64x8x4banks

MEM_DQ[7:0]

GND SHIELD PINS FOR INCLK1

U20G BANK 7

P3D1438
EP4CE15M9C7N

GND SHIELD PINS FOR INCLK1

ADDR & COMMAND GROUP

Place terminations close to memory at end of net.

DATA

Place terminations close to FPGA at end of net.

1.8V TO 0.9V DDR_VTT & DDR_VREF

U9
TPS51200DRCR

DDR TERMINATION VOLTAGE

TOTAL CAPACITANCE ON DDR_VREF CANNOT EXCEED 470nF.

FPGA FLASH

U18
MX25L3233FM2I-08Q
2.65-3.6V

U20A BANK 1

P3D1438
EP4CE15M9C7N

PLACE ODD SIDE ON BOARD EDGE

J1
Wurth
61201021621

EXT PROGRAMMING CONNECTION

J11
HDR,10P,2R,SHROUDED

J12
GND MISO MOSI CSZ CLK

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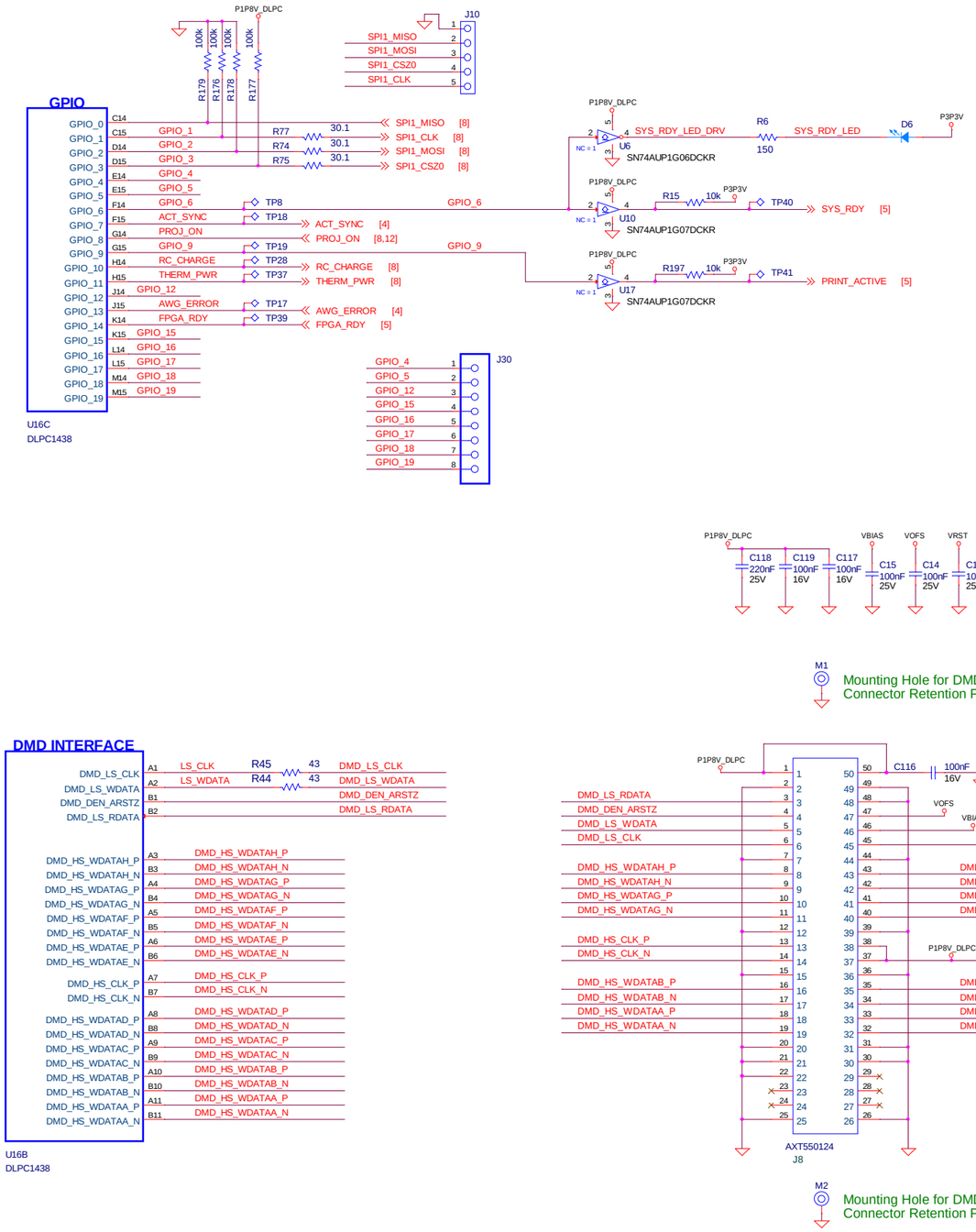
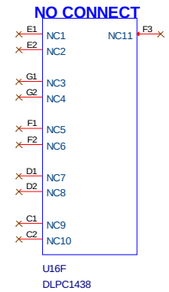
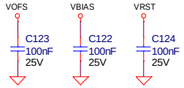


M1
Mounting Hole for DMD
Connector Retention Plate

The DSI Port is not supported by the DLPC1438. Inputs are left unconnected per datasheet recommendation.





M2
Mounting Hole for DMD
Connector Retention Plate

DMD INTERFACE

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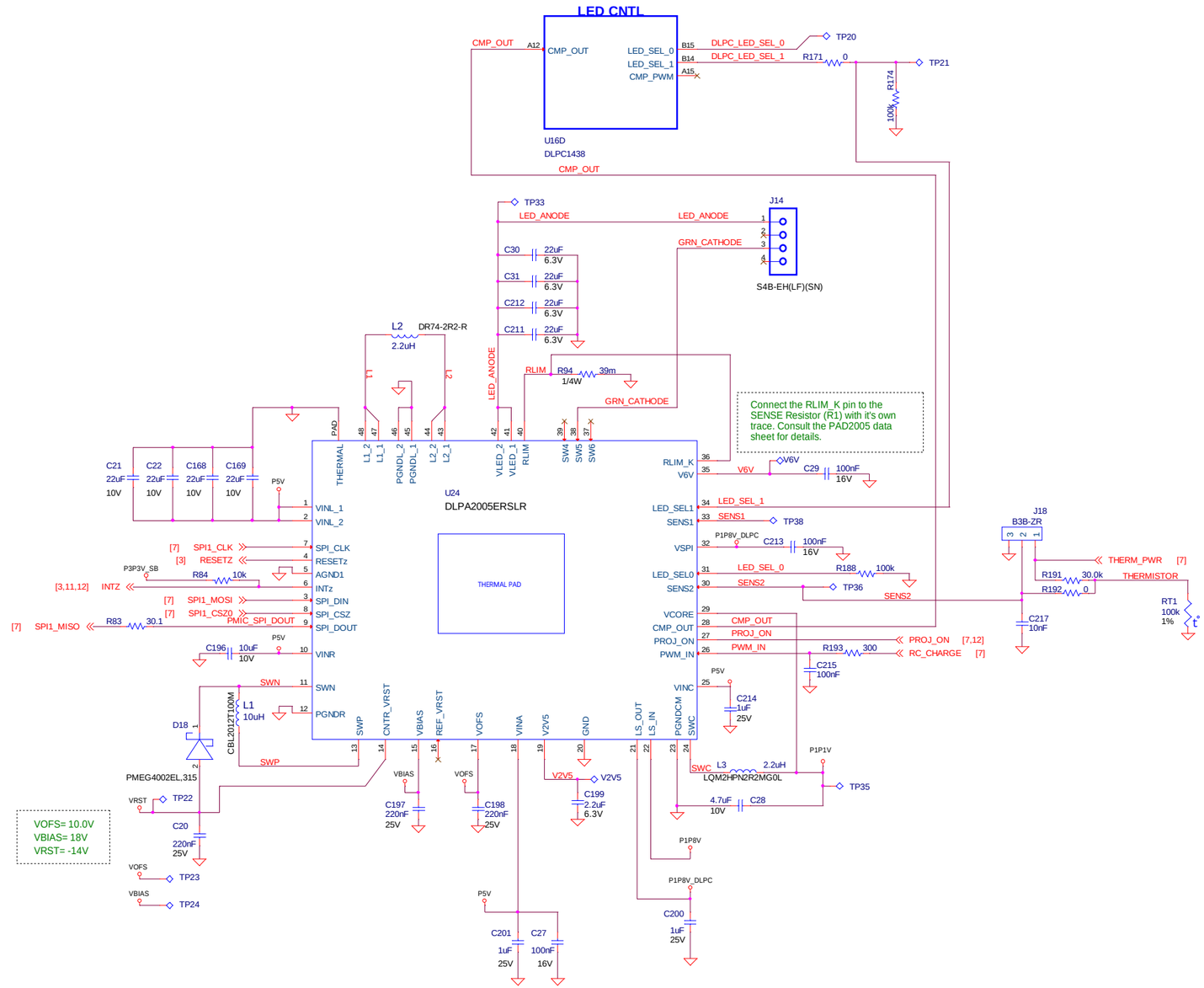

DLPA3000/DLPA3005 INTERFACE

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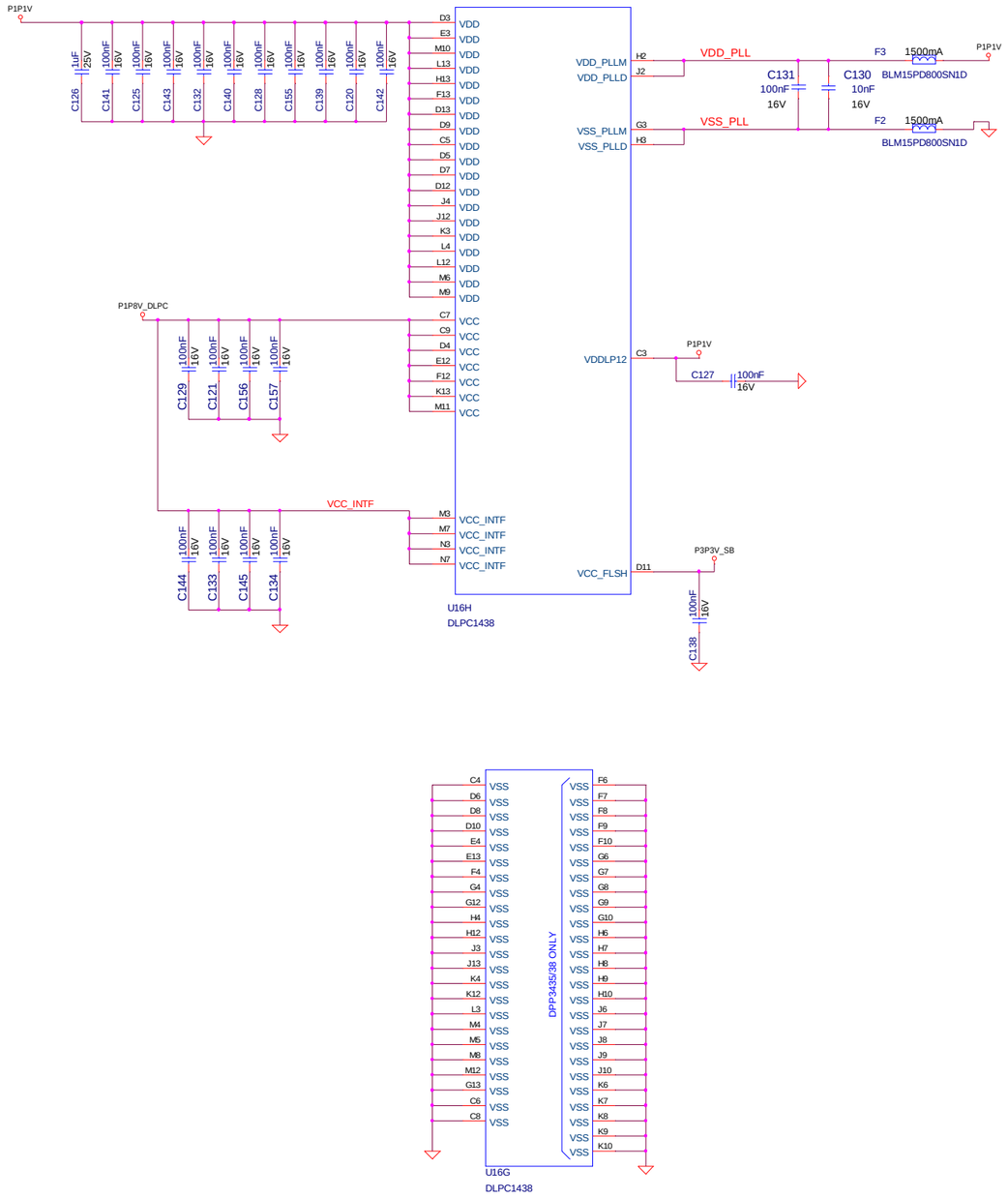

POWER - DLPC3436

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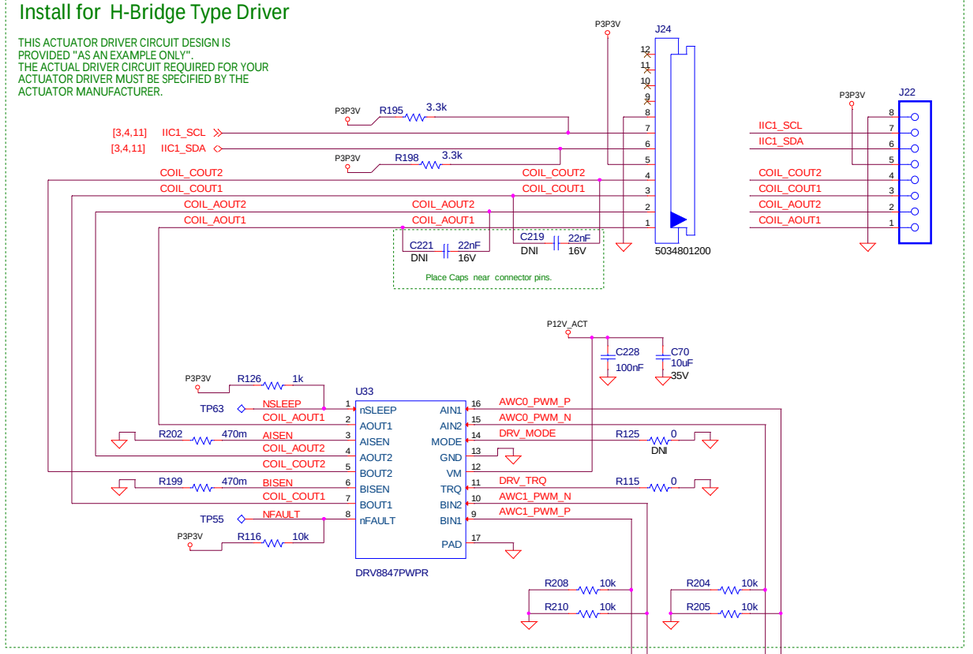
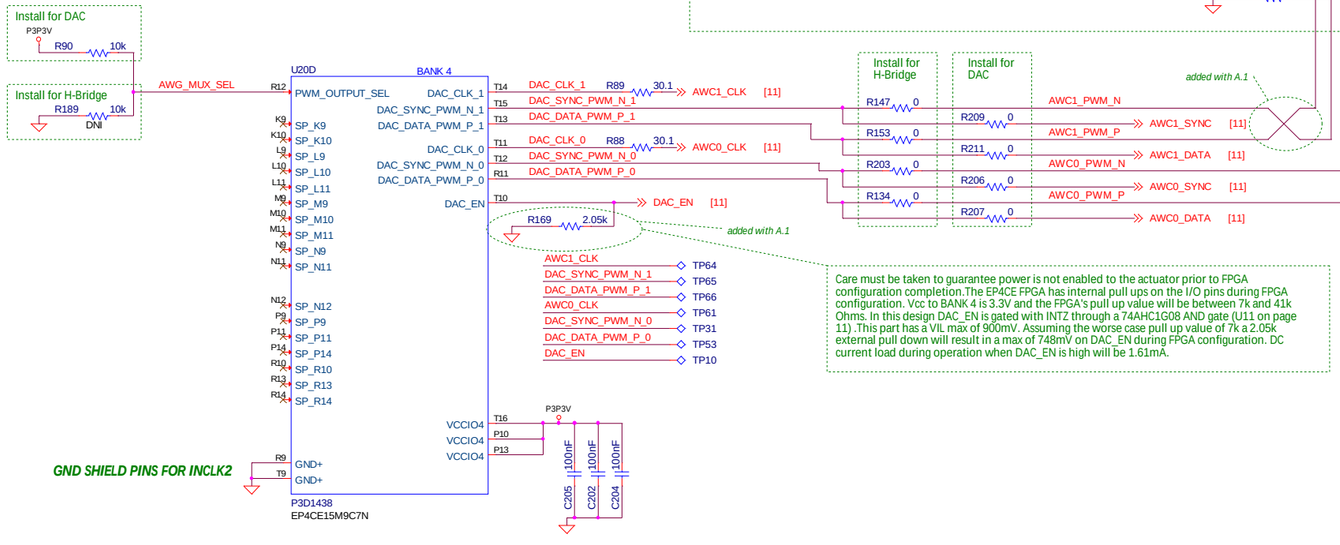
Install for H-Bridge Type Driver

THIS ACTUATOR DRIVER CIRCUIT DESIGN IS PROVIDED "AS AN EXAMPLE ONLY". THE ACTUAL DRIVER CIRCUIT REQUIRED FOR YOUR ACTUATOR DRIVER MUST BE SPECIFIED BY THE ACTUATOR MANUFACTURER.





Care must be taken to guarantee power is not enabled to the actuator prior to FPGA configuration completion.The EP4CE FPGA has internal pull ups on the I/O pins during FPGA configuration. Vcc to BANK 4 is 3.3V and the FPGA's pull up value will be between 7k and 41k Ohms. In this design DAC_EN is gated with INTZ through a 74AHC1G08 AND gate (U11 on page 11) .This part has a VIL max of 900mV. Assuming the worse case pull up value of 7k a 2.05k external pull down will result in a max of 748mV on DAC_EN during FPGA configuration. DC current load during operation when DAC_EN is high will be 1.61mA.

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Install for DAC Type Driver

THIS ACTUATOR DRIVER CIRCUIT DESIGN IS PROVIDED "AS AN EXAMPLE ONLY". THE ACTUAL DRIVER CIRCUIT REQUIRED FOR YOUR ACTUATOR DRIVER MUST BE SPECIFIED BY THE ACTUATOR MANUFACTURER.

P3P3V
P3P3V_DAC
L11 BLM15PX121SN1D
C94 100nF
C93 100nF
C101 100nF
U35 DAC081S101CIMK/NOPB
[10] AWC1_DATA
[10] AWC1_SYNC
[10] AWC1_CLK
AWC1_DAC_VOUT
TP62
R144 33k
R146 10k
R145 10k
AWC1_DAC_OUTPUT
C95 100nF
U34 DAC081S101CIMK/NOPB
[10] AWC0_DATA
[10] AWC0_SYNC
[10] AWC0_CLK
AWC0_DAC_VOUT
TP57
R131 33k
R133 10k
R132 10k
AWC0_DAC_OUTPUT
L9 BLM15PX121SN1D
0.38V_REF_IN
C89 100nF
C90 100nF
R129 76.8k
0.38V_REF
R130 10k
C91 100nF

P12V_ACT
C230 100nF
C69 1uF
U32 TCA0372DWR2G
COIL_C_2OUT1
C80 1nF
R122 9.88k 0.1%
R120 100
R121 0
COIL_C_2OUT
C234 100nF
C229 1uF
COIL_C_P
C81 1nF
COIL_C
R123 1k
COIL_C_N
R124 910m
0.38V_REF
TP60

P12V_ACT
C223 100nF
C52 1uF
U30 TCA0372DWR2G
COIL_A_2OUT1
C62 1nF
R114 9.88k 0.1%
R113 100
R105 0
COIL_A_2OUT
C225 100nF
C224 1uF
C63 1nF
COIL_A
R106 1k
COIL_A_N
R107 910m
0.38V_REF
TP54

COIL_C_P
COIL_C_N
COIL_A_P
COIL_A_N
[3,4,10] IIC1_SCL
[3,4,10] IIC1_SDA
C222 22nF DNI 16V
C220 22nF DNI 16V
Place Caps near connector pins.
J19 5034801200
J21
IIC1_SCL
IIC1_SDA
COIL_C_P
COIL_C_N
COIL_A_P
COIL_A_N

12V/3.0A Output

VIN_ACT
C104 4.7uF
C103 4.7uF
C105 100nF
U36
P12V_BOOT
P12V_EN
P12V_RT
floating EN = ENABLE
TP69
TPS54340
P12V_SW
L10 5.6uH SRP5030T-5R6M
D14 B560C-13-F
P12V_ACT
TP43
P12V_COMP
R150 56.2k
C106 6.8pF
C107 680pF
P12V_RC_1
R159 93.1k
R152 147k
R151 10.5k
C92 22uF
C100 22uF
P12V_FB

VIN
D
Q6 NDT456P
D2
D1
R140 10k
VIN_QG
R141 10k
C99 10uF 50V
VIN_ACT
C98 22uF 35V
C235 22uF 35V
C236 22uF 35V
C97 22uF 35V

P3P3V
U11 74AHC1G08
[3,8,12] INTZ
[10] DAC_EN
VIN_ACT_EN
R142 10k
DRV_EN_G
Q5 RK7002BMT116
DRV_EN_D
R143 10k

P3P3V
U8 SN74AUP1G06DCKR
NC = 1
DAC_EN_DRV
R8 200
DAC_EN_LED
D8 Green

Install for DAC Type Driver

N12V_VIN
C85 4.7uF
C102 220nF
C88 2.2uF
C87 100nF
C84 1uF
Q2 CSD18543Q3A
N12_HG
L8 5.6uH XAL7030-562MEB
D11 VS-50WQ10FNTRL-M3
N12_BOOT
C77 100nF
N12_SW
C66 820pF
N12_CS1
R111 3
N12_CS
N12V_CSG
R118 11m
N12_OUT
N12_FB
U31 LM25088MHX-2/NOPB
TP56
floating EN = ENABLE
N12_EN
N12_RES
N12_VCC
N12_RAMP
N12_RT
N12_SS
C68 22nF
C86 220nF
R128 223k
C78 240pF
R119 10k
C79 33nF
N12_COMP
C226 75pF
N12_RC1
C227 1100pF
R200 19.6k
R201 14.7k
R112 1.65k
C76 22uF 35V
C75 22uF 35V
C231 22uF 35V
C232 2.2uF
N12V_CSG

-12V/3.0A Output

FB1 10A 35F0121-1SR-10
N12V
TP50
C233 22nF
C60 22nF
C67 100uF

ANALOG BIPOLAR ACTUATOR DRIVER

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14V - 20V OPERATING VOLTAGE.

JPWR1
HDR,6P,2R
Molex 0039301060
Mate: Molex 0039012060

JPWR2
CUI Stack PJ-082BH

ALTERNATE POWER CONNECTOR.
20V - 10A LIMIT.
shield pins
pin 2 - sleeve
shield pins
jack insert direction

EXT_VIN
R149 100k
R139 100k
EXT_VIN_TRIP
R148 5.76k
D16 LMV431
D15 BZX84C8V2LT1G
Vref = 1.24V
Trip when EXT_VIN > 22.775V.

Q1 IPD50P04P4L11ATMA1
D13 BZX84C8V2LT1G
EXT_VIN_SW_G
R127 100k
R137 20k
R138 15k EXT_VIN_CNTL_D
J25 B2B-EH-A(LF)(SN)
EXT_VIN_CNTL_G
Q3 ZVN4106FTA
Q3 was specifically selected to have a high gate threshold (>1.3V). Do not make substitution without taking this into account..
Q4 CSD13383F4
SW1 GT12MSCBE
C237 100nF
POWER ON SWITCH
R136 1k
[5] FE_PWR_ONz
R135 30.1 PWR_ONz

VIN
R117 3.3k VIN_LED D12 Green
C96 100uF 35V
C83 100uF 35V
C82 100uF 35V
C74 10uF 35V
C72 10uF 35V
C73 10uF 35V
C71 10uF 35V

C26 100nF 16V
U26
3.5A Out
P5V_BOOT
P5V_EN
P5V_RT
P5V_SW
P5V_COMP
P5V_COMP2
P5V_FB
TPS54340
Vout = 0.8 x (1 + Rt/Rb)
4.5V<= VIN <=42V
Float EN pin to enable.
C25 4.7uF 25V
C19 4.7uF 25V
TP32
R93 78.7k
R95 22.1k
C41 12pF
C51 100pF
L6 XAL5030-472MEB 4.7uH
MBRB4030T4G
D10
R100 53.6k
R99 10.2k
5V FOR FAN IF NEEDED
J16 B2B-EH-A(LF)(SN)
J13
P5V
R96 270 P5V_LED
D9
C42 47uF
C216 22uF 10V
C218 22uF 10V

PROJ_ON can be driven from Front End card, External Source or on board Switch.

C111 100nF DNI
R160 10k FE_PROJ_ON1
[5] FE_PROJ_ON
R161 0
J28 B3B-EH-A(LF)(SN)
R215 10k EXT_PROJ_ON
C240 100nF DNI SW_PROJ_ON
U41 74AHC1G32
U40 74AHC1G32
PROJ_ON
PROJ_ON_2
R214 10k SW_PROJ_ON_PD
SW2
SW_PROJ_ON_PU
R216 10k
TP68 To PMIC card. PROJ_ON [7,8]
U42 SN74AUP1G06DCKR
PROJ_ON_DRV
R162 200 PROJ_ON_LED
D17 Green
NC = 1
U43 74AHC1G08
TP71 FPGA_PWREN
[3,8,11] INTZ

C32 22uF 10V
C34 22uF 10V
C35 22uF 10V
C33 22uF 10V
C36 100nF 16V
U27
1A MAX Output
C43 4.7uF 50V
C44 220nF 35V
FPGA_PWREN
P1P2V_PG
TP49
R101 10k
LMR33610BDDAR
Vout = 1.0 x (1 + Rt/Rb)
max VIN = 36V
min VIN = 3.8V
L4 3.5uH
P1P2V_SW
P1P2V_BOOT
C45 100nF 16V
C46 1uF 25V
P1P2V_VCC
P1P2V_FB
C59 4.7uF 50V
R103 100k
R102 499k
P1P2V_OUT
J17
P1P2V
TP29

C37 22uF 10V
C38 22uF 10V
C39 22uF 10V
C40 100nF 16V
U28
1A MAX Output
C47 4.7uF 50V
C48 220nF 35V
R196 10k P1P8V_EN
P1P8V_PG
TP51
R97 10k
LMR33610BDDAR
Vout = 1.0 x (1 + Rt/Rb)
max VIN = 36V
min VIN = 3.8V
L5 3.5uH
P1P8_SW
P1P8_BOOT
C49 100nF 16V
C50 1uF 25V
P1P8_VCC
P1P8_FB
C61 10nF 50V
R104 100k
R98 124k
P1P8_OUT
J15
P1P8V
TP30

C54 10uF 35V
C53 10uF 35V
C55 100nF 16V
U29
1A MAX Output
C56 4.7uF 50V
C57 220nF 35V
P3P3V_PG
TP52
R108 10k
LMR33610BDDAR
Vout = 1.0 x (1 + Rt/Rb)
max VIN = 36V
min VIN = 3.8V
L7 5.2uH
P3P3V_SW
P3P3V_BOOT
C58 100nF 16V
C65 1uF 25V
P3P3V_VCC
P3P3V_FB
C64 18nF 50V
R110 100k
R109 43.2K
P3P3V_OUT
J20
P3P3V
TP34

P5V
C110 4.7uF 10V
U39
600mA MAX Output
STBY_P3P3V_SW
L12 2.2uH
STBY_P3P3V_FB
TPS62260DDCT
Vout = 0.6 x (1 + Rt/Rb)
max VIN = 6V
R212 78.7k
R213 360k
C109 10uF 6.3V

TPGND2 TPGND3 TPGND4 TPGND5 TPGND1 TPGND7 TPGND8 TPGND9

POWER INPUT & GENERATION

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Revisions

Revisions:

A.0 - Initial release

A.1 - Added R217 (10k) to pull down AWG_ERROR. (page 4)

- Swapped signals going to U33 (page 10) pins 9 and 10 (BIN1 and BIN2). AWC1_PWM_N now connects to AIN2 and AWC1_PWM_P connects to AIN1. R208 is now connected to AWC1_PWM_P and R210 is connected to AWC1_PWM_N.
- Changed R169 (page 10) to 2.05k. This is to assure DAC_EN does not exceed 900mV (VIL of U11 page 11) during FPGA configuration at power up.

REVISION NOTES

DWN	DATE		DRAWING NO	REV
K. Lowderman	2021-06-28		2517670	A.1
ISSUE DATE		SIZE D	SHEET 14 OF 14	
2021-06-28				

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