Schematics Drafted in : Allegro Design entry CIS 17.2

REV	Revision Notes	Designer	Approver	Date
A1	First release	VVDN	TI	12-09-2019
A2	Replaced the option to enable the internal RTC of processor by TPS65218_GPIO3, with PGOOD_BU.	VVDN	TI	16-09-2019
B1	Second release	VVDN	TI	14-11-2019
B2	1) Value of R831 changed to 0E 2) Value of R68 changed to 2.2K	VVDN	TI	23-12-2019

TIXU_MX8M

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03	PMIC LP8733 AND RTC
04	PMIC TPS65218D0
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TIXU MX8M

TIDA-050038

VVDN TECHNOLOGIES

A3 | Title : COVER_PAGE

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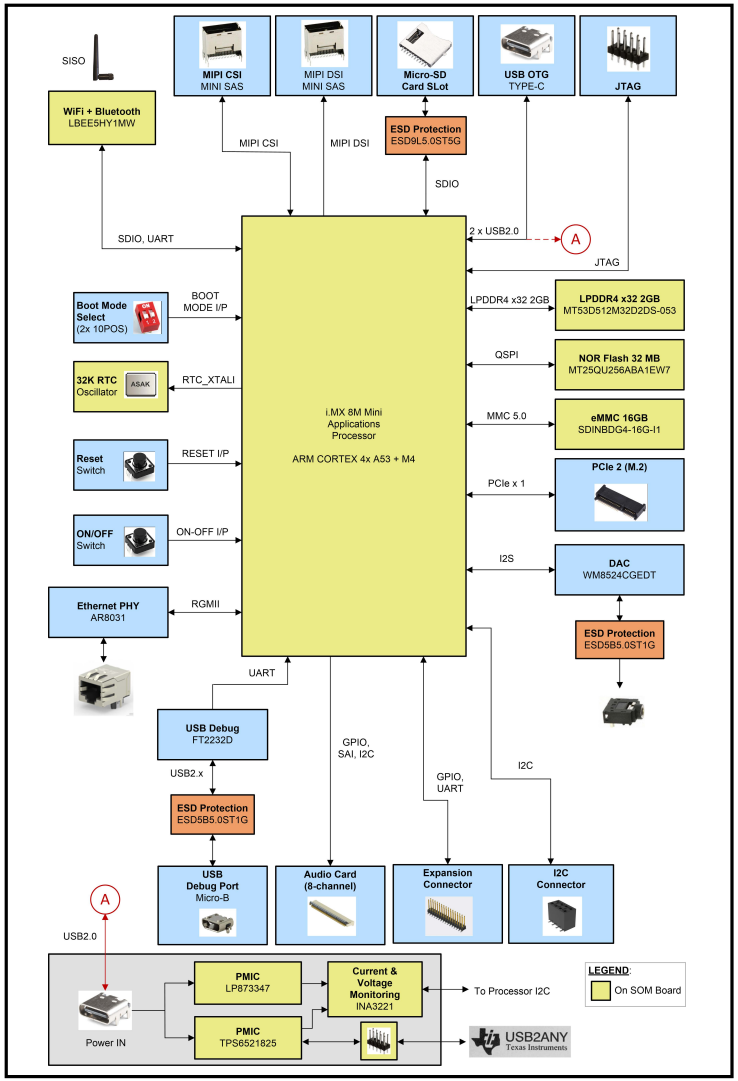
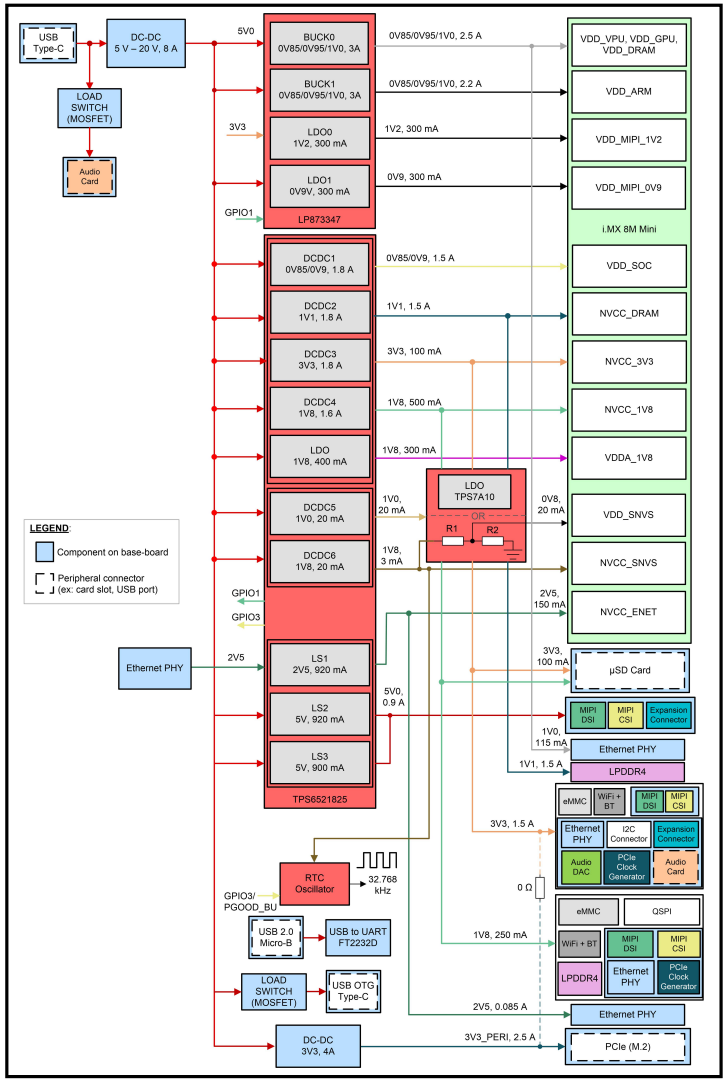
BLOCK DIAGRAM



POWER ARCHITECTURE



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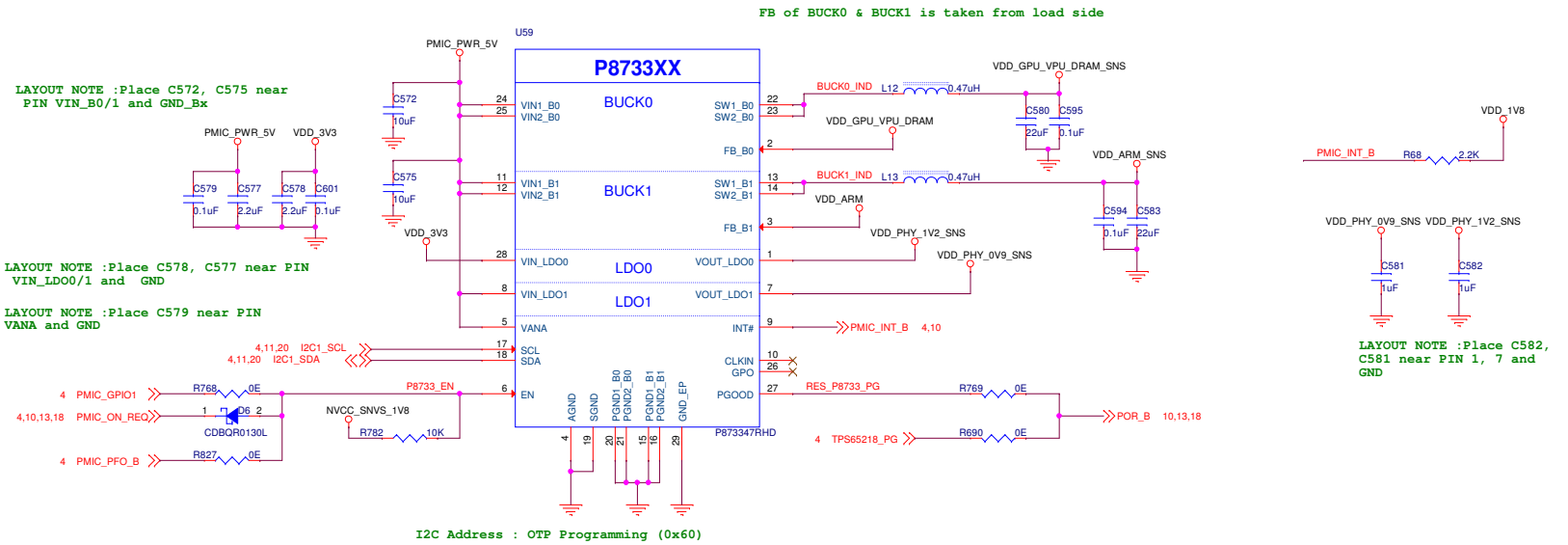
VVDN TECHNOLOGIES	A3	Title : BLOCK_DIAGRAM
	Fab No : 501-1-01019	Rev: B2
	Asy No : 701-1-01225	Sheet 2 of 21

PMIC LP8733 AND RTC



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VVDN TECHNOLOGIES	A3	Title : PMIC LP8733 AND RTC
	Fab No : 501-1-01019	Rev: B2
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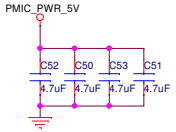
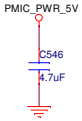
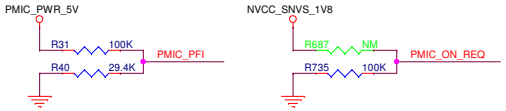
PMIC TPS65218





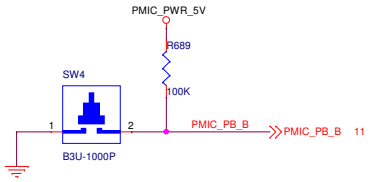
Input Capacitor for power rails -
Place near U53 pins 1, 43, 37,12

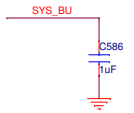
Place C546 near Pin 5



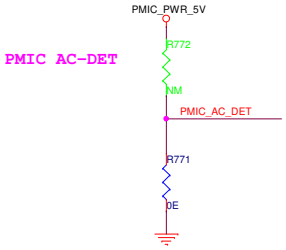
Power failure is notified to system
if PMIC_PWR go below 3.52V

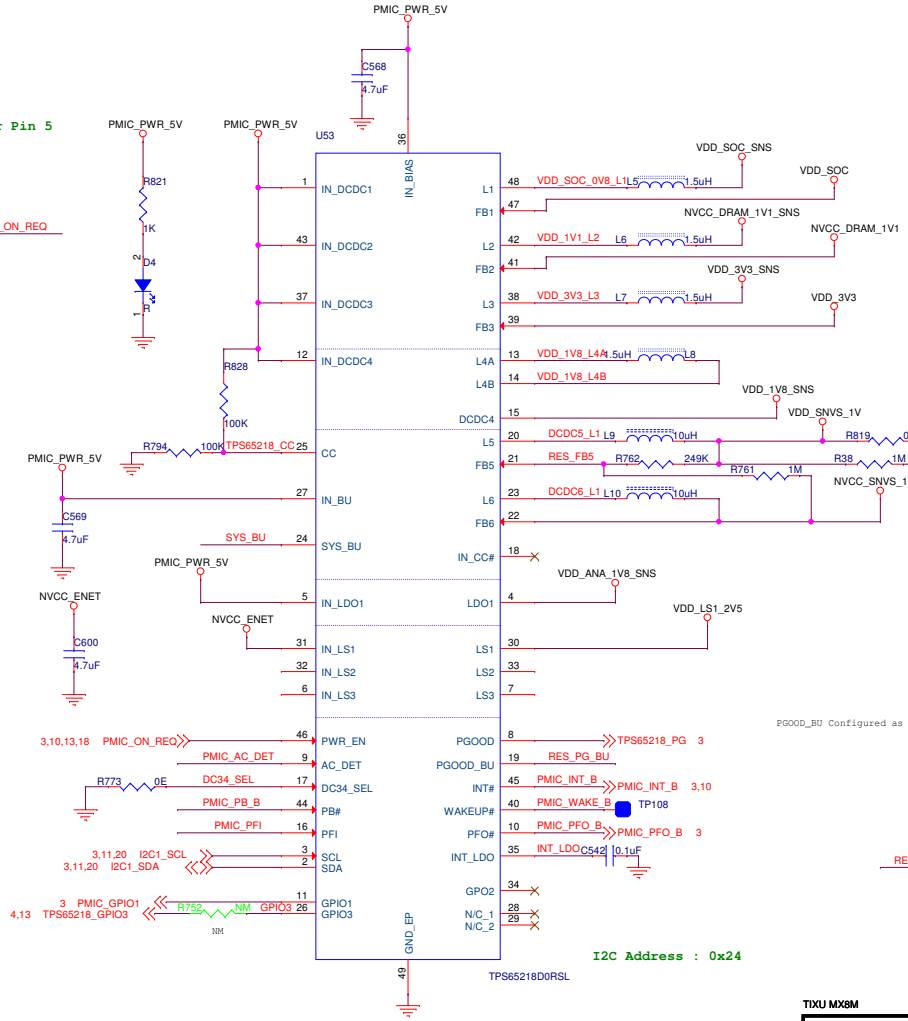
PMIC PB





PMIC AC-DET

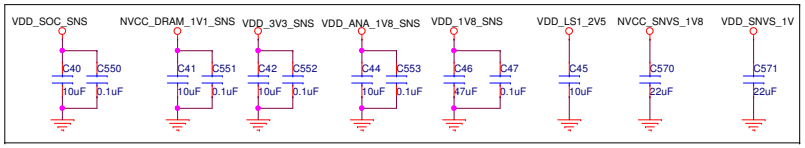




I2C Address : 0x24

GPIO1/3, PGOOD, INT#, WAKEUP#, PFO# Configured as Open Drain

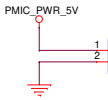
Output Capacitor for all the power rails -
Place near the output Inductor/ Pins



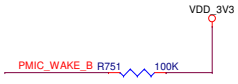
Change the part R762 to 0E in BoM.
For using output of DCDC5 as VDD_SNVS_0V8 ;
1) Mount the resistors R761, R38 & R819
2) Change R762 as 249K
3) NM R820

FB of DCDC1, 2 &3 is taken from load side

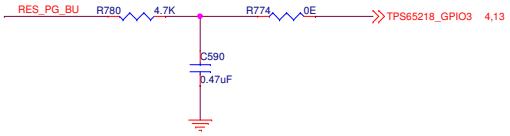
Backup PWR Supply



PGOOD_BU Configured as Push-Pull



For using PGOOD_BU, Mount R774
and remove R752 & R102



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VVDN TECHNOLOGIES	A3	Title : PMIC TPS65218D0
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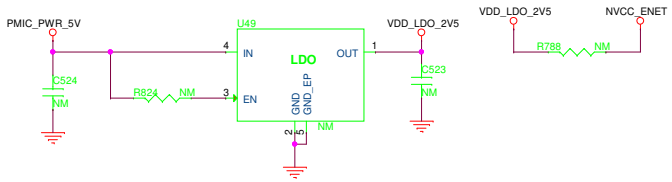
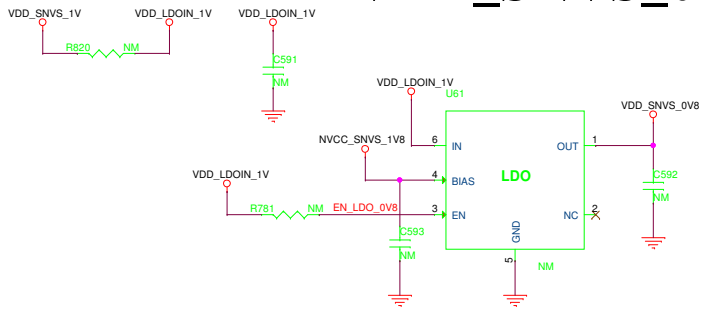
DC TO DC CONVERTERS

VDD_LDO_2V5



VDD_SNVS_0V8



TIXU MX8M

VVDN TECHNOLOGIES	A3	Title : DC TO DC CONVERTERS
	Fab No : 501-1-01019	Rev: B2
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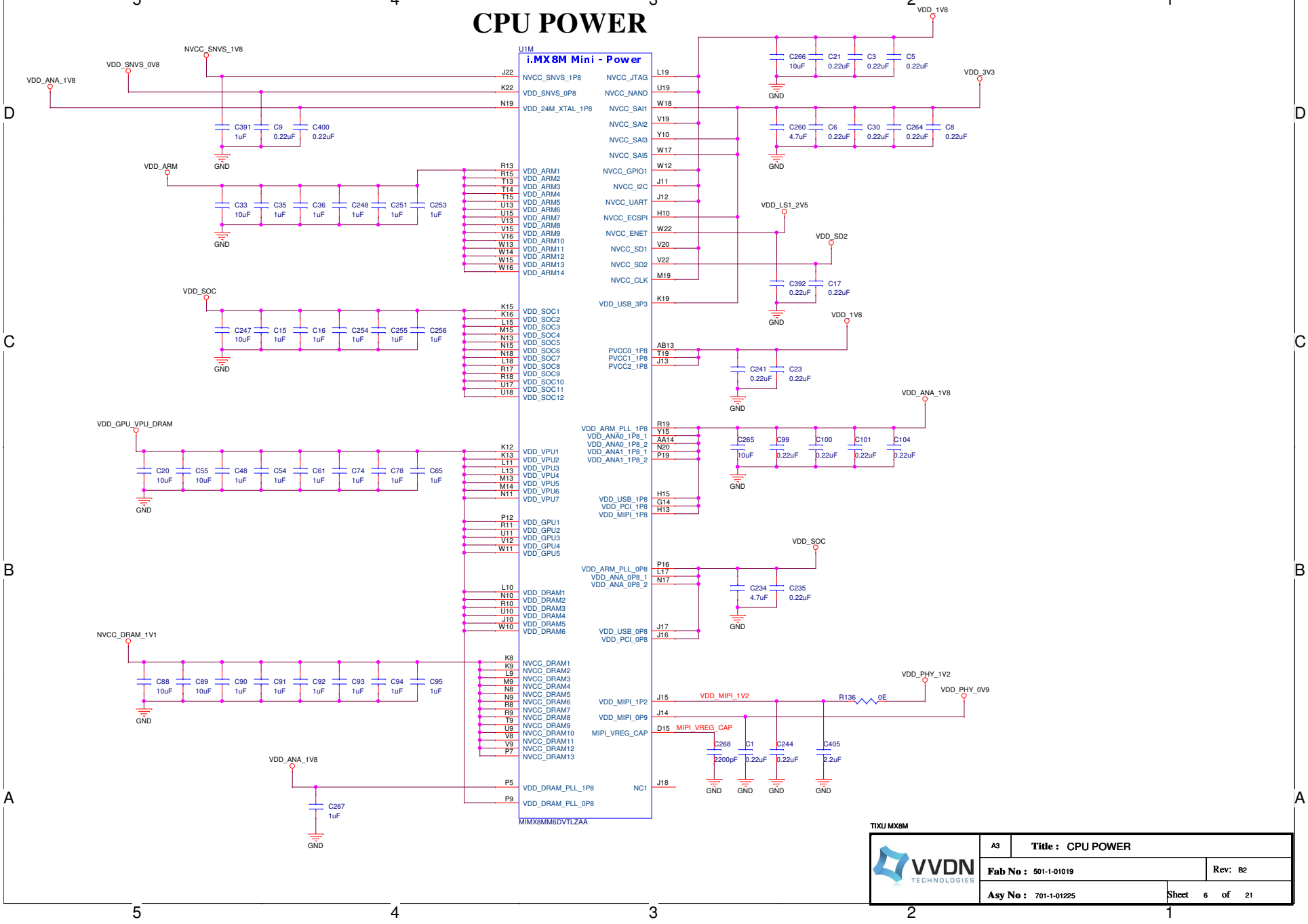
CPU POWER



TIXU MX8M

VVDN TECHNOLOGIES	A3	Title : CPU POWER
	Fab No : 501-1-01019	Rev: B2
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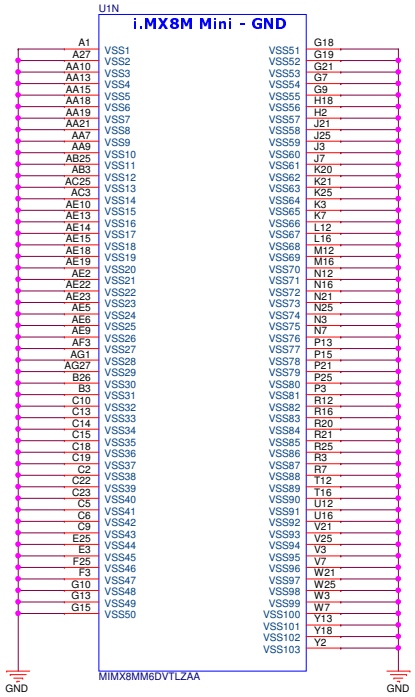
CPU GROUND



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VVDN TECHNOLOGIES	A3	Title : CPU GND
	Fab No : 501-1-01019	Rev: B2
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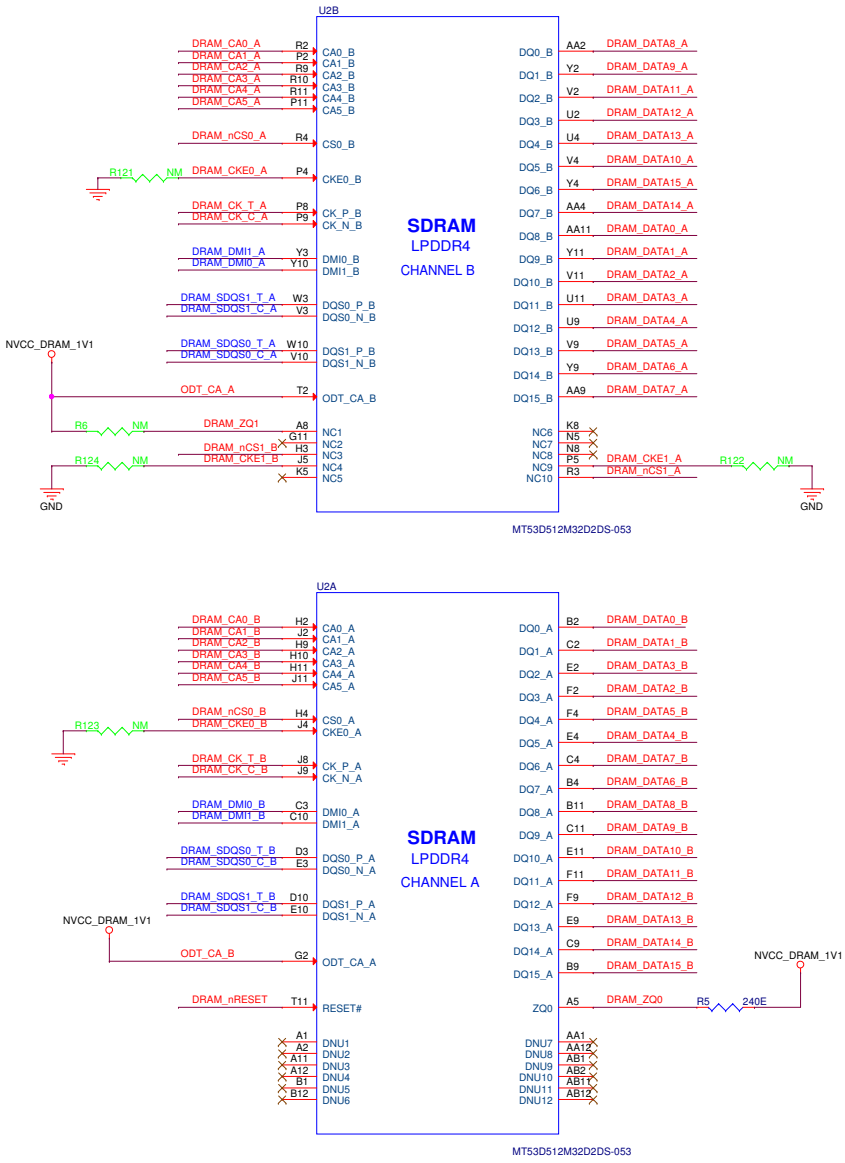
LPDDR4 2GB



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VVDN TECHNOLOGIES	A3	Title : LPDDR4
	Fab No : 501-1-01019	Rev: B2
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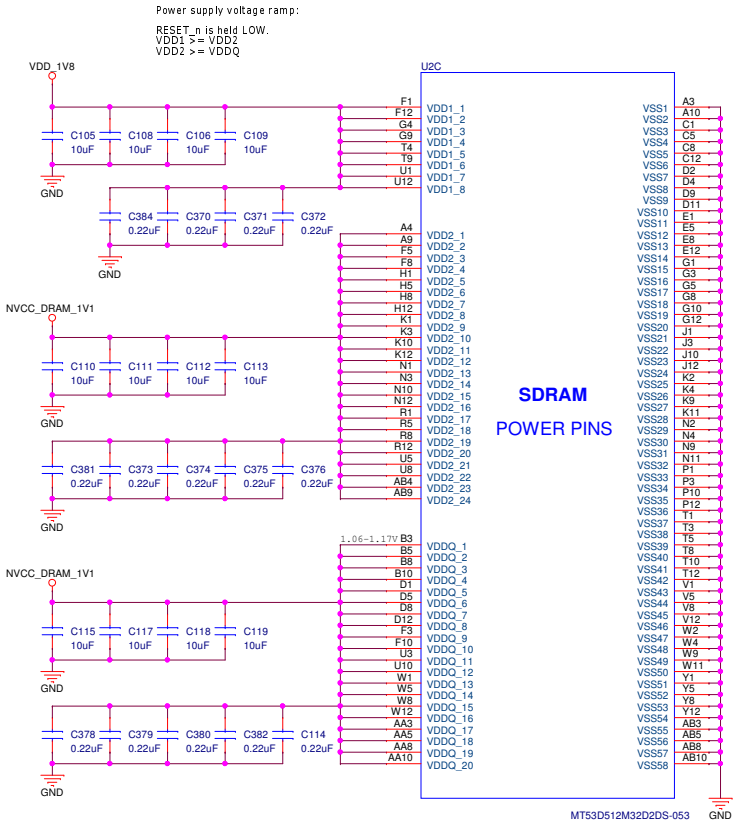
LPDDR4 POWER



Data Bus

Pin Name	LPDDR4	DDR4
DRAM_DQS0_P	DQS0_t_A	DQSL_t_A
DRAM_DQS0_N	DQS0_c_A	DQSL_c_A
DRAM_DM0	DMI0_A	DML_n_A / DBIL_n_A
DRAM_DQ00	DQ0_A	DQL0_A
DRAM_DQ01	DQ1_A	DQL1_A
DRAM_DQ02	DQ2_A	DQL2_A
DRAM_DQ03	DQ3_A	DQL3_A
DRAM_DQ04	DQ4_A	DQL4_A
DRAM_DQ05	DQ5_A	DQL5_A
DRAM_DQ06	DQ6_A	DQL6_A
DRAM_DQ07	DQ7_A	DQL7_A
DRAM_DQS1_P	DQS1_t_A	DQSU_t_A
DRAM_DQS1_N	DQS1_c_A	DQSU_c_A
DRAM_DM1	DMI1_A	DMU_n_A / DBIU_n_A
DRAM_DQ08	DQ08_A	DQU0_A
DRAM_DQ09	DQ09_A	DQU1_A
DRAM_DQ10	DQ10_A	DQU2_A
DRAM_DQ11	DQ11_A	DQU3_A
DRAM_DQ12	DQ12_A	DQU4_A
DRAM_DQ13	DQ13_A	DQU5_A
DRAM_DQ14	DQ14_A	DQU6_A
DRAM_DQ15	DQ15_A	DQU7_A
DRAM_DQS2_P	DQS0_t_B	DQSL_t_B
DRAM_DQS2_N	DQS0_c_B	DQSL_c_B
DRAM_DM2	DMI0_B	DML_n_B / DBIL_n_B
DRAM_DQ16	DQ0_B	DQL0_B
DRAM_DQ17	DQ1_B	DQL1_B
DRAM_DQ18	DQ2_B	DQL2_B
DRAM_DQ19	DQ3_B	DQL3_B
DRAM_DQ20	DQ4_B	DQL4_B
DRAM_DQ21	DQ5_B	DQL5_B
DRAM_DQ22	DQ6_B	DQL6_B
DRAM_DQ23	DQ7_B	DQL7_B
DRAM_DQS3_P	DQS1_t_B	DQSU_t_B
DRAM_DQS3_N	DQS1_c_B	DQSU_c_B
DRAM_DM3	DMI1_B	DMU_n_B / DBIU_n_B
DRAM_DQ24	DQ08_B	DQU0_B
DRAM_DQ25	DQ09_B	DQU1_B
DRAM_DQ26	DQ10_B	DQU2_B
DRAM_DQ27	DQ11_B	DQU3_B
DRAM_DQ28	DQ12_B	DQU4_B
DRAM_DQ29	DQ13_B	DQU5_B
DRAM_DQ30	DQ14_B	DQU6_B
DRAM_DQ31	DQ15_B	DQU7_B

Command/Address

Pin Name	LPDDR4	DDR4
DRAM_RESET_N	RESET_N	RESET_n
DRAM_ALERT_N	MTEST1	ALERT_n / MTEST1
DRAM_A_C00	CKE0_A	CKE0
DRAM_A_C01	CKE1_A	CKE1
DRAM_A_C02	CS0_A	CS0_n
DRAM_A_C03	CS1_A	C0
DRAM_A_C04	CK_t_A	BG0
DRAM_A_C05	CK_c_A	BG1
DRAM_A_C06	/	ACT_n
DRAM_A_C07	/	A9
DRAM_A_C08	CA0_A	A12
DRAM_A_C09	CA1_A	A11
DRAM_A_C10	CA2_A	A7
DRAM_A_C11	CA3_A	A8
DRAM_A_C12	CA4_A	A6
DRAM_A_C13	CA5_A	A5
DRAM_A_C14		A4
DRAM_A_C15	/	A3
DRAM_A_C16	/	CK_t_A
DRAM_A_C17	/	CK_c_A
DRAM_A_C19	MTEST	MTEST
DRAM_A_C20	CKE0_B	CK_t_B
DRAM_A_C21	CKE1_B	CK_c_B
DRAM_A_C22	CS1_B	/
DRAM_A_C23	CS0_B	/
DRAM_A_C24	CK_t_B	A2
DRAM_A_C25	CK_c_B	A1
DRAM_A_C26	/	BA1
DRAM_A_C27	/	PARITY
DRAM_A_C28	CA0_B	A13
DRAM_A_C29	CA1_B	BA0
DRAM_A_C30	CA2_B	A10 / AP
DRAM_A_C31	CA3_B	A0
DRAM_A_C32	CA4_B	C2
DRAM_A_C33	CA5_B	CAS_n / A15
DRAM_A_C34		WE_n / A14
DRAM_A_C35	/	RAS_n / A16
DRAM_A_C36	/	ODT0
DRAM_A_C37	/	ODT1
DRAM_A_C38	/	CS1_n
DRAM_ZN	ZQ	ZQ
DRAM_VREF	VREF	VREF

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VVDN TECHNOLOGIES

A3	Title : LPDDR4 POWER	
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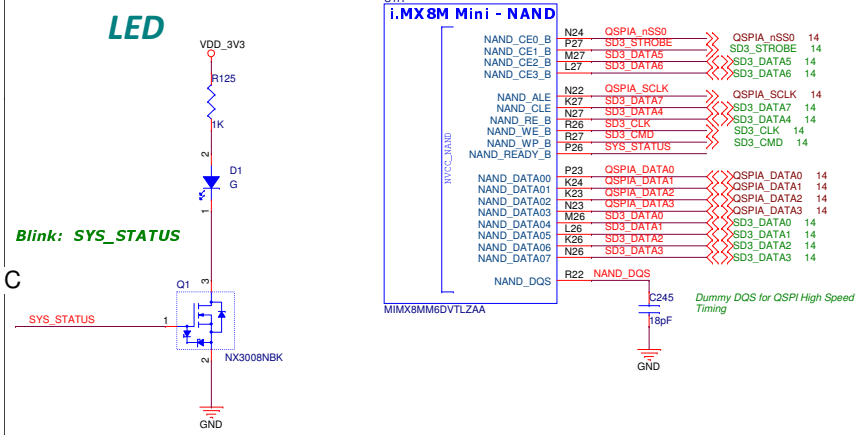
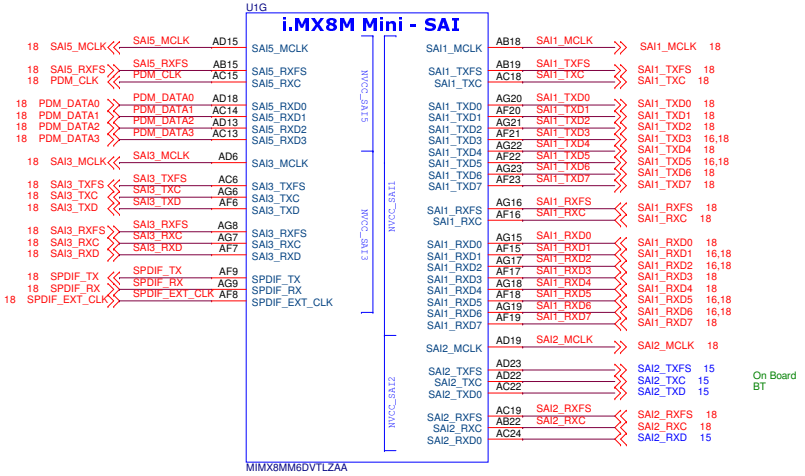
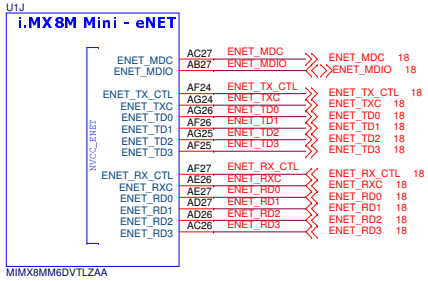
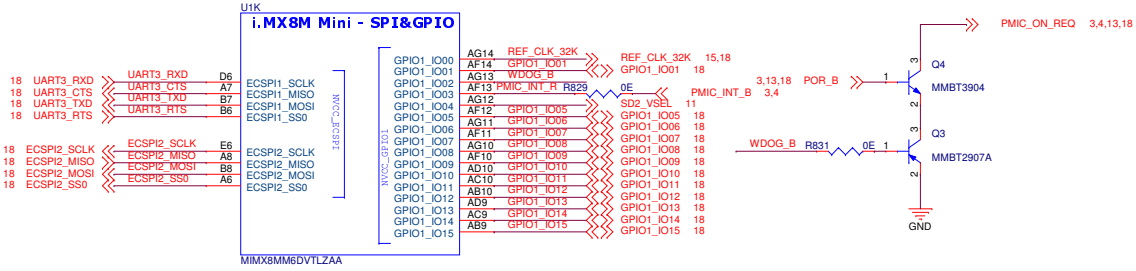
CPU IO 1

Caution:
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.









Configure internal pull up at CPU side, open drain output
Configure internal pull up at CPU side

TIXU MX8M

VVDN TECHNOLOGIES

A3	Title : CPU IO 1	
Fab No : 501-1-01019		Rev: B2
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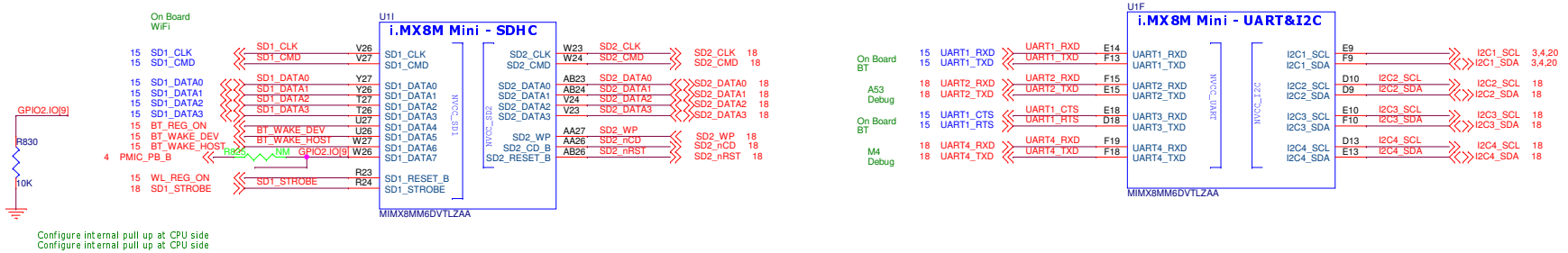
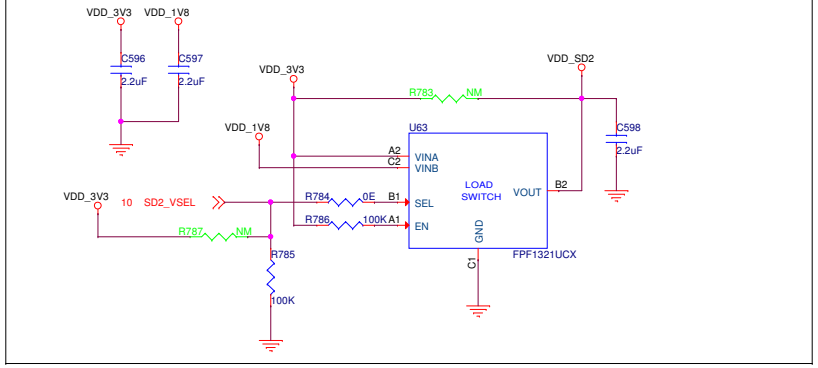
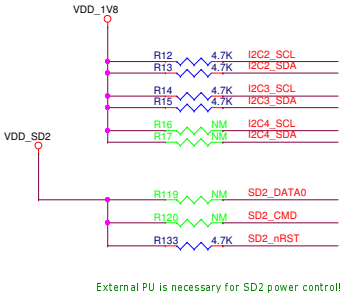
CPU IO 2



VDD_SD2 SELECTION





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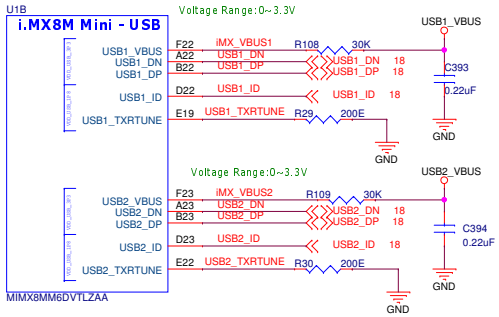
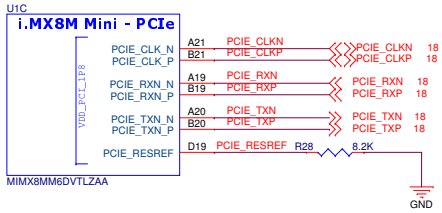
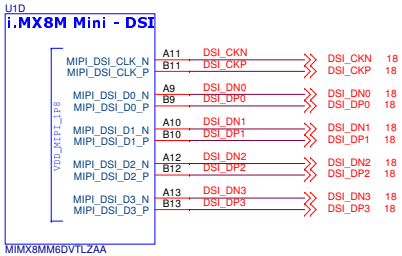
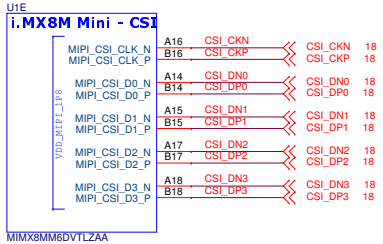
VVDN TECHNOLOGIES	A3	Title : CPU IO 2
	Fab No : 501-1-01019	Rev: B2
	Asy No : 701-1-01225	Sheet 11 of 21

i.MX8M Mini PHYs









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VVDN TECHNOLOGIES	A3	Title : CPU PHY
	Fab No : 501-1-01019	Rev: B2
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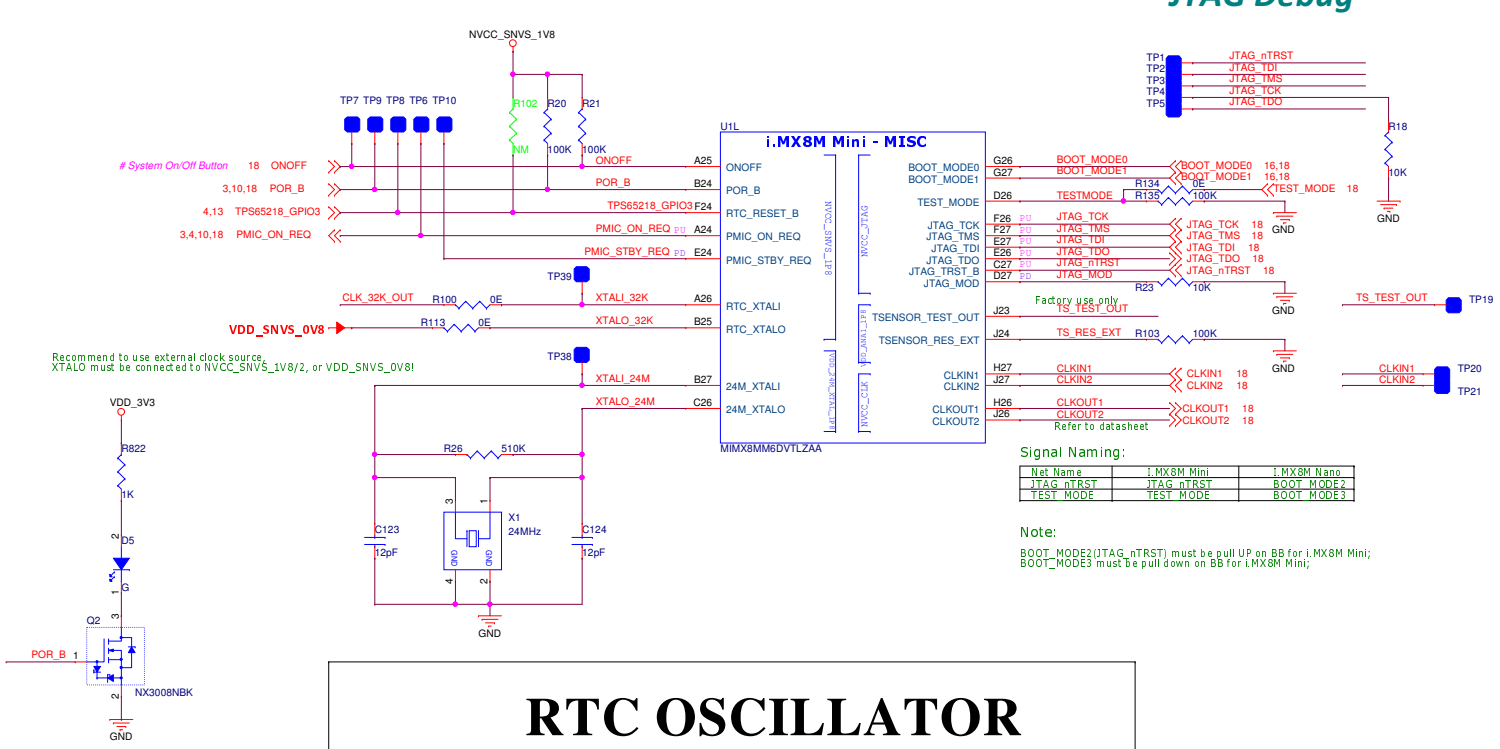
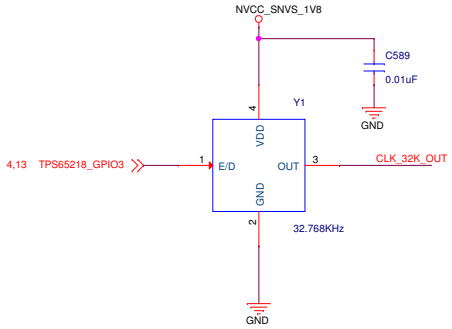
i.MX8M Mini MISC



RTC OSCILLATOR



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VVDN TECHNOLOGIES	A3	Title : CPU MISC
	Fab No : 501-1-01019	Rev: B2
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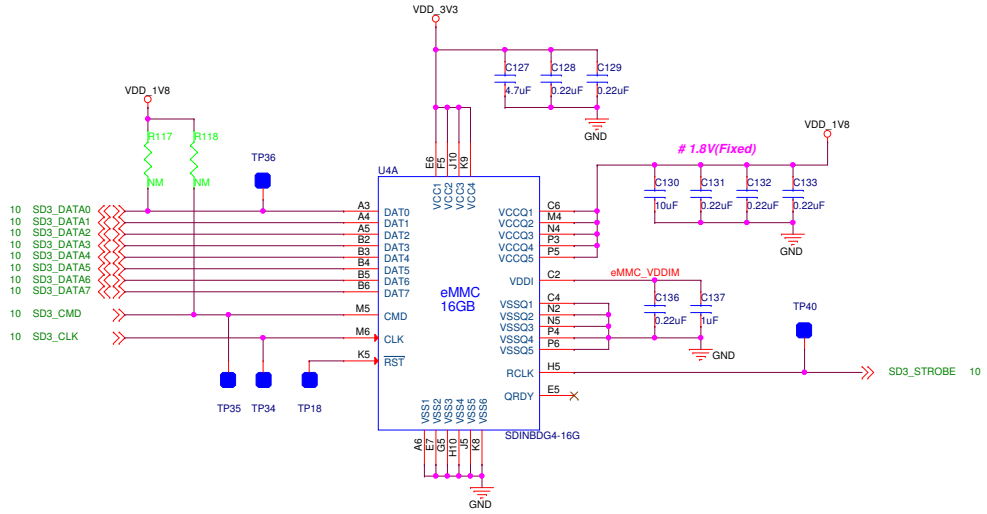
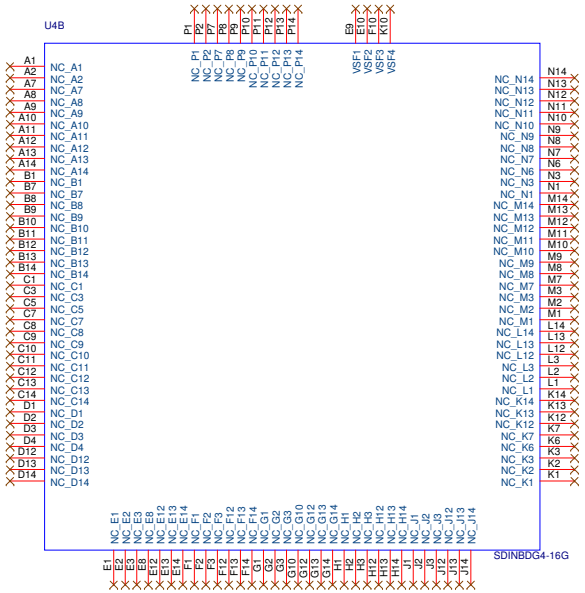
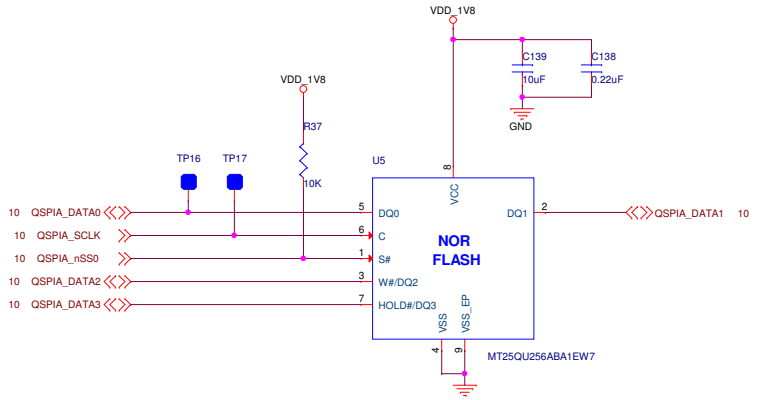
eMMC





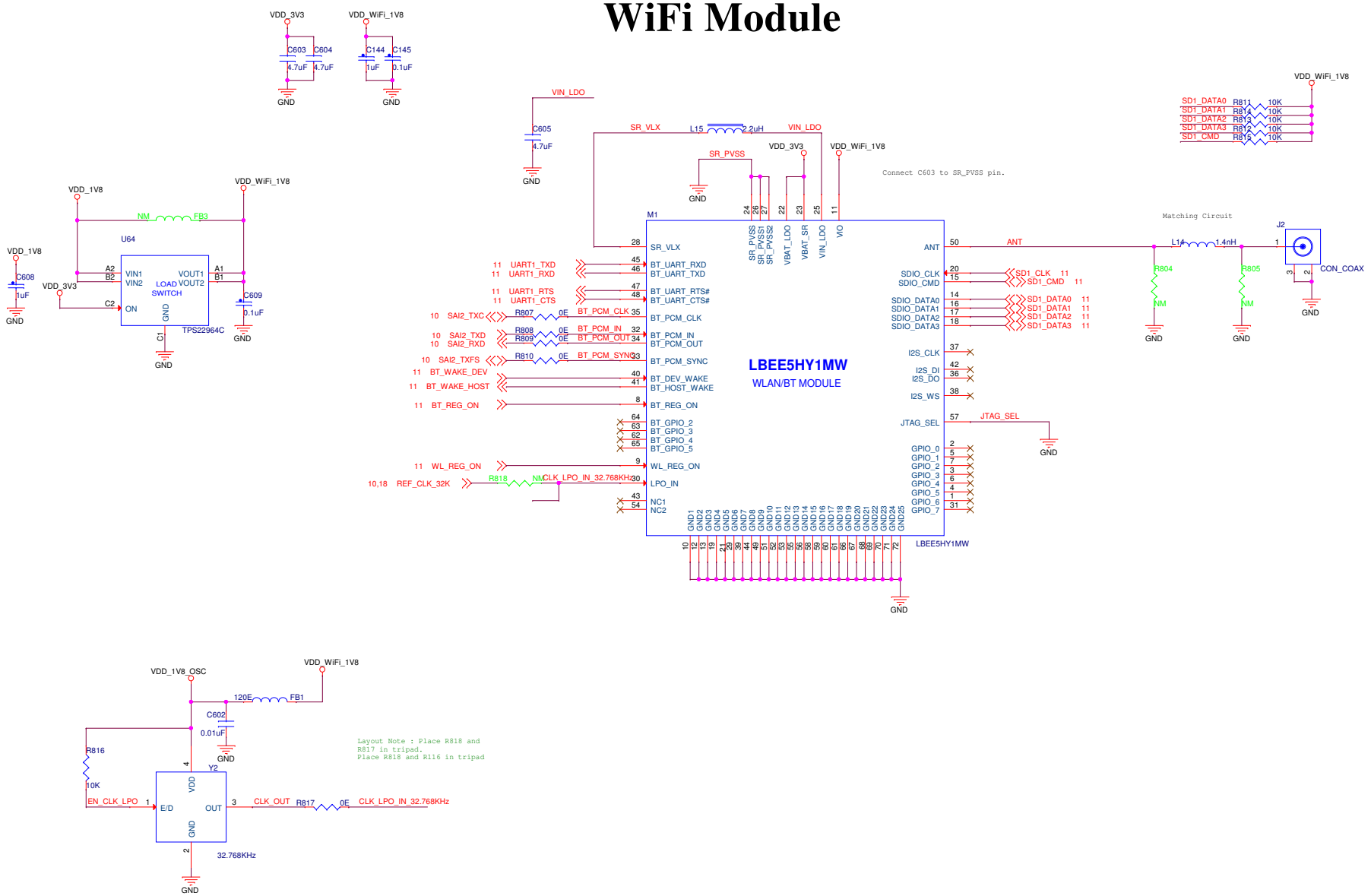
NOR FLASH



TIXU MX8M

VVDN TECHNOLOGIES	A3	Title : eMMC/FLASH
	Fab No : 501-1-01019	Rev: B2
	Asy No : 701-1-01225	Sheet 14 of 21

WiFi Module



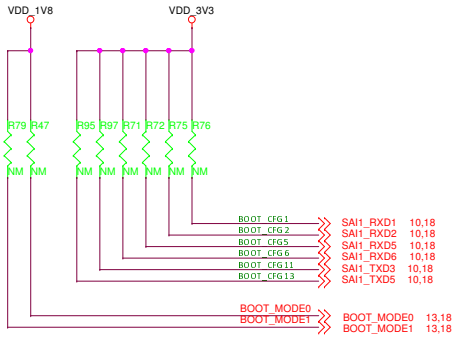
TIXU MX8M

VVDN TECHNOLOGIES	A3	Title : WIFI+BT
	Fab No : 501-1-01019	Rev: B2
	Asy No : 701-1-01225	Sheet 15 of 21

BOOT MODE SELECT

Caution:

IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.



Note:

1. Bootcfg/SAI1 singals have internal PD before and after POR_B reset is deasserted!

2. Standalone SOM board can support eMMC/SDHC3 boot, by populating R71, R72, R75, R76, R79, R95, R97!

3. When using Base Board for Multi boot selection, you must keep the resistors DNP on SOM board!

Boot Mode

BOOT_MODE1	BOOT_MODE0
BOOT TYPE:	
00 Boot From Fuses	
01 Serial Downloader	
10 Internal Boot (Development)	
11 Reserved	

BT_CFG Pins:

SAI1_RXD0	BOOT_CFG0
SAI1_RXD1	BOOT_CFG1
SAI1_RXD2	BOOT_CFG2
SAI1_RXD3	BOOT_CFG3
SAI1_RXD4	BOOT_CFG4
SAI1_RXD5	BOOT_CFG5
SAI1_RXD6	BOOT_CFG6
SAI1_RXD7	BOOT_CFG7
SAI1_RXD8	BOOT_CFG8
SAI1_RXD9	BOOT_CFG9
SAI1_RXD10	BOOT_CFG10
SAI1_RXD11	BOOT_CFG11
SAI1_RXD12	BOOT_CFG12
SAI1_RXD13	BOOT_CFG13
SAI1_RXD14	BOOT_CFG14
SAI1_RXD15	BOOT_CFG15

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VVDN TECHNOLOGIES

A3	Title : BOOT SELECT	
Fab No : 501-1-01019		Rev: B2
Asy No : 701-1-01225	Sheet 16 of 21	

BOOT MODE Description

	Address	7	6	5	4	3	2	1	0
	0x470[15:8]	BOOT_CFG[15]	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]
	0x470[15:8]	Infinit-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD			Port Select: 00 - uSDHC1 01 - uSDHC2 10 - uSDHC3		Power Cycle Enable '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
	0x470[15:8]		010 - MMC/eMMC						
	0x470[15:8]		011 - NAND			Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	
	0x470[15:8]		100 - QSPI			Flash Auto Probe	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR		
	0x470[15:8]		110 - SPI NOR			Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3			SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)
	0x470[15:8]	Others - Reserved for future use							

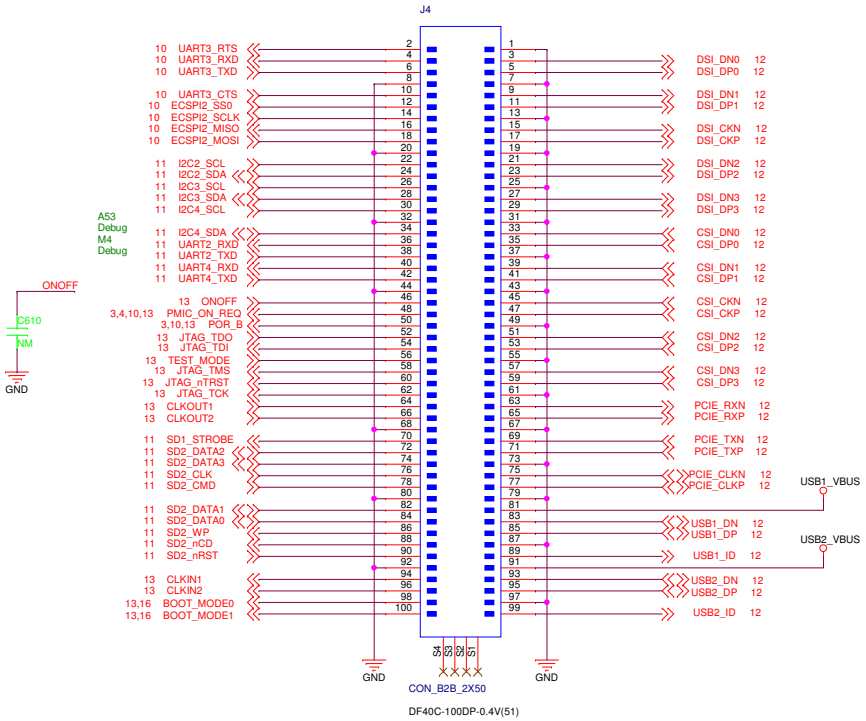
		BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC4.4) 110 - 8-bit DDR (MMC4.4) Else - reserved.			Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V	USDHC IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V
NAND	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111'- 15 GPMICLK cycles.			Reserved
FlexSPI	0x470[7:0]	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		FLASH Auto Probe Type		FlexSPI FLASH Dummy Cycle			
SPINOR	0x470[7:0]	CS select SPI only: 00 - CS#0 default 01 - CS#1 10 - CS#2 11 - CS#3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

VVDN TECHNOLOGIES

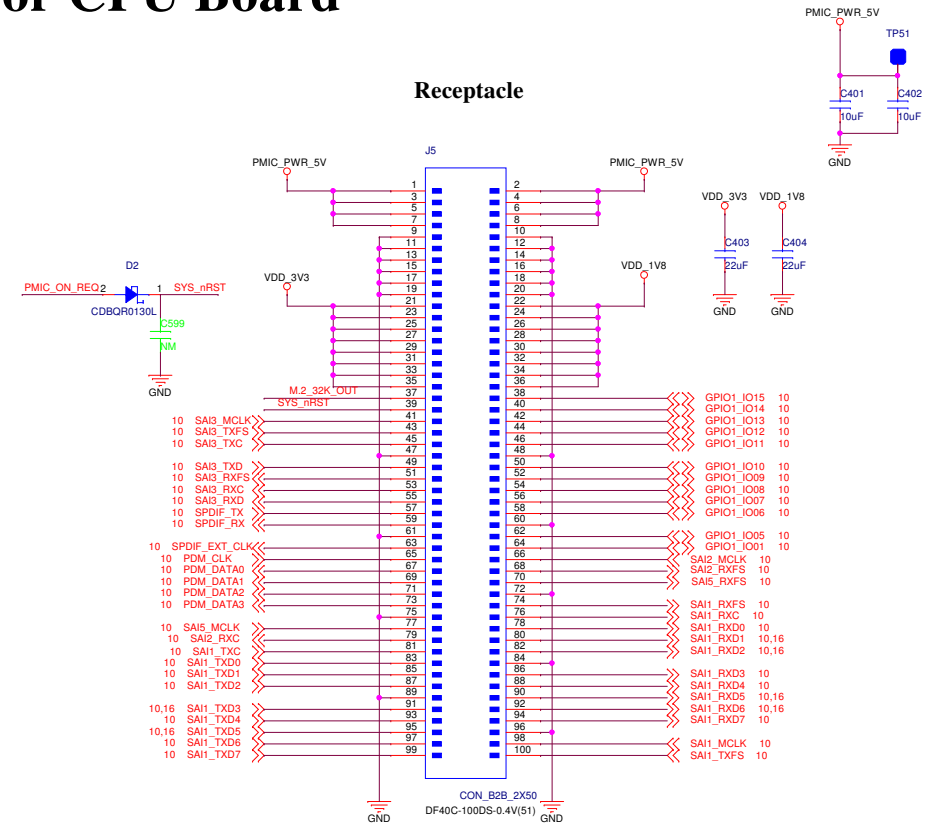
A3	Title : BOOT MODE DESCRIPTION	
Fab No : 501-1-01019		Rev: B2
Asy No : 701-1-01225		Sheet 17 of 21

B2B Connector for CPU Board

Header



Receptacle



Caution:
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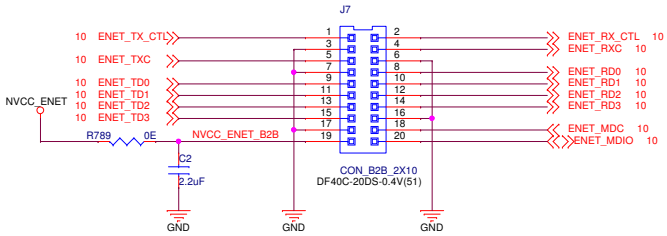
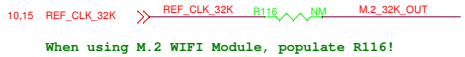
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

Receptacle



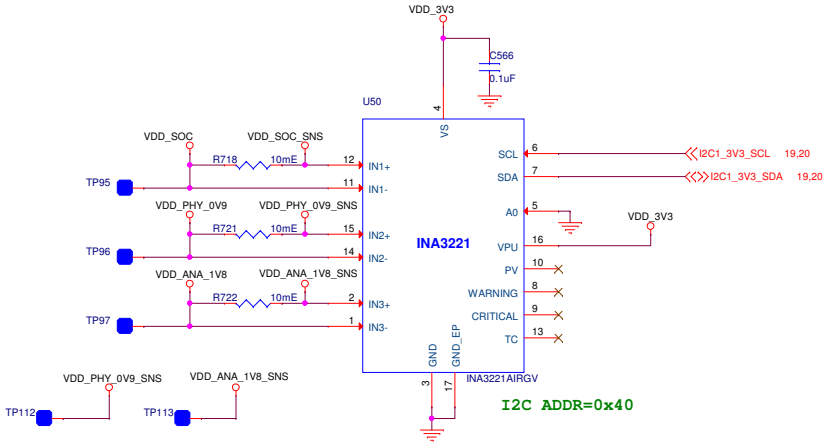


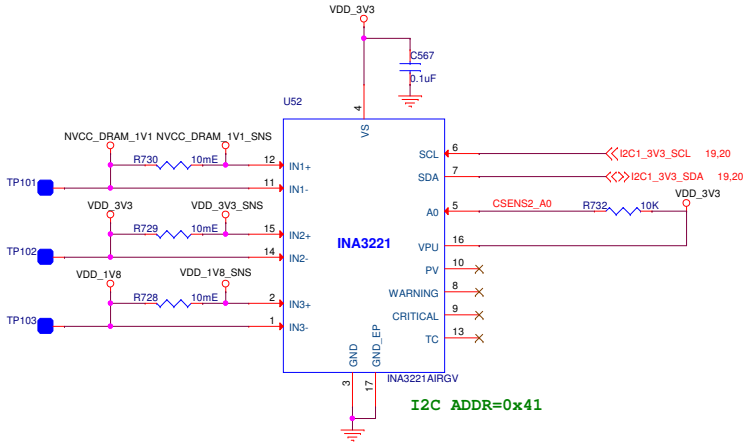
When using M.2 WIFI Module, populate R116!

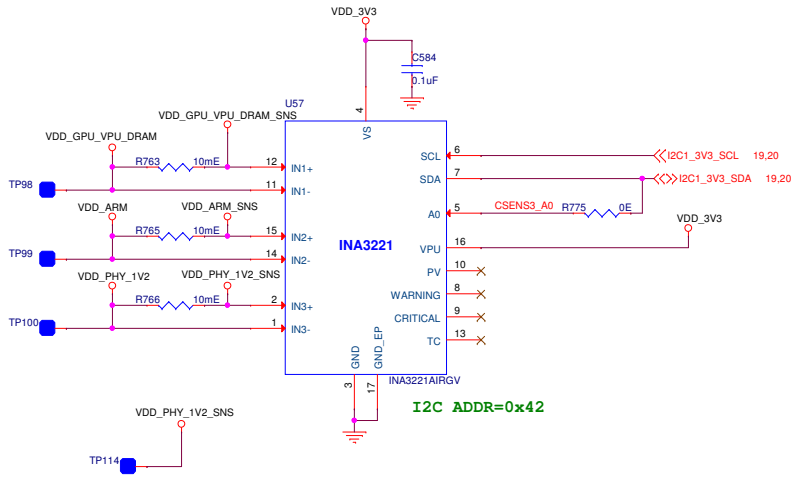
TIXU MX8M

VVDN TECHNOLOGIES	A3	Title : B2B CONNECTORS
	Fab No : 501-1-01019	Rev: B2
	Asy No : 701-1-01225	Sheet 18 of 21

CURRENT AND VOLTAGE MONITORING







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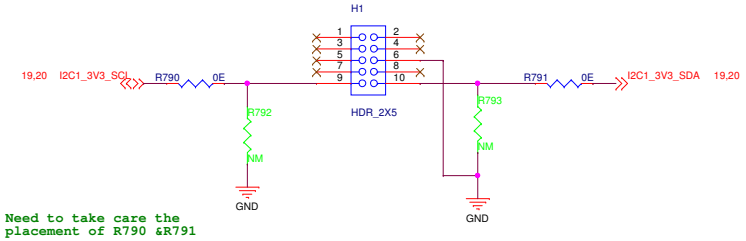
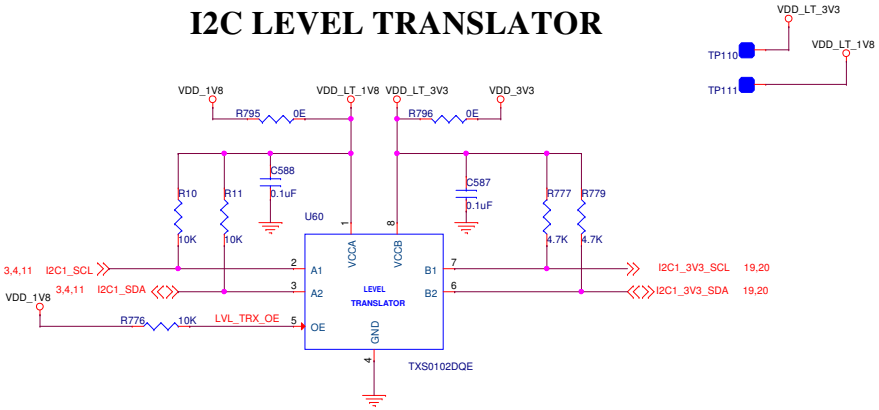
VVDN TECHNOLOGIES	A3	Title : CURRENT MONITORING
	Fab No : 501-1-01019	Rev: B2
	Asy No : 701-1-01225	Sheet 19 of 21

USB2ANY



Need to take care the placement of R790 &R791

I2C LEVEL TRANSLATOR



TXS0102 Have internal pull up of value 10K at A1, A2, B1, B2 pins

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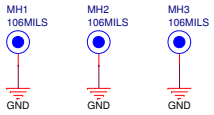
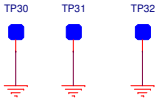
VVDN TECHNOLOGIES	A3	Title : USB2ANY
	Fab No : 501-1-01019	Rev: B2
	Asy No : 701-1-01225	Sheet 20 of 21

MISCELLANEOUS

MOUNTING HOLES



GND TEST POINT



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VVDN TECHNOLOGIES	A3	Title : MISCELLANEOUS
	Fab No : 501-1-01019	Rev: B2
	Asy No : 701-1-01225	Sheet 21 of 21

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